

ANALYSIS AND DESIGN OF 3-PHASE UNFOLDING BASED AC-DC BATTERY  
CHARGERS

by

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## ABSTRACT

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This thesis presents the analysis and design of high-efficiency, isolated, 3-phase ac-dc rectifiers for battery charging applications. The rise in popularity of electric vehicles (EVs) due to their increased efficiency over conventional internal combustion engines, has driven the need for more battery charging infrastructure. Furthermore, heavy duty vehicles are also being converted to electric to fill needs such as public transportation via bus fleets as well as cargo delivery via semi-trucks. Such heavy duty vehicles require more energy than personal transportation vehicles and thus require larger battery packs. To charge heavy duty battery packs in the same amount of time as the typical EV, higher power chargers are required.

Energy is distributed through the 3-phase ac grid network, and a battery charger is responsible for rectifying the power into a dc output for battery charging. The novel battery charging topologies under investigation in this thesis are classified as quasi-single stage approaches to ac-dc rectification and are designed to work with a soft dc-link generated by an Unfolder rather than a stiff dc-link produced by an active-front-end (AFE). Unfolding-based rectification requires a 3-port dc-dc converter to process the time varying voltage from the soft dc-link input ports. In this thesis, the isolated, 3-port, dc-dc converter is realized in two different topologies referred to as the three-level (3L) asymmetrical full bridge (3LAFB) and 3L asymmetrical dual active bridge (3LADAB). The operation of each converter is briefly

discussed to help develop context for the hardware and controller designs. The controller design for the 3LAFB topology is developed to explain the control objectives of the 3-port dc-dc converter. Hardware results from the 2kW 3LAFB prototype design are presented to validate proposed topology and controller designs. The modular structure for a 350 kW extreme fast charger (XFC) is proposed. The optimal building block for the full power XFC is determined to be an 18 kW 3LADAB module. The design for the high-efficiency 18 kW 3LADAB is presented and hardware results are given.

(143 pages)

## PUBLIC ABSTRACT

## Analysis and Design of 3-Phase Unfolding Based AC-DC Battery Chargers

Rees R. Hatch

This thesis presents the analysis and design of high-efficiency battery chargers for heavy duty EV applications. The rise in popularity of the electric vehicles (EVs) due to their increased efficiency over conventional internal combustion engines, has driven the need for more battery charging infrastructure. Furthermore, heavy duty vehicles are also being converted to electric to fill needs such as public transportation via bus fleets as well as cargo delivery via semi-trucks. Such heavy duty vehicles require more energy than personal transportation vehicles and thus require larger battery packs. To charge heavy duty battery packs in the same amount of time as the typical EV, higher power chargers are required.

Energy is distributed through the grid network, and a battery charger is converts the grid power into a regulated output for battery charging. The novel battery charging designs investigated in this thesis are classified differently than traditional designs because they have fewer switching stages to convert the power. The unique approach taken allows these designs to have higher efficiency overall than a traditional battery charger design. The new converter designs are referred to as the three-level (3L) asymmetrical full bridge (3LAFB) and 3L asymmetrical dual active bridge (3LADAB). The operation of each converter is briefly discussed to help develop context for the hardware and controller designs. The controller design for the 3LAFB topology is developed to explain the control objectives of the 3-port dc-dc converter. Hardware results prototype designs are presented to validate proposed chargers and controller designs. A high power extreme fast charger (XFC) structure is proposed using multiple lower power modules. The high-efficiency design of a single module is presented and hardware results are given.

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## ACRONYMS

AC	alternating current
AFE	active front end
DAB	dual active bridge
DABSRC	dual active bridge series resonant converter
DC	direct current
EV	electric vehicle
HF	high frequency
MOSFET	metal oxide semiconductor field effect transistor
PCB	printed circuit board
PLL	phase-locked loop
PSFB	phase shifted full bridge
PWM	pulse width modulation
SiC	Silicon Carbide
SoC	state of charge
TAB	triple active bridge
THD	total harmonic distortion
XFC	extreme fast charger
ZVS	zero voltage switching
3L	3-level
3LADAB	3-level asymmetrical dual active bridge
3LAFB	3-level asymmetrical full bridge

## CHAPTER 1

### INTRODUCTION

With the increase in popularity of electric vehicles (EV), the challenges surrounding battery energy storage has formed a core area of research in the field of power electronics. Current projections for the EV market estimate an annual growth of 36 %, leading to 245 million vehicles in 2030 [1]. The growth is not only limited to the light-duty EVs; the electrification of public transportation has led to fully electrified bus fleets. The electrification of heavy-duty vehicles such as busses or trucks, necessitates larger energy demand requirements from the vehicle which lead to larger battery capacity requirements and longer recharge time.

Currently, the gasoline engine has established a precedent for vehicular mobility that is tough to compete with for modern EV. This is largely due to the sheer mismatch in energy density of the fuel. Lithium ion (Li-ion) batteries have many modern chemistries that have energy densities ranging from 50 Wh/kg (low end of Lithium Titanate (LTO) chemistry) to 220 Wh/kg (high-end of Lithium Nickel Manganese Cobalt Oxide (NMC) chemistry) [2]. However, gasoline has an energy density of 13 kWh/kg which is about 65 times more dense than the NMC chemistry. This greatly limits the energy storage capabilities of the EV and the vehicle range when compared with typical internal combustion engines.

To combat the range anxiety of the EV users or potential EV users, the problem of battery refueling must be addressed. To compete with gasoline standard, EV battery charging needs to be done at higher powers so that more energy can be delivered in a smaller amount of time. Because Li-ion batteries are very sensitive to over-charging, the charging process must be controlled to avoid overheating the cells or causing a thermal runaway. Modern Li-ion chemistries such as LTO, have the ability to withstand higher charging and discharging currents at a wider range of operating temperatures [3].

Electrical energy is typically distributed by the grid via power lines in the form of ac

(alternating current) voltage. This voltage cannot be directly used to charge the EV because the battery voltage is dc (direct current). Therefore an ac-dc converter is needed to process the ac voltage delivered by the grid into a dc voltage for charging the batteries. An ac-dc converter is referred to as a rectifier in the case of unidirectional power flow from the grid to the load.

The rectification process is ideally 100 % efficient so that no power is lost when recharging; however, practically this is not achievable due to the losses within the converter. High-efficiency designs are desired because less power is lost from the supply and the reduced losses (which are dissipated as heat) require simpler thermal management.

## 1.1 Contributions and Organization

The work presented in this thesis will pertain to the 3-Level Asymmetric Full Bridge (3LAFB) and 3-level asymmetric dual active bridge (3LADAB). The average model and controller design of the 3LAFB are derived in Chapter 3. The hardware results from the 2 kW 3LAFB prototype are included to show the achieved high-efficiency from the topology during ac-dc power conversion. In Chapter 4, the proposed modular structure of the 350 kW battery charger are presented. The steps leading to the selection and the design of the 18 kW 3LADAB module are detailed. In Chapter 5 the design procedure is detailed for the 3LADAB module and an 18 kW prototype is designed. The hardware results from 3LADAB module testing are summarized to validate the proposed design procedure and hardware implementation.

## CHAPTER 2

### REVIEW OF AC-DC RECTIFICATION

#### 2.1 Modern Low-Harmonic AC-DC Rectification

The increased power level required to charge EV batteries faster necessitates a three-phase grid connection. Single-phase distribution networks are common for low power electronics; however, at higher power levels three-phase power is preferred for multiple reasons. Firstly, the neutral conductor can be omitted in the case of a balanced three phase load thus reducing the required cabling. Secondly, the instantaneous power being delivered is constant in the three-phase case where single-phase power has a 120 Hz ripple. Lastly, there are electromagnetic compatibility (EMC) standards (IEEE-519, IEC 61000-3-4) that govern the quality of the current waveform shape in terms of the total harmonic distortion (THD) and power factor. These standards are imposed to limit the voltage and current distortions caused by consumers and increase the interoperability of the utility grid. A power factor corrected (PFC) rectifier complies with the grid standards by have having good power factor (near 1.0) and a low THD ( $< 5\%$ ).

An ideal rectifier presents a resistive load to the grid [4]. The current drawn by a resistive load is in phase with the voltage and does not produce/exhibit any low-frequency harmonics that are not present in voltage waveform for fulfilling the the PFC requirements. Ideally, the rectifier can provide constant dc output power with 100 % efficiency because the instantaneous 3-phase input power is constant. This leads to the notion that an ideal 3-phase rectifier does not need any internal energy storage. For battery charging applications, the output of the ideal rectifier should be controllable and variable to accommodate the wide voltage variation needed for the constant-current constant-voltage (CC-CV) charging scheme.

Practically, near ideal rectifiers are realized with power converters switching at high-frequency to convert the power from the utility to a dc output. The general approaches to rectification can be classified into the following categories: two stage, single stage (ac-ac), quasi-single stage (Unfolder with 3-port dc-dc). A comprehensive review and comparison of the rectification approaches is given [5] and summarized in following paragraphs. Further details and classifications on modern approaches to PFC rectification are given in [6, 7].

The two stage rectifier is the most well known approach due to its simplicity in control and popularity with industry [8]; the first stage is known as the active-front-end (AFE) and is typically a boost-type PFC rectifier designed to have a fixed dc output known as the dc-link. The dc-link connects the AFE with a dc-dc converter. The down-stream dc-dc handles the CC-CV charging of the battery. The control of the two-stage rectifier is simplified by decoupling the AFE and dc-dc power stages with the dc-link energy buffer. The large dc-link capacitor provides a sufficient energy buffer that helps to decouple the control of each stage. The downside of the two stage approach is that the power is processed and filtered by two power converters which switch at high-frequency (HF). This increases the required number of switching devices and losses ultimately limiting the achievable efficiency of the combined rectifier.

The single stage rectifier refers to the class of rectifiers which directly convert the low-frequency grid voltage into a HF voltage waveform. These topologies are known as ac-ac or matrix-type converters. The HF waveform is passed through an isolation transformer and rectified to a dc output. This approach boasts the highest achievable efficiency found in literature today [9] due to the reduced number of switching stages and devices. The drawback of the single-stage typologies is that they require highly complex modulation schemes and controllers [10].

The topologies under investigation in this thesis fall into the category of quasi-single stage which refers to the rectifiers which operate with an Unfolder working in combination with a 3-port dc-dc converter. The Unfolder is responsible for commutating the phases of the utility grid to provide two, positive, time-varying outputs which is referred to as the

soft dc-link as opposed to the stiff dc-link which is produced by an AFE in a two stage rectifier. The two input ports of the 3-port dc-dc converter connect to the soft dc-link and the remaining port serves as the dc output of the rectifier. This approach differs from the two stage approach in that the Unfolder does not regulate the power drawn from the grid and does not contain any HF switching.

## 2.2 Unfolding Based Rectification

The Unfolder is the least complex stage in the ac-dc converter due to the low switching frequency and simple control. The output of the Unfolder is called the soft dc-link to distinguish it from the stiff dc voltage produced by an AFE. The soft DC-link has a 360 Hz ripple that follows the envelope of the grid line-line voltages.

Each of the Unfolder's 3-phases are comprised of a single-pole triple-throw switch that simply connect the input ac phases to correct soft dc-link rail. The Unfolder schematic shown in Fig. 2.1 realizes the single-pole triple-throw switch as a T-type switching leg comprised of MOSFET switches. The Unfolder has three output rails denoted as P, O, and N. The P rail should always have the highest positive potential with respect to the neutral point of the ac grid, and, thus is always connected to the ac phase with greatest positive voltage. Likewise, the N rail should always have the lowest voltage with respect to neutral or the greatest negative potential of the ac phases. The remaining grid phase is connected to the O rail through a four-quadrant (4Q) switch that is also called an injector switch. A 4Q switch is capable of blocking voltage in either direction as well as allowing current flow in either direction. The 4Q device is typically realized with the traditional two-quadrant devices connected in series but with opposite orientations as is the case in the T-type switching legs shown in Fig. 2.1.

For unidirectional ac-dc power flow the Unfolder can be realized by a three-phase diode bridge rectifier composed with 4Q injector switches as shown in Fig. 2.2. The 4Q switch can be realized by a common source connection of two MOSFETs. The diodes will passively connect the ac phases with highest and lowest potential to the P and N rails respectively and only the 4Q switches Qa3, Qb3, and Qc3 need to be modulated to commute the appropriate



sinusoidal and in phase with the phase voltages. The modulation of the Unfolder switches is represented by a 3L waveform that denotes the position of the single-pole, triple-throw switch.

The 360° grid period is broken into 12 sectors that each described by a number and letter. Out of all possible combinations of the Unfolder switch positions, only 6 unique combinations are used and each one has been assigned a number 1 through 6. The letter for each sector (“P” or “N”) denotes which port of the Unfolder should be processing more power. For example, a grid angle of 15° falls into sector “1N” meaning that the Unfolder is currently commutating in position “1” (grid phase A to Unfolder rail O, phase B to rail N, and phase C to rail P) and that  $v_{on} > v_{po}$  or sector “N”.

It is important to understand that the Unfolder is not capable of controlling the amount of current or power processed by the Unfolder. The power flow is entirely controlled by the 3-port dc-dc converter connected to the soft dc-link. Therefore, it is also the role of the dc-dc converters to provide the PFC correction with the grid as well as providing minimal THD. The dc-dc converters must draw piece-wise sinusoidal input currents, so that the reflected grid current appears sinusoidal after the unfolder muxes the soft dc-link rails to the appropriate grid phase.

An advantage to the unfolding approach is the reduction in size of the input filter when compared with the two-stage approach [5]. The soft dc-link is populated with some capacitance (typically much less than the dc-link of a two-stage) to filter in the HF switching ripple of the 3-port dc-dc converter. The input of the Unfolder can be connected with the grid through a series inductance,  $L_g$  of much smaller value than required for a two-stage AFE. However, the HF switching ripple on the soft dc-link capacitance can be problematic around Unfolder sector crossovers.

Excessive negative voltage across the terminals of a soft dc-link port will forward-bias the body diodes present in the T-type switching legs of the dc-dc converters. The conduction path formed by the diodes temporarily shorts the Unfolder phases and distorts the average voltage impressed on the grid filter inductors causing a current distortion around sector

crossovers. One novel solution to this problem [11], uses pulse width modulation (PWM) control on the 4Q injector switches to mitigate the voltage distortion impressed on the grid inductors. Other solutions include minimizing the ripple voltage on the soft dc-link by using interleaved dc-dc modules to achieve ripple cancellation and increasing the effective modulation frequency.

### 2.3 Literature Review of Unfolding Based Rectification

This section is intended to review the different topologies that have been employed in literature to function as the 3-port dc-dc converter intended to operate with the Unfolder. A topology can be considered isolated if there is galvanic isolation between the input and output terminals. For safety and improved interoperability of different systems, isolation is preferred for battery charging applications [12, 13]. Isolated topologies can also be modularized and series stacked on the input or output to increase the voltage rating of the converter, and this concept is utilized in the design of 350 kW in Section 5.

One of the first approaches to implement the 3-port dc-dc converter used two, isolated, dc-dc converters to independently process the power from each soft dc-link port [14]. The dc-dc topology chosen was the Dual Active Bridge Series Resonant Converter (DABSRC). The DABSRC modules were paralleled at the output so the combined power appears constant to the dc load; however, each dc-dc modules processed a time-varying power. This method was effective for control but the design of the dc-dc modules was challenging due to the wide voltage variation required by each module and components in each modules must be rated to withstand the peak power of the load and on average only deliver half of the power.

Another approach is to combine the two independent dc-dc modules into a single 3-port dc-dc modules. A non-isolated topology example of this is the Swiss Rectifier which utilizes the 3L implementation of the buck converter topology [15]. This topology has incredibly high efficiency in literature [16] due to the high device utilization and the direct power flow from soft dc-link to output owing to the lack of a HF isolation transformer.

There have been several attempts to derive an isolated version of the Swiss rectifier. In [17] the 3L forward converter topology is adopted and utilizes two HF transformers.

In [18] two full bridge structures are proposed to process the power from each soft dc-link port and again two HF isolation transformers are required. The outputs of transformers are in series and connected to the diode rectifier and LC output filter, and the proposed modulation is based of the phase shift full bridge topology. In [19] the triple active bridge is introduced and a modulation scheme is presented to soft-switch all switching devices. The triple active bridge utilizes two HF transformers and can be used to series stack in the inputs and operate with an Unfolder fed from medium voltage [5]. Finally, in [20] the 3-level asymmetric full bridge (3LAFB) topology was introduced which uses a 3L T-type full bridge to drive one HF transformer from both soft dc-link inputs simultaneously.

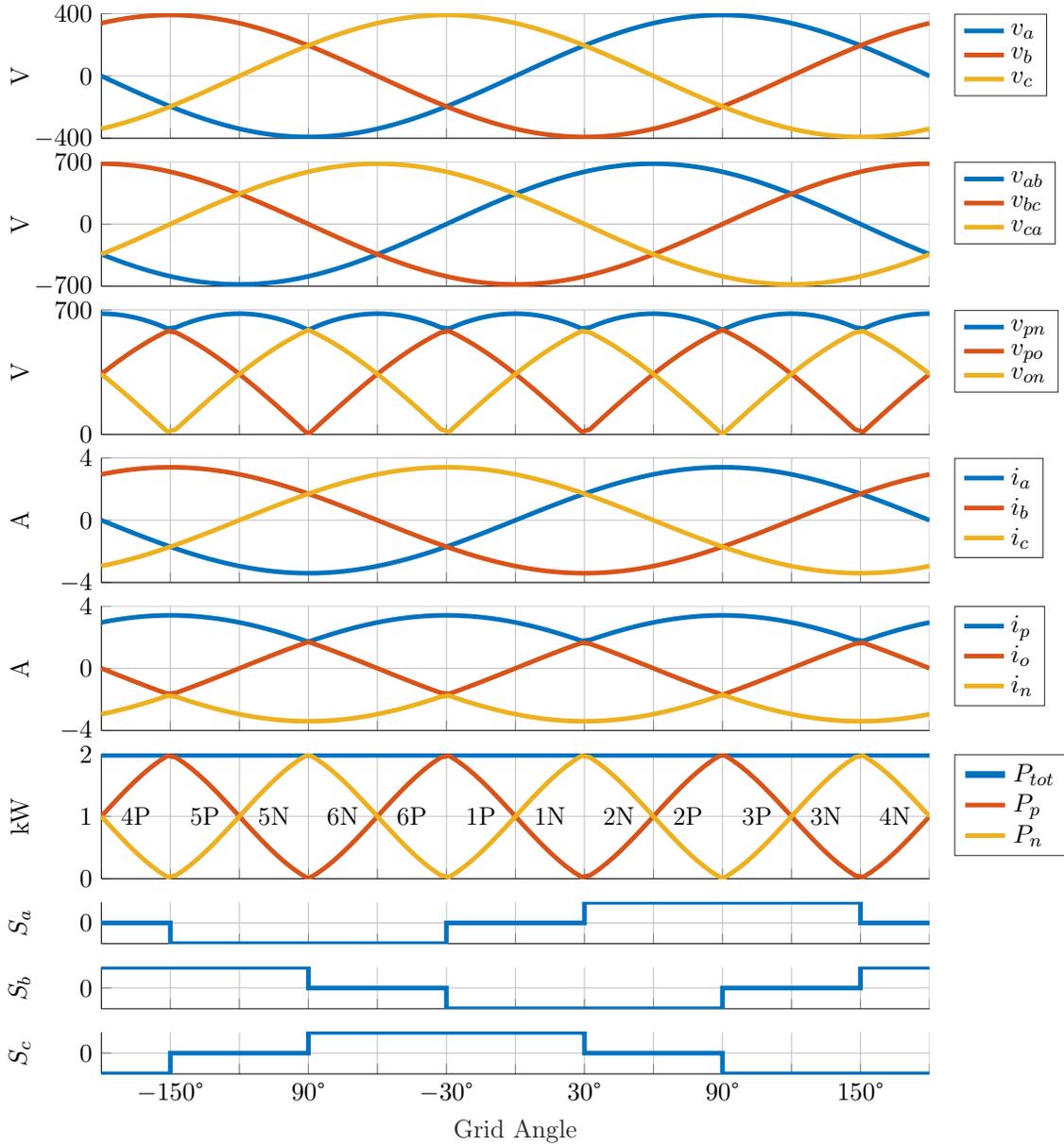


Fig. 2.3: Ideal waveforms for a 2kW Unfolder fed from a 480 V utility. The first two subplots show the phase and line-line input voltage. The unfolded voltage waveforms are shown in subplot 3. The fourth subplot shows the grid currents. The fifth subplot shows the piecewise sinusoidal currents drawn from the soft dc-link by the 3-port dc-dc converter. The sixth plot shows the instantaneous power drawn by the dc-dc. The last three plots show the modulation of the Unfolder by specifying the position of the single-pole, triple-throw switches.

## CHAPTER 3

## THREE-LEVEL ASYMMETRIC FULL BRIDGE (3LAFB)

The first topology of interest is the 3LAFB. The 3LAFB, proposed in [20] (Appendix A.1) and shown in Fig. 3.1, is a novel 3-port dc-dc candidate need for unfolding-based rectification. This topology excels in battery charging applications due to the high-efficiency achievable over a wide variation in output voltage. The operation of the 3LAFB is similar to the phase shifted full bridge (PSFB) topology with the primary side full bridge replaced with a 3-level (3L), T-type, full bridge. To distinguish this topology from 3-level PSFB operating with balanced dc inputs, the asymmetry in the soft dc-link voltages gives the topology the name 3-level asymmetric full fridge (3LAFB).

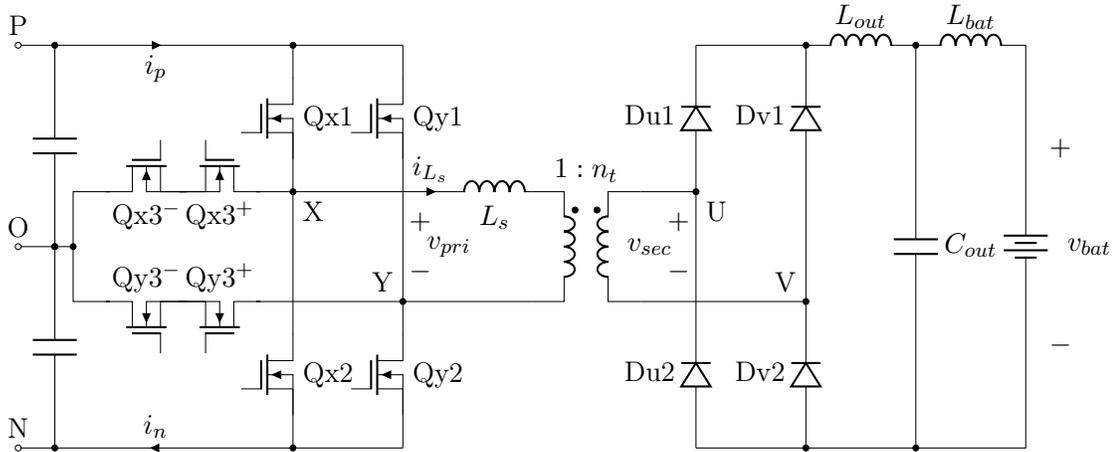


Fig. 3.1: The 3LAFB topology with diodes as the rectification devices and transformer leakage inductance  $L_s$  shown on the primary side of the transformer. Each T-type switching leg of the 3LAFB contains 4 devices: 2 H-bridge switches ( $Q_{x1}$ ,  $Q_{x2}$ ) and 2 back-back switches ( $Q_{x3^+}$ ,  $Q_{x3^-}$ ).

This chapter opens with a brief introduction on the basic operation of the 3LAFB topology. A detailed description of the control parameters and modulation implementation is presented to highlight the unique challenge presented by asymmetric input voltages. Switch

network averaging is applied to develop an intuitive large-signal non-linear model. The model is linearized and the controller design for the ac-dc operation is discussed. Finally, hardware results from a 2kW prototype are given to validate the proposed high-efficiency design and control approach.

### 3.1 Topology Description

The 3LAFB topology shown in Fig. 3.1 is a 3-port dc-dc with galvanic isolation between the dc output on the secondary and soft dc-link input provided by an Unfolder. This section covers the basic operation and control parameters for the 3LAFB. The modulation implementation is described in detail. The challenges of the secondary voltage ringing and clamping methods are discussed and referenced.

#### 3.1.1 Operating Principle

The asymmetry in the input voltage is owing to the soft dc-link voltage waveforms produced by the Unfolder commutating the 3-phase utility. The two input ports of the 3LAFB are between Unfolder nodes P-O and O-N, and they are denoted as the p-port and n-port respectively. The output port is connected across the EV battery which is on secondary side of the HF transformer to provide electrical isolation between the input and output.

A new modulation scheme was proposed in [20] which allows for all semiconductor devices to be soft switched. The proposed modulation scheme is similar to the traditional duty PWM methods; however, there are two different control parameters denoted as  $d_p$  and  $d_n$  which are the duty cycles for the p-port and n-port respectively. The modulation also has another consideration which is whether  $d_p$  is greater than  $d_n$  or vice versa. If  $d_p > d_n$  then the 3LAFB is modulating in sector p otherwise sector n. When the applied duties are equal in magnitude, then the concept of sector p and n does not effect the modulation waveforms, but only the gating signals.

The proposed modulation scheme for sector p, shown in Fig. 3.2, gives insight on how duty cycles affect the transformer voltage and input current waveforms. The diode rectifier

on the secondary bridge is connected to a LC output filter which rectifies the HF transformer voltage into a constant DC output. This topology utilizes the parasitic leakage inductance of the transformer (or externally added a series inductance) denoted as  $L_s$  to assist in the soft switching of the semiconductor devices.

Note that the rising edge of the  $v_{xy}$  waveform switches the voltage from the zero state (0 V) to the full soft dc-link potential ( $v_{po} + v_{on}$ ). This is accomplished by switching a single T-type leg from the P rail to the N rail. The alignment of the switching transition from the P rail to the O rail with the switching transition from the O rail to the N rail is essential for soft switching all devices. This is because the energy stored in the ZVS inductor which is required to soft switch the transition begins to diminish with the switching transition from the P rail to the O rail.

During the zero-state, where no voltage is applied to primary side of the transformer, the current flowing through the ZVS inductance,  $L_s$ , free-wheels through only two H-bridge devices. In the case of sector p ( $d_p > d_n$ ) shown in Fig. 3.2 the devices connected to the P rail are both conducting during the zero-state which is superior to free-wheeling through the back-back devices because there are less devices (hence lower  $R_{ds,on}$ ) in the conduction path when free-wheeling through just H-bridge devices.

Modulation for sector n ( $d_n > d_p$ ) operates in a mirrored fashion of sector p where the devices connected to the n-rail conduct during the free-wheeling period. The only time the back-back devices need to conduct is when the applied duty cycles for the p and n ports are unequal. Unequal duty cycles are essential for drawing different input currents from each port for the PFC regulation.

Similar to the PSFB topology, the 3LAFB incurs a duty cycle loss while the current in the ZVS inductance changes polarity which happens twice every switching period. The duty cycle loss affects the applied duty's for both input ports resulting in less average input current. Furthermore, the duty cycle loss reduces the voltage applied to the secondary side of the transformer.

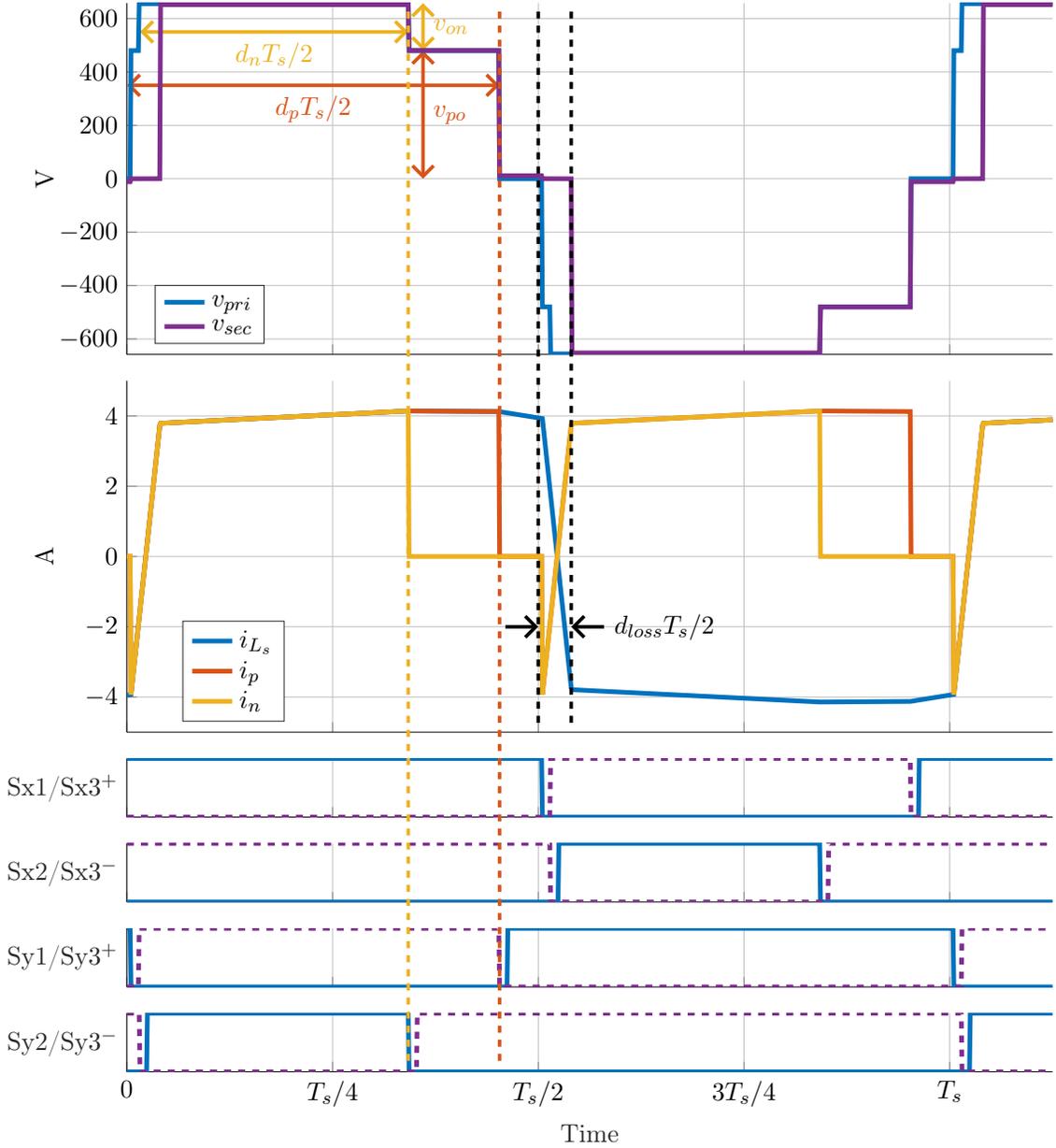


Fig. 3.2: Idealized 3LAFB simulation waveforms for operating point “b” when operating in a sector p (i.e.  $d_p > d_n$ ). The first subplot contains the transformer voltages on the primary and secondary side of the transformer. The second plot shows the transformer current as well as the input currents for the two input ports of the 3LAFB. The last 4 plots give the gating signals required to produce the primary voltage waveform and soft switch all devices. The H-bridge switches have their gating signal given in the solid waveform while the corresponding complimentary switch gating signal are shown by the dashed lines.

### 3.1.2 Modulation Implementation

The primary bridge of the 3LAFB contains eight active switches and requires only 4

unique gating signals to modulate the H-bridge devices while the back-back switches need to be driven with the complement of their H-bridge switches. The T-type switching leg functions equivalent to two H-bridges stacked in series, but there is a more complicated modulation structure to ensure soft switching of all devices, namely the back-back switches.

For simplicity, only sector p is discussed in this section; however, modulation for sector n operates in a mirrored fashion. During the rising edge of the  $v_{xy}$  voltage, the voltage potential of one switching leg swings from the P rail to the N rail. In the case of equal voltages on the soft dc-link ports, the switches  $Q_1$  and  $Q_3^-$  turn off synchronously, and the current that was free-wheeling in the ZVS inductance discharges the parasitic output capacitance of  $Q_2$  and  $Q_3^+$  while charging the capacitance across  $Q_1$  and  $Q_3^-$ . By the end of the dead time, owing to the symmetry in the input voltages, the switches  $Q_2$  and  $Q_3^+$  can be turned on with zero volts synchronously.

However, consider that the p-port has higher voltage than the n-port. If the switches  $Q_1$  and  $Q_3^-$  were to turn off synchronously, then by the end of the dead time the capacitance of switch  $Q_2$  would be discharged to zero volts while  $Q_3^+$  would have only been partially discharged. When the switches  $Q_2$  and  $Q_3^+$  are turned on then the energy stored in the output capacitance of  $Q_3^+$  is dissipated through the device.

To deal with the asymmetry in soft dc-link voltages, the transition from the P rail to N rail is slightly staggered so that the back-back switches are completely soft switched. This is accomplished by first turning off  $Q_1$  and letting the voltage across  $Q_3^+$  completely discharge before turning off  $Q_3^-$ . Once  $Q_3^-$  is turned off, the voltage across  $Q_2$  will begin to be discharged to 0 V and can be turned on. This stagger that has been introduced is on the order of the dead-time and should not have a significant affect the behavior of the switching bridges during normal operation. Furthermore, this stagger should not be so long that all of the energy in the ZVS inductor is lost during the first transition from the P rail to the O rail; otherwise, the transition from the O rail to the N rail would be hard switched.

It is worth noting that the stagger cannot be introduced when the applied duty cycles are equal. This is due to the fact that the stagger decreases the applied duty for the staggered

port, and therefore the max staggering is limited by the difference in applied duty. If the difference in applied duty is greater than the dead time then the stagger should be limited to the dead-time. Due to the nature of the topology, the applied duty's are only equal when the the soft dc-link voltages are equal. In that case the stagger is not needed due to the symmetry in input voltages.

Up to this point, modulation in sector p has been covered, yet modulation in sector n is symmetrical so it has also been covered. However, the transition between sectors p and n has not been mentioned. A unique switching pattern is required for the sector crossover transition. This is due to the fact that the H-bridge switches are used for the free-wheeling or zero-state portions of the switching period.

These unique transitions occur when the duty cycles are very close in magnitude, so the applied duties to the p-port and n-port are equal during the sector crossover transition. Furthermore, the unique transitions still soft switch all primary devices. For the transition from sector p to sector n, the modulation sequence begins in sector p as normal, leg y transitions from the P rail to the N rail in order to apply positive voltage to the transformer. The transition back to the zero state occurs after the applied duty via leg x transitioning to the N rail as opposed to the y rail transiting back to the P rail as it normally would during modulation in sector p. After this simple transition, the remaining portion of the period is modulated as if it were in sector n. This means that at  $T_s/2$  leg y will transition to the P rail. After the appropriate duty has been applied, leg y transitions back to the N rail and the next modulation sequence is ready to begin in sector n because both the bottom devices are free-wheeling the ZVS inductor current.

### 3.1.3 Secondary Voltage Ringing

A major drawback/challenge in the design of this topology is the voltage ringing that occurs across the secondary rectifier which is common to most isolated buck-derived topologies with an inductive output filter. The problem arises when the secondary side of the transformer is excited by the primary. The parasitic output capacitance of the diodes that are not conducting are initially at 0V and need to be charged to the reflected primary

voltage. The diodes' output capacitance on the rectifier form and LC circuit with the series inductance in the tank which is excited further by any reverse recovery of the diodes. The ringing across the diodes is not clamped by the output voltage owing to the large output inductor,  $L_{dc}$ . The ringing observed across the devices can reach levels in excess of twice the reflected primary voltage which causes severe voltage stress on the diodes. This high stress leads to device failures or use of higher voltage devices which lowers device utilization and impacts overall efficiency/cost.

To deal with secondary voltage ringing, there have been numerous proposed solutions in literature such as lossy RCD snubbers [21], inductive clamp methods [22], and active clamps which try to recapture the oscillating energy [23]. The method adopted for the 3LAFB hardware prototype utilized a third transformer winding coupled tightly with the secondary winding which was clamped to the input of the soft dc-link via diodes. This method succeeded in reducing the voltage spike which occurs on the secondary rectifier without dissipating the ringing energy as it done in a simple RCD snubber circuit.

The clamp winding was able to limit the ringing during the transition from the zero state to the full reflected soft dc-link potential; however, it was not able to reduce the ringing when switching from the full soft dc-link input to a single port of the soft dc-link. That is to say that in sector p, when the applied voltage to the primary of the transformer transitions from  $v_{po} + v_{on}$  to just  $v_{po}$ , the secondary side voltage rings about  $v''_{po}$ . This is not a problem in terms of applied voltage stress on the components; however, the ringing in the voltage waveform changes the average voltage applied to the secondary.

This becomes a problem when operating with ac input and the applied duties are changing in order to maintain output power regulation and PFC. When the applied duty cycles are equivalent this problem does not occur, because there is no time where only one port of the soft dc-link is applied to the output. On the other hand, when the applied duties are very different there is enough time for the voltage ringing about  $v''_{po}$  or  $v''_{on}$  to settle; in other words, the applied average voltage is correct. However, when the applied duty's are different but close in magnitude, there is an interaction between the frequency of the ringing

and the applied duties which distorts the average voltage applied to the LC filter on the output. This phenomenon was observed in hardware as a ripple in the output voltage which was not able to be attenuated by the regulators or feed-forward control.

### 3.2 Averaged Switch Modeling and Control of the 3LAFB

In order to gain increased insights on the control and dynamic response of the 3LAFB topology, circuit averaging over a switching period is performed to derive the averaged switch network model. The averaged switch network model replaces the switch network in the 3LAFB topology. For further insight into model the large signal non-linear circuit is linearized around a quiescent operating point.

Due to the ac input voltage and the Unfolder, the input voltage to the soft dc-link is not dc, and a single operating point cannot describe dynamic behavior for the system over the entire line cycle. A quasi-static approximation of the system is made because the dynamics of the power converter system is much faster than of the low frequency oscillation of the grid. The dynamics can be analyzed for different input voltages which occur with the unfolding approach and stability can be checked at each one individually.

The linearized circuit can be analyzed using standard circuit analysis to find the dc solution as well as transfer functions of interest such as the response of the output voltage to perturbations from each of the duty cycle control variables. Following a quasi-static modeling approach, the system dynamics are analyzed considering different input voltages that occur during normal operation while being fed from a 480 V Unfolder.

#### 3.2.1 3LAFB Switch Network Averaging

$$I_2 = \langle i_2 \rangle_{T_s} \quad (3.1)$$

$$V_{1p} = \langle v_{1p} \rangle_{T_s} \quad (3.2)$$

$$V_{1n} = \langle v_{1n} \rangle_{T_s} \quad (3.3)$$

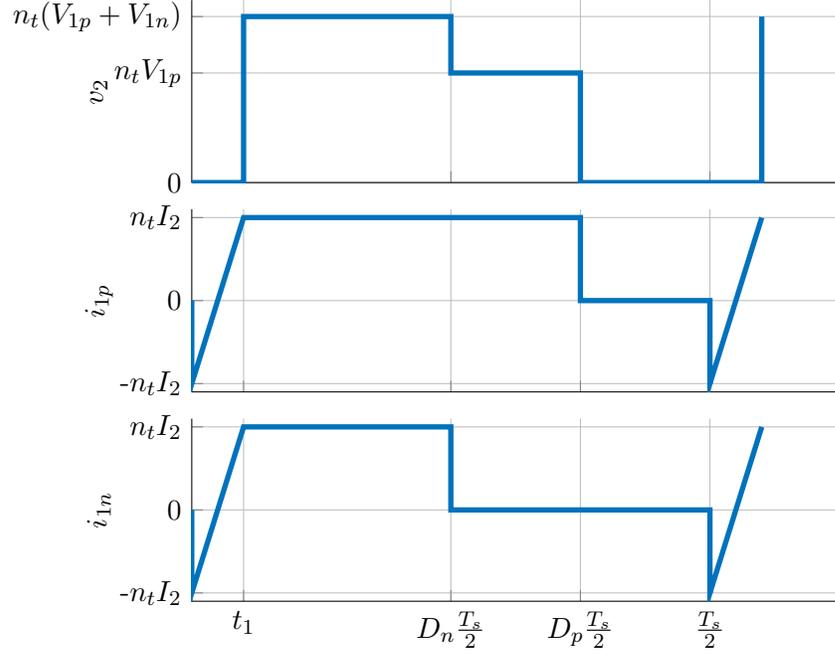


Fig. 3.3: The terminal waveforms for the input currents and output voltage of the 3LAFB switch network.

$$\langle v_2 \rangle_{T_s} = d_p n_t \langle v_{1p} \rangle + d_n n_t \langle v_{1n} \rangle - \frac{2t_1}{T_s} n_t (\langle v_{1p} \rangle + \langle v_{1n} \rangle) \quad (3.4)$$

$$\langle i_{1p} \rangle_{T_s} = d_p n_t \langle i_2 \rangle - \frac{2t_1}{T_s} n_t \langle i_2 \rangle \quad (3.5)$$

$$\langle i_{1n} \rangle_{T_s} = d_n n_t \langle i_2 \rangle - \frac{2t_1}{T_s} n_t \langle i_2 \rangle \quad (3.6)$$

$$t_1 = 2L_s \frac{n_t \langle i_2 \rangle}{\langle v_{1p} \rangle + \langle v_{1n} \rangle} \quad (3.7)$$

$$R_e \triangleq \frac{4L_s n_t^2}{T_s} \quad (3.8)$$

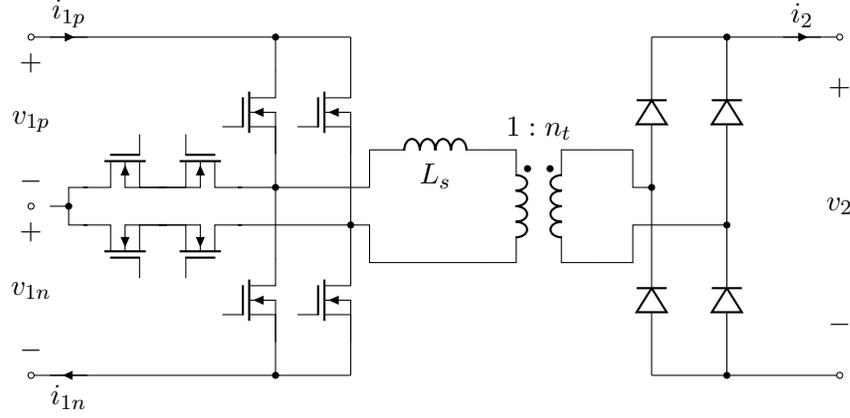


Fig. 3.4: The switch network for the 3LAFB topology.

$$\langle v_2 \rangle_{T_s} = d_p n_t \langle v_{1p} \rangle + d_n n_t \langle v_{1n} \rangle - R_e \langle i_2 \rangle \quad (3.9a)$$

$$\langle i_{1p} \rangle_{T_s} = d_p n_t \langle i_2 \rangle - R_e \frac{\langle i_2 \rangle^2}{\langle v_{1p} \rangle + \langle v_{1n} \rangle} \quad (3.9b)$$

$$\langle i_{1n} \rangle_{T_s} = d_n n_t \langle i_2 \rangle - R_e \frac{\langle i_2 \rangle^2}{\langle v_{1p} \rangle + \langle v_{1n} \rangle} \quad (3.9c)$$

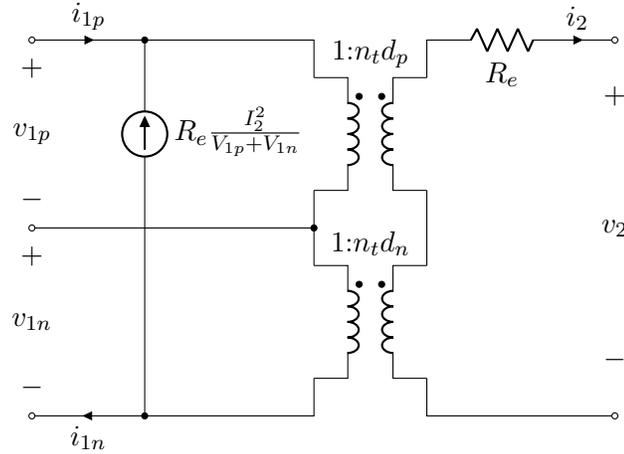


Fig. 3.5: The large signal, nonlinear averaged switch network for the 3LAFB topology.

### 3.2.2 Perturbation and Linearization

The first step in linearization is to replace all time-varying quantities by their average value plus the small-signal deviation. Doing so results in the following expressions. The small-signal quantities are denoted with a (^) character and DC quantities are capitalized as a convention.

$$\langle v_2 \rangle_{T_s} = V_2 + \hat{v}_2 \quad (3.10a)$$

$$\langle i_2 \rangle_{T_s} = I_2 + \hat{i}_2 \quad (3.10b)$$

$$\langle v_{1p} \rangle_{T_s} = V_{1p} + \hat{v}_{1p} \quad (3.10c)$$

$$\langle v_{1n} \rangle_{T_s} = V_{1n} + \hat{v}_{1n} \quad (3.10d)$$

$$\langle i_{1p} \rangle_{T_s} = I_{1p} + \hat{i}_{1p} \quad (3.10e)$$

$$\langle i_{1n} \rangle_{T_s} = I_{1n} + \hat{i}_{1n} \quad (3.10f)$$

$$d_p = D_p + \hat{d}_p \quad (3.10g)$$

$$d_n = D_n + \hat{d}_n \quad (3.10h)$$

By plugging 3.10 into 3.9 the solution for the dc operating point can be separated from the first order terms, and higher order products of small signal quantities can be neglected under the small-signal assumption. The resulting dc solution is given:

$$V_2 = D_p n_t V_p + D_n n_t V_n - R_e I_2 \quad (3.11a)$$

$$I_{1p} = D_p n_t I_2 - R_e \frac{I_2^2}{V_{1p} + V_{1n}} \quad (3.11b)$$

$$I_{1n} = D_n n_t I_2 - R_e \frac{I_2^2}{V_{1p} + V_{1n}} \quad (3.11c)$$

The two objectives of the 3LAFB control are to maintain regulation of the output power, and PFC on the input. Output power regulation is achieved by maintaining a DC output current reference,  $i_{out}^{ref}$  or voltage reference,  $v_{out}^{ref}$ . The PFC regulation is achieved

by maintaining the correct ratio of input currents,  $i_{p/n}^{ref} = I_{1p}/I_{1n}$ . The input current ratio reference,  $i_{p/n}^{ref}$ , is determined by the instantaneous input voltages of the grid. This behavior ensures that input phase currents drawn from the grid are proportional to the grid phase voltage (after unfolding), and thus would appear as a resistive load to the grid. Note that the absolute value of input current is not being regulated by the PFC loop in order to weaken the coupling between the output regulation and input current shaping. The two objectives are formulated mathematically by the following equations.

$$V_2 = v_{out}^{ref} = R_{out}i_{out}^{ref} = V_{bat} + R_{bat}i_{out}^{ref} \quad (3.12a)$$

$$i_{p/n}^{ref} = \frac{\max(v_{abc})}{|\min(v_{abc})|} = \frac{I_{1p}}{I_{1n}} \quad (3.12b)$$

$$i_{p/n}^{ref} = \frac{D_p n_t I_2 - R_e \frac{I_2^2}{V_{1p} + V_{1n}}}{D_n n_t I_2 - R_e \frac{I_2^2}{V_{1p} + V_{1n}}} \quad (3.12c)$$

Here 3.12a is extended to show the relationship between the voltage on the output port  $V_2$  as and the voltage and current references for both resistive load ( $R_{out}$ ) and voltage source load ( $R_{bat}$  and  $V_{bat}$ ). With the two reference equations, the two steady-state duty cycles can be computed. The dc conversion ratio,  $M$ , for the 3LAFB is defined by the ratio of the output voltage to the sum of the soft dc-link voltage ports. The equivalent output resistance,  $R_o$ , is defined as the ratio of the output voltage to output current.

$$M \triangleq \frac{V_2}{V_{1p} + V_{1n}} \quad (3.13)$$

$$R_o \triangleq \frac{V_2}{I_2} \quad (3.14)$$

$$D_\Delta \triangleq (1 - i_{p/n}^{ref}) \frac{R_e I_2}{n_t (V_{1p} + V_{1n})} = (1 - i_{p/n}^{ref}) \frac{M R_e}{n_t R_o} \quad (3.15)$$

$$D_p = i_{p/n}^{ref} D_n + D_\Delta \quad (3.16)$$

A new variable is defined,  $D_\Delta$  to simplify the resulting expressions. Plugging 3.16 into 3.11a, the steady state solution to the duty cycles can be obtained.

$$D_n = \frac{V_2(1 + \frac{R_e}{R_o}) + n_t V_{1p} D_\Delta}{n_t(i_{p/n}^{ref} V_{1p} + V_{1n})} \quad (3.17a)$$

$$D_p = i_{p/n}^{ref} D_n + D_\Delta \quad (3.17b)$$

These solutions can be used as feed-forward terms to operate the 3LAFB in open loop with unfolded ac input voltage. These solutions can also be used to investigate the small signal dynamics about the dc operating points. The resulting small signal dynamics of the averaged 3LAFB switch network are given below.

$$\hat{v}_2 = n_t(D_p \hat{v}_{1p} + V_{p1} \hat{d}_p + D_n \hat{v}_{1n} + V_{n1} \hat{d}_n) - R_e \hat{i}_2 \quad (3.18a)$$

$$\hat{i}_{1p} = n_t(D_p \hat{i}_2 + I_2 \hat{d}_p) - R_e \left( \frac{2I_2}{V_{1p} + V_{1n}} \hat{i}_2 - \frac{I_2^2}{(V_{1p} + V_{1n})^2} (\hat{v}_{1p} + \hat{v}_{1n}) \right) \quad (3.18b)$$

$$\hat{i}_{1n} = n_t(D_n \hat{i}_2 + I_2 \hat{d}_n) - R_e \left( \frac{2I_2}{V_{1p} + V_{1n}} \hat{i}_2 - \frac{I_2^2}{(V_{1p} + V_{1n})^2} (\hat{v}_{1p} + \hat{v}_{1n}) \right) \quad (3.18c)$$

The linearization of the output voltage equation resulted in a dc transformer with independent voltage sources controlled by duty cycle perturbations and the equivalent series output resistance remained. Linearization of the input current equations resulted in a dc transformer paired with an independent current source controlled by the duty cycle perturbation of the respective port. Additional terms arise to account for the duty cycle loss which are manifested as a parallel input resistance,  $R_{in}$ , and dependent current source based on output current with a gain factor of,  $C_1$ .

$$C_1 \triangleq 2M \frac{R_e}{R_o} \quad (3.19)$$

$$R_{in} \triangleq \frac{1}{M^2} \frac{R_o^2}{R_e} \quad (3.20)$$

The circuit representation of the 3LAFB small signal dynamics from 3.18 are given in Fig. 3.6. The linearized switch network is substituted back into the original circuit replacing the original switch network. The resulting circuit with the variables renamed is given in Fig. 3.7.

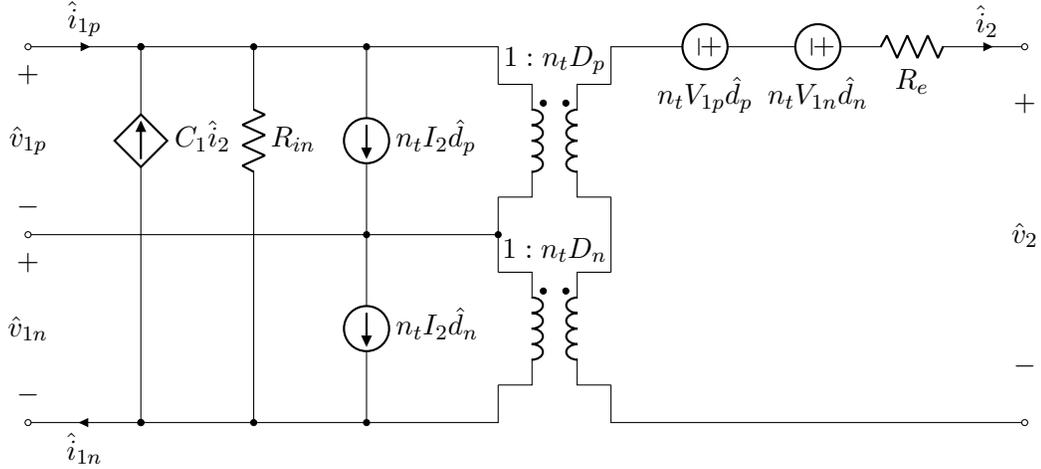


Fig. 3.6: The linearized small signal model of the averaged switch network for the 3LAFB topology.

The resulting second order system is now linear and time-invariant and can be solved using traditional circuit analysis. Note that this circuit does not consider the ac input from the Unfolder and should only be used to investigate the dynamics under the quasi-static approximation which considers dc input voltages. This assumption is valid due to time separation between slow changing ac input and the HF switching dynamics of the 3LAFB.

### 3.2.3 State Space Formulation and Transfer Functions

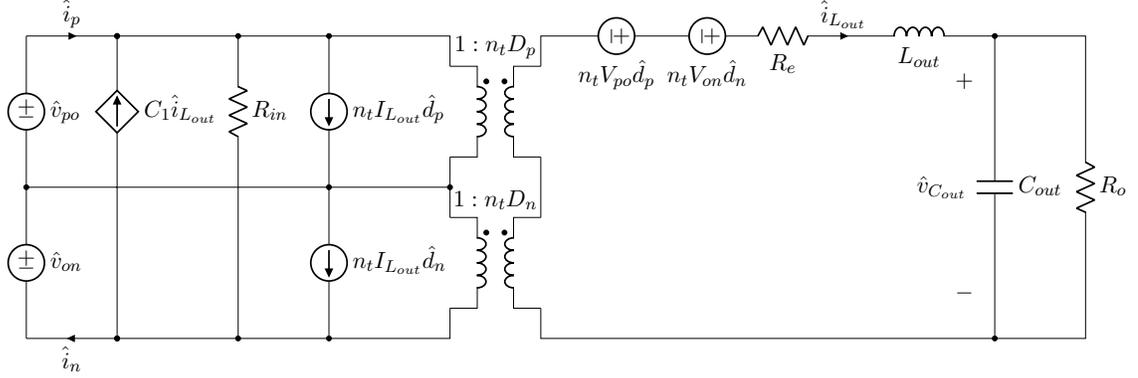


Fig. 3.7: The 3LAFB topology with the switch network replaced with the linearized small signal model of the averaged switch network.

This section formulates the small signal dynamics of the 3LAFB in state space representation. The 3LAFB has two state variables which are the output inductor current and output capacitor voltage. The two control inputs are placed into the duty cycle vector,  $\hat{\mathbf{d}}$ , and input voltages are given the  $\hat{\mathbf{u}}$ . The output of the system,  $\hat{\mathbf{y}}$ , is taken to be the input currents. The following equations are formal definitions for each vector.

$$\hat{\mathbf{x}} = \begin{bmatrix} \hat{i}_{L_{out}} \\ \hat{v}_{C_{out}} \end{bmatrix}, \quad \hat{\mathbf{d}} = \begin{bmatrix} \hat{d}_p \\ \hat{d}_n \end{bmatrix}, \quad \hat{\mathbf{u}} = \begin{bmatrix} \hat{v}_{po} \\ \hat{v}_{on} \end{bmatrix}, \quad \hat{\mathbf{y}} = \begin{bmatrix} \hat{i}_p \\ \hat{i}_n \end{bmatrix} \quad (3.21)$$

With the state, inputs, and outputs well defined the dynamics can be written in a the standard state-space representation. Following basic circuit analysis on Fig. 3.7 the resulting dynamics can be expressed in matrix format.

$$\frac{d\hat{\mathbf{x}}}{dt} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{F}\hat{\mathbf{d}} + \mathbf{B}\hat{\mathbf{u}} \quad (3.22a)$$

$$\hat{\mathbf{y}} = \mathbf{C}\hat{\mathbf{x}} + \mathbf{G}\hat{\mathbf{d}} + \mathbf{E}\hat{\mathbf{u}} \quad (3.22b)$$

With the matrices defined as,

$$\begin{aligned}
\mathbf{A} &= \begin{bmatrix} \frac{R_e}{L_{out}} & \frac{-1}{L_{out}} \\ \frac{1}{C_{out}} & \frac{-1}{R_o C_{out}} \end{bmatrix}, & \mathbf{F} &= \begin{bmatrix} \frac{n_t V_{po}}{L_{out}} & \frac{n_t V_{on}}{L_{out}} \\ 0 & 0 \end{bmatrix}, & \mathbf{B} &= \begin{bmatrix} \frac{D_p n_t}{L_{out}} & \frac{D_n n_t}{L_{out}} \\ 0 & 0 \end{bmatrix} \\
\mathbf{C} &= \begin{bmatrix} D_p n_t - C_1 & 0 \\ D_n n_t - C_1 & 0 \end{bmatrix}, & \mathbf{G} &= \begin{bmatrix} n_t I_2 & 0 \\ 0 & n_t I_2 \end{bmatrix}, & \mathbf{E} &= \begin{bmatrix} \frac{1}{R_{in}} & \frac{1}{R_{in}} \\ \frac{1}{R_{in}} & \frac{1}{R_{in}} \end{bmatrix}
\end{aligned} \tag{3.23}$$

With the small-signal state space representation of the 3LAFB dynamics, the transfer functions can be defined using standard techniques. For example, to find the transfer function from duty cycle perturbations to input currents the following equations will result in 2x2 matrix of transfer functions since there are two duty cycles and two input currents that are of interest.

$$\mathbf{W}_{id} \triangleq \begin{bmatrix} \hat{i}_p \\ \hat{d}_p \\ \hat{i}_n \\ \hat{d}_n \end{bmatrix} = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{F} + \mathbf{G} \tag{3.24}$$

Another transfer function of interest in the controller design is response of the output voltage to perturbations in the output inductor current. This transfer function is useful for designing an outer voltage loop around an inner current loop which is regulating the output inductor current. This transfer function can be described in terms of elements from the  $\mathbf{A}$  matrix.

$$G_{vi} \triangleq \frac{\hat{v}_{C_{out}}}{\hat{i}_{L_{out}}} = \frac{a_{21}}{s - a_{22}} \tag{3.25}$$

### 3.2.4 Controller Design

The controller design for the 3LAFB operating with ac input is a combination of feed-forward with traditional proportional integral (PI) and integral (I) controllers. The two control objectives are to regulate the output power delivered to the battery and to provide PFC on the ac input. The output power control is implemented as a current controller which is typical for battery charging applications. The PFC controller is responsible for

keeping the power factor of the input power close to unity as well as minimizing the THD. The control inputs are the duty cycles  $d_p$  and  $d_n$ .

The duty cycle control variables affect the operation of each loop which makes it difficult to regulate the duties directly with single-input single-output (SISO) controllers. To weaken the coupling between the control loops, new control variables have been defined:  $v_{mag}$  and  $d_{p/n}$ .

The decoupled control variable for the output regulator,  $v_{mag}$ , is used to determine how much average voltage should be applied to the transformer. Regardless of the time varying soft dc-link input, the output port of the converter should receive constant average voltage in steady state. The output control loop has a low bandwidth (100 Hz) integral controller,  $G_{c,out}$  which regulates  $v_{mag}$  based of the output current reference error. The feed-forward duty cycles are used to calculate  $v_{mag}^{FF}$  which is added to the output of the integral controller. The feed-forward term accounts for 360 Hz variations in the duty cycle loss which are introduced by the varying magnitude of the soft dc-link.

The decoupled control variable for the PFC regulator,  $d_{p/n} = d_p/d_n$  is simply the ratio of applied  $d_p$  to  $d_n$ . This control variable adjusts the ratio of applied duties in order to maintain the ratio of input currents  $i_{p/n} = i_p/i_n$  to a desired value. The reference ratio of input currents,  $i_{p/n}^{ref}$ , is a dynamic reference that is determined by the input voltages. The ratio of the highest grid phase voltage,  $v_p$ , with the lowest grid phase voltage  $v_n$  should align with the ratio of the p-port current,  $i_p$  with the n-port current,  $i_n$  for PFC. The instantaneous input voltages or the PLL angle can be used to calculate and set  $i_{p/n}^{ref}$ . Using the PLL angle is less sensitive to sensing noise and the angle can be adjusted to draw phase shifted input currents. The integral controller for the PFC loop,  $G_{c,PFC}$  sets the duty cycle ratio  $d_{p/n}$  based on the sensed error in ratio of input currents. Again, the output of the regulator is complemented by a feed-forward term which accounts for duty cycle loss.

The duty cycle ratio determines the modulating sector of the 3LAFB. In sector p, the  $d_p$  duty is greater than the  $d_n$  and thus  $d_{p/n} > 1$ . To convert the  $v_{mag}$  control variable into a duty cycle, the term is normalized by the available soft dc-link voltage,  $v_{dc,pseudo}$ . The

normalizing term,  $v_{dc,pseudo}$ , is dependent on the current soft dc-link input voltages,  $v_{po}$  and  $v_{on}$ , as well as the duty ratio,  $d_{p/n}$ . The control variable  $v_{mag}$  is normalized to  $d_{mag}$  which is selected to be either  $d_p$  or  $d_n$  depending on the sector. The control loops are summarized by Fig. 3.8.

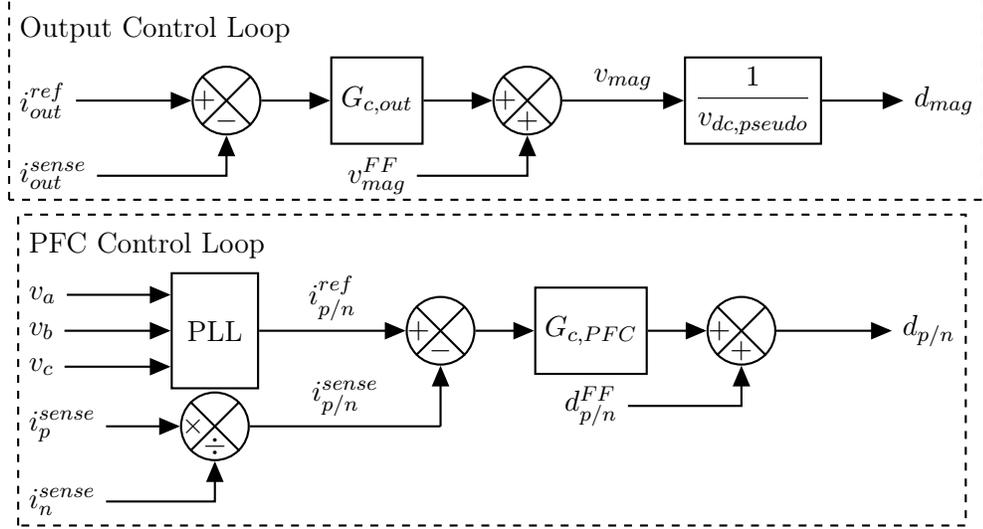


Fig. 3.8: The control block diagram for 3LAFB showing the independent control loops for output current and PFC.

The duty ratio,  $d_{p/n}$ , determines the modulation sector according to Table 3.1. The calculation of the  $v_{dc,pseudo}$  depends on  $d_{p/n}$  in order to weaken the coupling between the output and PFC loops. For example in sector p, the p-port duty can be at most 1 which means that the full p-port voltage,  $v_{po}$ , is part pseudo dc-link voltage. The n-port voltage also contributes to  $v_{dc,pseudo}$ ; however, the applied duty ratio must be respected so only a portion of the n-port voltage is available to be added to the  $v_{dc,pseudo}$  term based on the value of  $d_{p/n}$ . Now  $d_p$  is set directly by  $d_{mag}$  which is the slow regulated intermediate control variable,  $v_{mag}$  normalized by  $v_{dc,pseudo}$ . Finally,  $d_n$  can be calculated from  $d_p$  using the other intermediate control variable,  $d_{p/n}$ .

The design of the output current controller,  $G_{c,out}$ , and PFC controller,  $G_{c,PFC}$  is done using standard bode plot techniques. The output controller considers the transfer function,  $G_{iv}$  between the small signal perturbations in  $\hat{v}_{mag}$  to the output current  $\hat{i}_{out}$ . From simple

Table 3.1: Calculation of the actual control parameters from the decoupled control parameters for the 3LAFB.

Parameter	Sector p	Sector n
$d_{p/n}$	$d_{p/n} > 1$	$d_{p/n} < 1$
$v_{dc,pseudo}$	$v_{po} + \frac{v_{on}}{d_{p/n}}$	$v_{on} + d_{p/n}v_{po}$
$d_p$	$d_{mag}$	$d_{p/n}d_{mag}$
$d_n$	$\frac{d_{mag}}{d_{p/n}}$	$d_{mag}$

circuit analysis on Fig. 3.9, the decoupled control-to-output transfer function can easily be deduced.

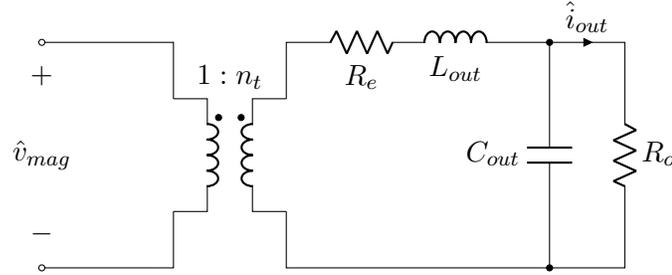


Fig. 3.9: The equivalent circuit for 3LAFB used to find the decoupled control-to-output transfer function,  $G_{iv}$ .

$$G_{iv} \triangleq \frac{\hat{i}_{out}}{\hat{v}_{mag}} = \frac{n_t}{R_e + R_o} \frac{1}{1 + \frac{R_e R_o C_{out} + L_{out}}{R_e + R_o} s + \frac{R_o C_{out} L_{out}}{R_e + R_o} s^2} \quad (3.26a)$$

$$= G_{iv,0} \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (3.26b)$$

$$G_{iv,0} = \frac{n_t}{R_e + R_o}, \quad \omega_0 = \sqrt{\frac{R_e + R_o}{R_o C_{out} L_{out}}}, \quad Q = \frac{1}{\omega_0} \frac{R_e + R_o}{R_e R_o C_{out} + L_{out}} \quad (3.26c)$$

An integral controller can easily be designed using the total uncompensated loop gain which accounts for the bandwidth of the feedback sensors,  $T_{u,out} = G_{iv} H_{sense,iout}$ . The crossover frequency of the system is targeted at a low bandwidth ( $>100$  Hz) in order to avoid stability issues with the grid or the PFC loop.

The design of the PFC controller uses a transfer function which gives the approximate behavior of the system at low frequencies,  $G_{id,p/n}$ . The approximation relies on the assumption that the output loop is decoupled from the PFC loop so that perturbations in  $\hat{d}_{p/n}$  do not cause perturbations in  $\hat{i}_{L_{out}}$ . Furthermore, the perturbations in  $\hat{v}_{po}$  and  $\hat{v}_{on}$  are ignored for a well designed input filter.

$$\hat{i}_{p/n} = \frac{\hat{i}_p}{\hat{i}_n} \quad (3.27a)$$

$$= \frac{n_t(D_p \hat{i}_{L_{out}} + I_{L_{out}} \hat{d}_p) - R_e \left( \frac{2I_{L_{out}}}{V_{po} + V_{on}} \hat{i}_{L_{out}} - \frac{I_{L_{out}}^2}{(V_{po} + V_{on})^2} (\hat{v}_{po} + \hat{v}_{on}) \right)}{n_t(D_n \hat{i}_{L_{out}} + I_{L_{out}} \hat{d}_n) - R_e \left( \frac{2I_{L_{out}}}{V_{po} + V_{on}} \hat{i}_{L_{out}} - \frac{I_{L_{out}}^2}{(V_{po} + V_{on})^2} (\hat{v}_{po} + \hat{v}_{on}) \right)} \quad (3.27b)$$

$$\approx \frac{n_t I_{L_{out}} \hat{d}_p}{n_t I_{L_{out}} \hat{d}_n} = \hat{d}_{p/n} \quad (3.27c)$$

$$G_{id,p/n} \triangleq \frac{\hat{i}_{p/n}}{\hat{d}_{p/n}} \approx 1 \quad (3.27d)$$

The resulting transfer function is simply a unity gain, so the total uncompensated loop gain for the PFC loop is  $T_{u,PFC} = H_{sense,i_{p/n}}$ . To achieve low THD and unity power factor, the ratio of input currents drawn by the 3LAFB are regulated to a dynamic reference,  $i_{p/n}^{ref}$  which has frequency of  $6f_{grid} = 360$  Hz. The feed-forward term should track the 360 Hz component; however, any errors in the model will be accounted for by the integral regulator,  $G_{c,PFC}$ , which is designed for a bandwidth of 1 kHz.

Revisiting the feed-forward equations from 3.12 and 3.17, the feed-forward terms,  $v_{mag}^{FF}$  and  $d_{p/n}^{FF}$  can be formally defined. The input and output voltage, equivalent resistance introduced by the duty cycle loss, output resistance, and the PFC input current reference ratio are required in the calculation of the feed-forward terms. Alternatively, the output current can be used instead of output resistance in the case of a voltage source load such as

a battery by replacing  $R_o = V_{out}/I_{out}$ .

$$D_n^{FF} = \frac{V_{out}(1 + \frac{R_c}{R_o}) + n_t V_{po} D_\Delta}{n_t (i_{p/n}^{ref} V_{po} + V_{on})} \quad (3.28a)$$

$$D_p^{FF} = i_{p/n}^{ref} D_n + D_\Delta \quad (3.28b)$$

$$d_{p/n}^{FF} = \frac{D_p^{FF}}{D_n^{FF}} \quad (3.28c)$$

$$v_{mag}^{FF} = \begin{cases} D_p^{FF} v_{dc,pseudo} & d_{p/n} \geq 1 \\ D_n^{FF} v_{dc,pseudo} & d_{p/n} < 1 \end{cases} \quad (3.28d)$$

One problem that arises with the PFC controller is the reactive 60 Hz current drawn from the grid. The impedance of the filter inductors is very small at 60 Hz which leads to a negligible phase shift between the soft dc-link voltage,  $v_{pon}$ , and the grid voltage,  $v_{abc}$ . However, the impedance of the soft dc-link capacitors draws current that is leading the grid voltage by 90°. This is a problem because it is difficult to sense and average the HF current drawn by the primary ports of the 3LAFB. It is easier to sense the average input current which is feeding the capacitor which only needs to be sensed one time per control update if the input ripple is small which it should be for a well designed grid filter.

This means that when operating with ac input, the sensed value for  $i_p$  and  $i_n$  is a combination of the averaged HF 3LAFB current and the reactive grid current then the calculation  $i_{p/n}^{sense}$  becomes distorted. This is especially problematic when the reactive current is significant compared to the real current consumed by the 3LAFB. The reactive current sourced by the capacitor can be calculated using the PLL information and the result can be subtracted from the sensed currents in order to get the average input current to the 3LAFB.

$$V_{ph} = \frac{1}{\sqrt{3}}V_{ll} \quad (3.29)$$

$$C_{pon,\lambda} = 3C_{pon,\Delta} \quad (3.30)$$

$$X_{c,\lambda} = -\frac{1}{\omega_{grid}C_{pon,\lambda}} \quad (3.31)$$

$$I_{ph,Im} \triangleq \text{Im}(I_{ph}) = \frac{V_{ph}}{X_{c,\lambda}} \quad (3.32)$$

If the 3LAFB input currents are in phase with the grid voltage then the resistive load emulated by the converter is seen in parallel with the soft dc-link capacitance. This leads to the power factor angle of the system to be positive meaning that there is negative reactive power exchanged with grid in addition to the real power delivered to the battery. This raises the apparent power seen by the grid and increases losses in the ac lines due to the increase magnitude of the phase currents,  $I_{ph}$ ; however, a positive power factor is typically accepted by the utility line due to the fact that most industrial loads appear inductive which needs to be compensated by capacitor banks to increase the power factor.

To account for this reactive current, the  $i_{p/n}^{ref}$  reference for the PFC control loop is phase shifted by a feed-forward term that is determined by the output power. The output power directly determines the emulated  $\lambda$ -connected resistance seen by the grid,  $R_{e,\lambda}$ . The efficiency of a well designed system should be close to 100% so the input power can be approximated as the output power. The real input current is based on the output power while the reactive input current is determined by the soft dc-link capacitance, and frequency and voltage of the grid.

$$P_{in} \approx P_{out} = V_{out}I_{out} \quad (3.33)$$

$$R_{e,\lambda} = \frac{V_{ll,RMS}^2}{P_{in}} \quad (3.34)$$

$$I_{ph,Re} \triangleq \text{Re}(I_{ph}) = \frac{1}{M^2} \frac{R_o^2}{R_e} \quad (3.35)$$

### 3.3 2 kW Hardware Prototype

To validate the 3LAFB and proposed controller design a 2 kW hardware prototype was developed and tested. The hardware implementation proves that the 3LAFB is a 3-port dc-dc converter capable of processing the time varying input voltages from the soft dc-link to produce a regulated, dc output port. The chapter will discuss the results taken with dc input voltages. The dc testing was used to characterize the efficiency over a wide range of output voltage and current at three different soft dc-link inputs. The results for ac-dc operation are also given and discussed.

The starting point for any converter design is the specifications. The input-output specifications for the prototype are summarized in Table 3.2. A design procedure for the 3LAFB is given in [20]. Following the referenced design procedure given the the specifications from Table 3.2, the hardware parameters for the 3LAFB were selected to yield a high efficiency design shown in Fig 3.10.

Table 3.2: Specifications for the prototype 3LAFB design.

Specification	Minimum	Nominal	Maximum
3-phase line-line input voltage	-10%	480 V <sub>RMS</sub>	+10%
Output power	–	–	2 kW
Output voltage	–	–	500 V
Output current	10%	–	4 A

The complete schematic of the 3LAFB with the Unfolder is shown in Fig. 3.11. The hardware parameters for each component in prototype design are given in Table 3.3. The same SiC switching devices used on the 3L primary bridge of the 3LAFB were re-used in the Unfolder for all switches; however, the switches connecting grid phases to the p and n rails can be replaced with diodes. The gate drivers for the Unfolder and 3L primary bridge switches were designed to be on a separate PCB and mount vertically onto the power board. The magnetic components were designed and built custom for the prototype; for more details on the design of the magnetic components refer to [5].

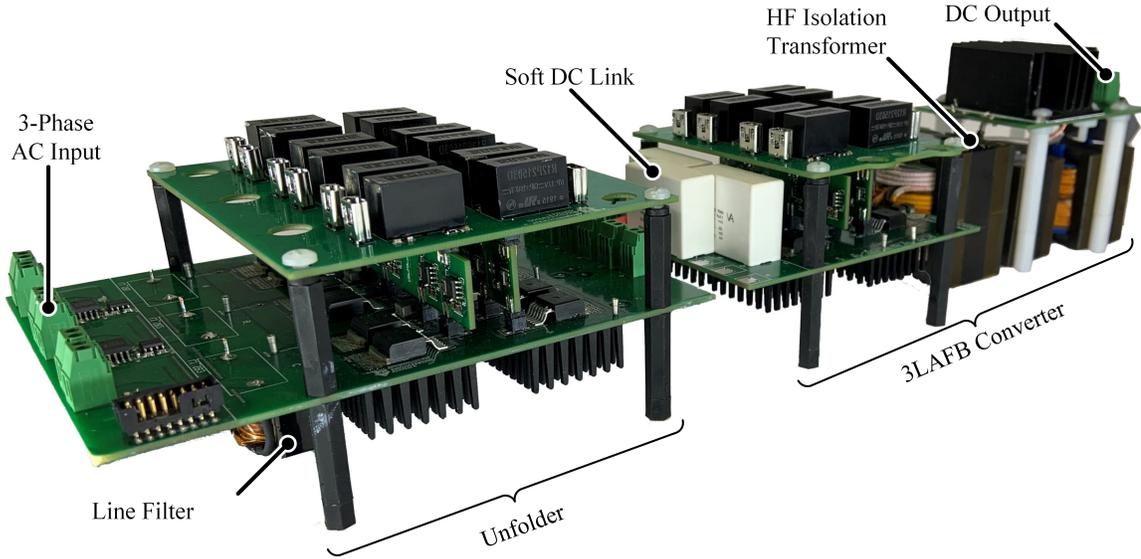


Fig. 3.10: Hardware prototype of the 2kW 3LAFB with Unfolder.

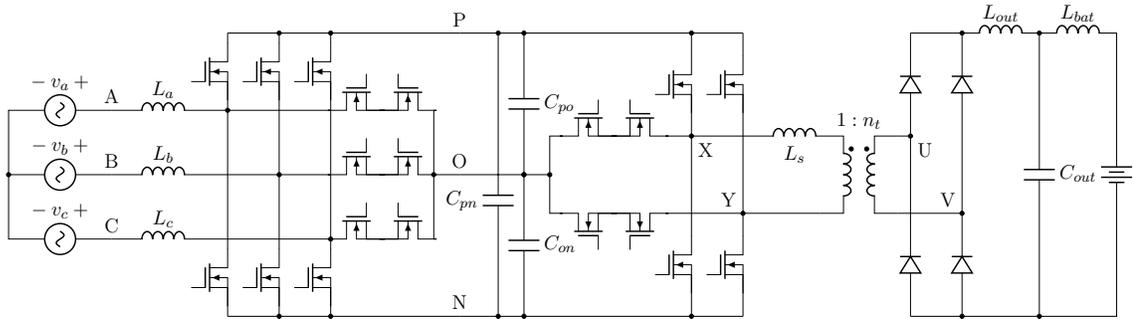


Fig. 3.11: Complete system schematic of the 3LAFB with Unfolder.

### 3.3.1 DC-DC Testing and Efficiency Map

To characterize the efficiency of the 3LAFB at all operating points a three-dimensional sweep was conducted over the following parameters: input soft dc-link voltages, output voltage, and output current. The input voltages that were tested correspond to the soft dc-link voltages at three different grid angles shown in Fig. 3.12. The selected operating points covers the full range of operation for the p sector. Operation in the n sector is symmetrical to the p sector, so the losses and efficiency will be the same.

Operating point “a” denotes the case of equal input voltages, and the concept of p and n sectors does not apply because the applied duty cycles, soft dc-link voltages, and input

Table 3.3: Hardware parameters for the prototype 3LAFB design.

Hardware component	Design
Unfolder MOSFETs	C3M0120100J, 1000 V, 120 m $\Omega$
3L primary bridge MOSFETs	C3M0120100J, 1000 V, 120 m $\Omega$
Rectifier Schottky diodes	C4D08120E, 1200 V, 8 A
Transformer turns ratio ( $n_t$ )	1:1:0.875 (Primary:Secondary:Clamp winding)
ZVS inductor ( $L_s$ )	30.76 $\mu$ H
Input capacitors ( $C_{po}$ , $C_{on}$ , $C_{pn}$ )	1.8 $\mu$ F, 1100 V (film)
Line inductors ( $L_a$ , $L_b$ , $L_c$ )	30 $\mu$ H
Output inductor ( $L_{out}$ )	1.3 mH
Output capacitor ( $C_{out}$ )	1.5 $\mu$ F, 1100 V (film)
Battery filter inductor ( $L_{bat}$ )	1.5 $\mu$ H
Switching frequency ( $f_s$ )	100 kHz

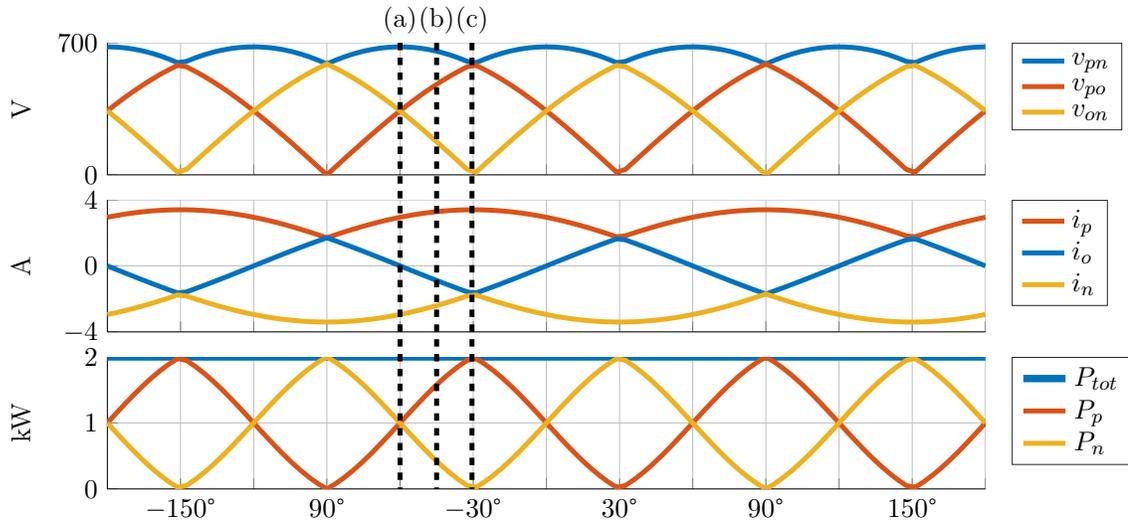


Fig. 3.12: Soft dc-link waveforms over a complete line cycle of the ac input with the dc operating point labeled at  $-60^\circ$ ,  $-45^\circ$ , and  $-30.5^\circ$ . These operating points are repeated throughout the grid cycle for both p and n sectors.

currents are the same. Operating point “b” is selected to be between the other two operating points in which the voltage on p-port is greater than that of the n-port in sector p. Operating point “c” denotes the case where the soft dc-link voltages are extremely unequal to the point that lesser port has 0 V. Practically, it is difficult to get results from testing the converter with 0 V across one of the input ports. This is due to the switching frequency ripple on the

soft dc-link capacitance which tries to apply a negative voltage across an input port; this negative voltage causes the body diodes of the switches in the primary 3L bridge to become forward biased and conduct which distorts the input currents. For this reason, the selected grid angle for operating point “c” was chosen to be  $-30.5^\circ$  rather than  $30^\circ$ . The dc operating points are summarized by Table 3.4.

Table 3.4: Operating points for testing the 3-port dc-dc with dc inputs in sector p.

<b>Parameter</b>	<b>(a)</b>	<b>(b)</b>	<b>(c)</b>
Grid angle	$-60^\circ$	$-45^\circ$	$-30.5^\circ$
$v_{po}$	340 V	480 V	585 V
$v_{on}$	340 V	176 V	6 V
$K_{ref} = i_p/i_n$	1	1.37	1.97

The efficiency map also included a sweep of the the output voltage and current. To emulate a battery source load, a power supply was used to regulate the output voltage. The output voltage was tested from 200 V to 500 V in steps of 100 V. The output current was regulated by the current control loop that was monitoring the output current and adjusting the magnitude of the duty cycles. The output current was tested from 0.8 A to 4 A in steps of 0.4 A. Furthermore, the PFC loop was also running during each of these tests to regulate the ratio of input currents. This loop is necessary to ensure that the dc testing coincides with operating points which occur during the ac-dc operation of the 3LAFB.

The efficiency measurements were made with the Yokogawa WT1806E power analyzer using the internal voltage and current sensing. The efficiency measurements did not include the conduction loss of the Unfolder stage; however the Unfolder losses are minimal due to the low  $R_{ds,on}$  of the SiC devices which were used and there is no switching at all during dc testing. Furthermore, the switching loss from the Unfolder is neglectable while operating with ac input because the devices are switched at only twice the line frequency which is very small compared to the switching frequency of the 3-port dc-dc stage. The results from the efficiency map of the prototype are shown in Fig. 3.13.

The highest efficiency achieved was above 98% for all three input voltage conditions.

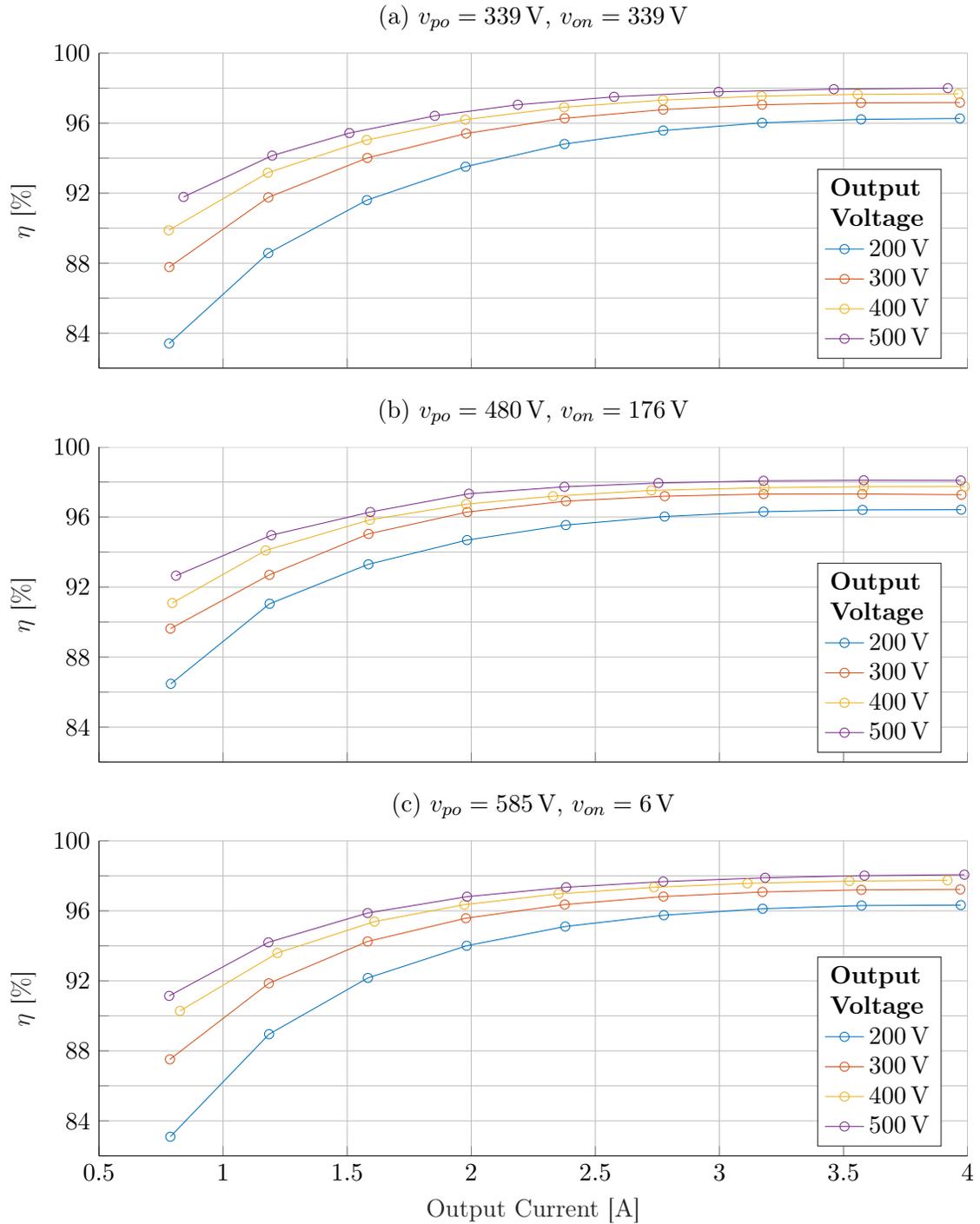


Fig. 3.13: Efficiency map of the 2 kW 3LAFB prototype operating with different DC input voltages. The map sweeps over the output voltage and current range of the converter.

This peak efficiency occurred at the rated output power (i.e. 500 V and 4 A) because the design was fully soft switching as well as utilizing most of the effective duty cycle which means that the circulating energy losses during the zero state was minimal. The converter waveforms were saved at the 2 kW operating points for each set of input voltages and are plotted in Fig. 3.14.

In each of the operating points shown in Fig. 3.14, the output voltage and current are fixed while the input voltages vary. The top row of plots shows how the input currents vary with input voltage. The second row of plots shows the constant output current overlaid with the HF transformer current. The spike in the rising edge of the transformer current is due to the ringing of the transformer leakage inductance with the parasitic output capacitance of the secondary rectifier diodes. The final row of plots shows the constant output voltage overlaid with the HF voltage waveform actuated by the 3L primary bridge.

### 3.3.2 AC-DC Testing

Validating the operation with dc inputs proves that the topology is possible candidate for the 3-port dc-dc converter to process the soft dc-link provided by an Unfolder. To validate the controller design and feed-forward terms the hardware was operated with ac input and the Unfolder. To simplify the control of both the Unfolder and the 3LAFB, the same microcontroller was used to modulate both switching stages which eliminated the need for communication between controllers.

The Unfolder stage was controlled by a PLL which tracked the grid angle and switched the Unfolder every  $60^\circ$ . The modulation of the Unfolder was updated at the switching frequency (100 kHz) meaning that the Unfolder switching occurs in steps of  $10\ \mu\text{s}$  instead of perfectly synchronized with zero crossings of the grid voltages. This timing error contributes to the sector distortion glitches that occur whenever the Unfolder is switched.

Special care was taken for the starting the Unfolder. First, the soft dc-link capacitance needs to be pre-charged to avoid inrush currents when connecting the ac input. During prototype testing, pre-charge was emulated by ramping up the ac input with a slew rate. The pre-charged soft dc-link capacitance has voltage levels corresponding to operating point

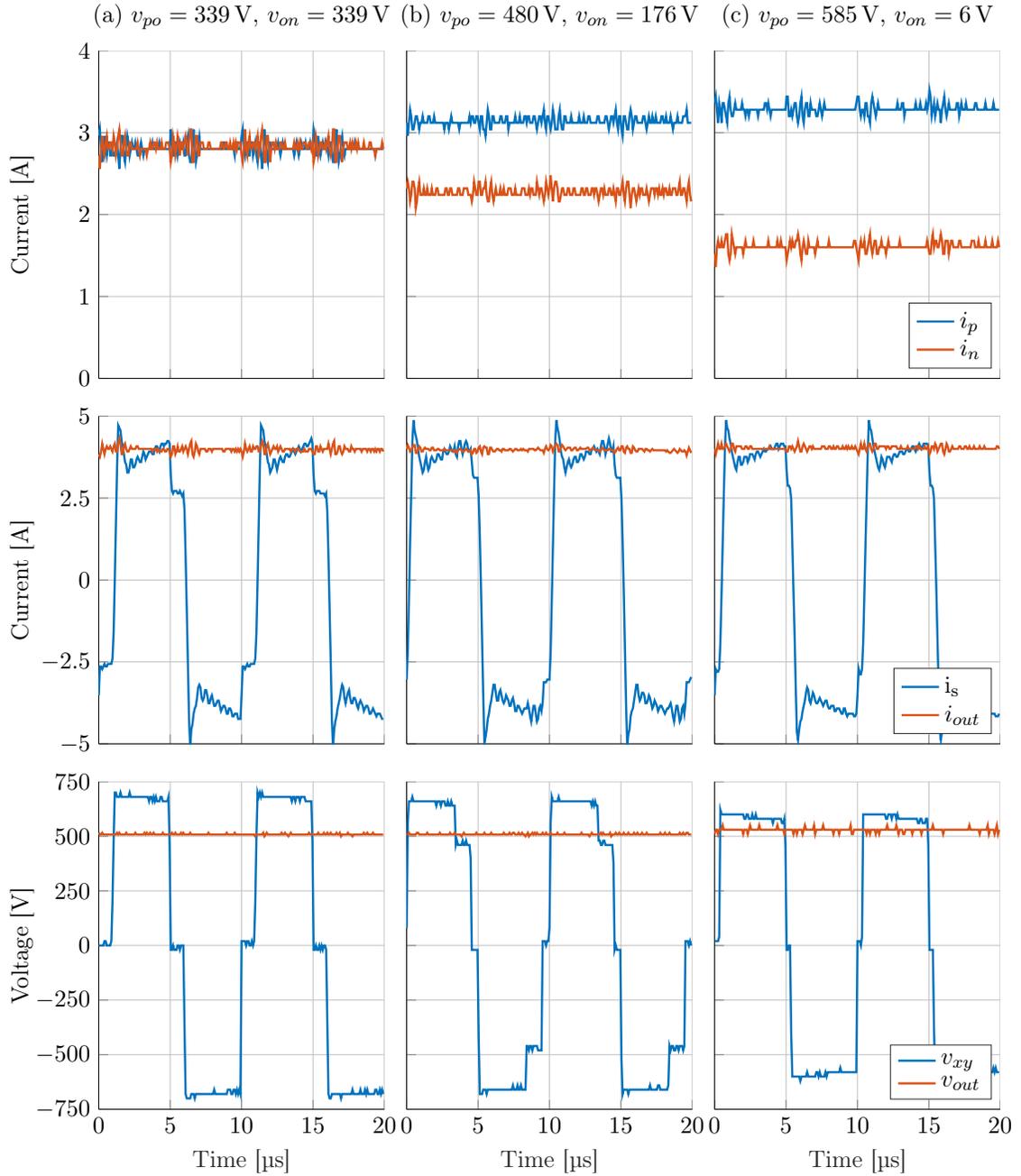


Fig. 3.14: Circuit waveforms of the 3LAFB hardware prototype at 2 kW and different input voltages.

“a” meaning that the voltage across the p and n ports are both equal to  $V_{ll}/\sqrt{2}$ . To avoid transients while starting to unfold, the unfolding must start when the grid voltages match the soft dc-link voltages which occurs at  $0^\circ$  and multiples  $60^\circ$ .

The single-pole triple-throw switches in the prototype Unfolder were implemented as MOSFETs as shown in Fig. 3.11. Using MOSFETs enables bidirectional input current to both charge and discharge the soft dc-link capacitance. This allows for the Unfolder to start unfolding with no loading other than the soft dc-link capacitance. This is useful because the unfolding can be started to establish the soft dc-link waveforms before the 3LAFB is modulated. If a 6-pulse diode bridge was used instead of MOSFETs, then the Unfolder would need loading when starting to unfold otherwise the voltage on each port of the its maximum value ( $\sqrt{3/2}V_{ll}$ ) because there is no means for discharging the capacitors. This is undesirable because the total soft dc-link would be  $\sqrt{6}V_{ll}$  which is much larger than the peak during normal operation which is only  $\sqrt{2}V_{ll}$ .

The 3LAFB modulation can be started after starting unfolding with no restrictions on grid angle. The 3LAFB was loaded with a passive resistive load for the ac-dc testing. To avoid large startup transients, the 3LAFB switching was initiated with low magnitude of the ac input (40 V). The voltage was ramped up after the switching was initiated so that ac-dc results were taken with the rated 3-phase input voltage of 480 V<sub>RMS</sub>.

The load for the ac-dc tests was 125  $\Omega$  and purely resistive so that there was no dynamics introduced by a power supply or electronic load. The load was selected in such a way that the rated power of 2 kW would be reached with the full output voltage of 500 V. The steady state waveforms of the 3LAFB processing 2 kW is shown in Fig. 3.15. The converter reached an efficiency of 98.0% during ac-dc power transfer, with a power factor of 0.999, and a low THD of 2.69%.

To test the controller design for the ac-dc system, a step response in the output current was tested from 4 A to 3 A which corresponded to a power step of 2 kW to the 1.13 kW. The results of the step response was captured and is shown in Fig. 3.16. The system responded very fast to the step response due to the feed-forward calculation using the reference output current rather than sensed output current.

### 3.4 Summary

This chapter investigated the 3LAFB which is the first isolated, 3-port dc-dc topology

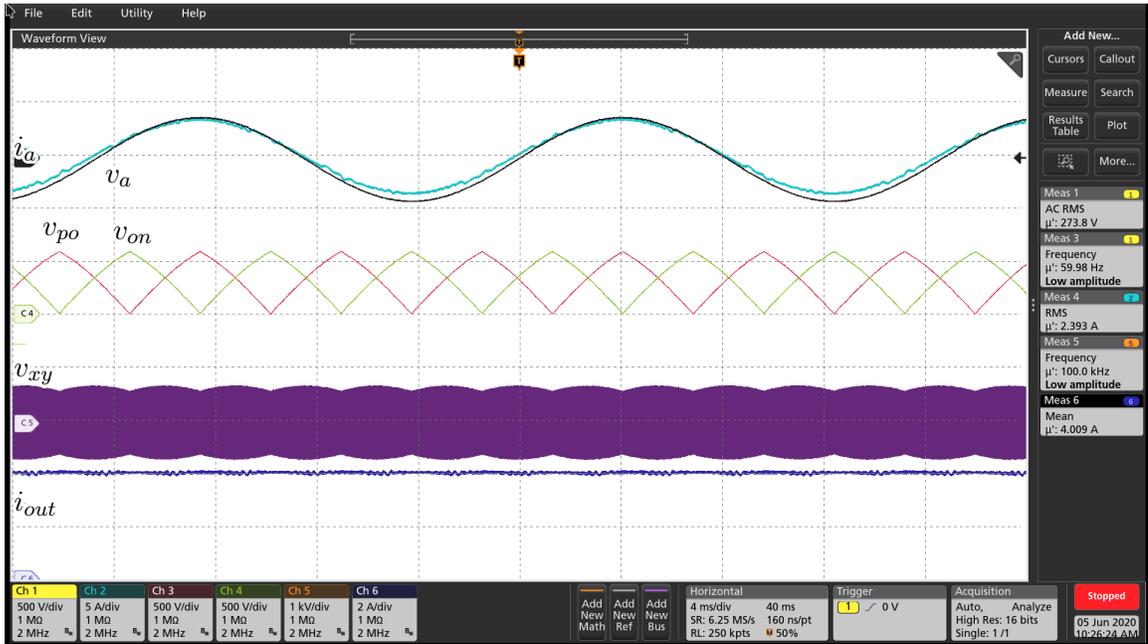


Fig. 3.15: Scope screen capture of the ac-dc converter waveforms for the 2kW prototype hardware.

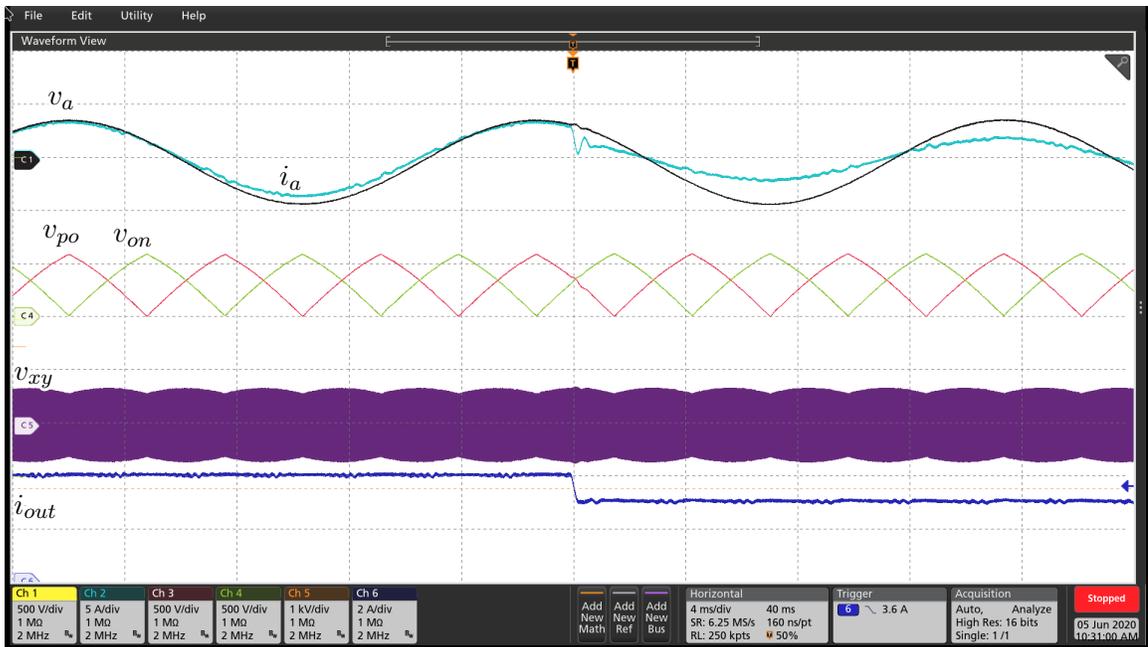


Fig. 3.16: Scope screen capture of the ac-dc converter waveforms for the 2kW prototype hardware during a step response in the output current.

discussed in this thesis. This chapter introduced the 3LAFB topology by explaining the operation and referencing prior publications. The topology was further explained using switch network averaging to gain a deeper understanding of the dynamic behavior and develop a controller design. Lastly, a lab scale 2 kW prototype was built to test the proposed topology and controller design.

The operation of the 3LAFB was described by drawing parallels to other converters in literature such as the PSFB. The unique implementation of the gating signals for the 3L primary bridge is described in detail as to why it is necessary and how it improves the efficiency of the hardware. The challenge presented by the parasitic voltage ringing on the secondary rectifier was discussed including how to mitigate the voltage overshoot as well as how it effects the ac operation.

A generic design procedure for the 3LADAB topology was presented. The design procedure gives insight to how to selected the transformer turns ratio, tank impedance, switching frequency, and input/output filters. A specific design for a 18 kW module is presented as an example with extra details on the component selection, PCB, and gate driver design.

One 2 kW 3LAFB prototype was built based to validate the topology and controller design. The prototype was experimentally tested as a dc-dc converter to characterize the efficiency in a variety of operating points. The operating conditions were varied to test different input voltages, load currents, and output voltages which would occur in normal operation with ac input and a battery load. The experimental results show that the converter achieves high efficiency over a wide range of of operating points. The converter was operated with ac input from a 3-phase Unfolder to validate the controller design. The ac operation achieved high efficiency and low THD with unity power factor.

CHAPTER 4  
MODULAR STRUCTURE OF 350 kW EXTREME FAST CHARGER

The understanding gained from analyzing the isolated unfolding-based approach in Chapter 3 was used to aid in the design of the full scale XFC for heavy duty EV. This chapter proposes a modular structure for developing a 350 kW unfolding-based XFC. Specifically, this chapter covers the topology selection and how the arrangement and number of modules and interconnection of modules were determined.

The specifications for the XFC are summarized in Table 4.1. The input voltage and output power level for the XFC was determined to be similar to the state-of-art Terra High Power Gen III Charger from ABB [24]. The specified output voltage and current limits were chosen to accommodate higher voltage EV batteries in order to reduce the current requirements of the connectors.

Table 4.1: Input/output specifications for the full scale XFC design.

Specification	Minimum	Nominal	Maximum
3-phase line-line input voltage	-10%	480 V <sub>RMS</sub>	+10%
Output power	–	–	350 kW
Output voltage	400 V	–	800 V
Output current	12.5%	–	450 A

It is difficult to have a single converter process the total power due to the current ratings of available devices on the market and difficulties that arise when trying to parallel multiple discrete devices or even power modules. Furthermore, it is difficult to debug and test such high power modules due to the required equipment and safety precautions. Instead, it is common to modularize high power converter designs into smaller converters which work together to achieve the full power ratings.

Using a modular structure, the total power processed is split amongst the individual

modules. The controllers of each module ensure equal power sharing between modules using feedback regulation. This solves the problem of trying to parallel many devices on a single converter. This also spreads out the losses between multiple converters and smaller components which make the system easier to cool.

The structure that was selected for the full scale XFC is shown in Fig. 4.1. The design consists of 20, 3-port dc-dc modules which are implemented by the 3LADAB topology. The 3LADAB converter is discussed in detail in Chapter 5. The system uses a single 3-phase Unfolder to commute the grid phases in the soft dc-link voltages. The power modules are connected in parallel on the input soft dc-link. The outputs of the modules are connected four in parallel and five sets of modules are stacked in series.

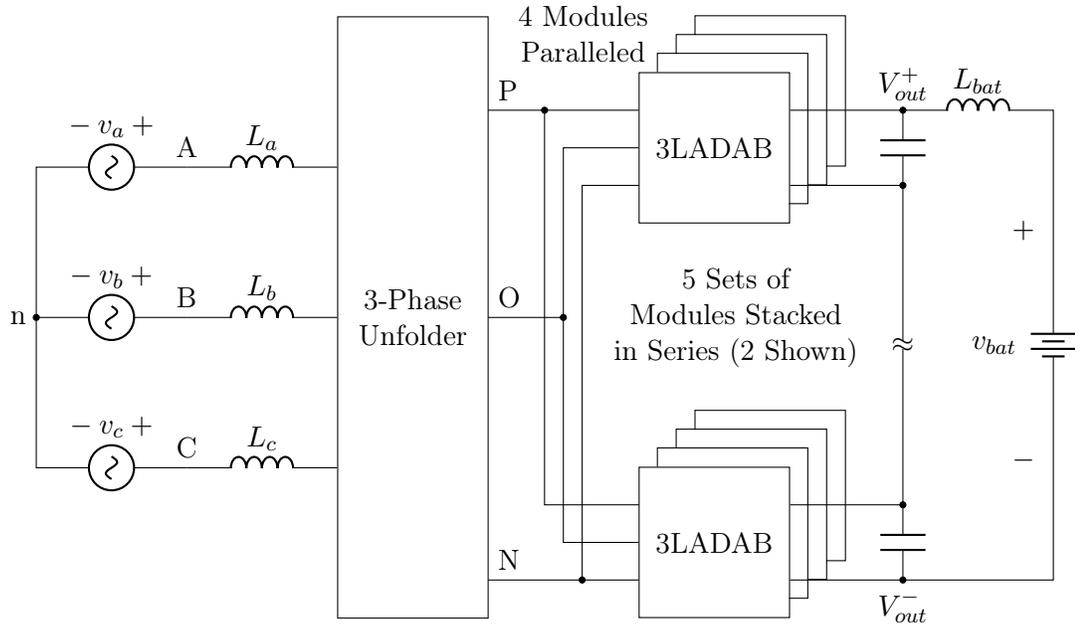


Fig. 4.1: Complete 350 kW XFC system diagram with Unfolder and 18 kW 3LADAB modules shown as blocks. All 3LADAB modules are connected in parallel at the input while the outputs are connected four in parallel and five sets of modules are stacked in series; however, only two series stacks are shown.

#### 4.1 Topology Selection

The chosen topology of the full scale XFC was selected to be the 3LADAB converter

which is discussed in detail in Chapter 5. This topology was selected because it can soft-switch all MOSFET devices over the entire grid cycle while following the proposed modulation scheme from [19]. The 3LADAB was selected over the 3LAFB topology for the full scale design because the transformer parasitic leakage inductance is better absorbed into the topology without needing a complicated clamping strategy for the secondary devices.

The excessive voltage ringing across the secondary devices in the 3LAFB topology requires the use of higher voltage components to avoid device failures. In the current application, with an output voltage of 800 V and expected overshoot of only 20% the peak voltage across the secondary would be 960 V which is 80% of the rating of 1200 V device. This could be a reliability issue which should be avoided by using the less common 1700 V devices. Due to the overrating of the of the devices needed for the secondary, the resulting design would have poor utilization and efficiency. To avoid using the overrated components the 3LADAB was selected over the 3LAFB topology.

## 4.2 Series Stacking Selection

The 3LADAB behaves similar to a DAB where the soft-switching range depends on the input/output voltage ratio and the applied phase shift. This make it difficult for DAB based typology's to have high efficiency over a wide range of output voltages while being fed with constant input. The design of the 3LADAB bridge is further complicated because the input voltage is not constant throughout the grid cycle because it follows the envelope of the line-line grid voltages which has a frequency of  $6f_{grid}$  and an average value of  $(3/\pi)v_{ll,m}$ . Furthermore, the 3LADAB uses duty cycle modulation to process the soft dc-link port with the lesser voltage to ensure that the input current is power factor corrected.

Regardless of the time-varying input voltage the dc output voltage will also need to be varied while the batteries are charged from 10% SoC to around 90% SoC. This variation must be handled by the 3-port dc-dc. It is useful to define a standard method for calculating the relative difference in output voltage. The method used in this chapter to calculate relative difference is to normalize the absolute output voltage swing with the highest output voltage as shown in equation 4.1.

$$\Delta V_{out,r} = \frac{V_{out,max} - V_{out,min}}{V_{out,max}} \quad (4.1)$$

From the XFC specifications in Table 4.1, it is clear that the relative difference in output voltage is 50%. This is a large variation in output voltage and it is very difficult to design a DAB with good efficiency throughout the entire operating region.

Instead of having all 3LADAB modules produce an output voltage with 50% variation, the output ports of the 3LADAB can be connected in series; by enabling and disabling some of the module outputs during operation, the variation required by each module can be reduced. The series stacking of the output voltages is possible due to the isolation transformer internal to the 3LADAB modules which allows the output ports to be connected arbitrarily. The modules are able to enable and disable without the use of additional contactors due to the active switches used on the secondary of the 3LADAB modules.

To determine how many modules should be stacked in series, a study was conducted to find how additional modules reduce the relative difference in output voltage. The key requirement for the series stacked modules is that the sum of all the output voltages must continuously go from  $V_{out,min}$  to  $V_{out,max}$  using  $n$  modules that each have a range from  $V_{module,min}$  to  $V_{module,max}$ . The diagram from Fig. 4.2 shows how the outputs from  $n$  connected modules produce the total output voltage.

$$v_{out} = \sum_{i=1}^n v_{out,i}, \quad v_{out,i} = \begin{cases} [V_{module,min}, V_{module,max}] & \text{module enabled} \\ 0 & \text{module disabled} \end{cases} \quad (4.2)$$

The process for calculating  $\Delta V_{out,r}$  as a function of number of modules,  $n$ , is as follows. The maximum module voltage is determined from simply dividing the total output voltage by the number of modules.

$$V_{module,max} = \frac{V_{out,max}}{n} \quad (4.3)$$

The next step is determine minimum number of modules that are required to produce

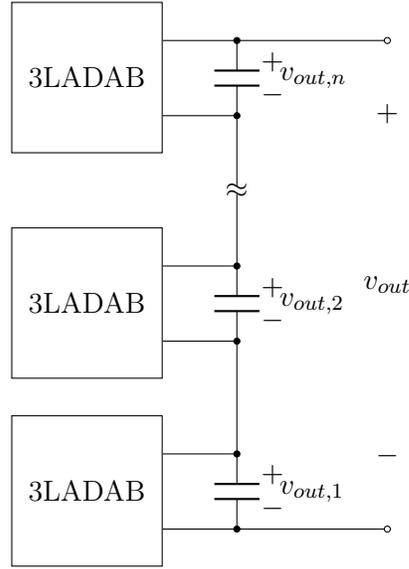


Fig. 4.2: Arbitrary number of series stacked 3LADAB modules with the output voltage of each module and total output voltage labeled.

the lowest output voltage,  $n_{min}$ . Note that if an integer number of modules can produce  $V_{out,min}$  using  $V_{module,max}$  then as soon as the voltage goes above  $V_{out,min}$  then additional modules will be required thus  $n_{min}$  will need to be padded with an extra module.

$$n_{min} = \begin{cases} \left\lceil \frac{V_{out,min}}{V_{module,max}} \right\rceil & \frac{V_{out,min}}{V_{module,max}} \notin \mathbb{N} \\ \frac{V_{out,min}}{V_{module,max}} + 1 & \frac{V_{out,min}}{V_{module,max}} \in \mathbb{N} \end{cases} \quad (4.4)$$

The next step is to determine the minimum output voltage required by the module which is one of two possibilities. The obvious being the minimum total output voltage divided by the minimum number of modules required.

$$V_{module,min}^1 = \frac{V_{out,min}}{n_{min}} \quad (4.5)$$

The second possibility occurs when an additional module is added to the minimum number of modules. This occurs when the minimum number of modules are operating with their maximum output voltage. During the transition, the same voltage will have to be produced by more modules which lowers the voltage required from each module. The minimum

module voltage is the minimum between the two possibilities.

$$V_{module,min}^2 = \frac{n_{min} V_{module,max}}{n_{min} + 1} \quad (4.6)$$

$$V_{module,min} = \min(V_{module,min}^1, V_{module,min}^2) \quad (4.7)$$

Now that the voltage range for the modules have been defined, the relative difference calculation from 4.1 can be applied to see how the variation in output voltage is reduced. The process was conducted for up to seven series stacked modules using the specifications from Table 4.1. The results were generated using a simple MATLAB script and are summarized by Table 4.2.

Table 4.2: Relative difference in output voltage for a varying number of series stacked modules for XFC structure.

$n$	$V_{module,min}$	$V_{module,max}$	$\Delta V_{out,r}$
1	400 V	800 V	50%
2	200 V	400 V	50%
3	178 V	267 V	33.3%
4	133 V	200 V	33.3%
5	120 V	160 V	25%
6	100 V	133 V	25%
7	91 V	114 V	20%

The results indicate that the more series connected modules yields lower relative difference required from each module in the stack. Interestingly an even number of modules yields the same relative difference in the output voltage as an odd number of one less module. This implies that it would be better to use an odd number of modules rather than even because the extra module for the even case would not yield any benefit in terms of reduction in output voltage variation.

The trade off with using extra modules is the increased complexity of the system and current rating required by the modules for the same output power. The extra modules

will need communication amongst themselves to determine the output voltage reference and whether or not the module should be enabled. Furthermore, the more modules that are used the lower the output voltage is for each module. This means that for the same power level, lower voltage modules will need to source higher currents which incur higher conduction losses in the switching devices.

The choice of five series stacked modules was selected because the voltage variation in the output is 25% which is half the value of the original 50% when only using one module. Furthermore, the output voltage ranges from 120 V to 160 V which can easily be blocked by 250 V silicon MOSFETs which are commonly available on the market in discrete packages.

The series stacking of module outputs reduces the voltage variation required by each module. This was done to increase the region in which all active devices on 3LADAB topology are soft switched. However, output voltage is only part of the soft switching conditions. The other factor in determining soft switching is the applied phase shift between the primary and secondary which has a strong correlation with output current.

### 4.3 Parallel Module Selection

Generic battery chargers should accommodate a wide range of load currents depending on the battery charging limits. In order to supply a wider range of output currents with same design, the number of modules placed in parallel should be increased. The concept for placing 3LADAB modules in parallel follows the same principles as the series stacking; however, instead of reducing the output voltage variation the output current variation is reduced. This means that when a parallel converter is not operating the switches on the output should be left open so that no power is sourced or sunk.

For light load conditions, the applied phase shift to the 3LADAB is small and the soft-switching is harder to achieve, especially when the input and output voltages are mismatched. Reducing the relative difference in required load current, reduces the variation of phase shift applied to the 3LADAB. This makes it easier to design the 3LADAB module, so that it is soft-switching for all possible operating conditions.

The project requirements do not specify a minimum load current that the XFC should be

able to supply so the value was left to the designers. To make the design of the module easier to implement with discrete devices, four modules were selected to be placed in parallel. With four modules in parallel, the maximum current required from each module is  $I_{out,max}/4 = 112.5$  A. If each module is capable of operating with 50% load current then the XFC is capable of outputting 12.5% of its total output current capability.

#### 4.4 Summary

This chapter proposes a modular design structure for creating an XFC intended for heavy duty EV using a quasi-single stage Unfolder approach paired with lower power 3-port dc-dc modules. Benefits of modular designs are briefly described. The topology selection was discussed for selecting the 3-port dc-dc modules and it was decided that 3LADAB would be the best candidate. Analysis on series stacked output ports of the dc-dc modules was presented in order to reduce the voltage variation required by each module. Similar analysis was presented for paralleling output ports of dc-dc modules to reduce the current variation required by each module. The ideal module size and specifications were determined and the design of the module is discussed in Chapter 5.

## CHAPTER 5

## THREE-LEVEL ASYMMETRIC DUAL ACTIVE BRIDGE (3LADAB)

The second topology under investigation in this thesis is the 3LADAB. The 3LADAB, shown in Fig. 5.1, is another novel 3-port dc-dc candidate for processing the soft dc-link voltage produced by an Unfolder. This topology is of specific interest to the thesis because it was selected as the module building block that makes up the design of the full scale XFC.

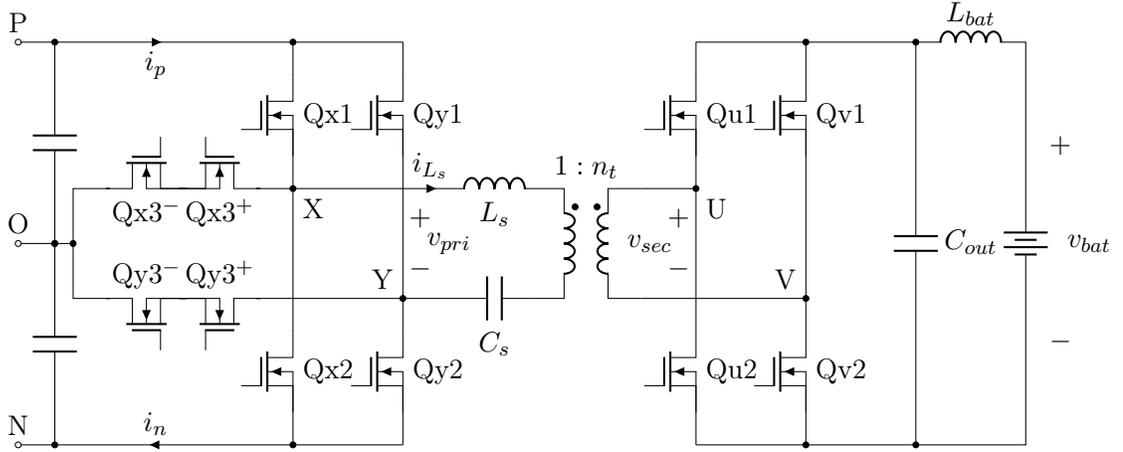


Fig. 5.1: The 3LADAB topology with series resonant inductor,  $L_s$ , and capacitor  $C_s$  shown on the primary side of the transformer. Each T-type switching leg of the 3LAFB contains 4 MOSFET devices: 2 H-bridge switches ( $Q_{x1}$ ,  $Q_{x2}$ ) and 2 back-back switches ( $Q_{x3+}$ ,  $Q_{x3-}$ ). The secondary side rectifier is a full bridge represented with MOSFETs as the switching devices and a capacitive output filter.

This chapter covers the basic operation of the 3LADAB with typical modulation waveforms shown to give insight to the inner workings of the converter. The design procedure for the 18 kW module is presented. Finally, the hardware results from the 18 kW prototype are given to validate the proposed design procedure.

### 5.1 Topology Description

The 3LADAB topology, shown in Fig. 5.1, is a 3-port dc-dc with galvanic isolation

between the dc output on the secondary and the soft dc-link input provided from an Unfolder similar to the 3LAFB. The section covers the basic operation principles of the 3LADAB. The modulation implementation is briefly discussed as it is very similar to the 3LAFB topology. Finally, the MATLAB simulation model that has been developed to simulate the 3LADAB is discussed as it provides a fast simulation of the converters dynamics.

### 5.1.1 Operating Principle

The 3LADAB is derived from the series resonate DAB topology by replacing the primary bridge with a 3L, T-type switching bridge. The rest of the system remains unchanged from the series resonant DAB. Similar to the naming of the 3LAFB, the asymmetry introduced by the time-varying soft dc-link waveforms is included in the name of the 3LADAB to distinguish it from traditional 3L DAB topologies.

Unlike the 3LAFB, the 3LADAB uses active devices on the secondary rectifier to control the voltage applied to the secondary which introduces new control variables. The capacitive output filter removes the possibility for the voltage ringing on the secondary devices which was a challenge for the 3LAFB that had a LC output filter. Furthermore, the series resonant capacitor in the HF tank, in addition to preventing saturation of the transformer core, allows the designer another degree of freedom in selecting the quality factor of the tank.

The 3LADAB has the same functionality as the TAB topology that was introduced in [19]. The fundamental difference between the TAB and 3LADAB is that the 3LADAB utilizes the the 3L T-type full bridge to process the power from the soft dc-link where the TAB uses two independent full-bridges. This allows the 3LADAB to operate with a single HF transformer similar to the 3LAFB.

The functionality of the 3L bridge on the primary side of the transformer is equivalent to two full bridges stacked in series as is the case of the TAB; however when using two full bridges, two transformers are required to couple both the p and n ports to the secondary. Having multiple transformers allows for series stacking of the primary side and allows for connections to medium voltage grids (1 kV to 35 kV). However, the T-type switching bridge has better utilization of the switches and requires only one HF isolation transformer. For a

480 V system with 10% higher voltage than nominal, the peak voltage of the soft dc-link is only  $\sqrt{2}V_{ll,RMS} = 747\text{ V}$  which can safely be blocked by 1 kV to 1.2 kV devices which are common on the market thus reducing the need for series stacking on the input side. Using a single transformer is superior to two transformers because a single transformer has better core and winding utilization and reduces the required components.

The two input ports created by the 3L primary bridge in addition to the secondary switching bridge provide a high level of flexibility for how the topology can be modulated. Typical simulation waveform for the 18 kW 3LADAB design are given in Fig. 5.2. The modulation waveforms are shown at operating point “b” which was defined in Section 3.3. Instead of showing modulation for sector p where  $d_p > d_n$  and  $v_{po} > v_{on}$ , the modulation waveforms shown in Fig. 5.2 are shown in sector n where  $d_n > d_p$  and  $v_{on} > v_{po}$ .

The traditional DAB topology with a single primary port has the potential to modulated with three-angle phase-shift control in order to maximize efficiency [25]. In three-angle phase-shift modulation of the primary and secondary bridge can have the pulse widths varied in addition to the phase shift between the primary and secondary. With the 3LADAB or TAB topology, the pulse width of of each primary port can be varied with control parameters  $d_p$  and  $d_n$ . Furthermore, the applied phase shifts between each input port to the secondary can also be different.

The 3LADAB has the same control objectives as the 3LAFB which are output power regulation and PFC. Similar to the 3LAFB, the PFC is achieved by regulating the input current ratio from each primary port. Since there is only one HF tank current, the input current can only be varied by changing the pulse width of the primary ports. In the case of the TAB, the pulse widths are varied by changing the phase shift between the H-bridges for each primary port; however, for the 3LADAB the pulse width is varied by applying a duty cycle for the lesser port. Regardless of how the pulse widths are varied with the input bridge, the resonant tank is driven with the same voltage waveforms.

The control of the 3LADAB uses the intermediate control variable,  $d_{p/n}$ , to ensure PFC grid currents. The concept of p and n sectors still applies. The corresponding input port to

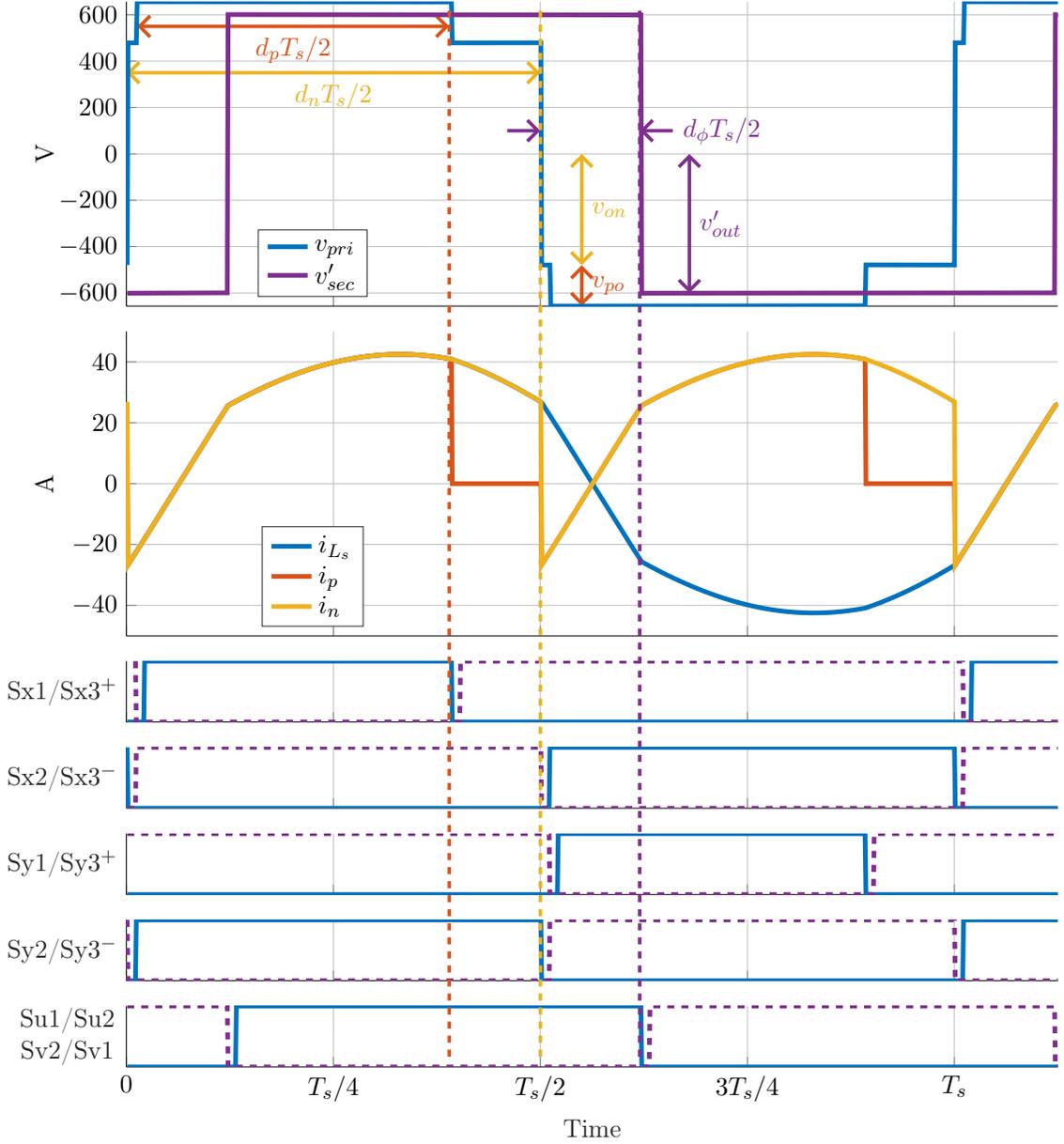


Fig. 5.2: Idealized 3LADAB simulation waveforms for operating point “b” when operating in a sector  $n$  (i.e.  $d_n > d_p$ ). The first subplot contains the switching bridge voltages on the primary and reflected secondary side of the transformer. The second plot shows the HF tank current as well as the input currents for the primary ports. The next 4 plots show the gating signals for the primary where the H-bridge switches have their gating signal given in the solid waveform while the corresponding complimentary back-back switches are dashed lines. The last plot shows the gating signals for the secondary side of the transformer:  $S_{u1}/S_{u2}$  being solid and  $S_{u2}/S_{v1}$  being dashed.

modulation sector is always set to full duty or 180° phase shift. Furthermore the secondary port, which is identical to a DAB also has full duty or 180° phase shift. The calculation of  $d_p$  and  $d_n$  from intermediate control variable,  $d_{p/n}$  is shown in Table 5.1.

Table 5.1: Calculation of the 3LADAB primary duty cycles from intermediate control variable  $d_{p/n}$ .

Parameter	Sector p	Sector n
$d_{p/n}$	$d_{p/n} > 1$	$d_{p/n} < 1$
$d_p$	1	$d_{p/n}d_n = d_{p/n}$
$d_n$	$\frac{d_p}{d_{p/n}} = \frac{1}{d_{p/n}}$	1

The output power of the 3LADAB is controlled by varying the applied phase shift,  $d_{phi}$ , between the HF voltage of the primary and secondary active bridges. This control variable has a strong correlation with the output power. This differs from the 3LAFB modulation because there is no active secondary bridge on the 3LAFB topology, so the output power is controlled with the absolute magnitudes of the primary duty cycles  $d_p$  and  $d_n$ .

Another restriction placed on the modulation of the 3LADAB is that the rising edge switching transitions for both ports of the primary bridge are aligned. This is done so that the same switching instant current is used to soft switch all devices in one T-type switching leg given that switching instant current is in the right direction to discharge/charge the output capacitance of the devices.

These restrictions on the modulation reduce the number of free control variables which yields only a single solution for satisfying both control objectives. With more sophisticated controllers, all control variables could be used in order to minimize reactive current and increase the soft switching range for higher efficiency operation; however, this level of control optimization is out of scope for this thesis.

### 5.1.2 Modulation Implementation

Since the primary bridge for the 3LAFB and 3LADAB are identical the modulation for both topologies is very similar. In fact, the modulation scheme for both topologies is exactly

the same with the exception that the 3LADAB modulation has been restricted by Table 5.1 to ensure that at least one duty cycle is always unity or full duty. This restriction eliminates the zero state or free-wheeling state that occurs during the modulation of the 3LAFB.

Recall from Section 3.1.2 that modulation in sector p and n differs because the devices that are free-wheeling in the zero state are different. In sector p the device connected to the P rail are used to free-wheel while in sector n the the devices connected to the N rail are used. Special modulation sequences were required to transition from modulating from one sector to the other.

In the case of the 3LADAB modulation, applying full duty eliminates the free-wheeling state entirely. Thus modulation in sectors p and n are identical, and no special modulation sequences are needed to switch between modulation sectors. This is convenient because it simplifies the modulation implementation for the embedded controllers used to generate the gating signals for hardware.

Similar to the 3LAFB, the 3LADAB operates with unbalanced input voltages from the soft dc-link. This necessitates a stagger when directly transitioning the switch node voltage of a T-type leg between the P and N rails.

For example, in sector n the voltage on the n-port is greater than the p-port. At the start of the switching period, T-type leg X is transiting from the N rail to the P rail. The turn off of  $Q_{x2}$  starts the voltage transition as the negative tank current charges the switch capacitance of  $Q_{x2}$  and discharging  $Q_{x3}^-$ . After the appropriate dead time,  $Q_{x3}^-$  can be turned on with zero volts while  $Q_{x3}^+$  can simultaneously turned off to begin the transition from the O rail to the P rail. The negative tank current continuous to charge the output capacitance of  $Q_{x3}^+$  and discharge  $Q_{x1}$ . After the dead time,  $Q_{x3}^+$  is charged to the p-port voltage and  $Q_{x1}$  can be turned on with zero volts.

The stagger introduced between the turn off of  $Q_{x2}$  and  $Q_{x3}^+$  is on the order of the dead time so it does not significantly impact the operation of the converter; however, without it the voltages across back-back devices would not be symmetrically discharged and thus partial hard switching would occur with the turn on of  $Q_{x3}^-$ .

The gate signal generated for the secondary side of the 3LADAB are exactly the same as the traditional DAB. Because the modulation of the secondary side has been restricted to only applying full duty cycle, the gating signals for Qu1 and Qv2 are the same just as the signals for Qu2 and Qv1 are the same. Thus only 2 unique signals are needed to modulate the secondary side of the 3LADAB.

### 5.1.3 Sinusoidal Analysis

To better understand the operation of the 3LADAB, the fundamental harmonic approximation (FHA) is applied to the topology to analyze the circuit. The FHA is a common and powerful tool used to analyze resonant power converter circuit topologies. The FHA replaces the square wave voltages which are generated by the switching devices with their fundamental harmonic component which retains the phase and magnitude information. The analysis is valid for resonant tanks with higher Q factors because tank impedance is excited primarily by the fundamental component while the higher order harmonics are attenuated.

The 3LADAB topology without the input and output filter is shown in Fig. 5.3. The labeling and notation used is similar to the switch network averaging of the 3LAFB shown in Fig. 3.4; however, the FHA will be applied to the circuit shown in Fig. 5.3 rather than switch network averaging. An equivalent circuit for the 3LADAB topology using transformers is shown in Fig. 5.4.

The equivalent circuit uses the switching functions of the 3LADAB:  $s_{1p}$ ,  $s_{1n}$ , and  $s_2$ . The switching functions are controlled by the modulation variables:  $d_p$ ,  $d_n$ , and  $d_{phi}$ . The switching functions can be represented as square wave signals for accurately capturing all the harmonics introduced from the switching bridges. Alternatively, the switching functions can just represent the fundamental component of the square wave signals as shown in Fig. 5.5.

The switching functions shown are for unequal duty cycles in sector n. The phase shift between the primary ports and the secondaries,  $\phi_{1p}$  and  $\phi_{1n}$ , are different because the rising edge of the square waves are aligned and the p-port is applying a duty cycle,  $d_p$ , while the n-port is applying full duty. The phase shift between the n-port and the secondary,  $\phi_{1n}$ , is

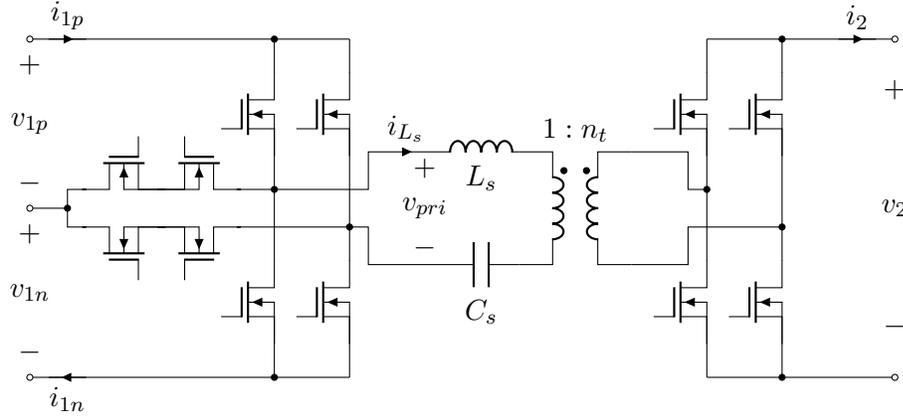


Fig. 5.3: The 3LADAB topology without the input and output filters and with labels that are relevant to the sinusoidal analysis.

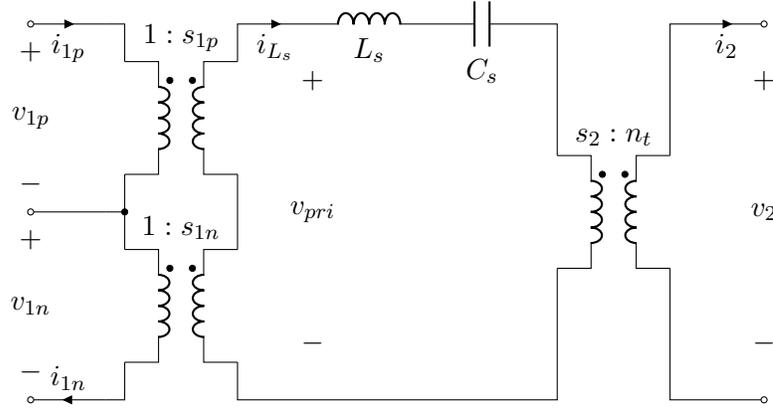


Fig. 5.4: An equivalent circuit for the 3LADAB topology using transformers and switching functions.

equal to the phase shift control variable,  $\phi_{edge} = \frac{\pi}{2}d_{phi}$  in sector  $n$ . The calculation for the individual primary port phase shifts is given in Table 5.2.

Table 5.2: Calculation of the 3LADAB primary port phase shifts with respect to the secondary.

Parameter	Sector p	Sector n
$\phi_{1p}$	$\frac{\pi}{2}d_\phi$	$\frac{\pi}{2}(d_\phi + 1 - d_n)$
$\phi_{1n}$	$\frac{\pi}{2}(d_\phi + 1 - d_p)$	$\frac{\pi}{2}d_\phi$

Phasor analysis is a powerful tool for analyzing sinusoidal circuits because it replaces the

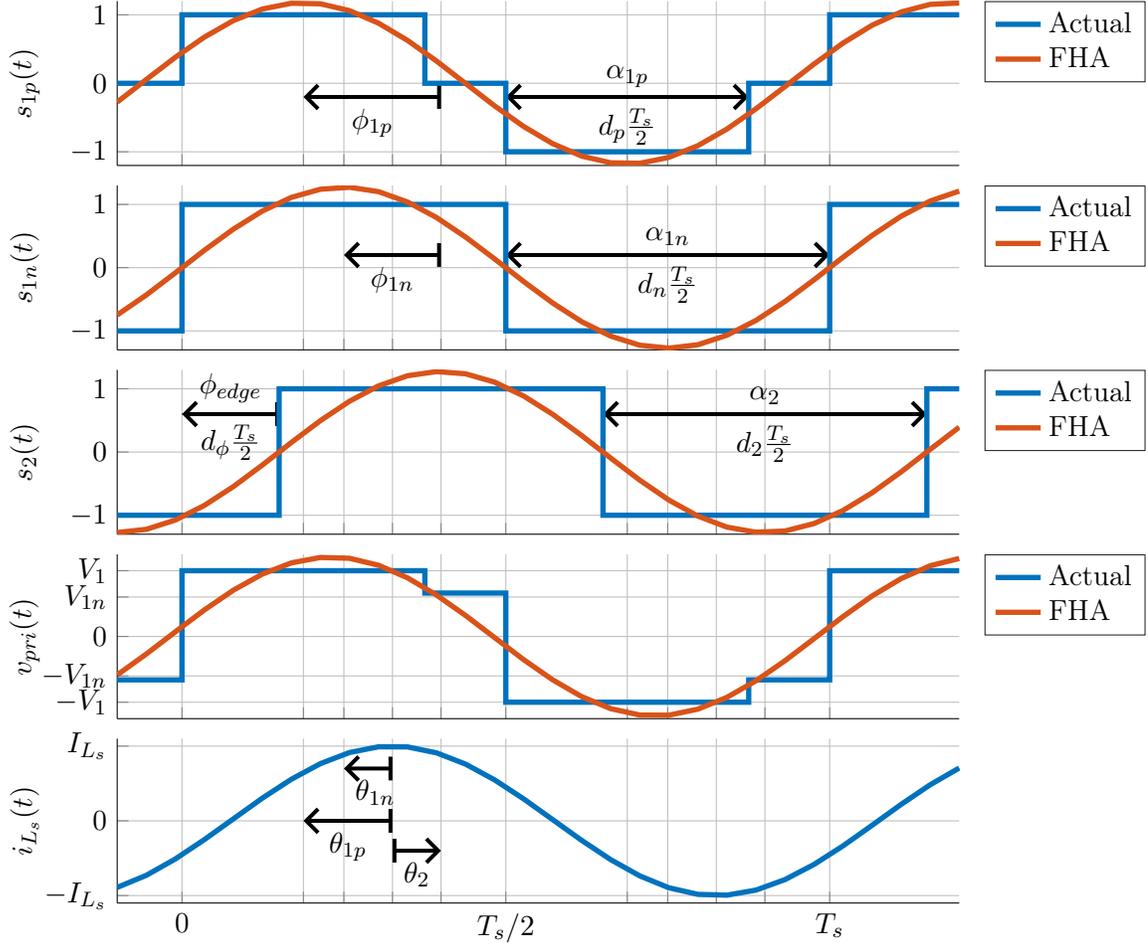


Fig. 5.5: The switching functions of the 3LADAB in sector  $n$ . The second to last plot shows the combination of both primary ports driving the resonant tank. The last plot shows the HF tank current.

rotational system with a stationary equivalent. To convert the circuit shown in in Fig. 5.4 to a phasor form, the transformation defined in [26] was used. The switching functions in the transformers are replaced with their phasor equivalents. The secondary voltage waveform is taken as the reference and all phase shifts are defined with respect to the secondary switching

function.

$$\vec{s}_{1p} = \frac{4}{\pi} \sin\left(\frac{\pi}{2}d_p\right) \angle \phi_{1p} \quad (5.1a)$$

$$\vec{s}_{1n} = \frac{4}{\pi} \sin\left(\frac{\pi}{2}d_n\right) \angle \phi_{1n} \quad (5.1b)$$

$$\vec{s}_2 = \frac{4}{\pi} \sin\left(\frac{\pi}{2}d_2\right) \angle 0 \quad (5.1c)$$

The resulting voltages that drive the HF resonate tank are nothing more than the switching functions scaled by the dc input and output sources.

$$\vec{v}_{1p} = V_{1p} \vec{s}_{1p} \quad (5.2a)$$

$$\vec{v}_{1n} = V_{1n} \vec{s}_{1n} \quad (5.2b)$$

$$\vec{v}_2 = \frac{V_2}{n_t} \vec{s}_2 \quad (5.2c)$$

The average input and output currents can be represented by the real portion of the complex conjugate (represented by  $*$ ) of the complex switching function multiplied with the complex tank current,  $\vec{i}_{L_s} = I_{L_s} \angle \theta_2$ .

$$\langle i_{1p} \rangle_{T_s} = \text{Re}[(\vec{s}_{1p})^* \vec{i}_{L_s}] = \frac{2}{\pi} I_{L_s} \sin\left(\frac{\pi}{2}d_p\right) \cos \theta_{1p} \quad (5.3a)$$

$$\langle i_{1n} \rangle_{T_s} = \text{Re}[(\vec{s}_{1n})^* \vec{i}_{L_s}] = \frac{2}{\pi} I_{L_s} \sin\left(\frac{\pi}{2}d_n\right) \cos \theta_{1n} \quad (5.3b)$$

$$\langle i_2 \rangle_{T_s} = \frac{1}{n_t} \text{Re}[(\vec{s}_2)^* \vec{i}_{L_s}] = \frac{2}{\pi} \frac{I_{L_s}}{n_t} \sin\left(\frac{\pi}{2}d_2\right) \cos \theta_2 \quad (5.3c)$$

The phase shifts between the primary switching functions and complex tank current are related through primary phase shifts.

$$\theta_{1p} = \phi_{1p} - \theta_2 \quad (5.4a)$$

$$\theta_{1n} = \phi_{1n} - \theta_2 \quad (5.4b)$$

In steady state, the dynamic components in the resonant tank are eliminated and only the resulting impedance from the phasor transform remains.

$$X_s = \omega_s L_s - \frac{1}{\omega_s C_s} \quad (5.5)$$

The complex tank current can now easily be solved for by the simple circuit shown in Fig. 5.6.

$$\vec{i}_{L_s} = \frac{\vec{v}_{1p} + \vec{v}_{1n} - \vec{v}_2}{jX_s} \quad (5.6)$$

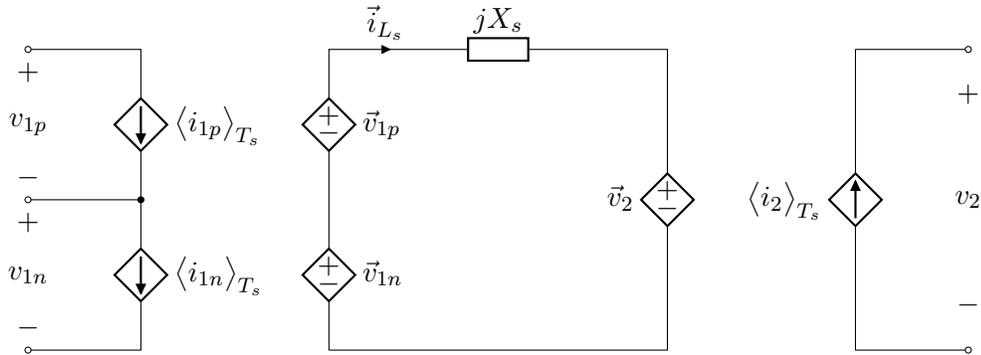


Fig. 5.6: Equivalent phasor transformed circuit for the 3LADAB.

The vector diagram of the complex phasors of the HF resonate tank operating in sector  $n$  is shown in Fig. 5.7. The combination of the primary voltage vectors is shown in a dashed line labeled as  $\vec{v}_1 = \vec{v}_{1p} + \vec{v}_{1n}$ .

The complex tank current can be transformed back into the time domain in order to

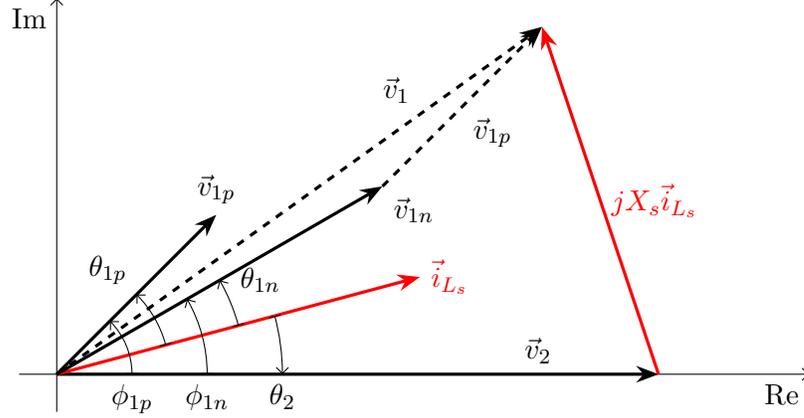


Fig. 5.7: Fundamental vector diagram of the 3LADAB in sector n.

solve for the instantaneous power flow. The following equations are specific to sector n in order to simplify the expressions:  $d_n = 1$ ,  $\phi_{1n} = \frac{\pi}{2}d_\phi$ ,  $\phi_{1p} = \frac{\pi}{2}(d_\phi + 1 - d_p)$ , and  $d_2 = 1$ .

$$i_{L_s}(t) = \frac{4}{\pi X_s} \left[ -V_{1p} \sin\left(\frac{\pi}{2}d_p\right) \cos\left(\omega_s t + \frac{\pi}{2}(d_\phi + 1 - d_p)\right) - V_{1n} \cos\left(\omega_s t + \frac{\pi}{2}d_\phi\right) + \frac{V_2}{n_t} \cos(\omega_s t) \right] \quad (5.7)$$

$$P_{1p}(t) = \frac{4}{\pi} V_{1p} \sin\left(\frac{\pi}{2}d_p\right) \sin\left(\omega_s t + \frac{\pi}{2}(d_\phi + 1 - d_p)\right) i_{L_s}(t) \quad (5.8)$$

$$P_{1n}(t) = \frac{4}{\pi} V_{1n} \sin\left(\omega_s t + \frac{\pi}{2}d_\phi\right) i_{L_s}(t) \quad (5.9)$$

$$P_2(t) = \frac{4}{\pi} \frac{V_2}{n_t} \sin(\omega_s t) i_{L_s}(t) \quad (5.10)$$

By integrating the instantaneous powers from each port over a switching period and normalizing the result, the average power can be obtained.

$$\begin{aligned}
\langle P_{1p} \rangle_{T_s} &= \frac{1}{2\pi} \int_0^{2\pi} P_{1p}(t) d(\omega_s t) \\
&= \frac{8}{\pi^2 X_s} V_{1p} \sin\left(\frac{\pi}{2} d_p\right) \left[ -V_{1n} \cos\left(\frac{\pi}{2} d_p\right) + \frac{V_2}{n_t} \cos\left(\frac{\pi}{2} (d_\phi - d_p)\right) \right]
\end{aligned} \tag{5.11}$$

$$\begin{aligned}
\langle P_{1n} \rangle_{T_s} &= \frac{1}{2\pi} \int_0^{2\pi} P_{1n}(t) d(\omega_s t) \\
&= \frac{8}{\pi^2 X_s} V_{1n} \left[ V_{1p} \sin\left(\frac{\pi}{2} d_p\right) \cos\left(\frac{\pi}{2} d_p\right) + \frac{V_2}{n_t} \sin\left(\frac{\pi}{2} d_\phi\right) \right]
\end{aligned} \tag{5.12}$$

$$\begin{aligned}
\langle P_2 \rangle_{T_s} &= \frac{1}{2\pi} \int_0^{2\pi} P_2(t) d(\omega_s t) \\
&= \frac{8}{\pi^2 X_s} \frac{V_2}{n_t} \left[ V_{1p} \sin\left(\frac{\pi}{2} d_p\right) \cos\left(\frac{\pi}{2} (d_\phi - d_p)\right) + V_{1n} \sin\left(\frac{\pi}{2} d_\phi\right) \right]
\end{aligned} \tag{5.13}$$

By dividing out the dc voltages from each port from average power processed by each port, another expression for the average input currents can be obtained.

$$\langle i_{1p} \rangle_{T_s} = \frac{8}{\pi^2 X_s} \sin\left(\frac{\pi}{2} d_p\right) \left[ -V_{1n} \cos\left(\frac{\pi}{2} d_p\right) + \frac{V_2}{n_t} \cos\left(\frac{\pi}{2} (d_\phi - d_p)\right) \right] \tag{5.14}$$

$$\langle i_{1n} \rangle_{T_s} = \frac{8}{\pi^2 X_s} \left[ V_{1p} \sin\left(\frac{\pi}{2} d_p\right) \cos\left(\frac{\pi}{2} d_p\right) + \frac{V_2}{n_t} \sin\left(\frac{\pi}{2} d_\phi\right) \right] \tag{5.15}$$

$$\langle i_2 \rangle_{T_s} = \frac{8}{\pi^2 X_s} \frac{1}{n_t} \left[ V_{1p} \sin\left(\frac{\pi}{2} d_p\right) \cos\left(\frac{\pi}{2} (d_\phi - d_p)\right) + V_{1n} \sin\left(\frac{\pi}{2} d_\phi\right) \right] \tag{5.16}$$

#### 5.1.4 MATLAB Simulation Model

In order to perform fast simulations of the 3LADAB topology without the use of conventional switching converter simulators a MATLAB script was created to simulate the dynamics of the topology. The conventional simulators used by power electronics designers include PLECs, or LTspice. This section explains how the simulation was created and which solvers are best depending on the simulation settings.

PLECs is a great tool for analyzing the dynamic behavior of switching converter systems and has transfer function identification capabilities. However, PLECs simulations do

not give the designer much choice when choosing a solver and the simulations cannot be run in an automated way which increases the time and effort from the control engineer when implementing new learning based controllers. LTspice is another useful tool for analyzing switching circuits. LTspice considers the non-linear switching behavior exhibited by MOS-FETs using data sheet parameters or even devices model supplied by the manufactures. The great detail in LTspice simulations makes it good for analyzing the converter in steady state; however, there is typically too much detail to run control simulations in reasonable time.

To overcome the challenges from the conventional simulators, a MATLAB simulation of the 3LADAB was created and is shown in Appendix B. The simulation defines the all circuit parameters of the from the 18kW 3LADAB module designed in Section 5.2. The states considered include the 2nd order LC resonant tank and the output capacitance is also considered instead of a stiff voltage source load. This makes the simulated system a 3rd order system overall. The load is represented as a resistor in parallel with the output capacitor.

The full simulation is broken into smaller simulations which are the length of the switching period,  $T_s = 1/f_s$ . The final state for the previous switching period simulation is used as the intial state for the next switching period simulation. The control parameters,  $d_p$ ,  $d_n$ , and  $d_\phi$  and input voltages,  $v_{1p}$  and  $v_{1n}$ , are all held constant for the simulation over one switching period. The simulation can be modified to provide ac input voltage but is left constant for now.

Before each switching period the control parameters are updated. As shown in Fig. 5.5 the control parameters control the switching functions for each port of the converter and each switching functions can be represented as the square wave signal actuated by the switching bridge or the fundamental harmonic. The simulation can be used to simulate both types of switching functions depending on which function is desired.

Using the square wave switching functions results in the most accurate simulation model because it include all of the harmonics introduced by the switching bridges in the 3LADAB. The downside to using square wave switching functions is that the system becomes stiff and

“ode45” solver in MATLAB does not solve the system correctly. However, using a stiff solver such as “ode23s” in MATLAB finds a fast solution but is a little slower than “ode45”. When simulating the fundamental of the switching functions, “ode45” is the best solver because the simulation is no longer stiff; however, the results from the simulation are not as accurate depending on the quality factor of the resonant tank.

After each switching period the average input current is calculated as the output of the simulation. After the simulation completes the simulation of all the switching periods, the data can be saved or plotted for future use.

## 5.2 Design of 18 kW 3LADAB Module

This section describes the design procedure for the 18 kW 3LADAB prototype. The common starting place for all converter designs is the input/output specifications. The specifications for the design at hand were determined from Chapter 4 and summarized in Table 5.3.

Table 5.3: Input/output specifications for the 3LADAB modules used in the modular XFC design.

Specification	Minimum	Nominal	Maximum
3-phase line-line input voltage	-10%	480 V <sub>RMS</sub>	+10%
Peak soft dc-link (total)	611 V	679 V	747 V
Peak soft dc-link (single port)	529 V	588 V	647 V
Output power	–	–	18 kW
Output voltage	120 V	–	160 V
Output current	50%	–	112.5 A

The specifications highlight the unique challenge at hand for the design an efficient DAB based topology due to the wide voltage variation in both the input and output voltage. The output voltage is not constant due to the intended application which is battery charging. The output voltage rises and falls with a relative difference of 25%. The input voltage is not constant throughout the grid cycle due to the nature of the soft dc-link envelope which rises and falls with the line-line voltage of the grid. The relative difference of the input voltage is

13.4% when considering a constant grid voltage; however; if one considers the  $\pm 10\%$  voltage variation that the grid allows for then the relative difference in the input voltage can be as high as 29.2%.

The peak value of the total soft dc-link voltage occurs at equal input voltages or operating point “a”. With equal input voltages the current drawn from each port should be the same for meeting PFC requirements, and thus the applied duty cycles are the same. When modulating the 3LADAB with equal duty’s and equal input voltage, the 3LADAB behaves exactly like a normal DAB because the back-back switches in the T-type legs never conduct.

On the other hand, the minimum value of the total soft dc-link voltage occurs at operating point “c” in which one soft dc-link port is operating with its maximum voltage while the other port has 0 V. This case also resembles the behavior of a DAB because the HF voltage driving the primary side does not appear as the a 3L waveform regardless of the duty cycle applied to the lesser port. This is due to the fact the lesser input port has 0 V and does not excite the resonant tank.

Thus the design of the 3LADAB can be performed in a similar manner as the traditional DAB design considering the maximum and minimum voltage operating points. The following proposed design procedure considers operating points “a” and “c” in order to determine the parameters in the design: turns ratio ( $n_t$ ), tank impedance ( $L_s, C_s, \omega_r, Q$ ), switching frequency ( $f_s$ ), maximum normalized phase shift ( $d_{\phi,max}$ ), input/output filter capacitors ( $C_{pon}, C_{out}$ ), and the switching devices for both the primary and secondary bridges.

The complete schematic of the 18 kW module is shown in Fig. 5.8. All four secondary bridges and secondary windings are shown explicitly; however, the operation of all secondaries is identical as to emulate a paralleled operation. The tank components,  $C_{s1}, C_{s2}$ , and  $L_{s2}$  can all be referred to the primary and combined to form an equivalent LC circuit consistent with Fig. 5.1.

### 5.2.1 Transformer Turns Ratio Selection

The transformer turns ratio,  $n_t$ , is an important parameter for the 3LADAB because it decides how the input voltage is scaled to the output voltage. In the traditional DAB design,

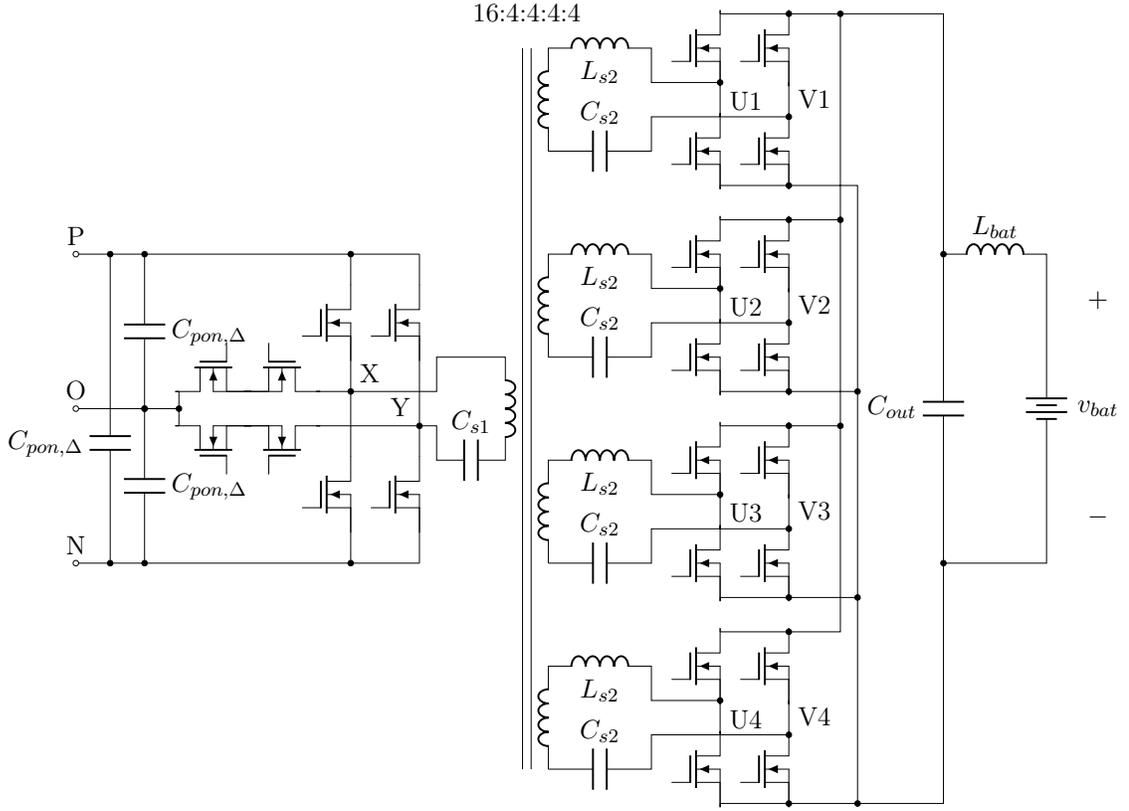


Fig. 5.8: The complete schematic of one 18 kW 3LADAB module.

the turns ratio is set by the nominal input to output voltage ratio; however in the case of the 3LADAB design there is no nominal input or output voltage as they both have a range of values. In order to determine a nominal input voltage for the 3LADAB the average value soft dc-link waveform,  $V_{pn,avg}$  was taken using the following calculation.

$$V_{ll,pk} = \sqrt{2}V_{ll,RMS} = 678.82 \text{ V} \quad (5.17)$$

$$V_{pn,avg} = V_{ll,pk} \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \cos(\omega_g t) d(\omega_g t) = \frac{3}{\pi} V_{ll,pk} = 648 \text{ V} \quad (5.18)$$

The nominal output voltage was also taken as the average of the output voltage,  $V_{out,avg}$  range which is simply 140 V. The ideal transformer turns ratio is determined by the ratio of these two average values.

$$n_{t,ideal} = \frac{V_{pn,avg}}{V_{out,avg}} = 0.216 \quad (5.19)$$

The ideal turns ratio was not selected due to the fact that it would be difficult to implement with a discrete number of windings on the primary and secondary side of the transformer. Instead of using the ideal ratio, ratios that were close to the ideal ratio and easy to implement with a discrete number of windings were considered. A list of the considered ratios and their corresponding conversion ratios is given in Table 5.4. The maximum conversion ratio,  $M_{max}$ , occurs at the lowest input voltage and highest output voltage while the minimum conversion ratio,  $M_{min}$ , occurs at the highest input voltage and lowest output voltage.

Table 5.4: Possible transformer turns ratio and the corresponding maximum and minimum conversion ratios.

$n_1 : n_2$	$n_t$	$M_{max}$	$M_{min}$
5:1	0.2	1.51	0.8
9:2	0.22	1.36	0.72
4:1	0.25	1.21	0.64

The selection for a transformer turns ratio of 4:1 or  $n_t = 0.25$  was selected due to the fact that this design puts the least amount of stress on the primary bridge in terms of soft switching range. That is to say when the conversion ratio  $M$  is greater than unity, the soft switching range of the primary bridge depends on the applied phase shift which is load dependent. On the other hand, when the the conversion ratio is less than unity the primary bridge is guaranteed to soft switch regardless of load while the secondary soft switching becomes load depended. Because the primary bridge has a higher voltage input, the priority was given to the primary bridge.

Furthermore, the selection of  $n_t = 0.25$  was greatly taken advantage of for the design of the transformer due to the fact that the transformer was implemented as 4, 1:1 transformers which were connected in series on the primary and paralleled on the output. This action

would not be possible if the turns ratio of 9:2 was chosen, and the 5:1 design would put more stress on the primary bridge which would make soft switching more difficult in a majority of the operation range.

### 5.2.2 Tank Impedance and Switching Frequency Selection

The selection of the tank impedance and switching frequency was an iterative process between design analysis and simulation. The starting point for selecting the tank impedance was to define a per unit normalization to the design in order to normalize the voltage and current quantities. The selected base values for the normalization are arbitrary; however, the highest phase shift is required when the input voltage is at its minimum and the while the output voltage is maximum so the reflected, nominal, minimum input voltage was used as the base value.

$$V_{base} = n_t V_{pn,min} = 147 \text{ V} \quad (5.20a)$$

$$I_{base} = I_{out,max} = 112.5 \text{ A} \quad (5.20b)$$

$$Z_{base} = \frac{V_{base}}{I_{base}} \quad (5.20c)$$

$$P_{base} = V_{base} I_{base} \quad (5.20d)$$

With the per unit definitions, the selection of the per unit tank impedance,  $X_{s,pu}$ , was determined using the normalized max phase shift,  $d_{phi,max}$ . The power equation 5.13 derived in 5.1.3 is converted to per unit for the special case of operating point “c” in which there is only input port operating with the minimum input voltage.

$$P_{out,pu} = \frac{8}{\pi^2 X_{s,pu}} \frac{V_{out,pu}}{n_t} V_{pn,min,pu} \sin\left(\frac{\pi}{2} d_\phi\right) \quad (5.21)$$

$$X_{s,pu} = \frac{X'_{s,pu}}{n_t^2} \quad (5.22)$$

$$V_{pn,min,pu} = \frac{V_{pn,min}}{n_t V_{pn,min}} = \frac{1}{n_t} \quad (5.23)$$

$$\frac{V_{out,pu}}{n_t} = \frac{V_{out}}{n_t^2 V_{pn,min}} = \frac{M}{n_t} \quad (5.24)$$

$$P_{out,pu} = \frac{8}{\pi^2 X'_{s,pu}} M \sin\left(\frac{\pi}{2} d_\phi\right) \quad (5.25)$$

Here the per unit power equation has been manipulated to be in terms of tank impedance referred to the secondary side of the transformer,  $X'_{s,pu}$  and the conversion ratio  $M = V_{out}/(n_t V_{pn,min})$ . The expression is now rearranged to solve for the tank impedance using the maximum conversion ratio,  $M_{max} = V_{out,max}/(n_t V_{pn,min})$ , maximum normalized phase shift,  $d_{\phi,max}$ , and maximum per unit output power,  $P_{out,max,pu} = V_{out,max} I_{out,max}/P_{base}$ .

$$X'_{s,pu} = \frac{8}{\pi^2} \frac{M_{max}}{P_{out,max,pu}} \sin\left(\frac{\pi}{2} d_{\phi,max}\right) \quad (5.26)$$

The maximum conversion ratio and maximum per unit power are determined by the converter specifications, and the free value to be selected by the designer is the maximum normalized phase shift,  $d_{\phi,max}$ . The maximum possible value for the maximum normalized phase shift is 0.5 which would correspond to a phase shift of 90°; however, this is a poor selection for the design as this forces the design to operate with higher RMS current in the resonant tank which increases the conduction losses in the tank components as well as the switching devices.

The value of  $d_{\phi,max}$  was selected by observing simulation waveforms of the resulting designs and increasing the value as necessary in order to maintain soft-switching of all devices while the load current is reduced to 50% of the maximum output current.

To determine the value of the tank components,  $L_s$  and  $C_s$ , there are two more free variables that need to be selected which are the quality factor of the resonant tank,  $Q$ , and

the switching frequency of the system,  $f_s$ . The quality factor of the tank is a dimensionless quantity that changes the shape of the tank currents. The higher the quality factor, the lower the value of resonant capacitor,  $C_s$ , which in turn results in a larger voltage swings for the same RMS current flowing through it. Increasing the quality factor gives the tank current a more sinusoidal shape due to the resonant capacitor voltage becoming more comparable to to the square wave voltages which are driving resonant inductor.

The cost of the increasing the quality factor is increased RMS currents for the same power flow. To minimize the RMS currents and therefore conduction losses, the quality factor can be reduced so much that the resonant capacitor becomes a dc blocking capacitor which results in the non-resonant DAB. However, this is undesirable because the sinusoidal analysis presented in 5.1.3 would not be valid. The non-resonant DAB also has more harmonics in the HF tank which result in higher switching instant currents and it is more difficult to filter the resulting EMI.

The quality factor selected for the design was chosen to  $Q = 0.9$  in order to reduce the RMS of the HF tank while also taking advantage of the resonant benefits such as reduced switching instant currents to avoid excessive ZVS currents. With the quality factor and per unit tank impedance decided, the calculation for the normalized switching frequency,  $F$  follows a straightforward calculation.

$$F \triangleq \frac{f_s}{f_r} = \frac{1}{2} \left[ \frac{X'_{s,pu}}{Q} + \sqrt{\left( \frac{X'_{s,pu}}{Q} + 4 \right)^2} \right] \quad (5.27)$$

The final free design parameter to determine the value of the tank components,  $L_s$  and  $C_s$ , is the switching frequency of the system,  $f_s$ . The switching frequency of the system directly determines the resonate frequency of the tank,  $f_r$ , through the normalized switching frequency. Note that the following value of the resonant inductance and capacitance find the impedance value referred to the secondary side of the transformer. The physical location of the reactive elements does not affect the operation of the topology if the impedance value is appropriately altered when pushing elements to the primary or secondary side of the resonant tank.

$$f_r = \frac{f_s}{F} \quad (5.28)$$

$$\omega_r = 2\pi f_r \quad (5.29)$$

$$L'_s = Z_{base} \frac{Q}{\omega_r} \quad (5.30)$$

$$C'_s = \frac{1}{L_s \omega_r^2} \quad (5.31)$$

The higher the switching frequency, the smaller the resulting tank components become. Thus, it is beneficial to increase the switching frequency in order to simplify the design of the tank components. However, the drawbacks to increasing the switching frequency arise when the switching devices are not properly soft switched which results in switching loss proportional to the switching frequency. Furthermore, higher switching frequency increase the ac resistance in the conductors which make up the HF resonant tank due to losses caused by the proximity effect and the skin effect.

For high power designs such as the one at hand, the current requirement of the HF tank increases with the power level which increases the required conductor thickness to carry such current. The design is intended to soft switch for the majority of the operating points, so the switching frequency was selected to 100 kHz in order to find a balance between tank size and increased ac losses due to skin effect.

### 5.2.3 Input/Output Filter Sizing

To size the input and output capacitors appropriately, the PLECs simulation of the 3LADAB with ideal voltage sources for the input and output ports was used. The highest RMS current to be filtered by the input or output capacitors occurs when the HF tank is operating with the highest RMS current which occurs with maximum power and conversion ratio.

The calculation for the output capacitance,  $C_{out}$ , depends on the desired voltage ripple on the output voltage,  $\Delta V_{out,pk-pk}$ , and the charge,  $\Delta q_{out}$ , which is sourced and sunk by the

capacitor twice a switching period. The ripple voltage is a value left to the designers while the charge is calculated from the PLECs simulation of the the 3LADAB.

$$\Delta q_{out} = \frac{T_s}{4} \left\langle |i_{out} - \langle i_{out} \rangle_{T_s/2}| \right\rangle_{T_s/2} \quad (5.32)$$

$$C_{out} = \frac{\Delta q_{out}}{\Delta V_{out,pk-pk}} \quad (5.33)$$

The input capacitors make up the soft dc-link capacitance,  $C_{pon}$ , and form a balanced 3-phase, delta connected load seen by the grid. The value of capacitance should be large enough to adequately filter the HF current drawn by the 3LADAB while remaining small enough to not significantly impact the reactive power with the grid.

By interleaving paralleled 3LADAB modules, some of the switching frequency ripple on soft dc-link capacitors can be cancelled and effective switching frequency increases; however, for initial module testing only a single 3LADAB module will be operating so the input capacitance should be sized accordingly.

Excessive voltage ripple on the soft dc-link causes sector distortions in the grid current around the switching of the Unfolder [11]. The sector crossing of the Unfolder also corresponds to the lowest input voltage on the soft dc-link which leads to highest RMS of the tank currents. Therefore the soft dc-link capacitance should be sized to keep the voltage ripple across the lesser port (in sector n this would be the p-port),  $\Delta V_{po,pk-pk}$  to a desired value in which the sector distortions are minimal.

The soft dc-link capacitors were also sized considering the equivalent wye connected arrangement. The effective charge,  $\Delta q_e$  which is responsible for causing the HF voltage ripple on the wye capacitor connected to the O rail can be found from the simulation at operating point ‘‘c’’ which coincides with the greatest charge sourcing requirements.

$$\Delta q_e = \frac{T_s}{2} \langle i_n - i_p \rangle_{T_s/2} = \frac{T_s}{2} \langle i_o \rangle_{T_s/2} \quad (5.34)$$

$$C_{pon,\lambda} = \frac{\Delta q_e}{\Delta V_{po,pk-pk}} \quad (5.35)$$

$$C_{pon,\Delta} = \frac{C_{pon,\lambda}}{3} \quad (5.36)$$

#### 5.2.4 Switching Devices Selection

The switching devices for the primary and secondary side were selected based of the device voltage ratings and the RMS current seen by the device overall the operating points. The RMS current stress was found using the PLECs simulation of the worst case operating points. The current stress in each leg of the primary and secondary are symmetrical due to the nature of the modulation and topology. The switching losses were not considered because the design was intended to soft switch all devices.

The maximum power loss for all the switches is expressed in a simply formula using maximum RMS current and the device on state resistance.

$$P_{sw,max} = R_{ds,on} I_{RMS,max}^2 \quad (5.37)$$

The primary devices used to compose the 3L T-type bridge were separated into two categories which are the H-bridge devices, and the back-back devices. The H-bridge devices connect the switch nodes to the P and N rails and see the more RMS compared to the back-back devices. The back-back devices are common source connected and allow create four quadrant connection from the switch node to the O rail. The H-bridge devices block the entire soft dc-link voltage when they are off, so 1200 V SiC MOSFETs were considered as possible candidates. The back-back devices are only required to block the voltage of a single soft dc-link port so 1000 V SiC MOSFETs were considered as well as the more commonly available 1200 V SiC MOSFETs.

The selected devices for the primary H-bridge switches was IMZ120R030M1HXKSA1 from Infineon Technologies. The H-bridge devices were implemented with two switches in

parallel and are driven by the same gate driver so that the devices are turned on and off ideally at the same time. The chosen device for the back-back switches was C3M0065100K from Cree/Wolfspeed. The back-back devices were not paralleled because the device has lower on state resistance and lower current stress.

The secondary devices are required to block a much lower voltage (160 V), so 250 V Si MOSFETs were considered. The RMS current flowing through the secondary side of the transformer was 4 times that of the primary so the devices used to implement the secondary required much lower  $R_{ds,on}$  or a higher number of devices in parallel were required.

In order to simplify the current sharing problems on secondary side of the transformer that arise due to paralleling many MOSFETs, the transformer was implemented with multiple secondary windings sharing the same magnetic core. The shared magnetic core forces all the secondary windings to share the same RMS current. Each secondary winding connects to its own secondary full bridge and the power is combined at the dc bus at the output. The multiple secondary bridges are always switching synchronously so that appear in parallel from the transformers perspective. Using this method, the current is shared equally amongst the secondary bridge.

By using four secondary windings and a transformer turns ratio of 4:1, the RMS current in primary windings is equivalent to the current flowing through each of multiple secondary windings. This simplifies the implementation of the secondary devices because they see current stress similar to the primary devices. By selecting devices with equivalent  $R_{ds,on}$ , the power loss will be similar and the same heat sink structure can be used to cool all devices given that have the same footprint. The package selected for the primary and secondary devices was chosen to be the TO-247 package because it is a common package for both primary and secondary devices.

The device chosen for the the secondary switching devices was IRF250P225 from Infineon Technologies. Each switch on each of the secondary full bridges was implemented with two paralleled devices which were driven by the same gate driver. With four secondary bridges and eight switches per full bridge, the total number of devices required by

the secondary was 32.

To simplify the cooling method for initial design, a forced air cooling design was selected. The selected heat sink was chosen to be the C40-058-VE from Ohmite which can mount up to two devices. When using two heat sinks mounted back-back, up to four devices can be cooled and a  $40 \times 40$  mm fan can be mounted between them in order to force air through the fins. To isolate the drain tabs of the TO-247 package from the heat sinks, a thermal sleeve was placed around all devices, CP33-TO247-28.5-17.5-5.8-0.3, from t-Global Technology. The silicon material of the sleeve also removes any gaps in the thermal connection removing the need for thermal paste.

### 5.2.5 Resonant Tank and Transformer Realization

The section discusses the design of the HF resonant tank including the resonant capacitor implementation, resonant inductor design and fabrication, and transformer design and fabrication. The tank components can be arbitrarily placed on either side of the transformer as long as the impedance value is appropriately adjusted. The selected design splits the resonant capacitor between both sides of the transformer while the resonant inductor was just implemented on secondary side.

Having capacitors in series with the primary and secondary windings is desirable because capacitors can block dc currents. This is beneficial in order to avoid saturating the transformer with switching bridges on either side of the transformer. Furthermore, splitting the resonant capacitor helps with the heat dissipation due to the heat generated from the losses. The value of the resonant capacitance that the design required,  $C_s = n_t^2 C'_s$ , was split equally amongst the primary ( $C_{s1}$ ) and secondary ( $C_{s2}$ ). The capacitance placed on the secondary side of the transformer needed to be split amongst the four parallel secondary windings so the value of capacitance was divided by four.

$$C_{s1} = (n_t^2)2C'_s = \frac{C'_s}{8} = 2C_s \quad (5.38)$$

$$C_{s2} = \left(\frac{1}{4}\right)2C'_s = \frac{C'_s}{2} = 8C_s \quad (5.39)$$

The resonant capacitors were implemented by paralleling multiple polypropylene film and foil capacitors intended for pulse applications, specifically the FKP series from WIMA were considered. To choose the appropriate number of capacitors to be placed in parallel the maximum ac voltage across each capacitor is calculated from the maximum RMS current of the resonant tank,  $\tilde{i}_{L_s}$ , where the  $\tilde{\phantom{x}}$  is used to denote the RMS value of the signal.

$$\tilde{v}_{C_s} = \frac{\tilde{i}_{L_s}}{\omega_s C_s} \quad (5.40)$$

Using the data sheet supplied by the capacitor manufactures, one can find maximum RMS voltage that each capacitor can take using the graphs which show the voltage derating with frequency. Once a value of capacitance is found to permit the maximum RMS voltage required by the tank then the designed must put enough of those capacitors in paralleled to reach the desired capacitance value. This process was repeated twice for the primary and secondary side capacitors because the capacitors had different stress due to the different capacitance value.

The design of the transformer was done prior to the design of the resonant inductor because the leakage inductance of the transformer should be subtracted from the external inductance added to the tank. The first step in the design of the transformer and inductors is to determine the wire which will be used to wind the magnetics. Litz wire is a popular choice for HF magnetics because the wire is made up of many insulated, paralleled strands which are wound in such a way to avoid losses that occur due to the skin effect and the proximity effect up to 1 MHz.

The litz wire diameter was selected by finding a wire which can carry more than the maximum RMS tank current assuming a permissible current density of  $J_{Litz} = 5 \text{ A/mm}^2$ .

The effective diameter of the litz wire,  $d_{\text{Litz}}$ , is calculated by multiplying the number of strands,  $n_{\text{strand}}$ , within the litz bundle by the diameter of each strand,  $d_{\text{strand}}$ . Ensuring that the ampacity of the litz wire,  $\text{Ampacity}_{\text{Litz}}$ , is greater than maximum RMS tank current will ensure that the winding losses will not overheat the wire.

$$d_{\text{Litz}} = n_{\text{strand}}d_{\text{strand}} \quad (5.41)$$

$$\text{Ampacity}_{\text{Litz}} = J_{\text{Litz}}d_{\text{Litz}} \quad (5.42)$$

The selected litz wire for the design was D1050/#38 which is a 1050 double insulated strands of 38 AWG wire. The physical diameter (not effective diameter,  $d_{\text{Litz}}$ ) of the litz wire was 6 mm which is important for calculating how many turns will fit into the window area of the ferrite cores.

The litz wire used for the inductors and transformer windings was terminated into a lug so that it can be connected to the PCB using bolts. The litz wire needs to be dipped into solder before crimping or soldering to the lug because it needs to be ensured that all strands of the litz wire are properly connected in order to take full advantage of the litz structure. This soldering was accomplished by dipping the litz into a solder pot for a few seconds with gentle agitation.

The next step in the transformer design is find a ferrite core which will guide the magnetic fields and couple the primary and secondary windings. The core losses are dependent on core material and magnetic flux density. The core material selection is highly dependent on the switching frequency and the metric for determining which material should be used is the performance factor. The performance factor is a measure of how much a power a core material can handle at different frequencies. At the selected operating frequency of 100 kHz, the performance of 3C94 material is among the highest available on the market so it was selected as the material for the transformer and inductor cores.

The peak flux density,  $\Delta B$ , can be calculated using the volt-seconds applied to the primary,  $\lambda_1$ , the number of turns on the primary winding,  $n_1$ , and the effective area of the

core,  $A_c$ .

$$\lambda_1 = \frac{V_{pn,max}}{2f_s} \quad (5.43)$$

$$\Delta B = \frac{\lambda_1}{2n_1 A_c} \quad (5.44)$$

The volt-seconds applied to the transformer cannot be changed as it is a function of the maximum input voltage and switching frequency; however, the number of turns on the primary can be adjusted in order to reduce swing in the peak flux density. From the data sheet of the core material, the specific power loss,  $P_v$ , can be calculated as function of the peak flux density. Using the volume of the core,  $V_c$ , the total core loss,  $P_{c,loss}$ , can be calculated.

$$P_{c,loss} = P_v V_c \quad (5.45)$$

The core selection was iterative process between selecting cores available on the market, and testing them to see which core provided the lowest losses. The process began by evaluating how many turns could be wrapped around the core because the more turns used the lower peak flux density is seen by the core. Because the secondary was implemented with four windings which each have a fourth of the number of turns as the primary, the transformer required enough window area in order to wind twice the number of turns as the primary. The next steps were calculating the peak flux density and resulting core loss.

The final selected design was two U cores, U93/76/30-3C94, from Ferroxcube. The primary winding was implemented with 16 turns with approximately four turns wrapped around each post of the transformer. Concentrically wrapped around the the primary winding, each secondary winding was wrapped with four turns its own post.

To help bring the heat generated from the primary winding to the outside of the transformer, a thermal epoxy, 8329TCF-50ML from MG Chemicals, was coated around the primary windings. A Nomex paper insulator with a thickness of 5 mil was used to separate the

primary windings from the secondary windings, as well as separating the secondary windings from each other as they are in close proximity on the inner side of the transformer.

With transformer fully designed, the leakage inductance can be estimated using a formula from [27]. The leakage inductance calculated was with respect to the secondary,  $L_{s2,ltk}$ . This leakage inductance could also have been calculated with respect to the primary; however, the resonant inductors were implemented on the secondary side, so this value is directly subtracted from the fabricated external inductors.

There is no benefit to having the resonant inductor on both sides of the transformer like there is with the capacitors, so the resonant inductance was just implemented on the secondary side. This was done because there are four secondary windings so the inductance was broken into four inductors which are placed in series with each secondary winding,  $L_{s2,ext}$ . This helps spread out the power dissipation which makes each inductor easier to cool. However, the value of inductance for each of the paralleled inductors is four times the resonant inductance referred to the secondary,  $L'_s = n_t^2 L_s$ .

$$L_{s2} = 4L'_s = \frac{L_s}{4} \quad (5.46)$$

$$L_{s2,ext} = L_{s2} - L_{s2,ltk} \quad (5.47)$$

The targeted value of inductance and the peak current through the inductor,  $i_{L_s,pk}$  are required for the inductor design. The peak is found through the simulation of the 3LADAB. The inductor design will use the same litz wire and core material as the transformer; however, different core shapes were considered specifically E cores. Another iterative design procedure was used to select the core.

The starting point for the design was to calculate the value of the inductance using the fringing factor,  $F_{FF}$ , area of the core,  $A_c$ , number of turns,  $n_{L_s}$ , length of the window area,  $l_w$ , and length of the air gap,  $l_g$ .

$$F_{FF} = 1 + \frac{l_g}{\sqrt{A_c}} \ln \frac{2l_w}{l_g} \quad (5.48)$$

$$L_{s2,ext} = F_{FF} \mu_0 A_c \left( \frac{nL_s}{l_g} \right)^2 \quad (5.49)$$

The length of the air gap can be implemented in discrete steps of 5 mil Nomex paper. The effective area of the core can be increased by using a discrete number of cores together which increases the inductance without increasing the peak flux density,  $B_{max}$ . The number of turns can be increased up to the value which can fit in window area and the inductance increases with square of the number of turns but also linearly scales the peak flux density.

$$B_{max} = \frac{i_{L_s, pk} L_{s2, ext}}{A_c n L_s} \quad (5.50)$$

The selected core, E47/20/16-3C94 from Ferroxcube, can fit up to four turns which completely fills the winding area, and this is desirable because no space is being wasted. The length of the air gap and number of core were adjusted in order to meet the targeted inductance value while ensuring the peak flux density does not cause too much power loss using the data sheet of the core material and volume of the core similar to the design of the transformer.

Custom bobbins were created for the transformer and inductors using selective laser sintering (SLS) with the Nylon 12 (SLS) material. This material is useful because it can withstand higher temperatures which are expected to occur due to the core and winding loss. The bobbins are used to insulate the windings from the core. The transformer bobbin was created in two halves which are each intended to mate with one U core on each side of the PCB. The inductor bobbins were designed to fit four pairs of E cores.

The inductors were wound onto the bobbins and high temperature hot glue was used to keep the windings in place. The Nomex sheets used to implement the air gap were glued together as well as glued to the E cores using HP250 from Devcon.

### 5.2.6 PCB Design

The first design of 18kW 3LADAB module was all done a single PCB. The PCB was designed to have all of the power components including the primary and secondary bridges with heat sinks, resonant capacitors, output capacitors, soft dc-link capacitors, input/output power connections, and space for mounting the magnetics and cooling fans. The gate drivers and embedded logic controller for all devices were not designed onto the power board. Instead, they were designed as separate PCBs intended to plug into the power board. The top side of the populated PCB is shown in Fig. 5.9 and the bottom side in Fig. 5.10.

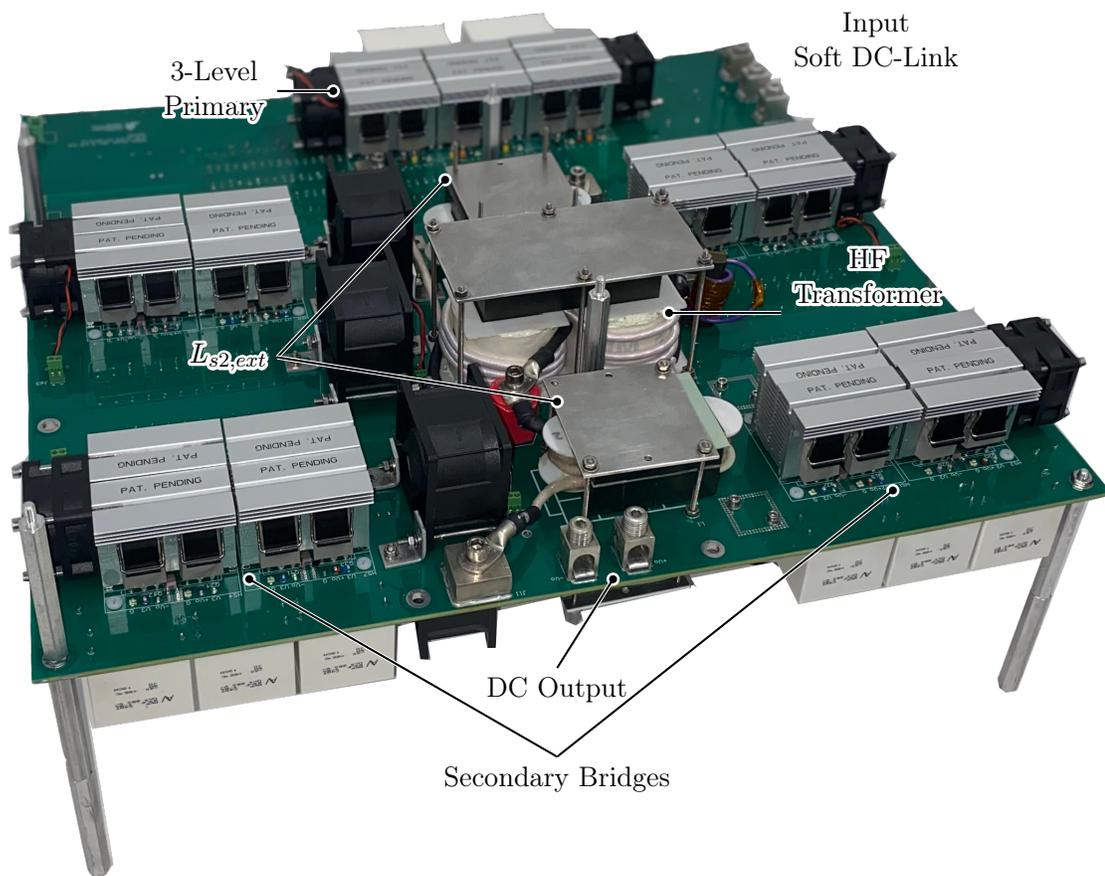


Fig. 5.9: The top side of the populated 3LADAB PCB.

The design of the PCB has many free parameters to choose such as the number of layers, layer spacing, copper weight, size dimensions, and the arrangement of components.

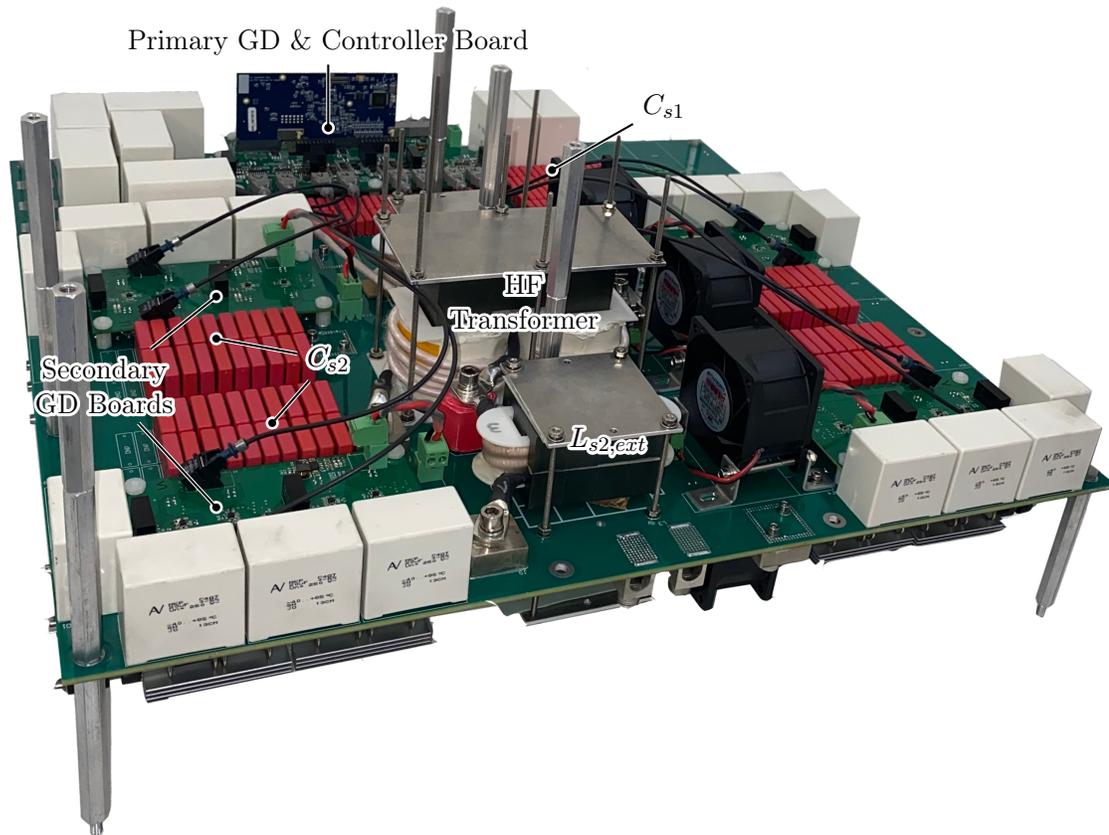


Fig. 5.10: The bottom side of the populated 3LADAB PCB.

The number of layers and layer spacing was determined primarily from the primary side voltage because it has higher voltage than the secondary. Because the input voltage from the soft dc-link is high voltage ( $480 V_{RMS}$ ), the clearance between adjacent layers must be carefully considered.

The voltage between the P and O rails or the O and N rails is at most 647V which requires 0.6175 mm spacing between internal conductors according to IPC-2221B. This distance is greater than the thickness of prepreg which is used to join adjacent PCB layers. In order to vertically space the conductors properly in the stack up, extra FR4 is needed between pairs of the PCB layers that are connected with prepreg. Considering the three power rails from the Unfolder, P, O, and N, plus an extra layer for routing the switch node connections from the T-type switching legs, there is a need for four layers. However, due to the minimum thickness of the prepreg, eight layers were used and layers connected by

prepreg were paralleled to increase the current carrying capability.

Extra distance (0.8675 mm) is required between the P and N rails because the peak voltage is higher (747 V). Because the switch node takes the voltage potential of all three Unfolder rails, it should maintain the maximum spacing between the P and N rails. The selected stack up is summarized by Table 5.5.

Table 5.5: The PCB layer stack up for the 3LADAB module.

Layer	Thickness	Node (Primary)	Node (Secondary)
L1 (Top)	105 $\mu\text{m}$	SW Node	SW Node
Prepreg	0.22 mm	–	–
L2	105 $\mu\text{m}$	SW Node	SW Node
FR4	0.25 mm	–	–
L3	105 $\mu\text{m}$	O	$V_{out}^+$
Prepreg	0.22 mm	–	–
L4	105 $\mu\text{m}$	O	$V_{out}^+$
FR4	0.25 mm	–	–
L5	105 $\mu\text{m}$	P	Auxiliary 12 V
Prepreg	0.22 mm	–	–
L6	105 $\mu\text{m}$	P	Auxiliary GND
FR4	1 mm	–	–
L7	105 $\mu\text{m}$	N	$V_{out}^-$
Prepreg	0.22 mm	–	–
L8 (Bottom)	105 $\mu\text{m}$	N	$V_{out}^-$

The layer stack up relaxed the spacing between the O and P rails to 0.25 mm because the average voltage is much less than the peak voltage and increased the spacing between the P and N rails to 1 mm to account for any voltage surges. The unsymmetrical board stack up led to a board warpage which was not a problem for the prototype design because everything was populated by hand.

The copper used for the switch nodes on both the primary and secondary bridges was minimized to reduce the capacitance to the switch node. The remaining area on the top 2 layers was used for the N rail on the primary side and  $V_{out}^-$  rail on the secondary side. The

common source connection between the back-back switches was routed on L4.

The copper weight of the PCB is decided by the current requirement of the of the switch nodes. The power rails are implemented with large copper planes so they generally have lower resistance than the switch node which should have minimized area for reducing the capacitance. Therefore the switch node decides copper weight requirements. Using paralleled layers helps to reduce the copper weight and two layers are being used to paralleled for the switch node routing. It was decided that 3oz copper was needed to avoid heating of the PCB.

The heat sinks should be tied to a voltage potential so that they do not function as an antenna that radiates EMI due to the HF switching of the devices. On the primary side the heat sinks were connected to the O rail because the O potential is mid point between the extremes of the P and N rail. On the secondary side the heat sink were tied to the negative rail of the DC output,  $V_{out}^-$ .

To simplify the wiring of the auxiliary power, the PCB was used to route the auxiliary 12 V power supply to each of the fans and gate drivers. The PCB does not have provisions to generate the 12 V power supply, but rather has input ports for an off board power supply to connect to. The secondary port has entire layers dedicated to the auxiliary routing while the primary side shared L4 to route the auxiliary power.

The primary switching bridge was designed to have all the switching devices mounted on three pairs of heat sinks which are chained together so the forced air flows through all heat sinks. Recall that each heat sink can mount two devices, and a pair of heat sinks can mount four devices. The H-bridge devices were arranged on the outer most heat sinks with the top and bottom switches arranged next to each other on a single heat sink to minimize the switching loop inductance. Because the H-bridge switches were implemented with paralleled devices the 4 H-bridge devices for a single T-type leg occupy a pair of heat sinks. The middle pair of heat sinks is used to cool the back-back switches because there is a total of four back-back switches between the two T-type legs. A  $40 \times 40$  mm fan is mounted on the edges of the outside pairs of heat sinks with a common direction of airflow to improve

the cooling capacity of the heat sinks.

The switching loop inductance is minimized by placing ceramic capacitors between all of the Unfolder power rails. The ceramic capacitors should be in close proximity with the devices in order to effectively reduce the loop inductance. The capacitors were placed on both sides of the PCB directly underneath the heat sinks so that they are equal distance from the paralleled H-bridges on either side of the heat sinks. The ceramic capacitors were chosen by finding the smallest footprint which has the voltage isolation capability and the highest value of capacitance. Both X7R and C0G/NPO capacitors were used to minimize the switching loop inductance.

The switch node of the T-type switching legs were connected to custom copper terminal blocks which were used to connect to the litz wire of the transformer. These terminal blocks were cut from copper and drilled to provide mounting holes for the bolt connection to the litz wire and PCB. The copper blocks were soldered directly to the PCB to ensure a good electrical connection. One of the T-type switching legs was connected to the terminal block with the primary resonant capacitor bank in series with the connection.

The transformer was mounted in the middle of the PCB with half of the core on each side of the PCB so that the two U core were joined through the PCB. To avoid having an air gap, cutouts in the PCB were created so that the U cores can sit flush together. The U cores are held together by metal plates that are secured to the PCB using 4-40 rods.

To avoid having extra terminations in the primary winding, a slot in the PCB was created so that the primary winding can be continuously wrapped around the core and through the PCB. The primary winding terminates directly to the terminal blocks from the primary bridge with one on either side of the PCB.

The secondary windings of the transformer (two on each side of the PCB) are terminated with one end to terminal block which is connected to a switch node of the secondary through the resonant capacitors similar to the primary bridge. The other end of the secondary is connected to the external resonant inductance using an insulated standoff. The other end of the resonant inductor is terminated to another terminal block connected to the other

switch node of the secondary. The four resonant inductors are located on both side of the transformer and on both sides of the PCB. The inductors are held to the PCB using metal plates and 4-40 rods similar to the transformer core.

Each inductor and each half of the transformer is cooled by a  $60 \times 60$  mm fan mounted beside it. The fans are used to force air around the magnetics in order to keep them cool. The fans are arranged so that the air blown is in the same direction as the air flow from the  $40 \times 40$  mm fans which are mounted on switch heat sinks.

The four secondary bridges are placed om each corner of the transformer so that they are in close proximity and do not require long connections. The eight devices used on each secondary bridge are mounted on two pairs of heat sinks, one pair for each H-bridge. A single  $40 \times 40$  mm fan is mounted to the outside of the heat sink and the forced air is used to cool both pairs of heat sinks.

Similar to the primary H-bridge layout, the top and bottom devices are located on a single heat sink to minimize the switching loop inductance. Because the secondary has lower voltage, a smaller ceramic capacitor can be placed directed in between the devices mounted to a single heat sink.

The bulk filter capacitance is place around the heat sink structures of the primary and secondary bridges to filter the HF current from the switching bridges. The internal power rails of the PCB are brought out of the PCB to high current lugs, B1/0-PCB-L from LugsDirect.

### 5.2.7 Gate Driver/Controller Design

The gate driver boards were designed separate to the power PCB because the gate drive boards have many components with finer pitch pin spacing which are difficult to manufacture on the power PCB which used heavy copper. Two different gate driver designs were created: one for the primary switches and one for driving the a single secondary full bridge. In total, one primary gate drive board and four secondary gate drive boards are required for one 3LADAB module because there is four different secondary bridges.

The primary gate driver was designed to have the logic controller that runs the control algorithms based off sensor feedback and generates the gating signals. The controller used for the TMDSCNCD28379D controller card from Texas Instruments. This controller sends the eight gating signals to the gate drivers on the primary board, IX4351NE from IXYS Integrated Circuits Division. The controller also generates the two gating signals for the secondary bridges and sends the information via fiber optics to each of the secondary boards.

The primary gate drive board also receives information from the input and output sensors via daisy chained SPI sensors. The controller acts as the master and controls the ADCs on the sensor boards. The information from each ADC in the daisy chain is pumped through the chain until all ADC information has reached the controller. This method reduces the amount of wiring required to talk to multiple ADCs with one SPI module. The SPI communication is also implemented with fiber optics for the initial design.

The secondary gate drive board is designed to receive the gating signals from the primary controller board and actuate the gate signal. The gate driver IC used for the secondary was IXDN609SI from IXYS Integrated Circuits Division.

### **5.3 18 kW Hardware Prototype**

The 18 kW 3LADAB module was built and tested in house to validate the proposed design procedure and topology. The hardware implementation proves that the 3LADAB is a 3-port dc-dc converter capable of processing the time varying input voltages from the soft dc-link to produce a regulated, dc output port. The section will discuss the results taken with dc input voltages. The results for ac-dc operation are not given due to time constraints and will be left as future work.

The specifications for the design have already been given in Table 5.3. The complete schematic for the topology has also already been shown in Fig. 5.8 and pictures of the hardware in Fig. 5.9 and 5.10. The design of the 3LADAB module by following the procedure outlined in Section 5.2 is summarized in Table 5.6.

Table 5.6: Hardware parameters for the prototype 3LADAB design.

Hardware component	Design
Primary H-bridge MOSFETs	IMZ120R030M1HXKSA1, 1200 V, 30 m $\Omega$ (x2 paralleled)
Primary back-back MOSFETs	C3M0065100K, 1000 V, 65 m $\Omega$
Secondary MOSFETs	IRF250P225, 250 V, 18 m $\Omega$ (x2 paralleled)
Transformer turns ratio ( $n_t$ )	0.25
Transformer number of turns	16:4:4:4 (Primary:Paralleled Secondaries)
Resonant Inductance ( $L_s$ )	44 $\mu$ H
External Inductance ( $L_{s2,ext}$ )	10.5 $\mu$ H
Leakage Inductance ( $L_{s2,lkg}$ )	0.5 $\mu$ H
Resonant Capacitance ( $C_s$ )	116 nF
Primary Resonant Capacitance ( $C_{s1}$ )	229 nF
Secondary Resonant Capacitance ( $C_{s2}$ )	940 nF
Soft dc-link capacitors ( $C_{pon,\Delta}$ )	7.5 $\mu$ F, 1200 V (film)
Output capacitor ( $C_{out}$ )	320 $\mu$ F, 250 V (film)
Switching frequency ( $f_s$ )	100 kHz

### 5.3.1 DC-DC Testing

The 18 kW 3LADAB module was tested at three different input voltage operating points which cover the full operation of the line cycle in sector n. The operating points are similar to those that were tested with the 3LAFB topology defined in Fig. 3.12 and Table 3.4; however, those operating points were defined for sector p. In this section, the operating points are redefined for sector n in Table 5.7.

Table 5.7: Operating points for testing the 3-port dc-dc with dc inputs in sector p.

Parameter	(a)	(b)	(c)
Grid angle	0 $^\circ$	15 $^\circ$	29.5 $^\circ$
$v_{po}$	340 V	176 V	6 V
$v_{on}$	340 V	480 V	585 V
$K_{ref} = i_p/i_n$	1	0.73	0.53

The operation of the topology is symmetrical between sector n and sector p with the

only difference being which soft dc-link port has the greater voltage and the lesser port has duty cycle modulation to reduce the average input current. Thus validating the three operating points in sector  $n$  is sufficient for proving that the topology will work with ac input.

In order to emulate the battery load for initial testing, a bidirectional power supply is used to power the isolated secondary port of the 3LADAB. The load power supply is used in constant voltage mode with the regenerative current limit set higher than maximum output current of the 3LADAB module to avoid any interactions with the module's current regulation. Furthermore, because the topology is capable of bidirectional power flow, the input supplies which emulate the soft dc-link voltage at the dc operating points should also be bidirectional in case that the power flow is reversed.

The 3LADAB module is equipped with dc voltage and current sensors on each input port and the output port. The 3LADAB controller uses software protection which is programmed to shut down the switching in the case of over current or over voltage events any port.

The initial prototype was not designed to have any monitoring of the HF tank current which ideally should be monitored and used to shut down the switching in the case of over current. An alternative protection mechanism to monitoring the tank current is to check the input and output voltage ratio. The 3LADAB can build up large tank currents when the input and output voltages are significantly mismatched. The protection conditions check whether the total soft dc-link voltage is twice the reflected output voltage or vice-versa and if either condition is satisfied then the switching is immediately shut down.

$$v_{pn} = v_{po} + v_{on} > 2 \frac{v_{out}}{n_t} \quad (5.51a)$$

$$2v_{pn} = 2(v_{po} + v_{on}) < \frac{v_{out}}{n_t} \quad (5.51b)$$

For each input voltage operating point, the 3LADAB module was tested with the maximum and minimum output voltage specified in Table 5.3. The maximum output power of 18 kW is only achievable with the maximum output voltage and maximum output current.

The maximum output power for the minimum output voltage is 13.5 kW. Hardware waveforms of the 3LADAB module in operating point “a” with its maximum output current are shown in Fig. 5.11 (maximum output voltage) and Fig. 5.12 (minimum output voltage).

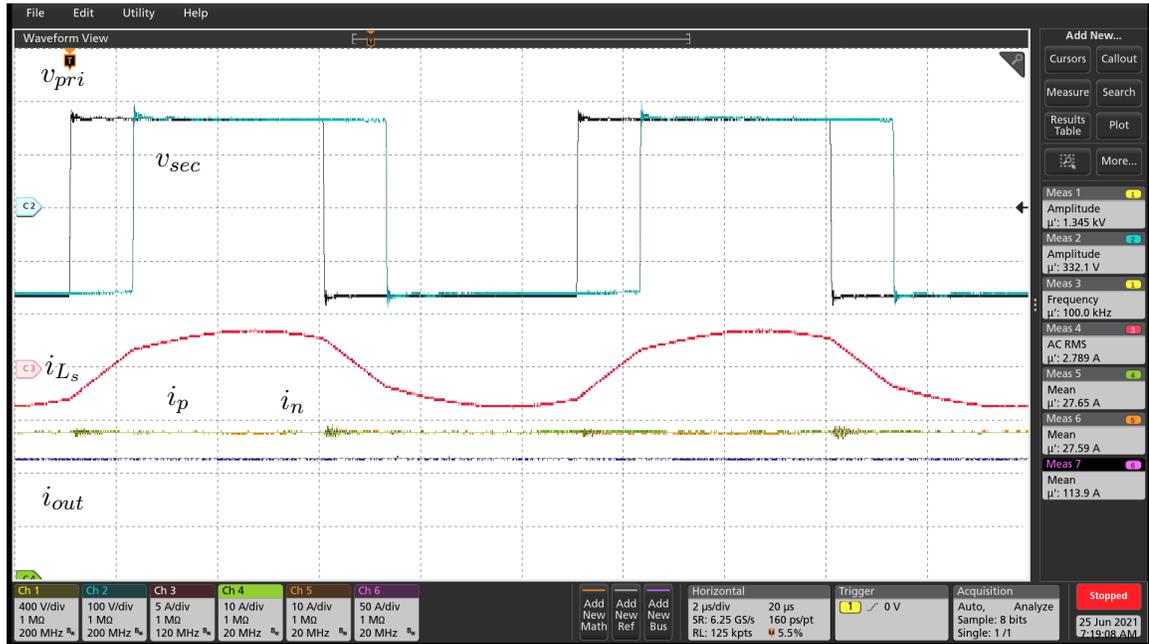


Fig. 5.11: Oscilloscope screen capture of the 18 kW 3LADAB module in operating point “a” during steady state with maximum output current and maximum output voltage.

The waveforms from operating point “a” resemble the typical waveforms seen in a DAB converter because the back-back switches are not being utilized due to the fact that equal input currents are required from each input port. Hardware waveforms of the 3LADAB module in operating point “b” with its maximum output current are shown in Fig. 5.13 (maximum output voltage) and Fig. 5.14 (minimum output voltage).

The waveforms from operating point “b” clearly shown the 3L waveform produced by the 3L primary bridge. The rising edge of the 3L waveform shows the slight stagger between the switching of the n-port switches and the p-port switches. This stagger is length of the applied dead-time to the n-port switches which is greater than necessary at the full load current. Having a look up table for the dead time based on load current and input voltage

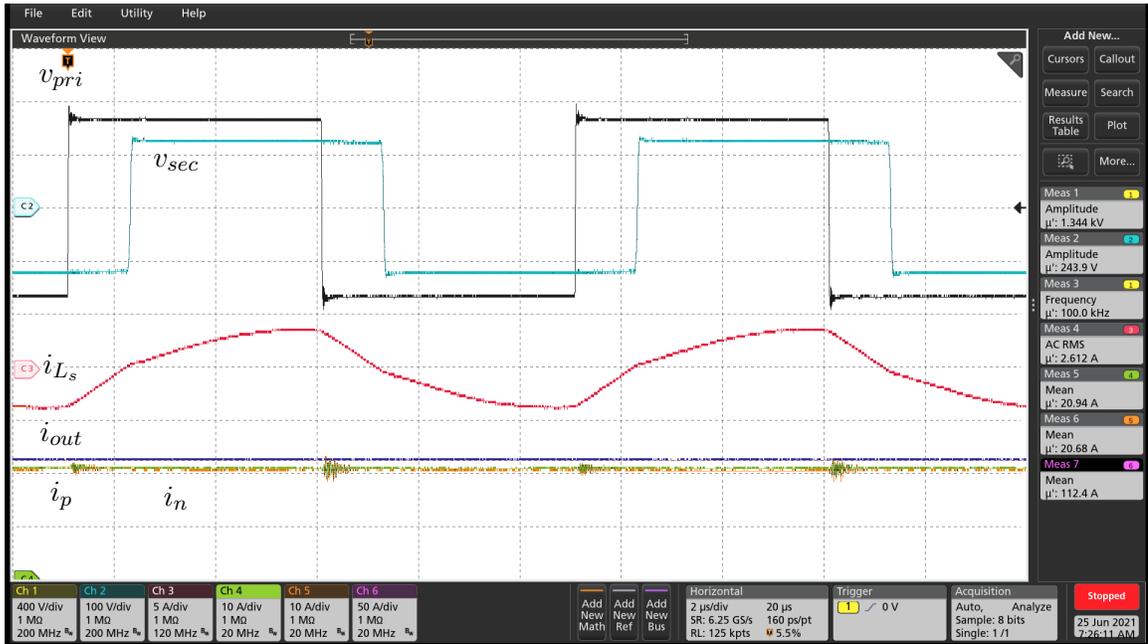


Fig. 5.12: Oscilloscope screen capture of the 18 kW 3LADAB module in operating point “a” during steady state with maximum output current and minimum output voltage.

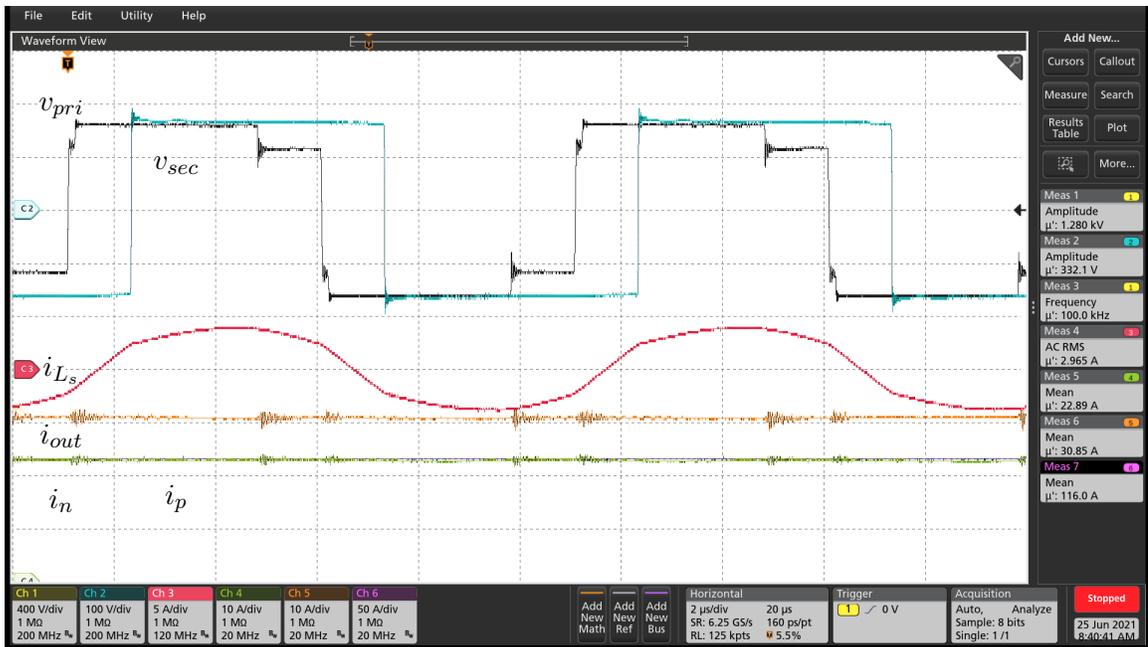


Fig. 5.13: Oscilloscope screen capture of the 18 kW 3LADAB module in operating point “b” during steady state with maximum output current and maximum output voltage.

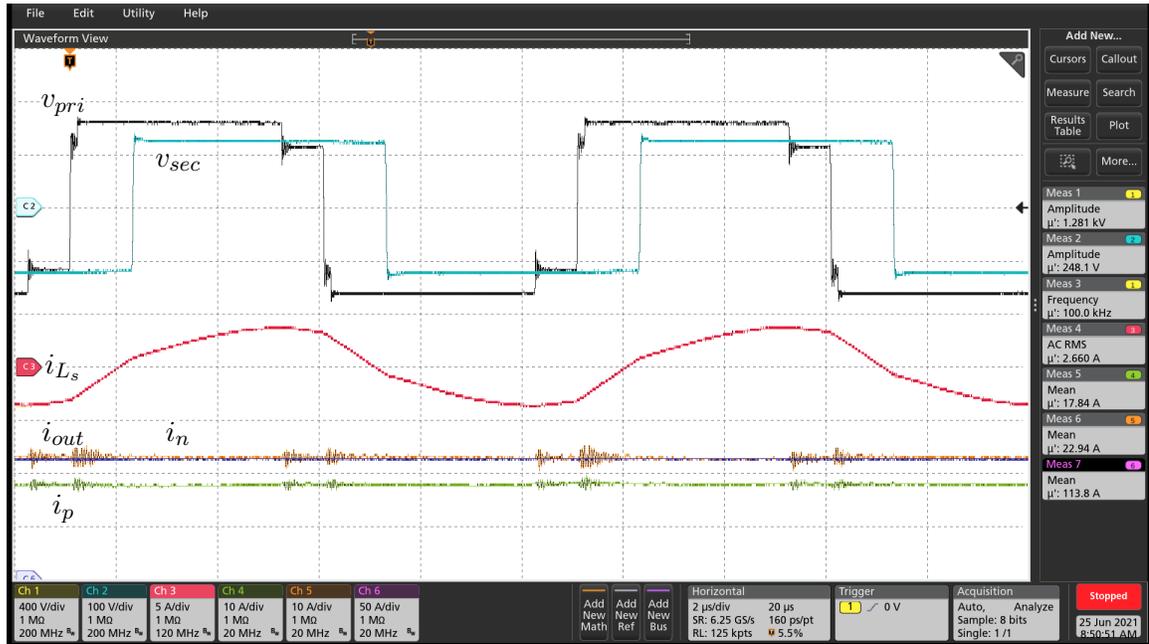


Fig. 5.14: Oscilloscope screen capture of the 18 kW 3LADAB module in operating point “b” during steady state with maximum output current and minimum output voltage.

can help to get a more optimal dead time and applied stagger. Hardware waveforms of the 3LADAB module in operating point “c” with its maximum output current are shown in Fig. 5.15 (maximum output voltage) and Fig. 5.16 (minimum output voltage).

The operation in “c” appears similar to operation in “a” with reduced input voltage; however, this is only due to the fact the one of the primary ports is near 0 V. This makes the 3L voltage waveform which drives the primary appear to be traditional 2-level waveform. The input current drawn by from the input ports are different because of the duty cycle applied to primary p-port.

The efficiency of the 3LADAB was characterized by the Yokogawa WT1806E power analyzer. The input power was measured directly by the power analyzer using two independent channels (one for each port) because the input current was below 50 A. The output power was measured using internal voltage measurement of the power analyzer, but the output current was measured using an external current sensor, LA 150-P from LEM USA Inc. The current sensor has an accuracy of  $\pm 0.5\%$  and the current sense resistors used to convert the

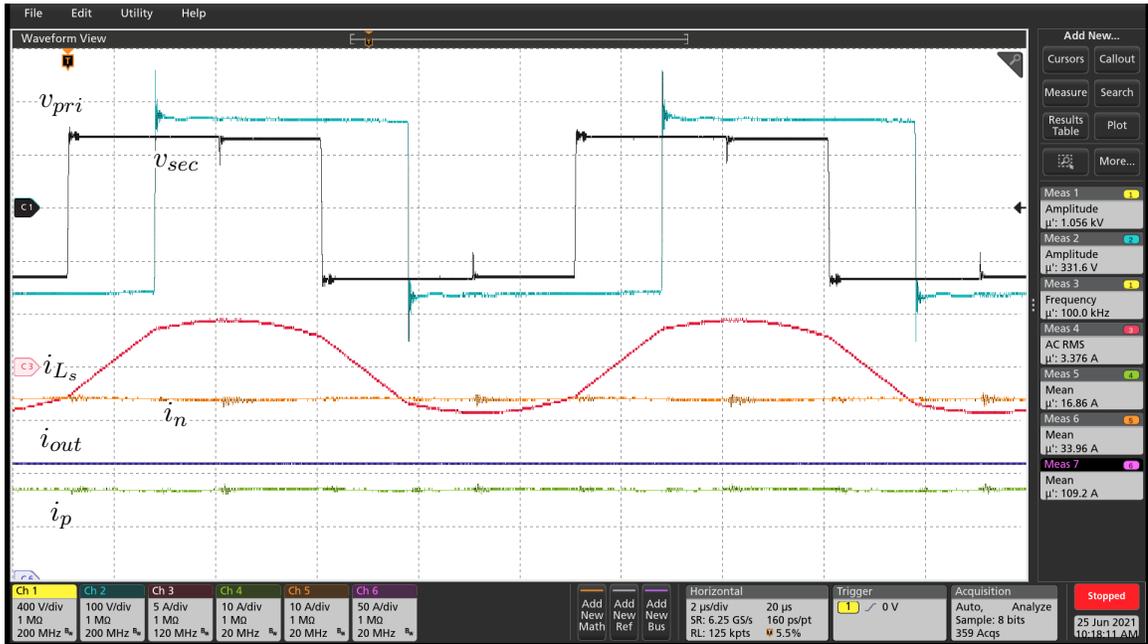


Fig. 5.15: Oscilloscope screen capture of the 18 kW 3LADAB module in operating point “c” during steady state with maximum output current and maximum output voltage.

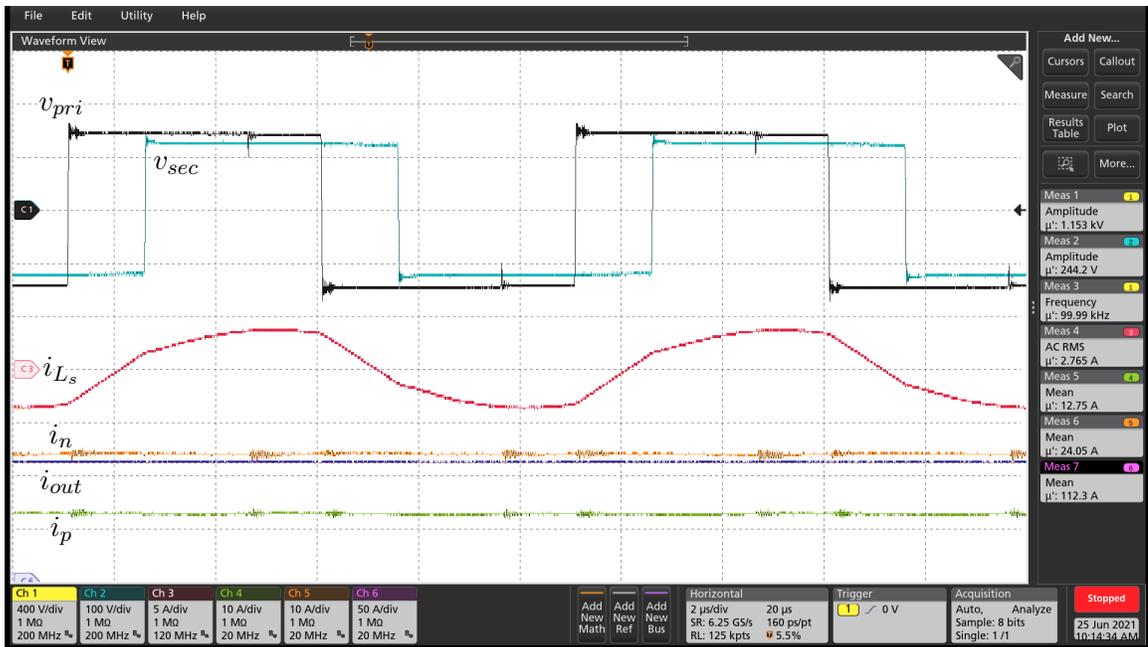


Fig. 5.16: Oscilloscope screen capture of the 18 kW 3LADAB module in operating point “c” during steady state with maximum output current and minimum output voltage.

current into a voltage signal was two  $30\ \Omega \pm 0.5\%$  resistors.

The efficiency of the 3LADAB prototype was recorded with power analyzer using a 3D sweep over input voltage, output voltage, and output current. The results are summarized by Fig. 5.17. The results for operating point “c” have the lowest efficiency due to the extra conduction losses in the back-back switches which are the only switching devices that are not being paralleled. The results for the 160 V output voltage for operating point “c” were not captured due to the system shutting down before the result could be taken due to failure of the gates for some of the switching devices on the primary bridge.

To validate the current sharing between all of the secondary transformer windings, each winding was probed using Tektronix TCP0030A AC/DC Current Probe 30A. Because the current in the secondary windings is greater than  $30\ A_{\text{RMS}}$ , current x10 transformers were designed to scale down the current into a valid range for the current probes. The currents were measured using an oscilloscope with the waveforms overlaid as shown in Fig. 5.18.

The overlaid currents can be seen as nearly identical which validates the current sharing between the secondary windings. The oscilloscope screen capture also captured the measurement of the RMS current in each winding which have a relative difference of only 3.0%.

#### 5.4 Summary

This chapter investigated the 3LADAB which has been selected as the topology building block for the XFC design from Chapter 4. This chapter introduced the 3LADAB topology by explaining the operation. A generic design procedure for presented along with an example design based off the specific specifications for an 18 kW module. Lastly, the example design was realized in hardware in order to validate the proposed topology and design procedure.

The operation of the 3LADAB was described by drawing parallels to other converters in literature such as the DAB and TAB as well as the 3LAFB discussed in Chapter 3. The unique implementation of the gating signals for the 3L primary bridge is described in detail as to why it differs from that of the 3LAFB described in Section 3.1.2. The converter was analyzed using the fundamental harmonic approximation to gain more insights to the

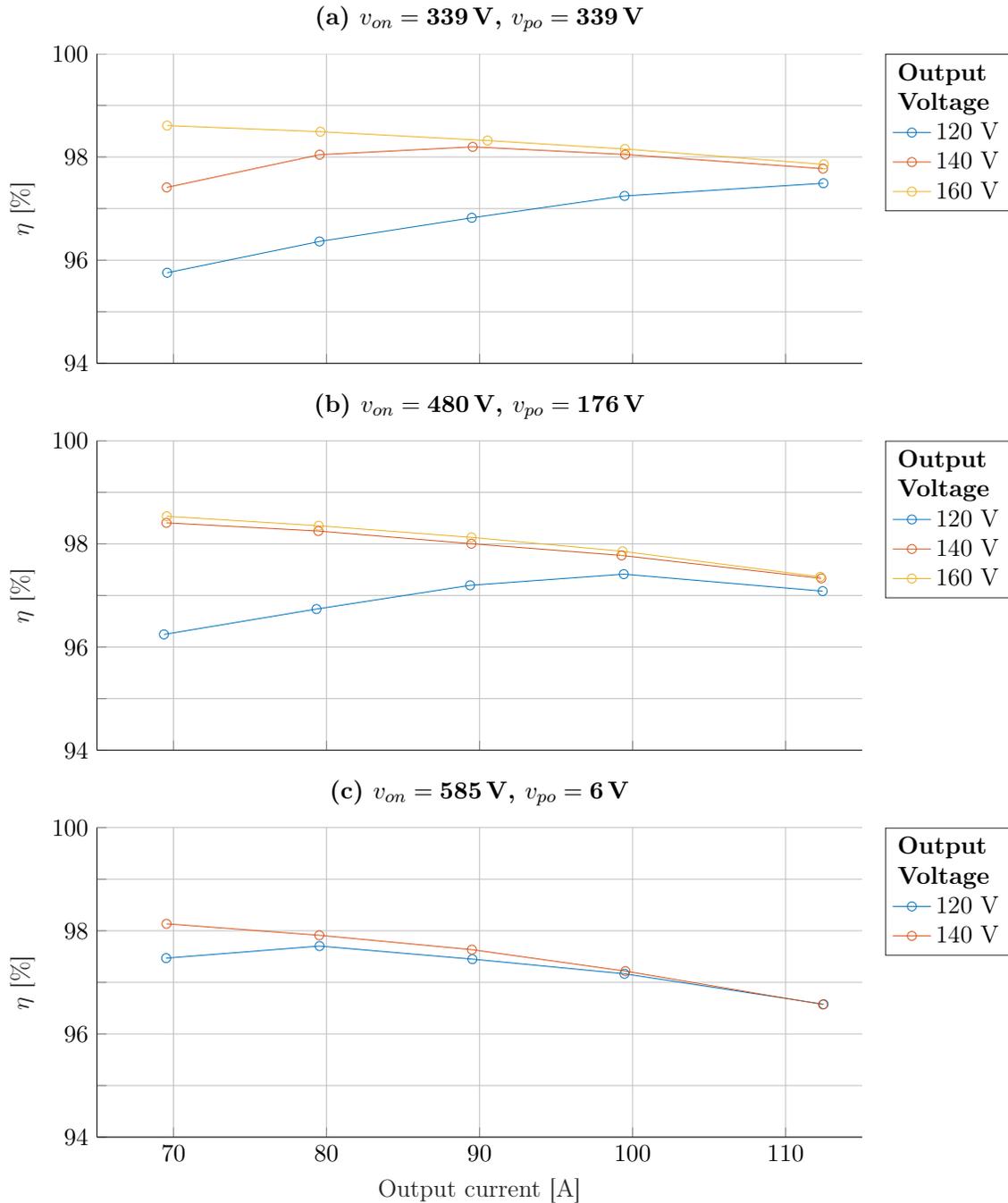


Fig. 5.17: Efficiency map of the 18 kW 3LADAB prototype module operating with different DC input voltages. The map sweeps over the output voltage and current range of the converter.

operation and design criteria. A simulation model for the 3LADAB was developed using MATLAB to simulate the idealized converter behavior.

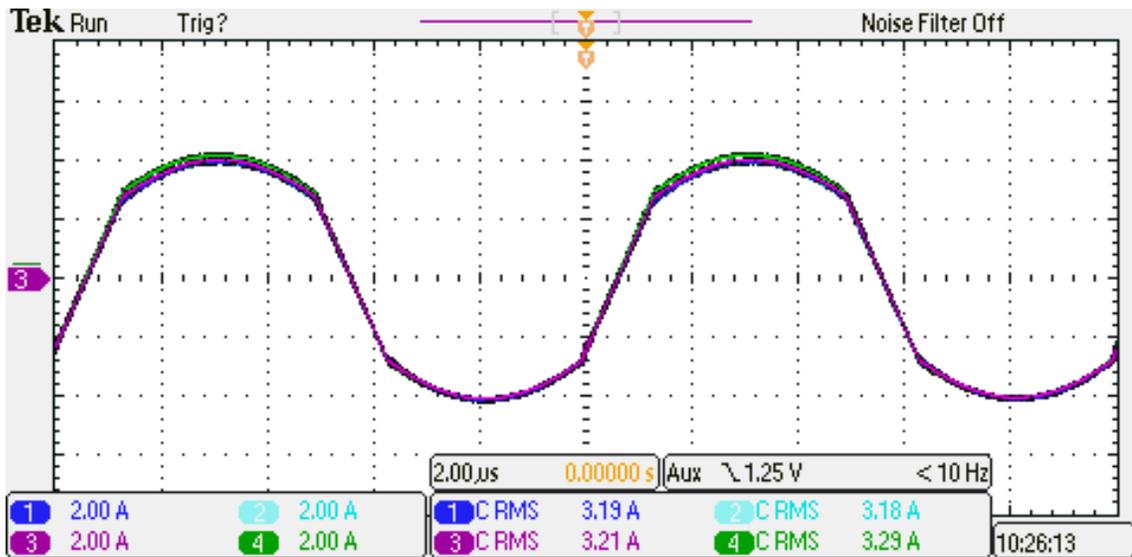


Fig. 5.18: Oscilloscope screen capture of the 18 kW 3LADAB module secondary transformer current in operating point “a” during steady state.

A generic design procedure for the 3LADAB topology was presented. The design procedure gives insight to how to select the transformer turns ratio, tank impedance, switching frequency, and input/output filters. A specific design for a 18 kW module is presented as an example with extra details on the component selection, PCB, and gate driver design.

One 18 kW 3LADAB module was built based off the presented design procedure. The prototype was experimentally tested as a dc-dc converter. The operating conditions were varied to test different input and output voltages which would occur in normal operation with ac input and battery load. The experimental results show that the converter achieves good efficiency at the full load operation even with variation in the output voltage.

## CHAPTER 6

### CONCLUSION AND FUTURE WORK

The extreme growth of EV has increased the demand for battery charging infrastructure. The electrification of heavy duty vehicles is driving the demand for higher power chargers in order to reduce charging times.

The topics investigated in this thesis directly contribute to the development of more power dense, higher efficiency, battery charger designs using a quasi-single stage approach. The Unfolder eliminates the need for an AFE rectifier and instead pushes the PFC action to the 3-port dc-dc converter. The isolated, 3-port, dc-dc topologies under investigation in this thesis are ideal candidates for Unfolding based rectification.

#### **6.1 Summary of Contributions**

The work presented in this thesis has many contributions to the design and analysis of 3-port dc-dc topologies intended for Unfolding based rectification. Improvements to the modulation of the 3LAFB and 3LADAB have been proposed and tested in hardware. Detailed modeling of the 3LAFB topology has been presented to develop a controller design for the ac-dc system. A modular structure for creating an XFC from lower power 3LADAB modules has been proposed. The design procedure of a 3LADAB module has been outlined and a prototype has been built to validate the results.

Specifically, the modulation of the primary 3L bridge for the 3LAFB and 3LADAB is of particular importance due to fact the primary devices would not properly soft switch without staggering the gating signals of the 3L p and n port switches. Furthermore, the crossover between p and n sectors in the modulation of the 3LAFB is needed in order to reduce conduction loss from free-wheeling in the back-back devices.

The switch network averaging of the 3LAFB topology is critical to analyzing the small signal behavior of the converter. The analysis can be used to design more complicated con-

trollers multiple-input multiple-output controllers instead of using the proposed decoupling control approach. Furthermore, the implementation of the ac-dc control on the 2 kW hardware proved the topology as a 3-port dc-dc capable of processing the soft dc-link voltage into a dc output.

The proposed modular XFC structure highlights how multiple 3-port dc-dc converters can be arranged to produce an XFC. The analysis presented shows how using isolated modules connected in series and parallel at the output reduces the voltage and current variation required by each module, thus making the design of each module easier. This is especially true for the 3LADAB converter which struggles to maintain high efficiency over a wide variation in output voltage.

The design procedure for a 3LADAB module is presented on how to selected the transformer turns ratio, tank impedance, switching frequency, and input/output filters. A specific design for a 18 kW module is presented as an example with extra details on the component selection, PCB, and gate driver design. The proposed design was built and the prototype was tested as a dc-dc converter. The experimental results show that the converter achieves good efficiency which validates the topology and design procedure.

## 6.2 Future Work

There is plenty of room to expand upon the work presented in this thesis. The ringing challenges presented by the 3LAFB need to be mitigated to use the topology to its full capability. The multi-module control structure of the XFC needs to be explored to share the voltage and current equally amongst the modules. The control strategy for the ac-dc operation of the 3LADAB can be improved. The cyber-physical security of the XFC system can be further explored and improved from the work presented in Appendix [A.2](#).

The 3LAFB topology was proven to be a good candidate for the 3-port dc-dc required by the Unfolding based rectification; however, the challenges presented by the secondary voltage ringing need to be overcome in order to have an output voltage with no ripple over the entire line cycle of the ac grid. This challenge was not addressed because the topology selected for the XFC building block was the 3LADAB.

The proposed structure for the XFC uses many 3LADAB modules which operate in parallel on the input and are connected in series and parallel on the output. In order to have a seamless transition in the output voltage and current, the 3LADAB modules will need to be synchronously powered up and down as the output voltage rises and the output current falls. Such control of the modules has not been implemented yet and is left to the future work.

The operation of a single 3LADAB has been proven with dc input and output voltage; however, the control of the 3LADAB module with ac inputs has not been demonstrated up to this point. The control of the 3LADAB modules with ac input from a 3-phase Unfolder is left to future work.

## REFERENCES

- [1] “Global EV Outlook 2020,” 2020.
- [2] M. Cloud, “What is the energy density of a lithium-ion battery?” 2020. [Online]. Available: <https://www.fluxpower.com/blog/what-is-the-energy-density-of-a-lithium-ion-battery>
- [3] X. G. Yang, G. Zhang, S. Ge, and C. Y. Wang, “Fast charging of lithium-ion batteries at all temperatures,” *Proceedings of the National Academy of Sciences of the United States of America*, vol. 115, no. 28, pp. 7266–7271, jul 2018. [Online]. Available: [www.pnas.org/cgi/doi/10.1073/pnas.1807115115](http://www.pnas.org/cgi/doi/10.1073/pnas.1807115115)
- [4] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Cham: Springer International Publishing, 2020. [Online]. Available: <http://link.springer.com/10.1007/978-3-030-43881-4>
- [5] D. Yelaverthi, “Three-Phase Unfolding Based Soft DC-Link Converter Topologies for AC to DC Applications,” *All Graduate Theses and Dissertations*, may 2021. [Online]. Available: <https://digitalcommons.usu.edu/etd/8015>
- [6] J. W. Kolar and T. Friedli, “The essence of three-phase PFC rectifier systems part i,” *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, 2013.
- [7] T. Friedli, M. Hartmann, and J. W. Kolar, “The essence of three-phase PFC rectifier systems-part II,” *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 543–560, 2014.
- [8] M. Yilmaz and P. T. Krein, “Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles,” pp. 2151–2169, 2013.
- [9] L. Schrittwieser, M. Leibl, and J. W. Kolar, “99three-phase matrix-type DAB buck-boost PFC rectifier,” *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 138–157, jan 2020.
- [10] P. Cortes, D. Bortis, R. Pittini, and J. W. Kolar, “Comparative evaluation of three-phase isolated matrix-type PFC rectifier concepts for high efficiency 380VDC supplies of future telco and data centers,” in *2014 16th European Conference on Power Electronics and Applications, EPE-ECCE Europe 2014*. Institute of Electrical and Electronics Engineers Inc., sep 2014.
- [11] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, “Novel SWISS Rectifier Modulation Scheme Preventing Input Current Distortions at Sector Boundaries,” *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5771–5785, jul 2017.
- [12] SAE, “SAE Electric Vehicle and Plug in Hybrid Electric Vehicle Conductive Charge Coupler Standard J1772-201210,” pp. 1–110, 2012.

- [13] I. Transportation and V. Technology, "IEEE Standard Technical Specifications of a DC Quick Charger for Use with Electric Vehicles IEEE Vehicular Technology Society IEEE Standard Technical Specifications of a DC Quick Charger for Use with Electric Vehicles," pp. 1–97, 2015.
- [14] W. W. Chen, R. Zane, and L. Corradini, "Isolated Bidirectional Grid-Tied Three-Phase AC-DC Power Conversion Using Series-Resonant Converter Modules and a Three-Phase Unfolder," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9001–9012, dec 2017.
- [15] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Swiss rectifier - A novel three-phase buck-type PFC topology for Electric Vehicle battery charging," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2012, pp. 2617–2624.
- [16] L. Schrittwieser, M. Leibl, M. Haider, F. Thony, J. W. Kolar, and T. B. Soeiro, "99.3 Distribution Systems," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 126–140, 2018.
- [17] M. Silva, N. Hensgens, J. Oliver, P. Alou, Ó. García, and J. A. Cobos, "Isolated Swiss-Forward three-phase rectifier for aircraft applications," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*. Institute of Electrical and Electronics Engineers Inc., 2014, pp. 951–958.
- [18] X. Wang, B. Zhang, S. Xie, and K. Xu, "A Soft Switching Swiss Rectifier Based on Phase-Shifted Full-Bridge Topology," in *Proceedings - 2018 IEEE International Power Electronics and Application Conference and Exposition, PEAC 2018*. Institute of Electrical and Electronics Engineers Inc., dec 2018.
- [19] D. B. Yelaverthi, M. Mansour, H. Wang, and R. Zane, "Triple Active Bridge Series Resonant Converter for three-Phase Unfolding Based Isolated Converters," in *IECON Proceedings (Industrial Electronics Conference)*, vol. 2019-Octob. IEEE Computer Society, oct 2019, pp. 4924–4930.
- [20] D. B. Yelaverthi, R. Hatch, M. Mansour, H. Wang, and R. Zane, "3-Level asymmetric full-bridge soft-switched PWM converter for 3-phase unfolding based battery charger topology," in *2019 IEEE Energy Conversion Congress and Exposition, ECCE 2019*. Institute of Electrical and Electronics Engineers Inc., sep 2019, pp. 2737–2743.
- [21] S. Y. Lin and C. L. Chen, "Analysis and design for RCD clamped snubber used in output rectifier of phase-shift full-bridge ZVS converters," *IEEE Transactions on Industrial Electronics*, vol. 45, no. 2, pp. 358–359, 1998.
- [22] R. Redl, N. O. Sokal, and L. Balogh, "A Novel Soft-Switching Full-Bridge DC/DC Converter: Analysis, Design Considerations, and Experimental Results at 1.5 kW, 100 kHz," *IEEE Transactions on Power Electronics*, vol. 6, no. 3, pp. 408–418, 1991.
- [23] M. Ilic and D. Maksimovic, "Phase-shifted full bridge DC-DC converter with energy recovery clamp and reduced circulating current," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 969–975, 2007.

- [24] ABB, “Terra HP GEN 3 - Infographic.” [Online]. Available: <https://search.abb.com/library/Download.aspx?DocumentID=9AKK107991A8620&LanguageCode=en&DocumentPartId=&Action=Launch>
- [25] L. Corradini, D. Seltzer, D. Bloomquist, R. Zane, D. Maksimović, and B. Jacobson, “Minimum current operation of bidirectional dual-bridge series resonant DC/DC converters,” *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3266–3276, 2012.
- [26] C. T. Rim and G. H. Cho, “Phasor Transformation and its Application to the DC/AC Analyses of Frequency Phase-Controlled Series Resonant Converters (SRC),” *IEEE Transactions on Power Electronics*, vol. 5, no. 2, pp. 201–211, 1990.
- [27] E. C. Snelling, *Soft Ferrites*, 1st ed. London: Arrowsmith, J. W., 1969.

APPENDICES

## APPENDIX A

### Publications

#### **A.1 3-Level Asymmetric Full-Bridge Soft-Switched PWM Converter for 3-Phase Unfolding Based Battery Charger Topology**

# 3-Level Asymmetric Full-Bridge Soft-Switched PWM Converter for 3-Phase Unfolding Based Battery Charger Topology

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**Abstract**—In this paper, the authors propose a new topology referred to as 3-Level Asymmetric Full Bridge (3LAFB) for back-end isolated DC-DC stage required in three-phase rectifiers based on unfolding approach. The three-phase unfolding based approach improves the power density and efficiency of the converter for isolated battery charging applications. The DC-DC stage used in this approach is usually implemented by two separate converters for processing different time-varying power from each of the two soft DC links. The authors propose a single 3-level DC-DC converter that can simultaneously process power from both the soft-dc links. This results in further reduction in size of the converters based on unfolding approach. Modulation strategy is also proposed for this 3LAFB topology such that the conduction duration of the 4-quadrant switches are minimized and all the active devices soft-switch. With the proposed modulation, converter has the ability to process different powers from each of the DC links that are required to maintain power factor correction (PFC) action on the grid side. Ideal converter simulation waveforms are used to explain the operation of the converter. Hardware results from a 2 kW prototype are presented at three different operating conditions that cover the full voltage range at the input. The results provided validate the proposed converter ability to meet the requirements of the DC-DC stage in an unfolding rectifier.

**Index Terms**—Battery charger, DC fast charger, three-phase rectifier, Unfolding, isolated DC/DC, three-level full bridge, high power density, soft switching, ZVS, wide voltage range

## I. INTRODUCTION

For high power battery charging applications such as DC fast charging for electric vehicles (EVs), three-phase rectifiers are used. Additionally, galvanic isolation is preferred or required to meet the safety requirements of the standards [1], [2] for EV charging when connecting to the utility grid [3], [4]. Reinforced or double insulation is required to meet IEEE EV fast charger standard [2]. Galvanic isolation within the converter will eliminate the need for a separate isolation transformer on the utility side.

State-of-the-art (SOA) solutions for high power battery charging systems are typically implemented as two-stage systems, comprising of a Power Factor Correction (PFC) rectifier input stage followed by an isolated DC-DC converter [4]–[6]. This approach allows the use of a simple and well-understood AC/DC Active Front End (AFE) rectifier and standard 2-level

isolated H-bridge topologies in the DC-DC stage. A 2-level Voltage Source Converter (VSC) is commonly used as AFE. The VSC is Pulse-Width Modulated (PWM) to shape the line currents sinusoidal and maintain a stiff intermediate DC link. An input LCL grid filter is typically employed to attenuate the harmonics to be compliant to the harmonic injection standards. The cascade DC-DC stage has a high-frequency transformer to provide galvanic isolation. LLC resonant converter and phase-shifted full-bridge converter are two of the most popular topologies used in this stage [5]–[7].

The two-stage approach gives tight, highly dynamic control over the output voltage to disturbances on grid side voltages. Simplifies control due to the decoupling provided by the intermediate stiff DC link. EV charging applications do not require high dynamic performance since battery charging applications are slow dynamic constant current (C.C) or constant voltage (C.V.) loads. There is no need for a stiff intermediate DC-link voltage for battery charger application. Since both the converter stages are switching at high frequency, switching loss occur and filters are required in the two stages. And usually, the AFE is a hard-switched topology that limits the operating frequency and hence power density. The state-of-the-art commercial 50 kW chargers have an efficiency of around 94% at nominal load [8].

Compared to stiff DC-link, soft DC-link based two-stage rectifier topologies improve the achievable efficiency and power density [9]–[14]. Three-phase unfolding based rectification is one such method that completely eliminates the switching loss in the front-end rectification stage and also minimizes the filtering requirement on the utility side [14], [15]. Unfolding based converters are ideal for battery charging applications because they meet all the application requirements while greatly improving efficiency and power density. Multiple three-phase converter topologies are reported in literature that can be classified under this rectification approach [14]–[16]. The topology in [14] used neutral point clamp 3-level legs for unfolding and two separate isolated DC-DC converters, one for each of the two soft DC-links. Another topology called the Swiss Rectifier [15] also uses the intermediate soft dc-link unfolding approach. There have been attempts to derive

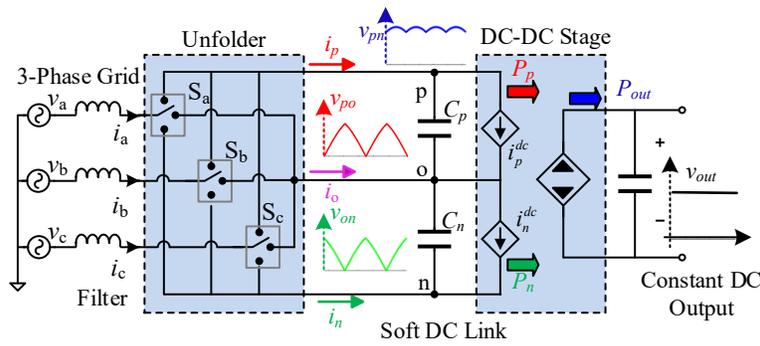


Fig. 1: Functional block diagram of 3-phase unfolded soft DC-link based rectifier topology

isolated versions of the Swiss Rectifier [17], [18] by replacing the buck converters with isolated DC-DC topologies. In all the above topologies, the basic idea is to use two DC-DC converter feeding power to a common DC output. Each of the two DC-DC converters has to be designed for a peak power equal to rated power of the rectifier. More details of the requirements for the DC-DC stage are discussed in section II, where, a generalized description of the unfolding rectification is given. To further improve the power density and efficiency of unfolding based topology, the authors propose using a single three-level full-bridge dc-dc converter that requires only one high-frequency transformer.

The paper focuses on validating the use of the proposed three-level full-bridge converter to achieve the functionalities that are required in the DC-DC stage of an unfolding based three-phase rectifier. The uniqueness is in using 3-level legs to differentially process power from both the DC-link capacitors simultaneously while only using a single isolation transformer to process the full power. Operating principle and modulation technique for zero-volt switching are explained. Ideal steady-state simulation results are provided. A 2 kW, 500 V output, hardware prototype that can connect to 480 V line to line RMS three-phase Unfolder is designed and built. Hardware results at three different input voltage operating points are included. The converter design optimization and closed-loop control required for synchronization with a 3-phase source will be dealt with in future publications.

## II. THREE-PHASE UNFOLDING APPROACH

In order to understand the requirements of the DC-DC stage, a generalized description of the 3-ph unfolding based converter is explained in this section. The functional block diagram for the unfolding based rectification approach is given in Fig.1. The AC to DC stage, referred here as Unfolder, only rectifies the line voltages. Neither the DC link is controlled nor the line currents are shaped by the AC to DC converter. Hence, this converter stage does not require to be pulse-width modulated (PWM). The intermediate DC link is soft, time-varying and unregulated. The line current shaping task is performed by the subsequent high frequency (HF) DC-DC stage. The same DC-DC stage also regulates the output bus voltage. The HF transformers in the DC-DC modules provide isolation and voltage transformation. Both the tasks of power

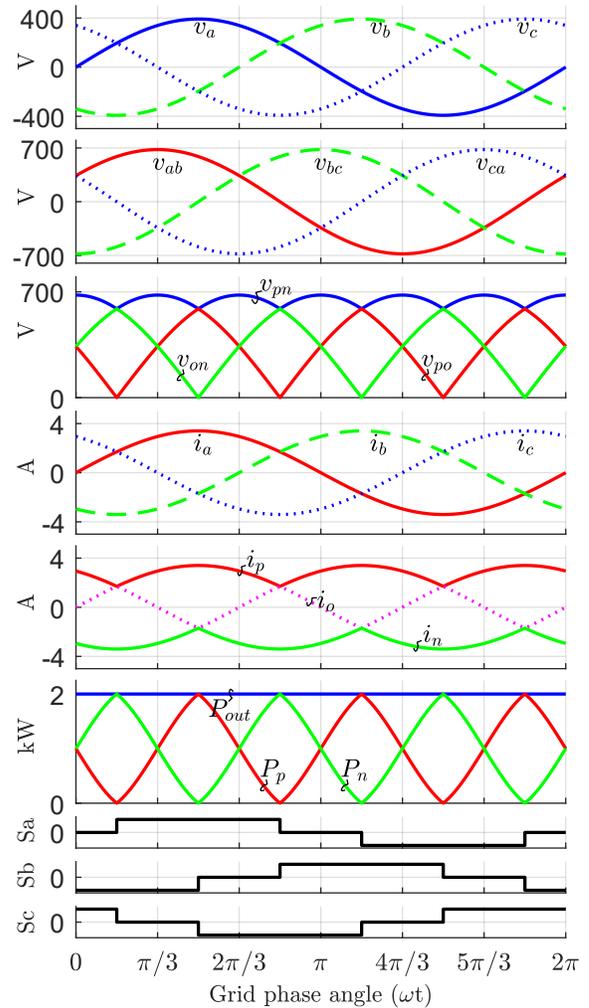


Fig. 2: Ideal waveforms for 480 V, 2 kW, 3-phase unfolded soft DC-link based converters

factor correction (PFC) and output bus voltage regulation that require high-frequency switching are performed only in the DC-DC converter stage.

Each phase of the Unfolder can be functionally represented by a single-pole triple-throw switch (SPTT). As shown in Fig. 1, the SPTT switches  $S_a$ ,  $S_b$ ,  $S_c$  can be connected to either 'p', 'o' or 'n' terminals of the soft DC-link. The switching

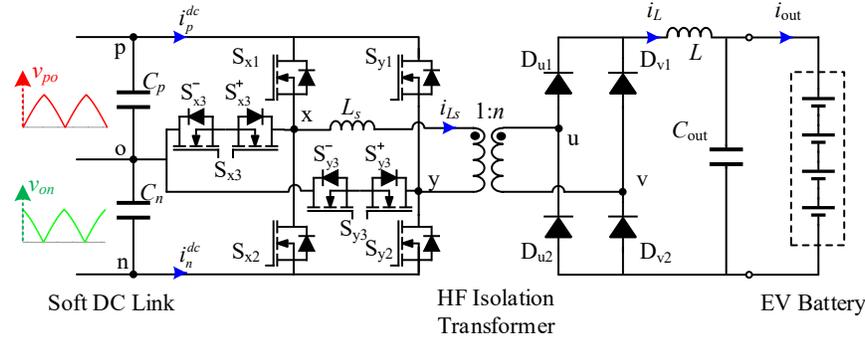


Fig. 3: Proposed 3-level Asymmetric Full-Bridge (3LAFB) converter for the dc-dc stage

states p(1), o(0) or n(-1) (see Fig. 2) for these devices are such that the instantaneous highest phase voltage connects to ‘p’ terminal and instantaneous lowest phase voltage connects to ‘n’ terminal, and the remaining phase gets connected to the midpoint rail ‘o’. The resulting soft DC link voltages  $v_{po}$  and  $v_{on}$  are piece-wise sinusoidal as shown in Fig. 2. The devices in the Unfolder switch at twice line frequency and switching takes place at zero volts across the devices. This essentially means that there are practically negligible switching loss in the Unfolder devices, only conduction loss occur in this stage. These voltage magnitudes are time-varying between 0 to  $(\sqrt{3}/2)v_m$ . Here,  $v_m$  is the line to line voltage magnitude of the utility grid. The currents drawn from the soft DC-links  $i_p^{dc}$  and  $i_n^{dc}$  by the DC-DC stage have to be controlled such that sinusoidal currents in phase with the voltage are drawn on the grid side. There is no bulk capacitance in the DC-link, capacitor  $C_p$  and  $C_n$  are designed to just filter out the switching ripple produced by the DC-DC stage. Hence, to achieve unity power factor (UPF) action, the switching average of the currents  $i_p^{dc}$  and  $i_n^{dc}$  drawn by the DC-DC stage should follow the  $i_p$  and  $-i_n$ . To represent this requirement, the input ports of the DC-DC stage are represented by controlled current sources and the output port as dependent power source. The instantaneous powers  $P_p$ ,  $P_n$  that should be drawn from each soft DC-link is time varying, between 0 to  $P_{out}$ . If the DC-DC stage is realized using one converter per DC-link then each of these converters has to be peak power rated to  $P_{out}$ , resulting in a peak power rating for DC-DC stage to be twice the average output power. The authors propose the use of a single three-port converter for the DC-DC stage to increase the utilization and thereby improve the efficiency and overall power density.

### III. TOPOLOGY DESCRIPTION AND MODULATION SCHEME

#### A. Topology Description

Phase-shifted full bridge (PSFB) is the most widely used dc-dc converter for medium to high power isolated converter. This converter maintains good efficiency over wide voltage range and hence is preferred for battery charging applications [19]. A 3-level (3-L) variant of the PSFB, shown in Fig. 3, is proposed as the back-end DC-DC stage. Compared to a typical 3-L

TABLE I: 3-level leg switching states and bridge voltages

Leg-x state	Leg-y state	Pole-x voltage	Pole-y voltage	Bridge voltage ( $v_{xy}$ )
$x_1$	$y_1$	$v_{pn}$	$v_{pn}$	0
$x_1$	$y_2$	$v_{pn}$	0	$v_{pn}$
$x_1$	$y_3$	$v_{pn}$	$v_{on}$	$v_{po}$
$x_2$	$y_1$	0	$v_{pn}$	$-v_{pn}$
$x_2$	$y_2$	0	0	0
$x_2$	$y_3$	0	$v_{on}$	$-v_{on}$
$x_3$	$y_1$	$v_{on}$	$v_{pn}$	$-v_{po}$
$x_3$	$y_2$	$v_{on}$	0	$v_{on}$
$x_3$	$y_3$	$v_{on}$	$v_{on}$	0

bridge, the main difference is that the two halves of the DC-link voltages are unequal, hence the name 3-L Asymmetric Full-Bridge (3LAFB). For switching strategy, a complex duty-cycle modulation is used rather than the typical phase-shift between the legs.

The proposed 3LAFB topology essentially acts as a three-port converter with two series connected input ports and a output port. The 3-L legs simultaneously process power from both the soft dc-links and generate a high frequency (HF) 3-L voltage waveform  $v_{xy}$ . The relative pulse duration of each of the voltage levels,  $d_p$  and  $d_n$  [see Fig. 4], are controlled such that the grid side currents are shaped sinusoidal. The absolute values of  $d_p$  and  $d_n$  are used to regulate the output current or voltage. Neglecting the duty cycle loss due to  $L_s$ , the average input currents and average output voltage can be given by the ideal equations below:

$$\langle i_p^{dc} \rangle_{T_s} = n d_p \langle i_L \rangle_{T_s}, \quad (1)$$

$$\langle i_n^{dc} \rangle_{T_s} = n d_n \langle i_L \rangle_{T_s}, \quad (2)$$

$$\langle v_{out} \rangle_{T_s} = n [d_p \langle v_{po} \rangle_{T_s} + d_n \langle v_{on} \rangle_{T_s}]. \quad (3)$$

Here,  $\langle \rangle_{T_s}$  represents the average of a variable over a switching period,  $T_s$ .

#### B. Modulation

The three-level legs in the bridge can be used to connect the bridge output poles to either positive (p), mid-point(o), or negative (n) bus of the DC-link. For conventional 3-L H-bridge with equal DC link voltages ( $v_{po} = v_{on}$ ), only 5 unique output states are present with 2 redundant states possible for the half

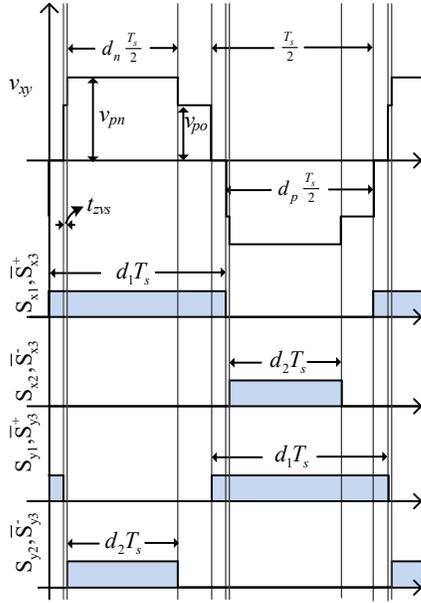


Fig. 4: 3-level bridge output voltage with proposed gating sequence

voltages and 3 redundant states possible for zero voltage states. But with unequal dc link voltages at bus 'p' and bus 'n', a total of 7 unique states are possible for the bridge voltage. The bridge voltage for all the possible states of legs 'x' and 'y' are given in Table I. Zero-voltage is the only redundant state with 3 possible realizations  $[x_1, y_1]$ ,  $[x_2, y_2]$ , and  $[x_3, y_3]$ .

The modulation strategy is an important aspect to keep the efficiency high. Modulation scheme for minimizing 4-quadrant (4-Q) switch conduction and to ZVS all the 8 switches in the 3-level legs is proposed. Below are the criteria for selecting the switching scheme:

- 1) The conduction duration of the 4-quadrant (4-Q) switches  $S_{x3}, S_{y3}$  should be minimized. Since, each device has conduction loss due to two MOSFETs. Only the zero-states  $[x_1, y_1]$  and  $[x_2, y_2]$ , are to be used.
- 2) Switching sequence is chosen such that  $i_{L_s}$  is in the right direction for ZVS of the devices. The commutation sequence of incoming and outgoing devices should favor zero-voltage soft-switching.

TABLE II: Control parameters based on the input operating point

	Sector-1	Sector-2
Operating condition	$d_p < d_n$	$d_p > d_n$
Top device duty, $d_1$	$\frac{d_p}{2}$	$\frac{2-d_p}{2}$
Bottom device duty, $d_2$	$\frac{2-d_n}{2}$	$\frac{d_n}{2}$
Zero-state	$[x_2, y_2]$	$[x_1, y_1]$

With the above two mentioned criteria, the switching scheme for the 3-level legs are chosen based on the Table. II and a sequence is shown in Fig. 4. Same set of input operating conditions repeat after  $60^\circ$  grid phase angle and the operating

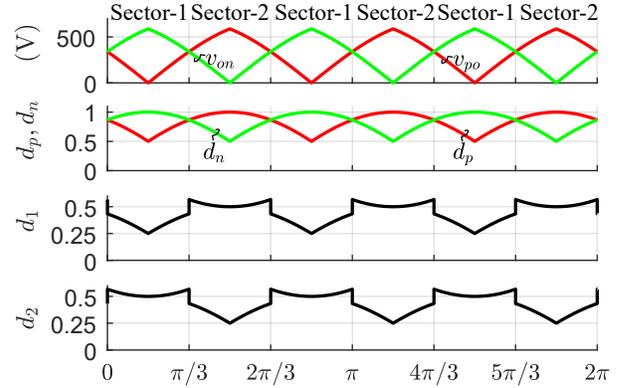


Fig. 5: Typical variation of pulse durations  $d_p$  and  $d_n$  for 3-L voltage waveform, the derived duty cycles  $d_1$  and  $d_2$  of devices  $S_{x1-3}$  and  $S_{y1-3}$  over one line cycle.

conditions can be divided into two sectors, Sector-1 and Sector-2. The timing diagram given in the Fig. 4 is for Sector-2 where,  $v_p > v_n$ . In these sectors,  $v_{po}$  is used for longer duration than  $v_{on}$  in the 3L voltage waveform so that  $\langle i_p^{dc} \rangle$  is greater than  $\langle i_n^{dc} \rangle$ . Hence, top devices are turned on for longer than bottom devices. The same top devices are also used to generate the zero-voltage states in these sectors, that is,  $[x_1, y_1]$  is for zero-voltage state. The duty cycle  $d_1$  of the top devices is greater than 0.5 in Sector-2. The roles of top switches and bottom switches are interchanged in the other sector. Bottom devices are used to generate the zero-voltage state in Sector-1. This creates a discontinuity in the modulation at the sector boundaries. At the intersection of the two sectors when  $v_p = v_n$ , the zero-voltage state from the previous sector can be used.

To ensure ZVS for all the devices, the zero-voltage state is distributed asymmetrically over the switching half cycle. The duration of the zero-state,  $t_{zvs}$  on the rising edge of the voltage has to be minimized to increase ZVS probability. A  $t_{zvs}$  equal to the dead-time used for the complementary devices is recommend. This small zero state on the rising edge is kept to ensure that only one pair of devices commutate at a given time and ZVS of the 4-Q switches are achieved even when the DC-link voltages  $v_p, v_n$  are unequal. Typical variation of pulse duration  $d_p$  and  $d_n$  of the 3-L  $v_{xy}$  and the derived duty cycles  $d_1$  and  $d_2$  over a line cycle are shown in Fig. 5.

The proposed modulation minimizes the conduction of 4-Q switches by avoiding the use of the zero-voltage state  $[x_3, y_3]$ . The switching instants are sequenced such that all the devices soft-switch over the entire input voltage range of 60 Hz line cycle. As with conventional PSFB, for complete ZVS of the devices there should be enough energy in the series inductor ( $L_s$ ) to discharge the device output capacitance. One additional advantage of the proposed duty-cycle modulation is that both the legs have similar switching and conduction losses, unlike in a phase-shifted bridge where the lagging legs might experience higher switching loss compared to leading

TABLE III: Prototype specifications and design parameters

Parameter	Description
Nominal Input	480 V <sub>AC</sub> 3-ph RMS unfolded voltage
Maximum output power	2000 W
Output voltage range	200-500 V <sub>DC</sub>
Max. output current	4 A <sub>DC</sub>
Switching Frequency	100 kHz
Switching Devices	C3M0120100J, 1000 V, 120 mΩ
Input capacitors, $C_p, C_n$	1.5 μF 1100 V film capacitor
Series inductor, $L_s$	44.8 μH (includes 11.1 μH transformer and PCB trace leakage inductance)
Clamp diodes	GB01SLT12, 1200 V, 2.5 A Schottky diodes
Transformer	1:1:0.875 turns ratio (Primary: Secondary: Clamp winding)
Rectifier diodes	C4D08120E, 1200 V, 8 A Schottky diodes
Output inductor, $L$	1.3 mH
Output capacitor, $C_{out}$	1.5 μF, 1100 V, film capacitor.

legs.

#### IV. SIMULATION RESULT

The design of the converter can be done similar to 2-L full bridge converter [20]. The soft-dc link primarily effects the design of the transformer turns ratio. The design of rectifier side components can be done similar to a 2-level PSFB. Since, the topology is buck derived the minimum input voltage and maximum output current and output voltage decide the turns ratio of the transformer. The minimum input voltage for the 3LAFB is when one of the soft DC-link voltages is zero. The converter specifications and designed parameters are given in Table III. Ideal simulations are performed for the designed converter. Mosfet and diode device output capacitances are not included in these simulations. The simulations results are in given in Fig. 6 for a operating point in Sector-2 encounter with a 480 V Unfolder. It can be seen that the average of  $i_p^{dc}$  over switching period is greater than that of  $i_n^{dc}$ . This result shows that the converter can operate with unequal DC-link voltages  $v_p$  and  $v_n$ , and also has the capability to draw different magnitude of average currents from each of the dc link capacitors while providing stable output voltage and current. From a careful examination of the series inductor current ( $i_{Ls}$ ) direction and switching instants, it can found that  $i_{Ls}$  is in the direction to aid ZVS of all eight devices in the 3-L bridge.

#### V. HARDWARE VALIDATION

A 2 kW lab prototype of the proposed 3LAFB converter is designed and fabricated. The prototype is shown in Fig. 7. and main components are highlighted. The effective series inductance( $L_s$ ) and rectifier diode parasitic capacitances ring at each active transition. This is expected in PWM converters with inductive output filter [19]–[21]. There are multiple methods that can be used to clamp the ringing voltage across

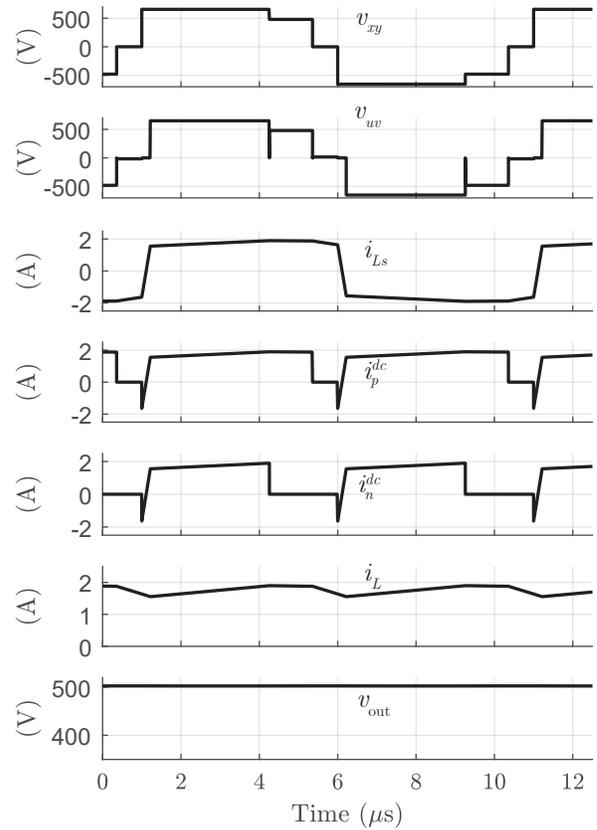


Fig. 6: Ideal converter simulation result for operating condition  $v_p= 480$  V,  $v_n= 175$  V,  $d_p = 0.87$ ,  $d_n = 0.65$ ,  $v_{out}= 500$  V,  $i_{out}= 3.5$  A

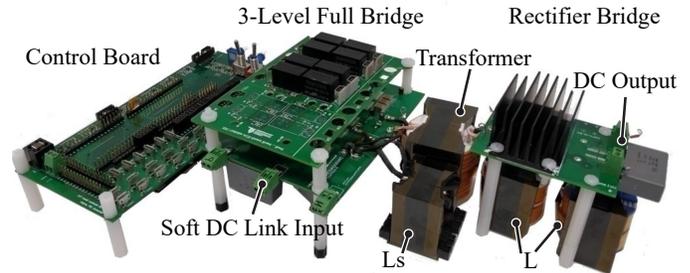


Fig. 7: 3LAFB hardware prototype with parameters of Table III built for evaluation

the rectifier diodes to a safe operating voltage [21], [22]. For the designed prototype, the transformer voltage is clamped to input full DC-link voltage  $v_{pn}$  using a clamp winding and four clamp diodes.

Hardware results are provided at three different input operating conditions that will be encountered when connected to 480 V<sub>AC</sub> 3-phase Unfolder. The output operating conditions 500 V<sub>DC</sub> and 3.5 A<sub>DC</sub> are same for all three results. Results are given in Fig. 8. 100 kilo sample data-points are used per signal to plot these waveforms.

Two programmable DC power supplies connected in series are used to emulate the input soft DC-link. A 2 kW peak

TABLE IV: Hardware result summary

	Input voltages	Pulse durations	Measured quantities	$\eta$ %
(a)	$v_{po}=334$ V $v_{on}=334$ V	$d_p=0.83$ $d_n=0.83$	$i_p^{dc}=2.7$ A $i_n^{dc}=2.7$ A $v_{out}=500$ V $i_{out}=3.5$ A	97.5%
(b)	$v_{po}=174$ V $v_{on}=478$ V	$d_p=0.69$ $d_n=0.91$	$i_p^{dc}=2.26$ A $i_n^{dc}=3.0$ A $v_{out}=501$ V $i_{out}=3.56$ A	97.7%
(a)	$v_{po}=5$ V $v_{on}=583$ V	$d_p=0.52$ $d_n=0.94$	$i_p^{dc}=1.57$ A $i_n^{dc}=3.04$ A $v_{out}=500$ V $i_{out}=3.5$ A	97.8%

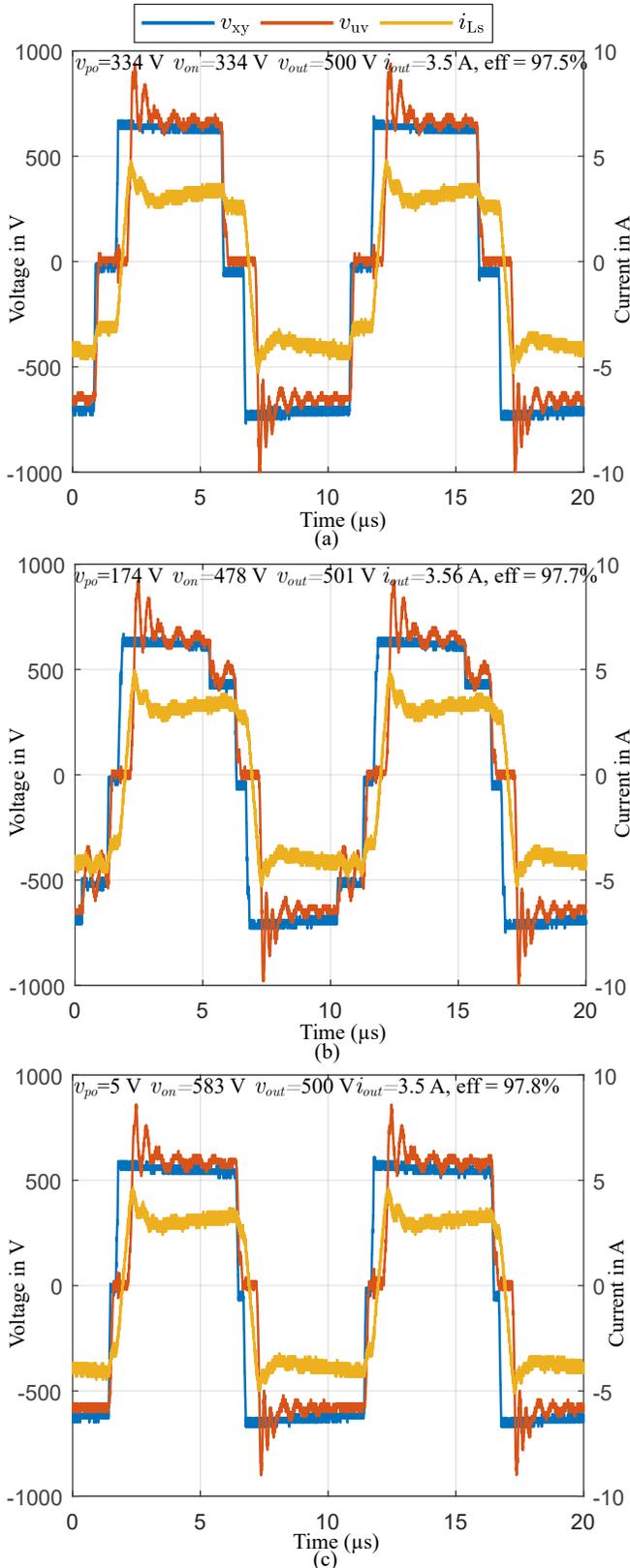


Fig. 8: Hardware prototype results at three operating conditions (a)  $v_{po}=334$  V,  $v_{on}=334$  V,  $v_{out}=500$  V, (b)  $v_{po}=174$  V,  $v_{on}=478$  V,  $v_{out}=501$  V, (c)  $v_{po}=5$  V,  $v_{on}=583$  V,  $v_{out}=500$  V.

rated electronic load is used to emulate load. A general-purpose control board built around F28379D microcontroller is used to generate the PWM signals. Pre-calculated values of duty-cycles  $d_1, d_2$  for each operating point are loaded on the microcontroller. The input and output DC quantities are measured using WT1806E Power Analyzer.  $1 \mu\text{H}$  inductors are used at each DC port of the converter to filter out the ripple currents to get accurate DC measurements. The measured quantities are summarized in Table. IV. Efficiencies of about 97.5% or higher are measured for all three operating points. Auxiliary supply losses of about 4 W are not included in this measured efficiency. High efficiency is achieved due to the ZVS turn-off of all eight mosfets. The rectifier diodes' conduction loss is estimated to be around 8.75 W for 1750 W output. For the same design, the losses can be further reduced by implementing synchronous rectification. With mosfets on the rectifier bridge ZVS range can be increased if active rectification is implemented [23].

## VI. CONCLUSION

Three-phase unfolding based isolated rectifiers have the potential to improve efficiency and power density of the system. Typically, this approach is implemented using two DC-DC converters in the DC-DC stage. Each DC-DC converter is processing time-varying power and has to be designed to temporarily process full power. This reduces the achievable power density and efficiency due to low utilization of the converters. A 3-level asymmetric full-bridge (3LAFB) is proposed as the back-end dc-dc stage for isolated 3-phase battery chargers. The proposed converter greatly improves the power density and efficiency since only one transformer is required and the converter is processing constant power. Pulse-width modulation scheme is proposed that minimizes the conduction duration of 4-quadrant switches and achieves zero-volt switching (ZVS) for all the active devices. A 2 kW rated lab prototype is built with 500 V peak output voltage that can work with a 480 V grid connected 3-phase Unfolder. Hardware results are provided at three different input operating conditions that cover the entire operating range. The converter was able to maintain high efficiency over all three operating conditions. The results validate the ability of the converter to operate with unequal DC-link voltages  $v_p$  and  $v_n$ , and also draw different magnitude of average currents  $\langle i_p^{dc} \rangle$ ,  $\langle i_n^{dc} \rangle$  from each of the soft DC-link capacitors required to perform the power factor correction.

## REFERENCES

- [1] "Electric vehicle and plug in hybrid electric vehicle conductive charger coupler," Standard, J1772 SAE, Oct. 2017.
- [2] "Ieee standard technical specifications of a dc quick charger for use with electric vehicles," *IEEE Std 2030.1.1-2015*, pp. 1–97, Feb 2016.
- [3] A. Albanna, M. N. Arafat, A. Gupta, M. Anwar, and M. Teimor, "Analysis of ground fault currents in isolated and non-isolated charging modules in electric vehicles," in *2015 IEEE Transportation Electrification Conference and Expo (ITEC)*, June 2015, pp. 1–6.
- [4] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2151–2169, May 2013.
- [5] D. Aggeler, F. Canales, H. Zelaya, D. L. Parra, A. Coccia, N. Butcher, and O. Apeldoorn, "Ultra-fast dc-charge infrastructures for ev-mobility and future smart grids," in *2010 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT Europe)*, Oct 2010, pp. 1–8.
- [6] "Using the latest wolfspeed c3mtm sic mosfets to simplify design for level 3 dc fast chargers," White Paper, CREE.
- [7] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, and K. Shiozaki, "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2606–2617, May 2014.
- [8] "Terra 53 cj multi-standard dc charger," Data Sheet, ABB. [Online]. Available: <https://new.abb.com/ev-charging/products/car-charging/multi-standard/terra-53-cj-ul>
- [9] Q. Lei and F. Z. Peng, "Space vector pulsewidth amplitude modulation for a buck-boost voltage/current source inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 266–274, Jan 2014.
- [10] V. K. Kanakesh, D. B. Yelaverthi, A. Ghoshal, A. K. Rathore, and R. Mahanty, "Analysis and implementation of closed-loop control of electrolytic capacitor-less six-pulse dc-link bidirectional three-phase grid-tied inverter," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 539–550, Jan 2018.
- [11] D. Menzi, D. Bortis, and J. W. Kolar, "Three-phase two-phase-clamped boost-buck unity power factor rectifier employing novel variable dc link voltage input current control," in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Nov 2018, pp. 1–8.
- [12] J. W. Kolar and T. Friedli, "The essence of three-phase pfc rectifier systems—part i," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, Jan 2013.
- [13] T. Friedli, M. Hartmann, and J. W. Kolar, "The essence of three-phase pfc rectifier systems—part ii," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 543–560, Feb 2014.
- [14] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase ac-dc power conversion using series-resonant converter modules and a three-phase unfold," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9001–9012, Dec 2017.
- [15] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, "Novel swiss rectifier modulation scheme preventing input current distortions at sector boundaries," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5771–5785, July 2017.
- [16] L. Schrittwieser, M. Leibl, M. Haider, F. Thöny, J. W. Kolar, and T. B. Soeiro, "99.3% efficient three-phase buck-type all-sic swiss rectifier for dc distribution systems," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 126–140, Jan 2019.
- [17] M. Silva, N. Hensgens, J. A. Oliver, P. Alou, . García, and J. A. Cobos, "Isolated swiss-forward three-phase rectifier with resonant reset," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4795–4808, July 2016.
- [18] X. Wang, B. Zhang, S. Xie, and K. Xu, "A soft switching swiss rectifier based on phase-shifted full-bridge topology," in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Nov 2018, pp. 1–6.
- [19] S. Bal, D. B. Yelaverthi, A. K. Rathore, and D. Srinivasan, "Improved modulation strategy using dual phase shift modulation for active commutated current-fed dual active bridge," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7359–7375, Sep. 2018.
- [20] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched pwm converter," in *Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition*, March 1990, pp. 275–284.
- [21] X. Ruan and L. Zhang, "Voltage oscillation elimination in output rectifier diodes in zero-voltage-switching pwm full-bridge converter: An overview," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015, pp. 6328–6335.
- [22] Song-Yi Lin and Chern-Lin Chen, "Analysis and design for rcd clamped snubber used in output rectifier of phase-shift full-bridge zvs converters," *IEEE Transactions on Industrial Electronics*, vol. 45, no. 2, pp. 358–359, April 1998.
- [23] S. Bal, D. B. Yelaverthi, A. K. Rathore, and D. Srinivasan, "Novel active rectification for extended zvs operation of bidirectional full bridge dc/dc converter for energy storage application," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Oct 2018, pp. 2103–2109.

## A.2 Electromagnetic Sensor and Actuator Attacks on Power Converters for Electric Vehicles

# Electromagnetic Sensor and Actuator Attacks on Power Converters for Electric Vehicles

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**Abstract**—Alleviating range anxiety for electric vehicles (i.e., whether such vehicles can be relied upon to travel long distances in a timely manner) is critical for sustainable transportation. Extremely fast charging (XFC), whereby electric vehicles (EV) can be quickly recharged in the time frame it takes to refuel an internal combustion engine, has been proposed to alleviate this concern. A critical component of these chargers is the efficient and proper operation of power converters that convert AC to DC power and otherwise regulate power delivery to vehicles. These converters rely on the integrity of sensor and actuation signals. In this work the operation of state-of-the-art XFC converters is assessed in adversarial conditions, specifically against Intentional Electromagnetic Interference Attacks (IEMI). The targeted system is analyzed with the goal of determining possible weak points for IEMI, viz. voltage and current sensor outputs and gate control signals. This work demonstrates that, with relatively low power levels, an adversary is able to manipulate the voltage and current sensor outputs necessary to ensure the proper operation of the converters. Furthermore, in the first attack of its kind, it is shown that the gate signal that controls the converter switches can be manipulated, to catastrophic effect; i.e., it is possible for an attacker to control the switching state of individual transistors to cause irreparable damage to the converter and associated systems. Finally, a discussion of countermeasures for hardware designers to mitigate IEMI-based attacks is provided.

**Index Terms**—cyber-physical system security, power converter security, intentional electromagnetic interference (IEMI) attacks

## I. INTRODUCTION

In order to increase the adoption of electric vehicles (EV) it is necessary that extremely fast chargers (XFC), along with the attendant battery management systems (BMS), be developed. These advances in charging technology will ensure that EVs can be charged in a time frame commensurate with that of refilling an internal combustion engine vehicle, and therefore alleviate concerns vehicle owners have regarding the feasibility of using EV for routine and long distance travel. The security of XFC chargers and BMS are of great importance since attacks on these systems could result in the overcharging of the EV battery (leading to, e.g., potential fire). Larger scale synchronized attacks on XFC chargers, since they connect the EV to the power grid, could cause instability in the grid leading to blackouts.

Until now the security of EV power converter systems has been largely ignored. In this work we seek to enhance the security of EVs by examining the potential vulnerabilities of XFC chargers and BMS. To this end we provide simulation and experimental results for attacks against critical

components of the systems, namely their sensor and actuator (switching) capabilities. For the first time, we demonstrate electromagnetic-based, non-intrusive attacks on actual power converters (comprising AC-DC and BMS power converters) and discuss possible countermeasures.

### A. Related Work

IEMI is known to be an important threat for analog sensor readings in the security literature. IEMI attacks have been reported on light sensors, temperature sensors, speed sensors, implantable cardiac devices and microphones [1]–[4]. Although each attack starts with injecting radiation at the resonance frequency of the targeted device, device-specific non-linearities, due to amplifiers [2], [4] and ADCs [1], can be exploited by attackers to manipulate the sensor data. The reader is referred to [5] for a comprehensive review of such attacks. Since amplifiers and ADCs are commonly used in power converters for sensing and feedback control, IEMI can be used to attack XFC power converters with both relatively low-cost and low-power.

### B. Contributions

In this work we examine the vulnerability of state-of-the-art XFC power converter designs to IEMI attacks. To the best of authors' knowledge, this is the first study that focuses on power converter security from the perspective of IEMI attacks. Specifically, we demonstrate three attacks to show that both the sensing and actuator signals of power converters can be manipulated via non-invasive means (i.e., no physical connection with the hardware are necessary, thereby allowing for proximate attacks). Our primary contributions are:

- Showing that the voltage and current sensor outputs of power converters, necessary to maintain the proper and safe control of the converters, can be manipulated with low-cost and low-power amplifiers and radiators.
- Demonstrating that, and proving an analytical model that explains how, drivers/switches can be controlled (i.e., open or closed) via difficult to shield IEMI. Such drivers/switches are ubiquitous in hardware and cyber-physical systems and we are the first to show and explain how their proximate manipulation may be effected.
- Proposing several widely applicable design changes to hardware level to mitigate IEMI attacks.

Attacks are experimentally validated and, for safety's sake, their effects demonstrated in simulation via Matlab Simulink.

\*Dayanıklı and Hatch are co-first authors.

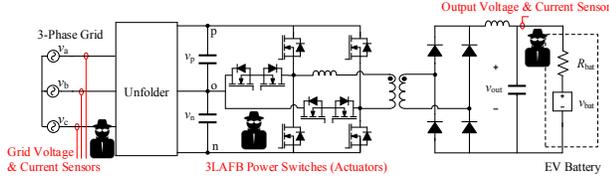


Fig. 1: Functional diagram of the 3-phase AC-DC converter with 3LAFB topology. The figure highlights attack points in red, viz. the output and grid voltage and current sensors as well as the gate signals to the power switches (actuators).

## II. SYSTEM MODELS

The targeted/victim system consists of an extreme fast charger (XFC) and battery management system (BMS). The XFC is a high-power (350 kW) converter designed to convert 3-phase AC power into DC voltage for EV charging; thus, it is known as an AC to DC (AC-DC) converter. As the power-level increases, the battery charging process poses potential safety risks to EV users in the event that an adversary gains control of the system, as described later. This section describes the AC-DC and BMS, their controls, and weak points from a theoretical perspective.

The specific AC-DC converter analyzed in this paper is the 3-Level Asymmetric Full Bridge (3LAFB) [6], which is an isolated converter topology intended for use in Unfolding based rectifiers. The functional diagram of the Unfolder and 3LAFB topology is shown in Fig. 1. Based upon a safety analysis, the diagram identifies the most sensitive points of attack to be the voltage and current sensors used to monitor the converter inputs and outputs, as well as the power switches. The control objective of the AC-DC converter is to regulate the charging of EV batteries. Battery charging is typically implemented in a constant current constant voltage (CC-CV) scheme. The EV battery is charged at a constant current until the max battery voltage is reached. The charger then switches to constant voltage (CV) control until the battery is fully charged. It is important to note that EV batteries subjected to charging currents or voltages greater than allowable values cause the cells to overheat which creates a fire hazard.

The control of the AC-DC is achieved by switching the 3LAFB to regulate average voltage and current. The feedback sensors are commonly implemented by low voltage analog hardware that is digitalized by an ADC. The controller updates the duty cycle for switches based on the sensed error. (The duty cycle determines the average amount of time the switches are turned on in one switching period.) In actuality, individual power transistors are turned on and off by gate drivers driven by pulse width modulation (PWM) signals.

The switches and their gate drivers can be thought of as the system actuators because they actuate the PWM gate signals from a micro-controller. The gating signals, being PWM signals, command the transistor to turn on (logic high) or off (logic low). The 3LAFB has 8 transistors and 8 gating signals while the unfolder requires 12 of each. Gate drivers operate similar to transistors in that they require the input

signal to rise above a certain threshold voltage in order to change the devices switching state.

The system's weak points, with respect to IEMI, lie within the feedback sensors and low-voltage gating signals. The converter can only regulate the output correctly if the feedback voltage/current sensors are measuring accurately. Furthermore, the system can only be controlled if the correct gate signal from the controller is being acted upon by the switches. Thus, large enough disruptions in the gating signal (3.3 V logic) can cause the gate driver to actuate a false turn-on or turn-off of a power switch.

The BMS operates on the same principles as the AC-DC converter. The purpose of the BMS, comprised of multiple DC-DC converters, is to balance the individual cells that make up an EV battery-pack. Each DC-DC converter has its own voltage and current sensors that measure the flow of power for that cell. The BMS employs a current and/or voltage feedback loop for each DC-DC by controlling the duty cycle (or equivalent control signal).

## III. ATTACK SIMULATIONS AND OUTCOMES

To explore the effects of IEMI attacks on the battery charging operation of the AC-DC, the attack scenario is simulated in Matlab. The system is modeled on a switching level using PLECS's Blockset add-on for Simulink. The hardware parameters from a 2 kW prototype [6] were used for the simulation. The operating point for the simulation is given in Table I. The 3LAFB attack is implemented at a DC operating point where the input voltages of the 3LAFB are held constant at a particular grid phase angle rather than the time-varying input that occurs during normal AC operation. The AC input should be considered when the attackers target the grid voltage and current sensors which will affect the Unfolder operation and AC-DC power quality. Due to space constraints, only the CV regulator will be investigated; however, the presented analysis can be extended to other parts of the system.

Based on an efficiency and safety analysis of the system, we consider a scenario wherein an attacker is able to overcharge the battery by manipulation of the power converter's feedback voltage signal. Such over-voltage charging would lead to increased charging current at the maximum voltage. The extra power dissipated as heat by the resistive losses of the battery would cause cell heating. Repeated attacks of this nature would lead to decreased battery capacity and lifespan. In the extreme case, where the battery is subjected to sustained over-current charging, the increase in cell temperatures could lead to thermal runaway in which the battery pack would ignite and create a self-sustaining fire. To cause damage to the battery it is simply necessary to subvert CV control (specifically the

TABLE I: Operating Point for CV IEMI Simulations

Parameter	Value	Parameter	Value
$V_{bat}$	500 V	$R_{bat}$	0.5 $\Omega$
$V_{out,ref}$	502 V	$\phi_{grid}$	45°
$V_p$	480 V	$V_n$	176 V

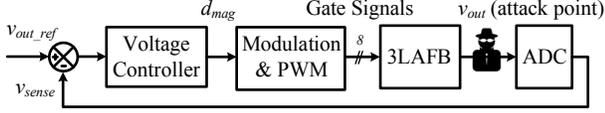


Fig. 2: Block diagram of the constant voltage controller for the 3LAFB. The attacker targets the analog circuitry before the sensing information is digitized by the ADC.

second phase of the CC-CV charging scheme). The CV control loop demonstrated in Fig. 2 uses feedback from the output voltage sensor to control the magnitude of applied duty cycles,  $d_{mag}$ . In this scenario, the attacker is targeting the  $v_{sense}$  which is the sensed feedback signal of  $v_{out}$ , the output voltage of the converter.

In the simulation shown in Fig. 3 an IEMI attack is initiated on the hardware at 10 ms. The attack is simulated by altering the feedback signal,  $v_{sense}$ , by subtracting 1 V from the actual output voltage; i.e., the attacker decreases the apparent output voltage which will cause the control system to compensate by increasing the output voltage. This alteration represents the average voltage distortion that is induced on an ADC sensor used to measure output voltage during an IEMI attack. The simulated attack is sustained for 30 ms.

As can be seen from the figure, the controller regulates the sensed voltage to the reference voltage of 502 V; however, the actual output voltage is 503 V. On the short time scale of the simulation, the battery voltage is approximately constant and 500 V. The extra 1 V on the output causes the battery current to increase from 4 to 6 A, a significant increase in current that would cause heating. The charging current is extremely sensitive to changes in  $v_{out}$  due to the small battery resistance ( $<1 \Omega$ ), which implies that small changes in sensed voltage result in geometrical increases in current (and thus heat).

#### IV. THEORY OF ATTACK

Our attacks are based on Faraday's law of induction, which states that a time varying magnetic field captured by a conducting loop results in a voltage on the loop [7]. By such means

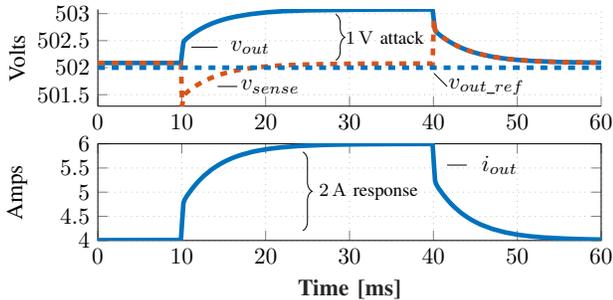


Fig. 3: Simulation of constant voltage controller attack. An attacker induces a 1 V offset into the  $v_{sense}$  signal causing the charging current to increase from 4 to 6 A, which indicates that a small change in sensed voltage can lead to a substantial increase in current (and thus heating of a battery).

are we able to modify the voltages measured by sensors, and used to control switches, in power converters. To observe how a time varying current,  $i_a$ , supplied by an attacker, induces a voltage,  $v_i$ , on a victim loop, an infinitely long, z-axis directed current is assumed to be positioned at distance  $d_a$  from the victim circuit having dimensions  $w$  and  $l$  (Fig. 4a). By Faraday's law and Ampere's law the relationship between the attacker signal,  $i_a$ , and the induced voltage,  $v_i$ , is:

$$v_i(t) = -\mu \left[ \frac{w}{2\pi} \ln \left( \frac{d_a + l}{d_a} \right) \right] \frac{d}{dt} i_a(t) \quad (1)$$

where the permeability of the medium is  $\mu$ .

The amplitude and shape (waveform) of  $v_i$  are determined by a geometry coefficient (square brackets) and the time derivative of  $i_a$ . In the following attack scenarios, the attacker uses a continuous sinusoidal  $i_a$  attack waveform, so the form of  $v_i$  is a sinusoidal with a phase shift due to transmitting hardware. We note that an increased victim loop size results in an increase induced  $v_i$ .

#### A. Threat Model

We assume an attacker aiming to manipulate the operation of an AC-DC converter and BMS through IEMI. It is assumed that the attacker can place EM radiators in proximity to the converters but there is no physical connection between the attacker hardware and victim circuitry. The attacker has access to commodity RF component devices and like components, e.g., waveform generators, RF amplifiers and EM radiators like toroids and antennas (Figure 4b). We consider an attacker who targets weak points of the victim system using a toroid with a focused magnetic field or a ZPSL antenna with a directive near field radiation pattern. The weak points discussed in detail in Section II are chosen as attack points (voltage sensor output,  $v_{out}$ , BMS current sensor output,  $i_{cell}$ , and the low voltage gate signals that control the AC-DC switches).

1) *Attack Point I - Voltage Sensor Output*: The attacker uses IEMI to manipulate the voltage sensor data  $v_{out}$  by inducing voltage  $v_i$  on the victim cable that connects the analog sensor output and the ADC input of the CV controller. The attack has two phases: the first phase is the efficient EM coupling to the victim cable through the use of cable resonant frequency as an attack frequency [4]. Before each attack, a frequency sweep is applied to detect the resonant frequency of the victim cable. The next phase is the manipulation of non-linearity of ADC. An ADC samples and digitizes an analog signal in the ADC input range ( $v_{min}$  to  $v_{max}$ ). A very common practice is to average the digitized data to filter out high frequency noise. It is discussed in [1] how a generic ADC transfer function and electrostatic discharge (ESD) diodes result in a phenomenon called clipping. We assume the input voltage of the ADC is compromised and a time varying voltage  $v_{ADC}$  is fed into the ADC as follows:

$$v_{ADC}(t) = V_s + v_i(t) \quad (2)$$

where  $V_s$  is a relatively low frequency sensor output which is assumed as a DC offset and  $v_i$  is a purely sinusoidal induced

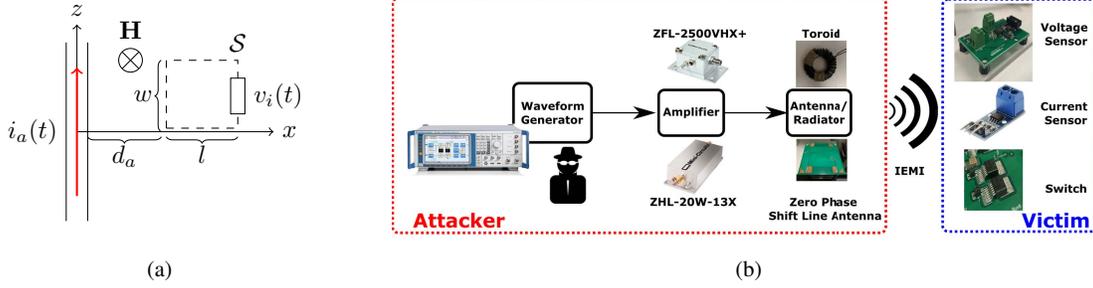


Fig. 4: (a) IEMI attack model [1] (b) Attacker hardware and attack points for power converters

signal by IEMI with frequency  $f$  and amplitude  $V_i$ . For small sensor output  $V_s$  close to  $v_{min}$  case, we assumed that  $v_i = 0$  V. In that case, the measured voltage by the ADC has the form of a half wave rectified signal assuming  $V_i < v_{max}$ . The average value (DC) of a half wave rectified sinusoidal waveform with amplitude  $V_i$  and period  $T = 1/f$  is:

$$V_{DC} = \frac{1}{T} \left( \int_0^{\frac{T}{2}} V_i \sin(2\pi ft) dt + \int_{\frac{T}{2}}^T 0 dt \right) = \frac{V_i}{\pi} \quad (3)$$

Note that Equation 3 assumes an infinite sampling frequency and ignores the effects which is observed when the attack frequency is a perfect multiple of sampling frequency (i.e., relative phase becomes important). Other affects also render Equation 3 an approximation that works well in practice; the reader is referred to [1] for a detailed discussion of inducing DC voltages via AC signals.

2) *Attack Point II - Current Sensor Output*: This attack point consists of the PCB trace between the analog current sensor output and the input of controller ADC (Figure 2). It is assumed that the attacker can place the EM radiator (e.g., an air gap toroid) to induce a high magnetic field. The two phase attack mechanism that includes the efficient coupling and manipulation of the ADC discussed in the previous section is applicable in this attack as well. However, this attack has a fundamental difference: the attack point is a PCB trace which requires the manipulation of smaller victim loops than *Attack I* and necessitates higher attack powers.

3) *Attack Point III-Gate Control Signal*: The 3LAFB employs a high current gate driver [8] that controls an SiC switch [9] as shown in Figure 5. The attacker aims to change the input voltage  $V_{IN}$  of gate driver to control the switch. To turn on the gate driver and switch, the attacker should satisfy the condition in 4 which is also demonstrated in Figure 5:

$$v_i(t) = V_i \sin(2\pi ft) > V_{th} \text{ Switch ON} \quad (4)$$

where  $v_i$  is the voltage induced at the input of the gate driver and  $V_{th}$  is the minimum voltage to activate the gate.

## V. EXPERIMENTAL RESULTS

Three attack points are experimentally tested against IEMI.

### A. Attack I: False Voltage Sensor Data Injection

The attacker locates the toroid around the victim cable as in Figure 6a. The toroid has an air-gap which can be filled with a ferrite piece which eliminates the need for the attacker to unplug any wire in the victim. The attacker system consists of a Mini-Circuits ZFL-2500VHX+ RF amplifier and a 30 coil toroid (Figure 4b). The attack power is fixed at 200 mW throughout Attack I.

**Measurement Methodology:** The voltage output of a DC supply is adjusted to 21 V and connected to the voltage sensor as reference voltage. The system is observed to function properly before the IEMI applied. To magnify the effect of IEMI attack (i.e. less power same data manipulation or same power more data manipulation), an attacker can use the resonant frequency of the victim system as attack frequency [4]. At resonance the imaginary component of the impedance is minimum, which results in higher induced voltages. To detect the resonant frequency of the victim cable, a frequency sweep between 100 MHz and 500 MHz is applied with 10 MHz increments and voltage sensor data manipulation is observed from a PC. Although all tested attack frequencies result in varying increases in the voltage readings, it is observed that between 380 MHz and 420 MHz, the effect is more pronounced.

**Results:** Figure 6b shows the voltage reading manipulation under IEMI. Depending on the frequency, the voltage readings are manipulated up to the range between 28 V and 42 V, while the reference voltage is 21 V. Specifically, at 380 MHz, the voltage reading is increased by % 100 to 42 V. Another observation is that the IEMI injection results in an increase of voltage readings throughout the frequency range. This observation is parallel to the ADC nonlinearity discussion in Section IV, as the 21 V test voltage results in sensor voltages

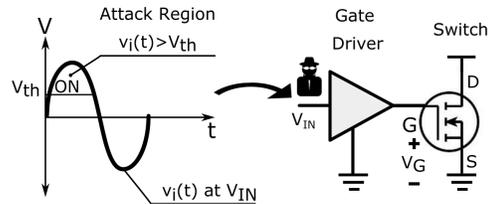


Fig. 5: The induced voltage  $v_i(t)$  to  $V_{IN}$  should exceed the gate driver threshold voltage  $V_{th}$  to turn the switch on.

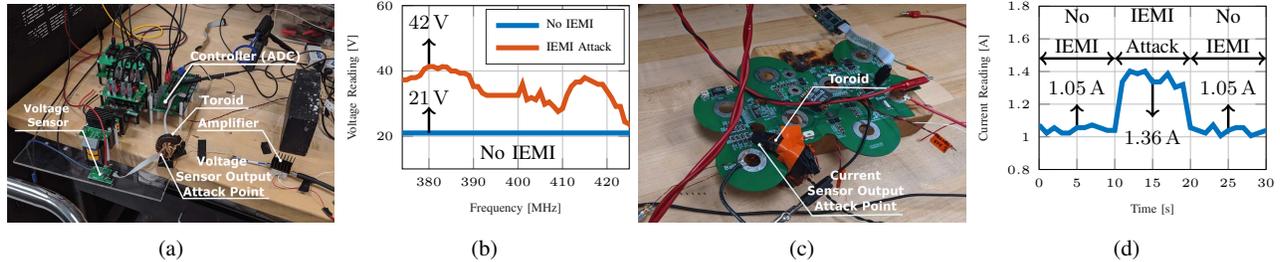


Fig. 6: False voltage and current sensor data injection attacks (a) Experimental setup for voltage sensor output manipulation (b) Voltage sensor output manipulation with regard to attack frequency: measured voltage increased by 21 V under IEMI (c) Experimental setup for current sensor output manipulation (d) Current readings with regard to time, when IEMI is applied between  $t = 10$  s and  $t = 20$  s, the average of current readings increased from 1.05 A to 1.36 A

on the lower half of ADC input range. The IEMI on voltage sensor output is a significant threat for a converter because of the low power nature of the attack. On the other side, Simulink analyze shows that even a 1 V data manipulation can increase the output current significantly (Figure 3).

### B. Attack II: False Current Sensor Data Injection

The attacker aims to manipulate the current sensor data on the printed circuit board (PCB) of the BMS. The air gapped toroid is positioned on the PCB trace as shown in Figure 6c. The attacker hardware consists of a 20 W RF amplifier (Mini-Circuits ZHL-20W-13X) and the toroid. The amplifier output power is adjusted to 2.5 W to eliminate any mismatch problem due to dominantly inductive impedance of the toroid.

**Measurement Methodology:** The current sensor is supplied with a 1 A test current and the system is tested before IEMI radiation. It is observed that the system is operating properly and correct current data is received by the controller. Then, a sinusoidal EMI with varying frequency between 10 MHz and 500 MHz with 10 MHz increments is applied and it is observed that in the vicinity of 100 MHz, the current data manipulation is much more pronounced.

**Results:** In Figure 6d, the current sensor outputs of the system is provided under a temporary IEMI attack between  $t = 10$  s and  $t = 20$  s. The attack frequency is 100 MHz. It is observed that when IEMI starts at  $t = 10$  s, the mean value of current readings increase by % 30 from 1.05 A to 1.36 A. Note that the test current of 1 A is still applied during the attack. On the other side, it is observed that the attack results in an increase in the sensor data which is parallel with the discussion made in Section IV. This attack shows that the PCB traces can be direct targets for IEMI which means PCB level countermeasures are necessary for secure systems.

### C. Attack III: False Gate Voltage Injection: Turning on Switches with IEMI

The attacker hardware includes a 20 W RF amplifier (Mini-Circuits ZHL-20W-13X) and a Zero-Phase-Shift Loop (ZPSL) antenna (Figure 4b). ZPSL antenna is a near field resonant antenna with a strong magnetic field at 72 MHz directed through z axis. The attacker positions the ZPSL antenna 10 cm

above intertwined and shielded cables that carry  $V_{IN}$  and ground of the gate driver. We will use the terminology where  $V_{IN}$  is the gate driver input or voltage and  $V_G$  is switch gate voltage (Figure 5).

**Measurement Methodology:** Attack frequency is chosen as 72 MHz and the attack power is increased by 1 dB increments from 100 mW to 20 W,  $V_{IN}$  and  $V_G$  are observed with an oscilloscope.  $V_{IN}$  is set to low throughout the measurements which results  $V_G$  is held at  $-3$  V to ensure the switch stays off. If the attack is successful (i.e., switch is turned on by gate drive), the gate voltage  $V_G$  is expected to increase to 18 V by the gate driver. To capture the turn on characteristic for  $V_G$  and  $V_{IN}$ , the oscilloscope is set to single trigger for a low to high transition at  $V_G$ .

**Results:** When the 20 W IEMI applied from an attack distance of 10 cm, it is observed that the IEMI is not sufficient to turn on the switch. This is an expected result, because the loop area between cables that carry ground and  $V_{IN}$  connection is small and differential voltage between  $V_{IN}$  and ground is not high enough to satisfy the condition in Equation 4. Although this shows that sending  $V_{IN}$  and ground cables through intertwined cables are relatively secure, in PCB based systems, the  $V_{IN}$  and ground traces/pads is not always close due to the minimum spacing requirements of manufacturing process. To observe this phenomenon, the green  $V_{IN}$  and the white ground cables are physically separated and a loop of  $4\text{ cm}^2$  is exposed as demonstrated in Figure 7a. When the attack power is to 20 W, it is observed that the  $V_G$  increases and switch turns on as shown in yellow plot of Figure 7b. First of all, it is observed that the switch turns on and off until it stabilizes at turn on condition. As we trigger the oscilloscope for a time window of  $100\ \mu\text{s}$ , the power increase is not observable in the  $V_{IN}$  (blue). A possible reason for this phenomenon is the output power increase is smaller than 1 decibel as the amplifier operates in saturation.

## VI. DISCUSSION OF ATTACKS

IEMI attacks on the prototype (Section V) have exposed potentially catastrophic weaknesses in the AC-DC and BMS systems. The ability for the attackers to significantly alter the average ADC values of the power converter's feedback sensors

poses a serious threat to the safety of XFC. The  $v_{out}$  voltage sensor with a range of 600 V had an induced error equivalent to 21 V of error. As was shown in Section III, an error of 1 V in the output voltage sensing was enough to significantly disrupt the operation of the CV controller.

Every voltage and current sensor used for control in the converter design is a potential weakness to be mitigated. The attacker's ability to control the switches through alteration of the gate signal is another attack point. The digital gate signals are not as sensitive to the IEMI as the sensed, analog signals; however as was shown, if the victim loop of the gate signal is large enough, the attackers are able to turn on switches that were intended to be closed. If this event occurs on live hardware, a short-circuit event is likely to occur. The incredible currents and heat generated in a short-circuit is highly likely to cause system wide device failure or at least system shutdown.

### Countermeasures

Although RF shielding (e.g., conductive sheet or foam) is effectively used against relatively high frequency signals, the low frequency ( $< 100$  MHz) and magnetic nature of the reported attack signal makes it very difficult to shield fast chargers [10]. Adding to that, none of the magnetic field shielding options (e.g., MuMetal and Faraday cage) are employed in commercial fast chargers. In order to protect PCB traces transmitting sensitive signals (e.g., analog sensor outputs and gate/switch control signals), hardware designers should be aware of IEMI threats from the first moment of layout generation and eliminate large loops between significant traces and ground pad/traces. However, due to minimum spacing restrictions of PCB manufacturing process and complex layout designs with many components, eliminating large loops may not always be possible. In those situations, we suggest using via-fenced striplines for analog sensor outputs and gate driver signals. Although via-fenced stripline is for eliminating

crosstalk between traces, it can also be used to eliminate high frequency IEMI from outside sources. We are also investigating alternative approaches that seek to randomize multiple sections of the pathway signals take from sensor to ADC, controller or actuator that would make the resonant frequency of traces unknown to the attacker and thus limit their ability to couple to circuits and affect signals.

### VII. CONCLUSION

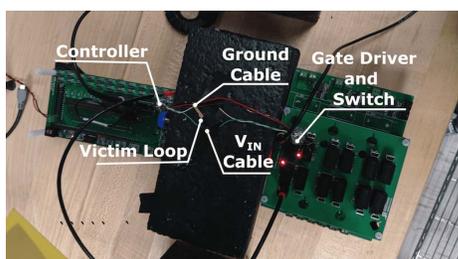
The AC-DC and Battery Management System (BMS) of the power converter is observed to be vulnerable to IEMI attacks. Both systems rely on feedback of the converter outputs to properly regulate the flow of power in the circuit. The system's low voltage current and voltage sensor outputs and gate control signals are susceptible to IEMI attacks which distort the converter's control by inducing a DC offset to the sensed value. The attackers can gain control of the system by manipulation of the feedback signal and can cause damage to the EV, XFC, and BMS systems with one or combination of attacks. Furthermore, the control signals from the microcontroller to the gate drivers can also be vulnerable given the victim loop and attacker power level is large enough to induce sufficient voltage. As a future work, we plan to investigate additional PCB level countermeasures and produce prototypes to test these ideas. Our end goal is to provide a design guideline for secure PCB layout design against IEMI.

### ACKNOWLEDGMENT

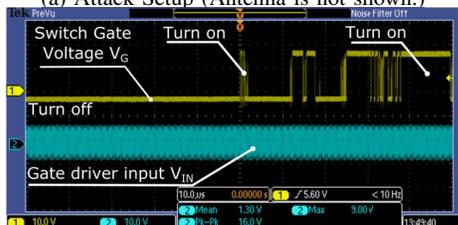
This work was supported in part by the Department of Energy under grant No. DE-EE0008453.

### REFERENCES

- [1] J. Selvaraj, G. Y. Dayanikli, N. P. Gaunkar, D. Ware, R. M. Gerdes, and M. Mina, "Electromagnetic induction attacks against embedded systems," in *Proceedings of the 2018 on Asia Conference on Computer and Communications Security*, ASIACCS '18, (New York, NY, USA), pp. 499–510, ACM, 2018.
- [2] Y. Tu, S. Rampazzi, B. Hao, A. Rodriguez, K. Fu, and X. Hei, "Trick or heat? manipulating critical temperature-based control systems using rectification attacks," in *Proceedings of the 2019 ACM SIGSAC Conference on Computer and Communications Security*, CCS '19, (New York, NY, USA), p. 2301–2315, Association for Computing Machinery, 2019.
- [3] Y. Shoukry, P. Martin, P. Tabuada, and M. Srivastava, "Non-invasive spoofing attacks for anti-lock braking systems," in *Cryptographic Hardware and Embedded Systems* (G. Bertoni and J.-S. Coron, eds.), vol. 8086 of *Lecture Notes in Computer Science*, pp. 55–72, 2013.
- [4] D. Kune, J. Backes, S. Clark, D. Kramer, M. Reynolds, K. Fu, Y. Kim, and W. Xu, "Ghost talk: Mitigating EMI signal injection attacks against analog sensors," in *Proc. Symp. Security and Privacy*, pp. 145–159, May 2013.
- [5] I. Giechaskiel and K. B. Rasmussen, "Sok: Taxonomy and challenges of out-of-band signal injection attacks and defenses," *arXiv preprint arXiv:1901.06935*, 2019.
- [6] D. B. Yelaverthi, R. Hatch, M. Mansour, H. Wang, and R. Zane, "3-level asymmetric full-bridge soft-switched pwm converter for 3-phase unfolding based battery charger topology," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2737–2743, Sep. 2019.
- [7] M. Clerk, *A treatise on electricity and magnetism*. 01 2010.
- [8] IXYS, *IXD 609 9 Ampere Low Side Ultrafast MOSFET Drivers*, 10 2017.
- [9] Cree, *C3M0120100J Silicon Carbide Power MOSFET*, 04 2017.
- [10] H. Ott, *Electromagnetic Compatibility Engineering*. Wiley, 2011.



(a) Attack Setup (Antenna is not shown.)



(b) Turn on increment of the transistor

Fig. 7: False  $V_{IN}$  injection: turning on switches with IEMI

## APPENDIX B

## MATLAB Simulation Code of the 3LADAB

```

1 function Simulate_3LADAB_DC()
2 close all;
3
4 %% Problem Setup
5
6 % Define OP by choosing grid angle between 0 and 30 degrees
7 OP = 'a'; % Choose a, b, or c
8 if OP == 'a' % Equal input voltages
9     wt_grid = 0; % Grid angle [rad]
10    P.d = [0.999; 0.999; 0.2132]; % Open loop control variables (square)
11 %    P.d = [1; 1; 0.2185]; % Open loop control variables (approx)
12 elseif OP == 'b' % Disequal input voltages
13    wt_grid = 15/180*pi; % Grid angle [rad]
14    P.d = [0.7409; 0.999; 0.2024]; % Open loop control variables (square)
15 %    P.d = [0.7251; 1; 0.2067]; % Open loop control variables (approx)
16 else % OP == 'c' % Extreme disequal input voltage
17    wt_grid = 29.5/180*pi; % Grid angle [rad]
18    P.d = [0.5960; 0.999; 0.2573]; % Open loop control variables (square)
19 %    P.d = [0.6009; 1; 0.2605]; % Open loop control variables (approx)
20 end
21
22 % Calculate grid phase voltages
23 Vph_m = 480*sqrt(2/3); % Grid phase voltage magnitude (V)
24 Va = Vph_m*sin(wt_grid); % Phase A grid voltage (V)

```

```
25 Vb = Vph_m*sin(wt_grid-2/3*pi); % Phase B grid voltage (V)
26 Vc = Vph_m*sin(wt_grid+2/3*pi); % Phase C grid voltage (V)
27
28 % Unfolder action from -pi/6 to pi/6 is fixed
29 Vp = Vc; % Phase C muxed to dc input Vp by Unfolder
30 Vo = Va; % Phase A muxed to dc input Vo by Unfolder
31 Vn = Vb; % Phase B muxed to dc input Vn by Unfolder
32
33 % Define dc input voltages
34 P.Vlp = Vp - Vo; % voltage on P-port input (V)
35 P.Vln = Vo - Vn; % voltage on N-port input (V)
36
37 % Define PFC control loop variables
38 P.Kref = Vp/(-Vn); % Ip/In current ratio reference
39 P.Ksense = 1; % Initialize sensed input current ratio
40
41 % Define output current regulation parameters
42 P.Iout_ref = 100; % Output current reference
43
44 % Define parameters
45 P.Rs = 10e-3; % resistance of resonant tank (ohm)
46 P.Ls = 2.75e-6; % inductance of resonant tank (H)
47 P.Cs = 1.855e-6; % capacitance of resonant tank (F)
48 P.Co = 320e-6; % capacitance of output filter (F)
49 P.Ro = 1.6; % equivalent output resistance (ohms)
50 P.nt = 1/4; % transformer turns ratio (nt2/nt1)
51 P.fsw = 100e3; % switching frequency (Hz)
52 P.Tsw = 1/P.fsw; % switching period (s)
```

```
53
54 % Define number of state, inputs, and controls
55 P.n_x = 3; % number of states (system order)
56 P.n_u = 2; % number of inputs (2 input voltages)
57 P.n_s = 3; % number of switching state variables (3Lprimary+secondary)
58 P.n_d = 3; % number of control variables (3L dutys + secondary phase)
59 P.n_y = 2; % number of outputs (2 input currents)
60
61 % Define control variable limits
62 P.max_duty = 1; % Maximum duty cycle for p and n ports
63 P.min_duty = 0; % Minimum duty cycle for p and n ports
64 P.max_phase = 0.5; % Maximum normalized phase 0.5 => 90deg phase shift
65 P.min_phase = -0.5; % Minimum normalized phase -0.5 => -90deg phase shift
66
67 % Define initial state
68 P.x0 = zeros(P.n_x,1); % Initial state
69
70 % Define simulation step size, length, and time
71 P.N = 500; % Number of switching cycles to simulate
72 P.n = 1000; % Number of high res steps within one switching cycle
73 P.dt = P.Tsw/P.n; % Simulation high res time step
74 P.tf = P.N*P.Tsw; % Final time of simulation
75 t_mat = [0:P.dt:P.tf]; % Simulation time at f_sw (control update)
76 P.len = length(t_mat); % Number of simulation data points
77 t_mat_Ts = [0:P.Tsw:P.tf]; % Simulation time at P.n*f_sw (high res)
78 P.len_Ts = length(t_mat_Ts); % Number of data points saved at switching
    frequency
79
```

```
80 % Allocate simulation vectors
81 x_mat = zeros(P.n_x,P.len); % High res sampled state variables
82 s_mat = zeros(P.n_s,P.len); % High res sampled modulation [only needed
    for debug/plots]
83 y_mat = zeros(P.n_y,P.len); % High res sampled output variable
84 x_mat_Ts = zeros(P.n_x,P.len_Ts); % Tsw sampled state variables
85 u_mat_Ts = zeros(P.n_u,P.len_Ts); % Tsw sampled input voltage
86 d_mat_Ts = zeros(P.n_d,P.len_Ts); % Tsw sampled control variable
87 y_mat_Ts = zeros(P.n_y,P.len_Ts); % Tsw averaged input currents
88
89 % Load initial state into state simulation vectors
90 x_mat(:,1) = P.x0; % Initialize state
91 x_mat_Ts(:,1) = P.x0; % Initialize state
92
93 % Create indices vectors for writing high res state and output
94 x_mat_ind = [1:P.n]+1;
95 y_mat_ind = 1:P.n;
96
97 % Set up handles for updating input and control variables
98 u = @(t) update_input(t, P); % Set the input voltages
99 d = @(t, x, u) update_control(t, x, u, P); % Set the control variables
100
101 % Choose the square wave modulation or fundamental harmonic
102 % approximation for changing s variables
103 % Fundamental harmonic approximation is much easier for ode45 to solve
104 % fast and accurately; however, ode23s is better at solving the square
105 % wave modulation accurately
106 s = @(t, d) update_s_square(t, d, P); % Set the switching state
```

```

107 %     s = @(t, d) update_s_approx(t, d, P); % Set the switching state
108
109
110 %% Simulate P.N number of switching periods
111 tic;
112 for k = (1:P.N)+1
113     % Define simulation time
114     t_k1 = t_mat_Ts(k-1); % start of switching period
115     t_k = t_mat_Ts(k); % end of switching period
116     t_sim = linspace(t_k1,t_k,P.n); % simulation time vector
117
118     % Extract initial state
119     x_k1 = x_mat_Ts(:,k-1); % state at start of switching period
120
121     % Calculate input voltage and control
122     u_k1 = u(t_k1); % input voltage at start of switching period
123     d_k1 = d(t_k1,x_k1,u_k1); % control variables for switching period
124
125     % Define handle for dynamics using constant u and constant d
126     f_sim = @(t,x)f_3LADAB(t, x, u_k1, s(t,d_k1), P);
127
128     % Simulate 1 switching period
129 %     [~,x_sim] = ode45(f_sim,t_sim,x_k1); % Use this for s =
update_s_approx
130     [~,x_sim] = ode23s(f_sim,t_sim,x_k1); % Use this for s =
update_s_square
131
132     % Store state data in state simulation vectors

```

```
133     x_mat_Ts(:,k) = x_sim(end,:)' ; % record states at Tsw intervals
134     x_mat(:,x_mat_ind) = x_sim' ; % record high res sampling of the states
135     x_mat_ind = x_mat_ind + P.n;
136
137     % Store input and control data in simulation vectors
138     u_mat_Ts(:,k-1) = u_k1; % record input voltage for Tsw simulation
139     d_mat_Ts(:,k-1) = d_k1; % record control variable for Tsw simulation
140
141     % Calculate high res switching state and output simulation vectors
142     for i = 1:P.n
143         % Extract state and time at index i
144         ind = i+(k-2)*P.n; % high res index
145         t_i = t_mat(ind); % high res time
146         x_i = x_mat(:,ind); % high res state at t_i
147         i_Ls_i = x_i(1); % high res tank current at t_i
148
149         % Calculate and extract high res switching state
150         s_i = s(t_i,d_k1); % high res sw state
151         slp_i = s_i(1); % P-port sw state
152         sln_i = s_i(2); % N-port sw state
153
154         % Calculate simulation output (P and N port currents)
155         Ip_i = P.nt*slp_i*i_Ls_i; % high res P-port current at t_i
156         In_i = P.nt*sln_i*i_Ls_i; % high res N-port current at t_i
157
158         % Store high res switching state and output simulation vectors
159         s_mat(:,ind) = s_i; % record high res sw state [only needed for
            debug/plots]
```

```
160         y_mat(:,ind) = [Ip_i; In_i]; % record high res sw state
161     end
162
163     % Perform averaging over switching period on input currents
164     y_mat_Ts(:,k) = mean(y_mat(:,y_mat_ind),2); % average high res input
        current
165     y_mat_ind = y_mat_ind + P.n;
166
167 end
168 toc;


---


169 %% Post Simulation
170
171 % Extract terminal time and state
172 tf = t_mat_Ts(end);
173 xf = x_mat(:,end)
174
175 % Calculate terminal input and control values
176 uf = u(tf);
177 df = d(tf, xf, uf)
178
179 % Extract terminal output
180 yf = y_mat_Ts(:,end)
181
182 % Compare reference vs. measured signal for PFC loop
183 Kref = P.Kref
184 Ksense_terminal = yf(1)/yf(2)
185
186 % Compare reference vs. measured signal for output loop
```

```
187     Iout_ref = P.Iout_ref
188     Iout_terminal = xf(3)/P.Ro
189 end
190
191 %% f_3LADAB — Define dynamics for 3LADAB converter
192 % Dynamics are defined for each state individually. The dynamics could be
193 % formed in state space representation however, the A and B matrices are
194 % time varying due to their dependence on the switching state s.
195 function xdot = f_3LADAB(t,x,u,s,P)
196
197     % Define parameters
198     Rs = P.Rs;
199     Ls = P.Ls;
200     Cs = P.Cs;
201     Co = P.Co;
202     Ro = P.Ro;
203     nt = P.nt;
204
205     % Extract state
206     i_Ls = x(1); % HF resonant inductor current
207     v_Cs = x(2); % HF resonant capacitor voltage
208     v_Co = x(3); % DC output capacitor voltage
209
210     % Extract the input
211     v1p = u(1); % P-port soft dc-link voltage
212     v1n = u(2); % N-port soft dc-link voltage
213
214     % Extract the switching state
```

```

215     s1p = s(1); % P-port switching state
216     s1n = s(2); % N-port switching state
217     s2 = s(3); % Secondary port switching state
218
219     % Calculate dynamics
220     xdot = zeros(P.n_x,1);
221     xdot(1) = -(Rs/Ls)*i_Ls - (1/Ls)*v_Cs - (s2/Ls)*v_Co + (s1p/Ls)*nt*v1p + (
                s1n/Ls)*nt*v1n;
222     xdot(2) = (1/Cs)*i_Ls;
223     xdot(3) = (s2/Co)*i_Ls - (1/(Co*Ro))*v_Co;
224
225 end
226
227 %% update_input — Update input voltages
228 % Currently this function is not doing much because the input voltage is
229 % constant for dc simulations; however, function was left in because it is
230 % used in the ac simulations
231 function u = update_input(t, P)
232     u = [P.V1p; P.V1n];
233 end
234
235 %% update_control — Update control variables (Duty cycles and phase shift)
236 % This function updates the duty cycle for the p-port (dp), duty cycle
237 % for the n-port (dn), and the phase shift from rising edge of the primary
238 % ports and the secondary port. For now there is no controller implemented
239 % so the dutys and phase are fixed.
240 function d = update_control(t, x, u, P)
241

```

```
242 % Set control variables to open loop values
243 dp = P.d(1);
244 dn = P.d(2);
245 dphi = P.d(3);
246
247 % Saturate the control variables
248 dp = min(dp,P.max_duty);
249 dp = max(dp,P.min_duty);
250 dn = min(dn,P.max_duty);
251 dn = max(dn,P.min_duty);
252 dphi = min(dphi,P.max_phase);
253 dphi = max(dphi,P.min_phase);
254
255 % Load control variables into output vector
256 d = zeros(3,1);
257 d(1) = dp;
258 d(2) = dn;
259 d(3) = dphi;
260 end
261
262 %% update_s_square — Updates the switching state variables w/ Square waves
263 % This function uses the duty cycles and phase shifts to implement
264 % modulation at the switching frequency. Square wave modulation is more
265 % accurate than the fundamental approximation because it captures all the
266 % harmonics that are actually applied to the tank when driving it with a
267 % switching H-bridges. However, this modulation has sharp edges and makes
268 % the simulation stiff. This leads to ode45 having bad performance
269 % while ode23s solves this much better at the cost of speed.
```

```
270 function s = update_s_square(t, d, P)
271
272 % Extract paramters
273 Tsw = P.Tsw;
274
275 % Normalize time
276 t_norm = mod(t,Tsw)/Tsw;
277
278 % Extract duty
279 dp = d(1);
280 dn = d(2);
281 dphi = d(3);
282
283 % Normalize the phase shifted counter for secondary modulation
284 t2_norm = mod(t-dphi*Tsw/2,Tsw)/Tsw;
285
286 % Apply dp to switching state for p-port
287 if (t_norm<(dp/2))
288     s1p = 1;
289 elseif (t_norm<=(1/2))
290     s1p = 0;
291 elseif (t_norm<=((dp+1)/2))
292     s1p = -1;
293 else
294     s1p=0;
295 end
296
297 % Apply dn to switching state for n-port
```

```
298     if (t_norm<(dn/2))
299         s1n = 1;
300     elseif (t_norm<(1/2))
301         s1n = 0;
302     elseif (t_norm<((dn+1)/2))
303         s1n = -1;
304     else
305         s1n=0;
306     end
307
308     % Apply full duty to secondary but using phase shifted counter
309     if (t2_norm<0.5)
310         s2 = 1;
311     else
312         s2 = -1;
313     end
314
315     % Load switching state into output vector
316     s = zeros(3,1);
317     s(1) = s1p;
318     s(2) = s1n;
319     s(3) = s2;
320 end
321
322 %% update_s_approx — Updates the switching state variables w/ Fundamental
    Harmonic Approximation
323 % This function uses the duty cycles and phase shifts to implement
324 % modulation at the switching frequency. The fundamental harmonic
```

```
325 % approximation replaces the square wave signal with fundamental sinusoidal
326 % from Fourier analysis of a square wave. The resulting approximation is
327 % close the square wave modulation because the high quality factor of the
328 % tank responds mostly to the fundamental while attenuating the higher
329 % order harmonics. This approximation is still less accurate that square
330 % wave modulation; however, it removes the stiffness from the simulation
331 % and allows ode45 to have an accurate and fast solution.
332 function s = update_s_approx(t, d, P)
333
334     % Extract paramters
335     fsw = P.fsw;
336
337     % Extract duty
338     dp = d(1);
339     dn = d(2);
340     dphi = d(3);
341
342     % Calculate angles
343     alpha_lp = dp*pi;
344     alpha_ln = dn*pi;
345     phi_edge = dphi*pi;
346
347     % Calculate switching states at time t using fundamental approximation
348     wt = 2*pi*fsw*t;
349     s1p = 4/pi*sin(alpha_lp/2)*sin(wt+(pi-alpha_lp)/2);
350     s1n = 4/pi*sin(alpha_ln/2)*sin(wt+(pi-alpha_ln)/2);
351     s2 = 4/pi*sin(wt-phi_edge);
352
```

```
353     % Load switching state into output vector
354     s = zeros(3,1);
355     s(1) = s1p;
356     s(2) = s1n;
357     s(3) = s2;
358 end
```