

THE FIELD-PROGRAMMABLE GATE ARRAY DESIGN OF THE GRIDDED
RETARDING ION DISTRIBUTION SENSOR

by

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ABSTRACT

The Field-Programmable Gate Array Design of the Gridded Retarding Ion Distribution
Sensor

by

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This thesis project is concerned with two instruments that are used to measure plasma in the low-Earth orbit space environment. These two instruments are the Retarding Potential Analyzer (RPA), and the Ion Drift Meter (IDM). Work has been done to combine the functionality from both of these instruments into one unit suitable for a small satellite in terms of size, power, and mass. An electrical and mechanical design has already been completed to this end and this new instrument is called the Gridded Retarding Ion Distribution Sensor (GRIDS). The focus of this thesis is completing a field-programmable gate array (FPGA) design for this instrument.

This document presents the design of the FPGA code along with the testing of that code. The design includes two modes of operation, referred to as the 50/50 mode and the 10 Hz mode. Also, descriptions of various systems critical to proper instrument function, such as the data output system and instrument ranging system, are included. Testing shows that the instrument performs as desired.

(50 pages)

PUBLIC ABSTRACT

The Field-Programmable Gate Array Design of the Gridded Retarding Ion Distribution
Sensor

Anthony P. Swenson

Mankind's ability to predict weather on earth has been greatly enhanced by new instrumentation technology. Similarly, mankind's ability to predict space weather benefits from new technologies. Just as increasing the amount of atmospheric measurements on earth heightened mankind's ability to predict Earth weather, many scientists expect that expanding the amount of plasma measurements in space could be key to enhancing mankind's ability to predict space weather. Small satellites are one of these new technologies that have the potential to greatly enhance our ability to predict space weather. Utilizing many low-cost small satellites allows scientists to take data from more locations than possible with a few high-cost large satellites.

Two instruments that have historic use measuring plasma are the Retarding Potential Analyzer and the Ion Drift Meter. Previous work has been done to combine the functionality from both of these instruments into one unit suitable for a small satellite in terms of size, power, and mass. An electrical and mechanical design has been completed to this end and this new instrument is called the Gridded Retarding Ion Distribution Sensor. This thesis describes the design and testing of the FPGA code that runs this new instrument.

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CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 Plasma the in Near-Earth Environment

Plasma makes up as much as 99% of the mass in the known universe. Plasma is hot ionized gas in which positive ions and free electrons move in complicated ways. The ionosphere, a portion of the Earth's atmosphere, is characterized by the plasma it contains [1].

Careful consideration of the interactions between space systems and plasma is critical for the success of space missions due to the harmful effects plasma can have on those systems. These effects include degradation of materials, unintentional charging, thermal changes, radiation damage, communication impediment, electrostatic discharges, and more [2]. As new instruments and techniques that measure plasma are developed, spacecraft system engineers are better able to plan for these interactions.

Periods of high solar activity causes storms in the ionosphere that severely degrade communication systems used by both military personnel and civilians [1]. The signal degradations caused by these storms affect a broad set of communication systems, including satellite communications, global positioning system (GPS) location, and high frequency radio. Scientists can use data generated by instruments measuring the plasma in the ionosphere to develop models of radio communications loss [3].

Two instruments have a long history of being used to make in-situ measurements of ions that make up plasma in the ionosphere. Those two instruments are the Retarding Potential Analyzer (RPA) [4], and the Ion Drift Meter (IDM) [5]. Together these instruments allow in-situ measurements of ion density, velocity, species ratio, and temperature [6].

1.2 History of the Retarding Potential Analyzer

The key components of an RPA include wire-mesh grids to which a voltage is applied, a current collector plate, and an opening in the direction of motion (ram direction) of the satellite. A visualization of an RPA is shown in Fig. 1.1. The instrument is placed on a spacecraft such that the opening is in line with the ram direction of the satellite. The grids shown in Fig. 1.1 are not all necessary for an RPA to function, as some RPAs don't use an aperture grid and some only use one retarding grid. A negative voltage is applied to the suppressing grid to repel all electrons. The positive voltage applied to the retarding grids sweeps across a range of values, reducing the number of ions that make it to the ion collection plate as it is increased. This is because as the voltage is increased fewer incident ions have the energy required to penetrate the grid and many will instead be repelled [7]. This interaction creates a system where all ions below a minimum retarding velocity get repelled from the instrument and don't make it to the current measuring ion collection plate.

A current-voltage plot (I-V curve) can be made using the current measured on the ion collection plate for a set of voltages applied to the retarding grids. From the I-V curve much can be learned about the ions in a plasma. For example, the magnitude of the derivative of the I-V curve is related to the ion energy distribution [8]. Additionally, using careful curve-fitting, the ion concentration, temperature, mass ratios, and relative speed of the ions can be inferred from the I-V curves [7].

The equation describing an I-V curve as a function of physical plasma parameters can be derived from the current density equation [9]. The current density, J , resulting from a plasma where the j^{th} particle has charge q_j collected by a flat plate is given by equation (1.1) where v_x , v_y and v_z are the components of the velocity vector of the ion and $f(\dots)$ is a distribution function of those components of the velocity vector. The velocity vector component v_z is chosen to be defined as the velocity in the negative of the ram direction of the satellite.

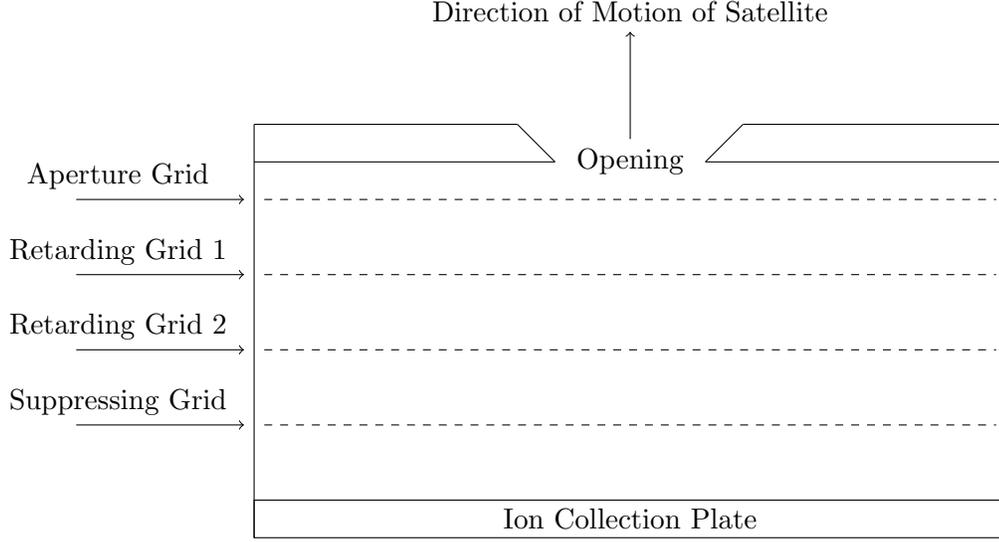


Fig. 1.1: Retarding Potential Analyzer Design

$$J = q_j \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} v_z f_j(v_x, v_y, v_z) d_{v_z} d_{v_y} d_{v_x} \quad (1.1)$$

If we consider the application of an RPA in a plasma with k different species of ions, a minimum retarding velocity v_{sj} , and ions with a Maxwellian velocity distribution we can expand (1.1) to (1.2).

$$J = \sum_{j=1}^k q_j n_j \left(\frac{m_j}{2\pi k_b T} \right)^{\frac{3}{2}} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \int_{v_{sj}}^{\infty} v_z \exp\left(\frac{-m_j(v_x^2 + v_y^2 + (v_z + v_d)^2)}{2k_b T_j} \right) d_{v_z} d_{v_y} d_{v_x} \quad (1.2)$$

In (1.2) q_j is the charge of the j^{th} species of ion in the plasma, n_j is the number density of the j^{th} species, m_j is the mass of the j^{th} species, T_j is the temperature of the j^{th} species, v_d is the drift velocity of the plasma as a whole, k_b is the Boltzmann Constant, and v_{sj} is the retarding velocity where $v_{sj} = \sqrt{\frac{2q_j}{m_j}(\phi_o - \phi_p)}$ and ϕ_o is the grid potential and ϕ_p is the plasma potential.

Completing this integration gives an expression for the current density. Using that expression and considering the current collected by a plate of area A_c leads to the final

equation; that the current, I , measured in an RPA due to a plasma is (1.3).

$$I = \frac{1}{2}v_d A_c \sum_{j=1}^k q_j n_j \left[1 + \operatorname{erf} \left(\sqrt{\frac{m_j}{2k_b T_j}} (v_{sj} + v_d) \right) + \frac{1}{v_d} \sqrt{\frac{2k_b T_j}{\pi m_j}} \exp \left(-\frac{m_j}{2k_b T_j} (v_{sj} + v_d)^2 \right) \right] \quad (1.3)$$

1.3 History of The Ion Drift Meter

The key components of an IDM consists of an opening placed in the ram direction of the satellite, an aperture grid with a positive voltage applied to it, a suppressing grid with a negative voltage applied to it, and an ion collector plate. However, the collector plate is segmented in the IDM as seen in Fig. 1.2. The aperture grid is used to screen out low mass ions, making the interpretation of IDM data easier.

The RPA is able to measure the ion drift velocity component in the look direction of the instrument (ram direction of the satellite), but cannot measure the ion drift velocity components in the other two orthogonal directions [6]. This is where the IDM can be of use. The ratio of currents to different collector plate segments allows direct calculation of the ion arrival angle [5].

The total current collected by a segment of the ion collection plate is given by (1.4), where q is the charge of incoming ions, N is the ion density, A is the area of the plate, χ is the transparency of the grid stack, and V is the velocity of the incoming particles perpendicular to the plate.

$$I = qNA\chi V \quad (1.4)$$

Understanding that the current to any segment of the collector plate is proportional to the illuminated area leads to an expression for the ratio of two currents [9]. That ratio is based on the physical parameters θ , W , and D as given in (1.5). θ is the arrival angle of the plasma, W is the width of the instrument opening, and D is the effective depth of the instrument. A visualization of these parameters is shown in Fig. 1.3. This equation solved

for θ is given in (1.6).

$$R = \frac{I_1}{I_2} = \frac{\frac{W}{2} + D \tan(\theta)}{\frac{W}{2} - D \tan(\theta)} \quad (1.5)$$

$$\theta = \tan^{-1} \left(\frac{W(1 - R)}{2D(1 + R)} \right) \quad (1.6)$$

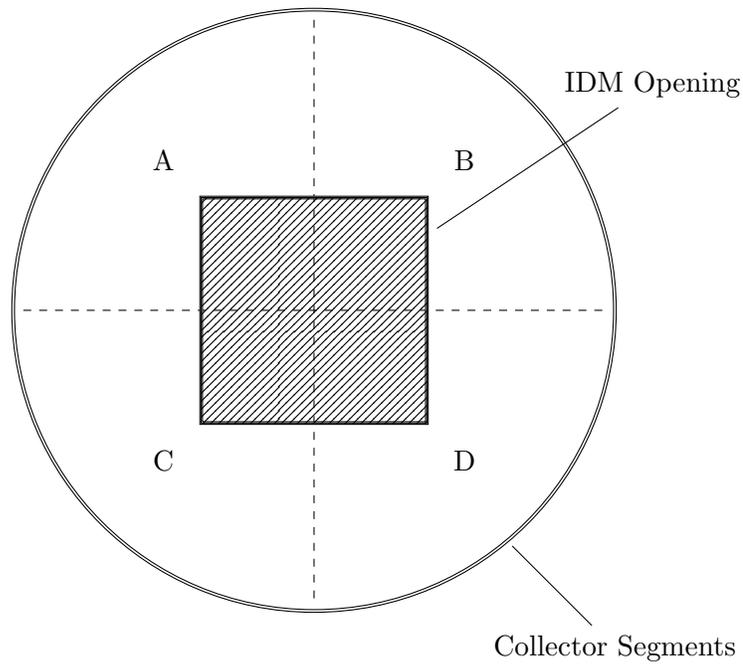


Fig. 1.2: Ion Drift Meter Collector Segments

1.4 Small Satellites

Historically, satellites that have included RPAs and IDMs in their instrumentation packages have traditionally been large satellites with substantial budgets. Some such missions are the Dynamics Explorer, [10], Communications/Navigation Outage Forecasting System [11], and Defense Meteorological Satellite Program (DMSP) satellites [12].

Smaller cube satellites (CubeSats) have recently become popular as an alternative to

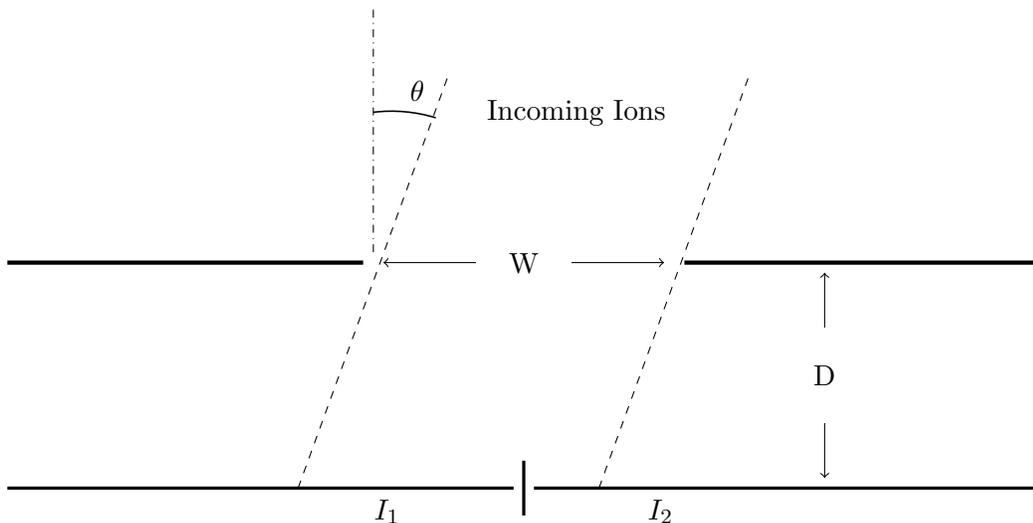


Fig. 1.3: Ion Drift Meter Parameters

big satellites for conducting meaningful science missions at a lower cost. Some missions, such as the Dynamic Ionosphere CubeSat Experiment (DICE) mission and Radio Aurora Explorer mission [13], have proven the worth of the CubeSat model. Another benefit of using CubeSats is that constellations of CubeSats (two or more) can be sent into orbit for a fraction of the cost of a constellation of large satellites. Constellations can provide a more detailed view of plasma processes with fewer spatial or temporal gaps in the collected data. For these reasons, equipping CubeSats with plasma measurement instruments has become an important area of research.

1.5 Previous Work Done on GRIDS

Mechanical and electrical design work has been previously done to combine the IDM and RPA instrument functionality into one lightweight, small, low-power unit ideal for small satellites [14]. This new instrument is called the Gridded Retarding Ion Distribution Sensor (GRIDS). Testing has shown that the design, while saving on power and space, does not compromise much in terms of instrument accuracy relative to using two separate instruments. A picture of the built sensor head is shown in Fig. 1.4.

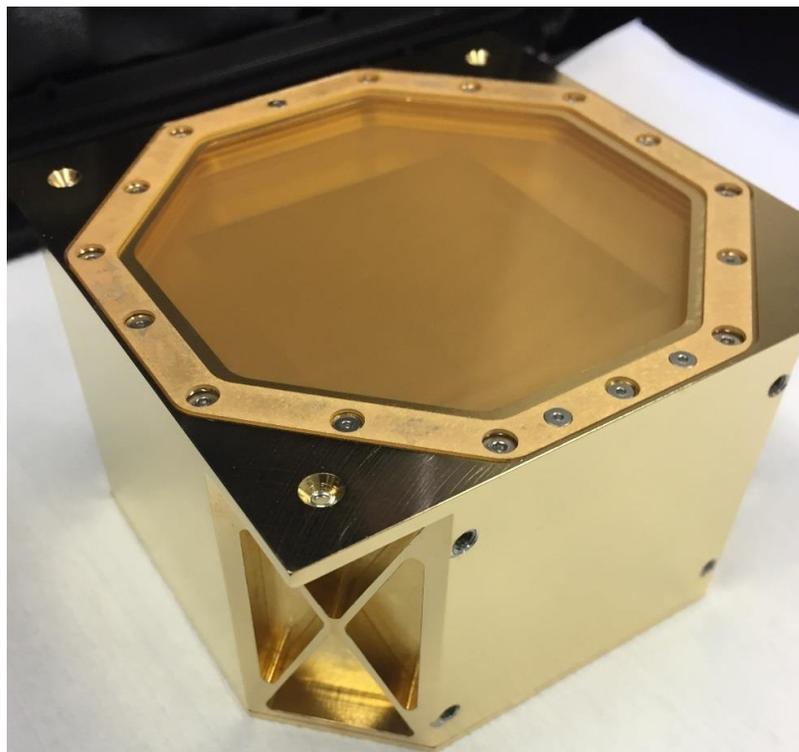


Fig. 1.4: The GRIDS Sensor Head

The electronics of GRIDS have already been picked out and have been placed on a circuit board. A picture of these electronics is shown in Fig. 1.5. The FPGA chosen for GRIDS is the AGLN250V5-VQG100 produced by the Microsemi Corporation. A quad channel DAC, Linear Technology's LTC2604, is used to produce the grid voltages GRIDS requires to operate correctly. To measure the small currents encountered in normal operations, the Texas Instrument's DDC114 chip was chosen. The DDC114 chip is a 20-bit precision quad channel current measurement device that takes measurements using a charge accumulation method.

1.6 Project Goals

The goal of this thesis is to develop and test a Field Programmable Gate Array (FPGA) design that provides the necessary instrument functionality. This includes sending out data that GRIDS produces through a standard protocol with a well-defined packet structure,

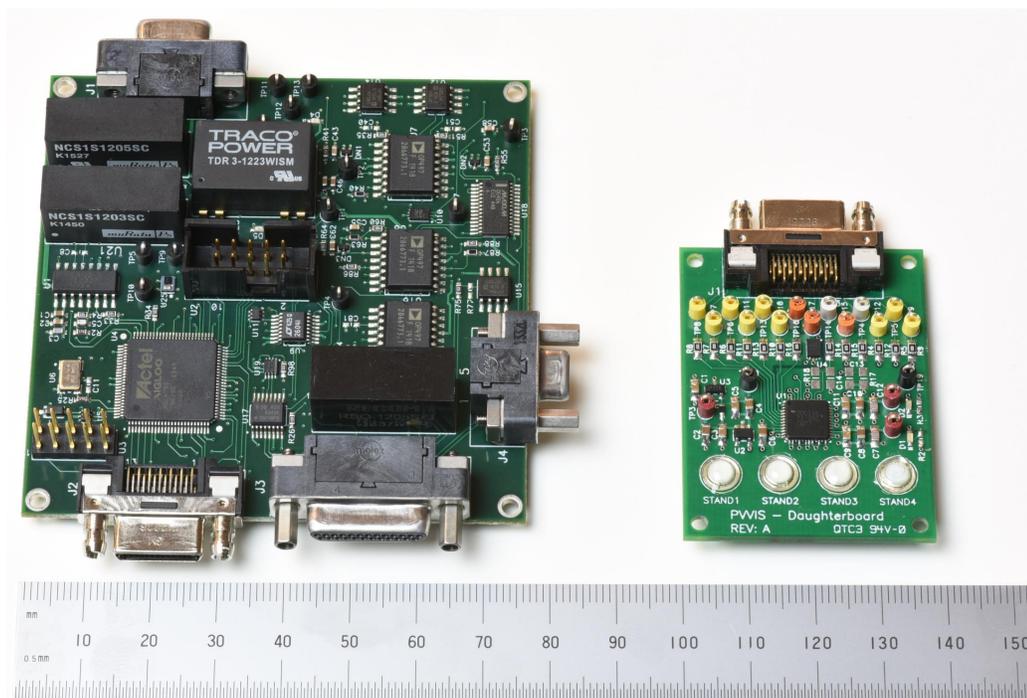


Fig. 1.5: GRIDS Electronics

controlling the grid voltage levels, and implementing current sensing.

The old debug code that was previously developed operates in a very limited capacity as can be seen on the left side of Fig. 1.6. The purpose of the debug code was to test the basic functionality of the instrument and only implemented the current measurement part of the design along with limited communications through a debug port.

The extent that the new prototype code operates is shown on the right side of Fig. 1.6. The prototype code also implements current measurement, but adds automatic ranging functionality to it. The prototype code implements a well defined packet structure and outputs those packets over a RS-422 communication bus. The prototype code additionally provides controls for the grid voltages. These features provide full instrument functionality and their design will be discussed in detail in the following chapters.

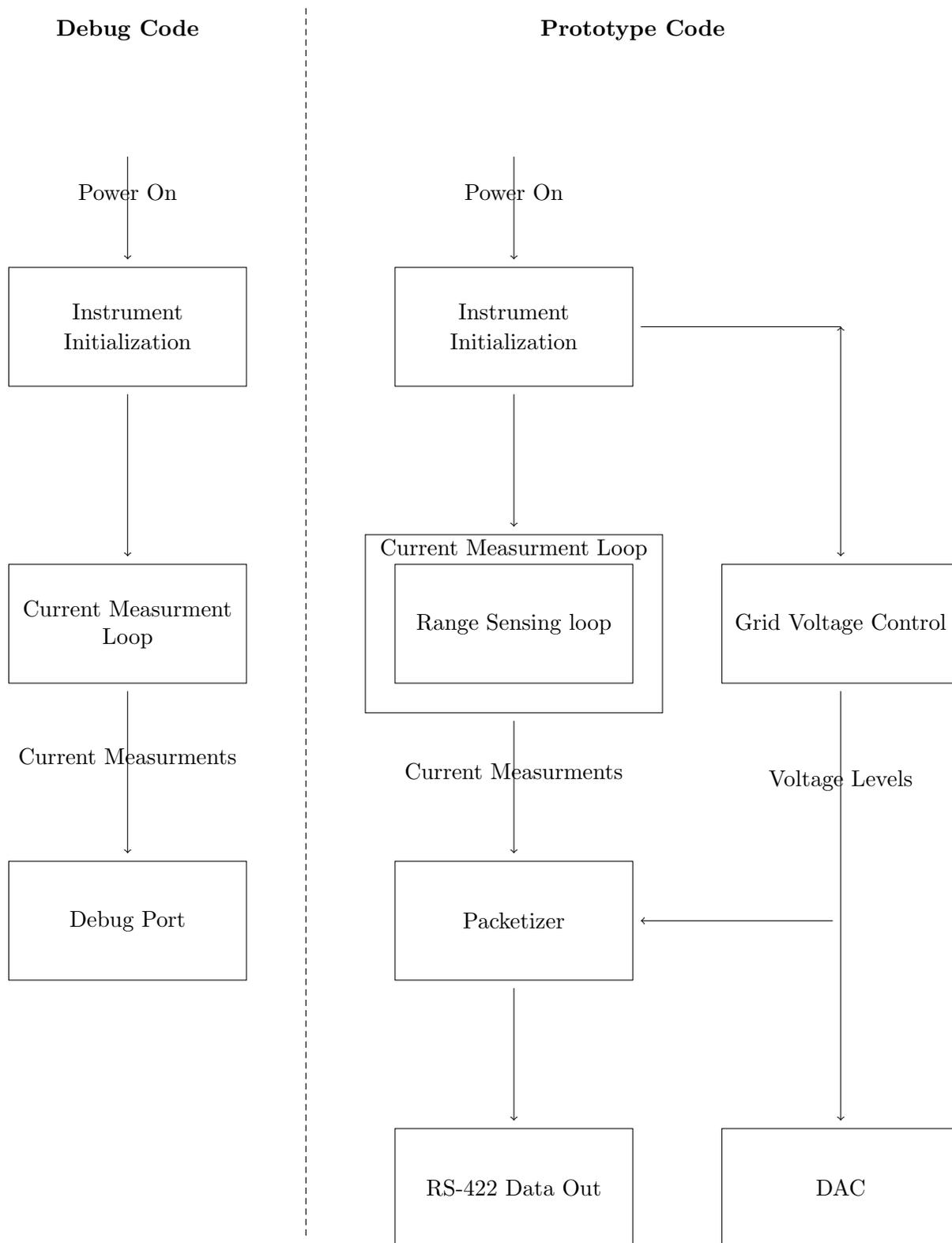


Fig. 1.6: Debug code functionality vs. Prototype code functionality

CHAPTER 2

FPGA DESIGN

2.1 Design Overview and Requirements

GRIDS takes measurements of plasma in two different ways, GRIDS enters RPA mode to take the same measurements an RPA would, and IDM mode to take the same measurements an IDM would. In the 50/50 mode of operation, GRIDS spends one half second in RPA mode, then the subsequent half second in IDM mode, then repeats indefinitely. Much of the operation of the instrument is the same during RPA mode and IDM mode, with the exception of the grid voltages. RPA mode requires stepping grid voltages while IDM mode does not. During both RPA and IDM modes, GRIDS takes current measurements, determines if it needs to range, and reports the data to the packetizer system. The packetizer system places the data into a well-defined packet structure and outputs that packet to an RS-422 port. The output RS-422 bus would be connected to a spacecraft's on-board computer in normal operation. A list of requirements is given in the list below.

1. The grid voltages are set to the correct level during IDM mode.
 - Aperture Grid: Non-zero constant
 - Retarding Grid 1: Zero volts
 - Retarding Grid 2: Zero volts
 - Suppressing Grid: Negative twelve volts

2. The grid voltages are set to the correct level during RPA mode.
 - Aperture Grid: Zero volts
 - Retarding Grid 1: Ramping voltage
 - Retarding Grid 2: Ramping voltage

- Suppressing Grid: Negative twelve volts
3. Ensure current measurements don't overlap from one voltage step to the next during RPA mode.
 4. Ignore current measurements that take place during voltage rise time during RPA mode.
 5. Report 100 current measurements in the telemetry every second; 50 in RPA mode and 50 in IDM mode.
 6. Implement an automatic current range sensing system.
 7. Define a packet structure for data output from the system.
 8. Follow the defined packet structure when outputting data from the system.
 9. Create code that communicates through the standard RS-422 protocol.
 10. Ensure the full code can be implemented on the FPGA.
 11. Implement a secondary mode for GRIDS based on taking 10 sets of measurements a second.

2.2 FPGA Parameters

An FPGA was chosen as the computing chip for GRIDS because of the accurate timing FPGAs are known for, the lack of complex math operations required to run the instrument, and the available low-power FPGA options. The FPGA that GRIDS uses is the AGLN250V5-VQG100 produced by the Microsemi Corporation. This FPGA is a part of Microsemi's IGLOO nano device line. The space available on the AGLN250V5-VQG100 is 6144 core cells, eight 4608-Bit RAM blocks, and 68 input/output ports. All of the FPGA code for GRIDS needs to be designed such that it fits within these resource constraints.

2.3 Grid Voltage / DAC

GRIDS has four electrically isolated grids that each need to be driven separately. A quad channel DAC, Linear Technology's LTC2604, is used to produce these grid voltages. These grids operate differently depending on the instrument mode (RPA or IDM). A concept of operations for the instrument is shown in Fig. 2.1. This figure details how the four different grid voltages operate during RPA and IDM modes, while additionally showing that the instrument runs in RPA mode for half a second, then IDM mode for half a second, then repeats.

During RPA mode: the aperture grid is set to zero volts, retarding grids 1 and 2 both step 50 times at even intervals between 0 and 12 volts, and the suppressing grid is set to -12 volts.

During IDM mode: the aperture grid is set to a non-zero constant voltage, retarding grids 1 and 2 are set to zero volts, and the suppressing grid is set to -12 volts.

2.4 Current Sensing / DDC chip

GRIDS measures four currents, one for each segment of the segmented current collector. These four current measurements are used separately to reconstruct IDM data and added together into one measurement to reconstruct RPA data. Texas Instrument's DDC114 chip is a 20 bit precision quad channel current measurement device. The DDC114 chip measures current by charging a capacitor for an amount of time, the integration time. The level of charge on the capacitor along with the integration time are used to determine the average current measured over that time. As a result of the DDC114 chip using charge accumulation to measure currents, the charge accumulators saturate at lower current values with a long integration timer than they would if the integration timer was short.

The DDC114 chip can only measure two currents at a time. The DDC_CONV signal (labeled Integration Channel) shown in Fig. 2.2 indicates both which two currents are being measured and how long the integration timer is. In order to get a measurement of all four currents the DDC_CONV signal needs to be both high and low for the same time, so all four currents are measured for the same integration time.

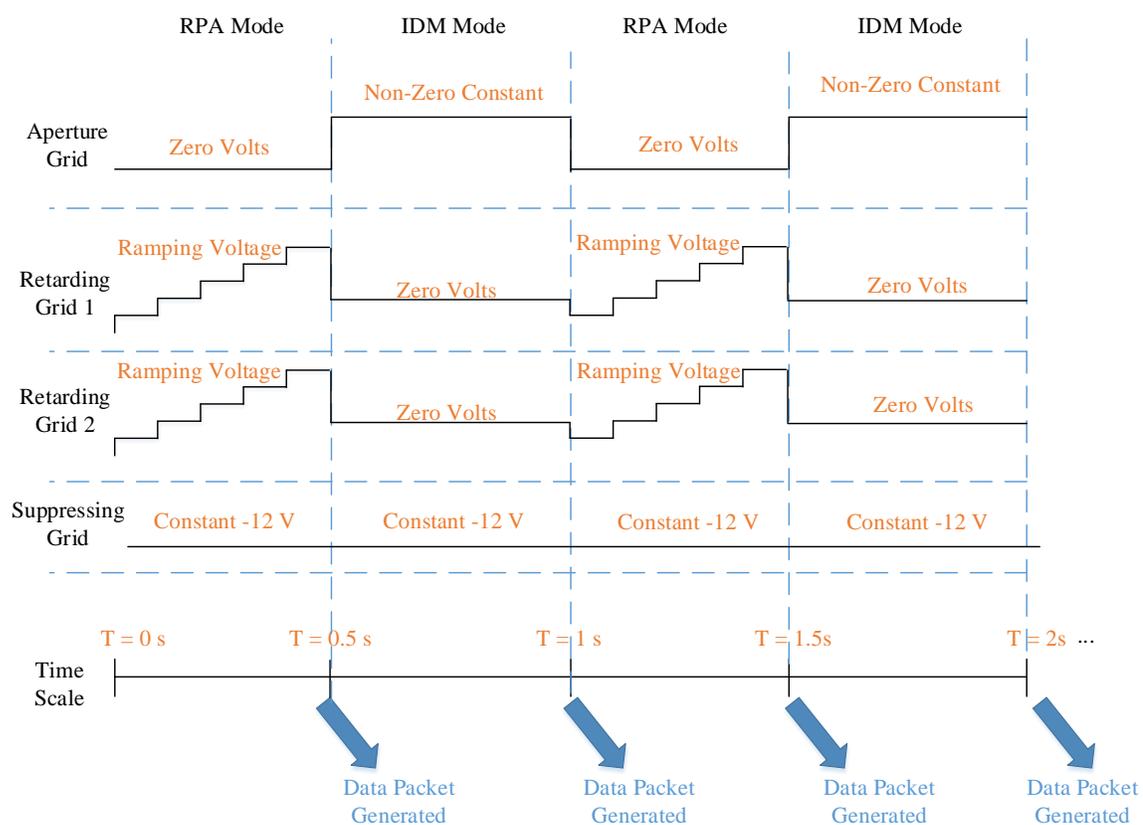


Fig. 2.1: Voltage Grid DAC Function

After the DDC_CONV signal changes, there is a delay of 1380 clocks (from the clock running the DDC114 chip) before the two currents the DDC114 chip just measured are placed in the output data registers. The DDC_DValid signal then pulses indicating that the digitized current values are ready to be read out of the data registers. The DDC114 chip's data register is 80-bits long and only updates the relevant 40-bits when the DDC_Dvalid signal pulses. Because of this, the instrument waits until after the DDC_CONV signal has gone high and low before reading out the data to ensure all four current measurements are present in the data registers.

When taking current measurements, the first 25% of the step time is discarded to account for rise time of the grid voltage. While the voltage rise time is only relevant in RPA mode, both RPA and IDM modes discard the first 25% of the step time for the sake of consistency. Then the instrument switches the DDC_CONV signal with precise timing a specified amount of times depending on the range the instrument is in, which is described in Table 2.1. The currents GRIDS is expected to encounter in operation have a larger range than the DDC114 chip can measure in any one configuration. To account for this, GRIDS is programmed with an automatic ranging feature. The ranging is possible because a shorter integration timer can measure a larger current than a longer integration timer at the trade-off of a higher noise floor.

The three different implemented ranges are listed in Table 2.1. A depiction of the low range is shown in Fig. 2.2, and high in Fig. 2.3. The Data Valid signal has been altered in these figures from what it would normally look like to only trigger when a full set of 4 current measurements are available. A large current jump is expected when switching from RPA to IDM mode because the grid voltages jump from a very high level to a relatively low level, which allows a lot more ions through to the collector plate. To account for this GRIDS automatically ranges to the highest range when it switches to IDM mode.

Because the DAC step timing doesn't change, it is possible to take multiple current measurements at the higher ranges. Currently the last two measurements are the ones reported in the telemetry.

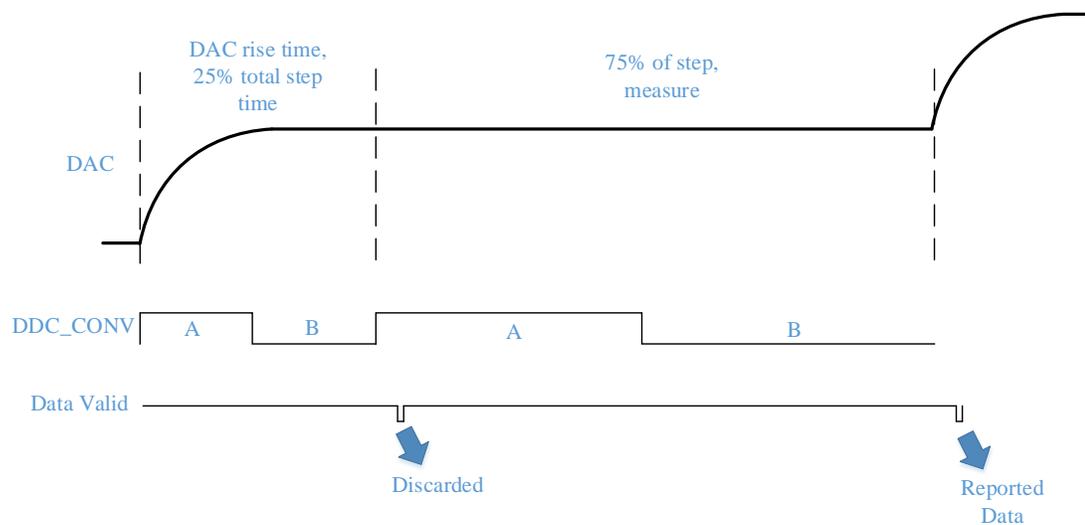


Fig. 2.2: Current measuring functionality at a slow measurement rate

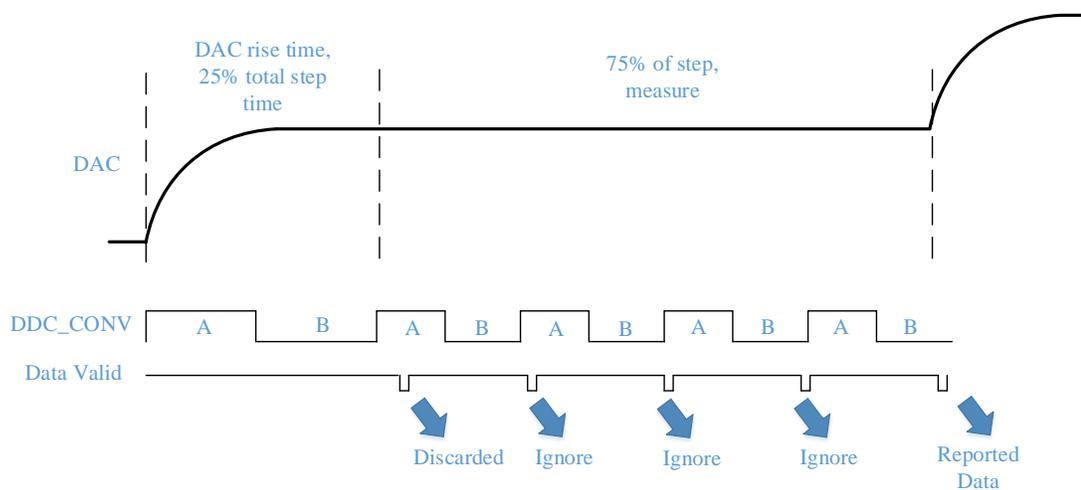


Fig. 2.3: Current measuring functionality at a fast measurement rate

Table 2.1: List of ranges for current sensing.

Range	Current Measurable	Time spent per DDC_CONV signal	# of DDC_CONV toggles
Low	0-35nA	3.73 ms	2
Medium	20-90nA	1.87 ms	4
High	70-300nA	0.94 ms	8

2.5 Packetizer

The Packetizer code takes the data produced by GRIDS and orders it into packets. Having well defined data packets is common practice for space instruments since many on-board computers on spacecraft require it. The on-board computer is responsible for, among other things, taking data output by all of the spacecraft’s various subsystems and organizing it into a format ready for radio downlink. Packets of fixed length or packets that contain information about their length in the header make this job much easier for the on-board computer. These packets are then parsed on the ground to retrieve the data produced by the subsystems.

The packet structure for GRIDS is defined in figure Fig. 2.4. Each packet always starts with a header which begins with a sync word. The sync word is 4 bytes, and is meant to help later packet parsing efforts. The next 4 bytes is the Packet Number Counter, which is a simple counter that is incremented by 1 every time a packet is generated by GRIDS. Next is the Packet Length, which holds information on how many bytes make up the whole packet. The rest of the header is made up of eight 2-byte values that contain various housekeeping information, such as voltage levels and temperature levels. The last of these 2-byte values labeled DDC_RANGE contains information on the DDC114 current sensor chip that is critical for converting the raw data into currents.

After the header is the data portion of the packet, which makes up the bulk of the packet. The data portion is made up of many 20-byte chunks that contain pertinent information for a single current measurement. First, the value of all four grid voltage levels is reported in a series of four 2-byte values. Then the next 10 bytes are used for the raw DDC114 chip data values. Because the DDC114 chip has 20-bit resolution and we are

measuring four currents there is a total of 80 bits of data reported every time a current measurement is taken. These four 20-bit measurements are placed one next to the other in the 10 byte data chunk as shown in Fig. 2.5. The last item is a 2-byte value containing the integration timer, represented as counts of a 10MHz clock. Because there are 50 data values reported per packet this makes the length of a total packet 1026 bytes.

The original design for the packetizer was to store all the data for a packet in RAM then to output all the data sequentially without delay. The FPGA hardware, however, ended up not supporting this design. The RAM module included in the FPGA was unable to store all the data required for a packet. This issue lead to the current design where the data is output as it is available rather than all at once. Using careful timing, the structure of the packet remains intact, despite the hardware limitations.

Packet Header Discription								
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7
0x0	Beginning Sync Word (0x53545254)				Packet Number Counter			
0x8	Packet Length (0x0400)		HK_VBUSMON		HK_3_VVDMON		HK_5VMON	
0x10	HK_15VMON		HK_DB_TMP		HK_TMP2		HK_TMP1	
0x18	DDC_RANGE							
Packet Body Discription								
0x1a	INT_APG2_RG1_1		INT_RG2_1		INT_RG3_1		INT_SG_1	
0x22	Data_1 (10 bytes)							
0x2a			IntegrationTimer		INT_APG2_RG1_2		INT_RG2_2	
0x32	INT_RG3_2		INT_SG_2		Data_2 (10 bytes)			
0x3a							IntegrationTimer	
...
0x1a + 0x14	INT_APG2_RG1_N		INT_RG2_N		INT_RG3_N		INT_SG_N	
	Data_N (10 bytes)							
			IntegrationTimer					

Fig. 2.4: Packet Structure

DATA Discription								
Data is a collection of four 20 bit words, giving data for four different channels								
Data is in most significant bit order first (eg. for channel A, bit 0 would be the most significant bit)								
bit	0 to 9	10 to 19	20 to 29	30 to 39	40 to 49	50 to 59	60 to 69	70 to 79
	Channel A		Channel B		Channel C		Channel D	

Fig. 2.5: Definition of data field from the packet structure

2.6 10 Hz mode

In addition to the primary mode of operation for GRIDS (the 50/50 mode) another operational mode labeled the 10 Hz mode was designed. The 10 Hz mode takes 200 measurements total in a second following a structure of 16 RPA measurements followed by 4 IDM measurements, with that being repeated 10 times in a second.

In 10 Hz mode the aperture and suppressing grids are still set to the same values as in 50/50 mode. The retarding grids still step over the whole voltage range during RPA mode, just using a larger step size since the instrument runs for the duration of 16 RPA measurements instead of 50. The retarding grids are set to the same values during IDM mode as they are in 50/50 mode.

The 10 Hz mode also requires changes to the packet structure. Both the 50/50 mode and 10 Hz mode use the same packet header and the same structure for the data portion of the packet but the number of measurements reported per packet changes. Instead of generating a packet of data every half second like in 50/50 mode, the 10 Hz mode generates a total of 20 packets in a second with 10 packets containing RPA data and the other 10 containing IDM data. While both IDM and RPA packets each contain 50 measurements in 50/50 mode, in the 10 Hz mode IDM packets contain 4 sets of measurements and RPA packets contain 16 sets of measurements. This makes 10 Hz mode IDM packets 106 bytes long and RPA packets 346 bytes.

The rest of the instrument functions the same in both 50/50 mode and 10 Hz mode. The same hardware is used, GRIDS still automatically ranges based on the measured current, and the packets are still output on the RS-422 port. 10 Hz mode was designed to take faster measurements than in 50/50 mode, hopefully with the ability to reveal new structures in plasma due to the higher temporal resolution.

2.7 Toolchain

Typical FPGA programming involves writing code using the VHDL or Verilog languages. This project takes a different approach and uses Matlab Simulink code. Routing the Simulink files through Matlabs HDL auto-coder converts Simulink code into an HDL file

that Libero, Microsemi's FPGA design software, can utilize. Libero runs place and route and compiles the code into a programming file. Place and route is a process integral to FPGA design where first the electronic components, circuitry and logic elements are placed on a FPGA fabric where there is limited space. Then routing decides the design of all the wires needed to connect the components placed in the previous step. Finally a utility program called FlashPro takes the programming data file (PDB) that Libero generated and loads it onto the FPGA. This process is shown in figure Fig. 2.6.

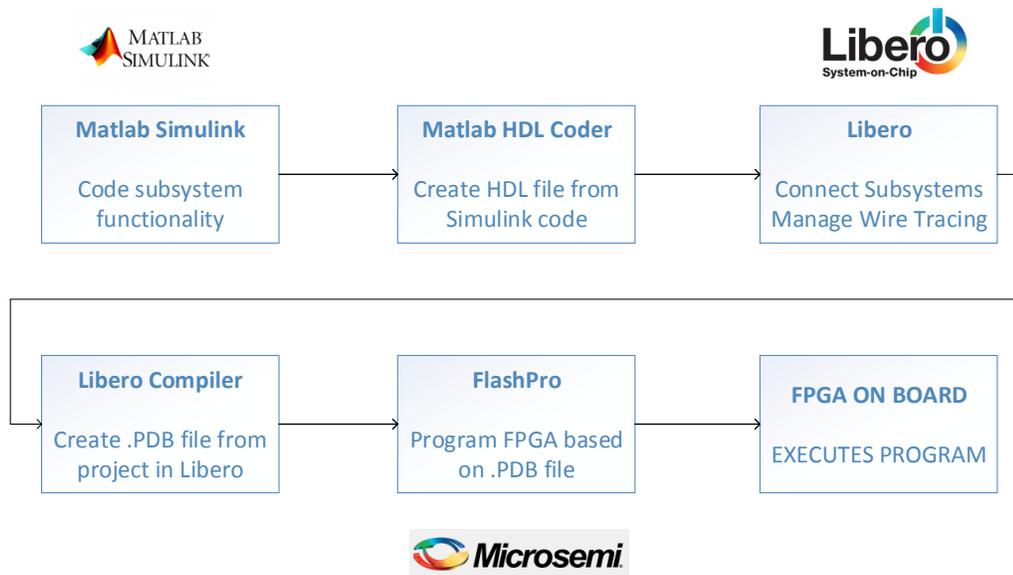


Fig. 2.6: Coding Toolchain

Two major benefits are gained through coding an FPGA this way. The first is the powerful simulation capabilities that Matlab Simulink provides. The ability to simulate code before testing it on an FPGA is integral to writing high quality code quickly and makes many bugs easier to find and fix. The second main benefit is that this toolchain is much easier to learn and use for an individual untrained in FPGA design.

CHAPTER 3

FPGA Testing

3.1 Requirement Completeness and Test Setup

A list of the requirements from Chapter 2 is below along with an indication on their current working level.

1. The grid voltages are set to the correct level during IDM mode.
 - Aperture Grid: Non-zero constant **Partially Working**
 - Retarding Grid 1: Zero volts **Working**
 - Retarding Grid 2: Zero volts **Working**
 - Suppressing Grid: Negative twelve volts **Working**
2. The grid voltages are set to the correct level during RPA mode.
 - Aperture Grid: Zero volts **Partially Working**
 - Retarding Grid 1: Ramping voltage **Working**
 - Retarding Grid 2: Ramping voltage **Working**
 - Suppressing Grid: Negative twelve volts **Working**
3. Ensure current measurements don't overlap from one voltage step to the next during RPA mode. **Working**
4. Ignore current measurements that take place during voltage rise time during RPA mode. **Working**
5. Report 100 current measurements in the telemetry every second; 50 in RPA mode and 50 in IDM mode. **Working**

6. Implement an automatic current range sensing system. Working
7. Define a packet structure for data output from the system. Working
8. Follow the defined packet structure when outputting data from the system. Working
9. Create code that communicates through the standard RS-422 protocol. Working
10. Ensure the full code can be implemented on the FPGA. Working
11. Implement a secondary mode for GRIDS based on taking 10 sets of measurements a second. Working

The test setup consists of multiple instruments and software. The National Instruments VirtualBench measures test points on the GRIDS circuit boards. Matlab is used to interpret data captured by the National Instruments VirtualBench. The RS-422 output from GRIDS is routed into a program created with LabView to parse the packets and plot data. The Keithley 6221 DC and AC current source is used to input current into the instrument.

3.2 FPGA Parameter State

Log files generated by Libero are used to confirm that the full code fits on the FPGA (requirement 10). The results from these log files for 50/50 mode are listed in Table 3.1 and for 10 Hz mode in Table 3.2.

3.3 Grid Voltage Testing

A plot of the four grid voltages is shown in Fig. 3.1. From 0 to 0.5 seconds GRIDS is in IDM mode, from 0.5 to 1 second GRIDS is in RPA mode, then from 1 to 1.1 seconds GRIDS is again in IDM mode. This plot demonstrates that retarding grid 1, retarding grid 2, and the suppressing grid are all working as intended. The plot does not, however, show the aperture grid changing to a non-zero constant while GRIDS is in IDM mode. This is due to a hardware failure with the DAC that controls the grid voltages. The FPGA code is setting the aperture grid to the correct value, as can be seen in the "INT_APG2_RG1.1"

Table 3.1: List of FPGA parameters for 50/50 mode.

Item	Total Available	Used	Does it fit
Core Cells	6144	4540	Yes
I/O ports	68	26	Yes
RAM blocks	8	4	Yes

Table 3.2: List of FPGA parameters for 10 Hz mode.

Item	Total Available	Used	Does it fit
Core Cells	6144	4313	Yes
I/O ports	68	26	Yes
RAM blocks	8	4	Yes

column in Fig. 2.5. This is why requirements 1 and 2 have the aperture grid labeled as partially working, and the other grids labeled as working. Correcting the hardware failure would result in the desired functionality without any code changes.

3.4 Current Sensing Testing

To test the current sensing portion of GRIDS the Keithley 6221 DC and AC current source was used to input a sine wave with 0-120 nA amplitude and 4 Hz frequency into GRIDS. A plot of one packet worth of DDC114 counts is shown in Fig. 3.2. The shape of a sine wave can easily be made out in this picture, but there are also two jagged jumps per curve. These jumps are due to the automatic ranging system changing the integration time. The DDC114 chip's 20-bit resolution means that the DDC114 counts can be any number between 0 and 1,048,575. To convert the DDC114 counts to a current, equation (3.1) is used. *RawValue* is the 20-bit value generated by the DDC 114 chip, *Offset* is equal to 4096, *Capacitance* is 300pF, and *IntegrationTime* changes based on what the automatic ranging is set to, but can be equal to 3.73 ms, 1.87 ms, or 0.94 ms.

$$Current = \frac{(RawValue - Offset) * Capacitance}{IntegrationTime * 2^{20}} \quad (3.1)$$

A plot of the DDC114 counts converted into a current is shown in Fig. 3.3. This

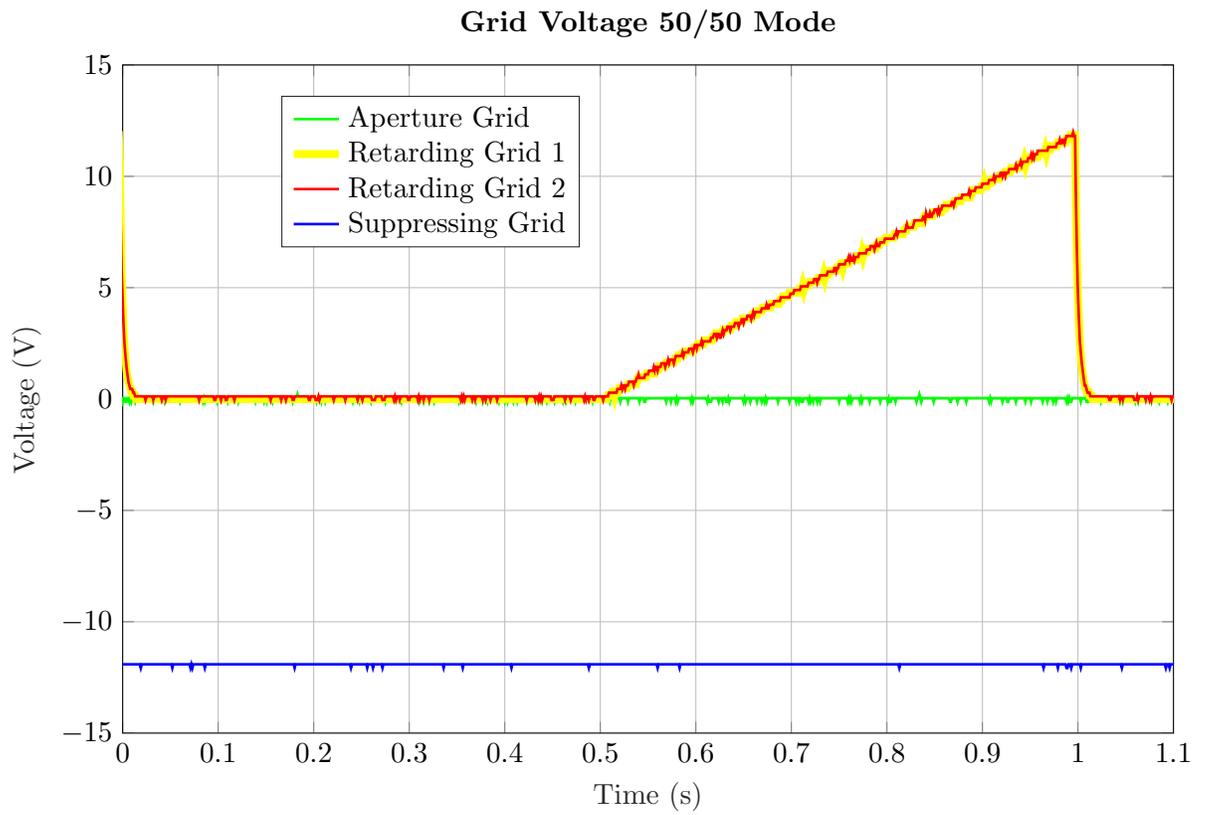


Fig. 3.1: Plot of the four grid voltages with GRIDS configured for 50/50 mode, data recorded for 1.1 seconds

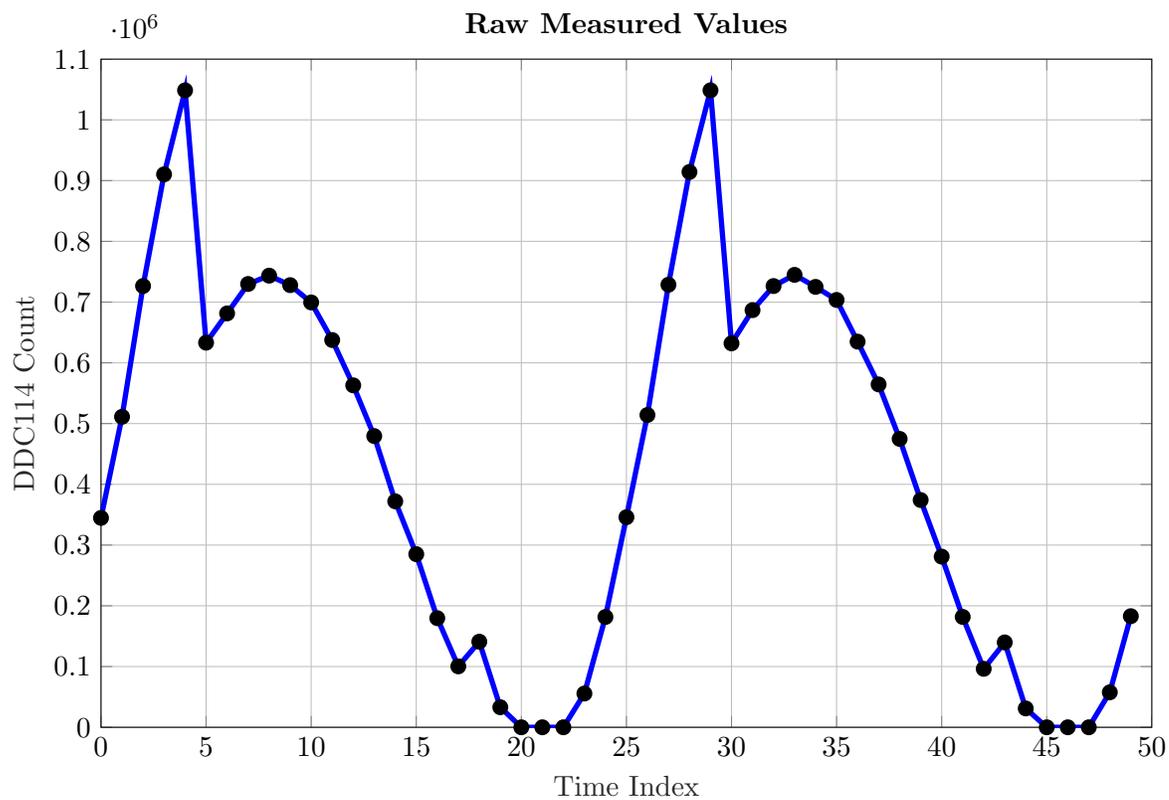


Fig. 3.2: Raw Values

meets requirement 6, implementing an automatic range sensing system, because the current measured by GRIDS matches the input current and ranging is shown happening in Fig. 3.2.

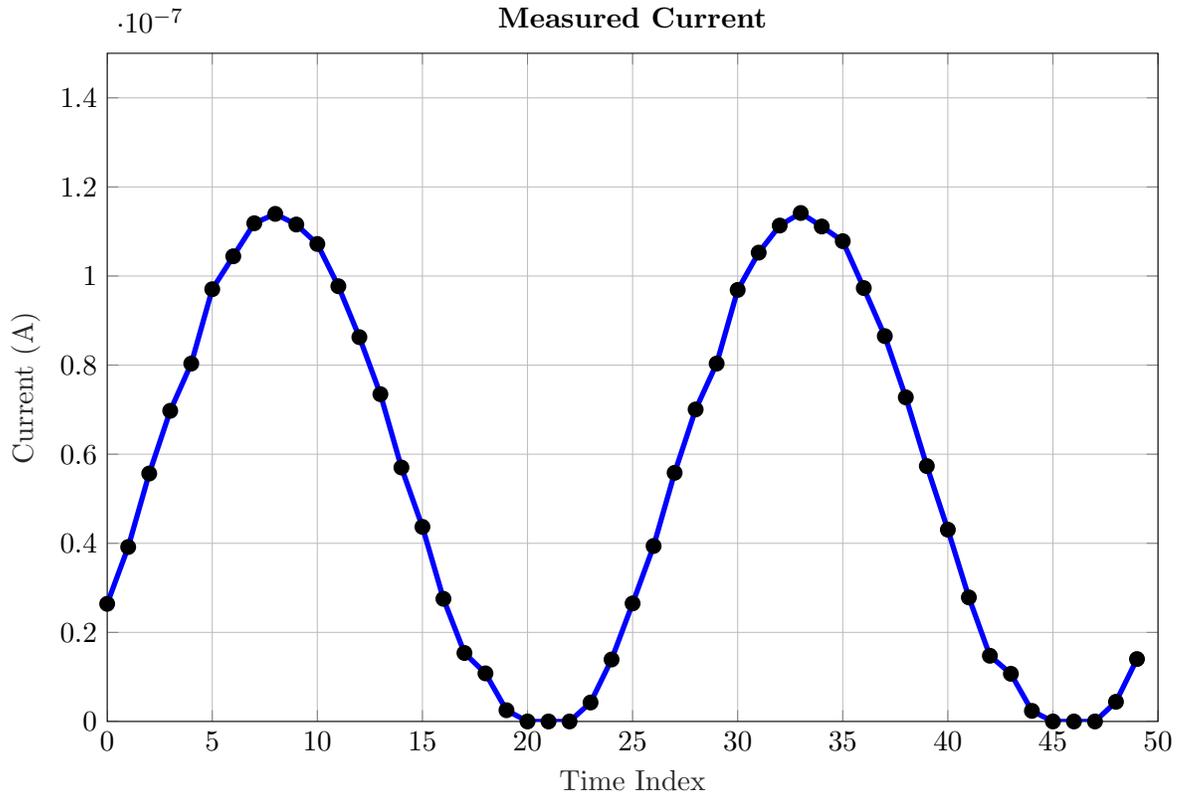


Fig. 3.3: Reconstructed Current

Another plot that demonstrates the automatic ranging functionality is presented in Fig. 3.4. This plot contains the voltage steps from retarding grid 1 during RPA mode, and the DDC_CONV signal that is generated during that same time. In this figure the DDC_CONV signal can be seen to switch from medium range to low range later in the plot. This figure also shows requirement 3, that the current measurements don't overlap from one voltage step to the next, is met. It can be seen that the DDC_CONV signal doesn't drift in relation to the stepping voltage.

Requirement 4, that GRIDS ignores current measurements during the voltage rise time, can also be shown to be complete by taking a closer look at Fig. 3.5. The DDC_CONV

signal switches from high to low in the first 25% of the step time to account for the grid voltage rise time, just like the intended function detailed in Fig. 2.2. It's thus concluded that current measurements made during the rise time aren't reported.

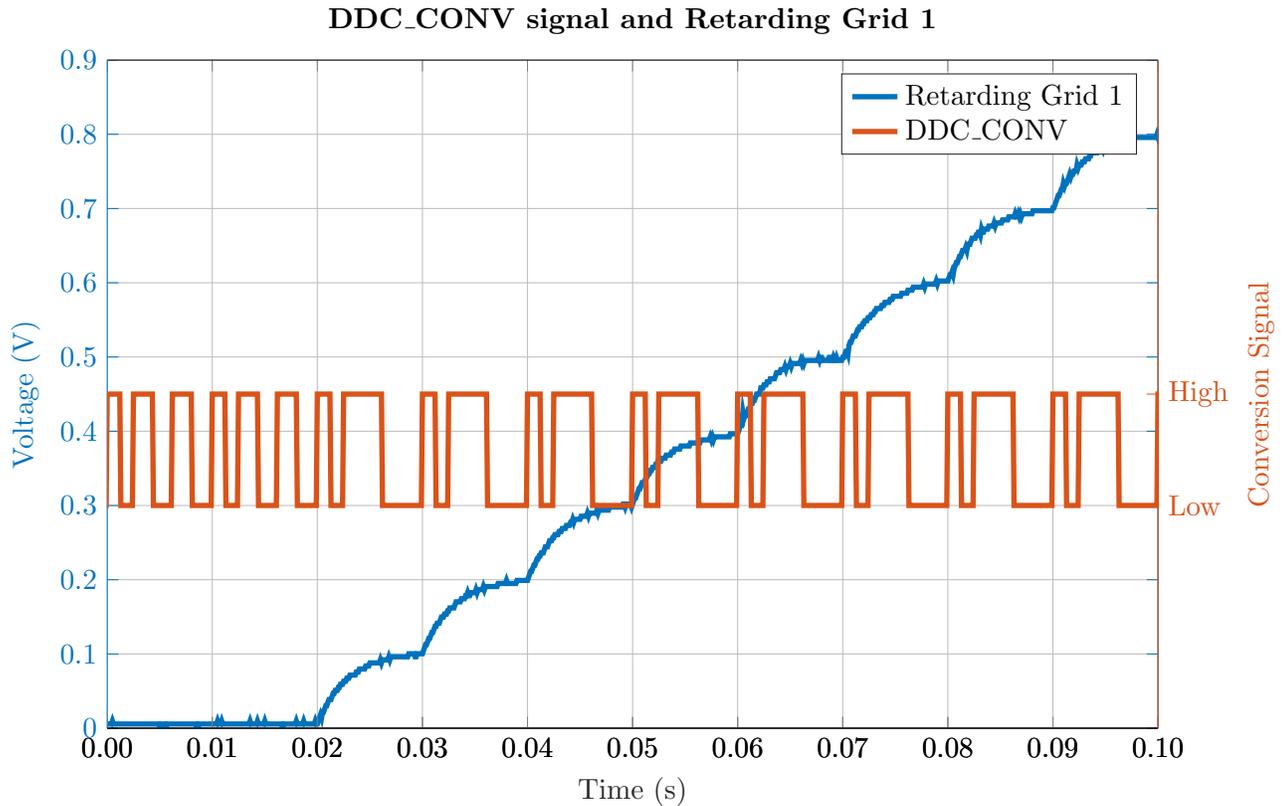


Fig. 3.4: Plot of Retarding Grid 1 overlaid with the DDC_CONV with GRIDS configured for 50/50 mode, data recorded for 0.1 seconds

3.5 Packetizer Testing

Requirement 7, defining a packet structure, is complete and shown in Fig. 2.4 and Fig. 2.5.

To test that the packetizer functions correctly a LabView parser program was created. The parser program reads in the data packets output by GRIDS, and parses the packet to retrieve the embedded data. The packet structure was described to Dr. Ryan Davidson, who used that information to create the parsing program in LabView. A picture of that

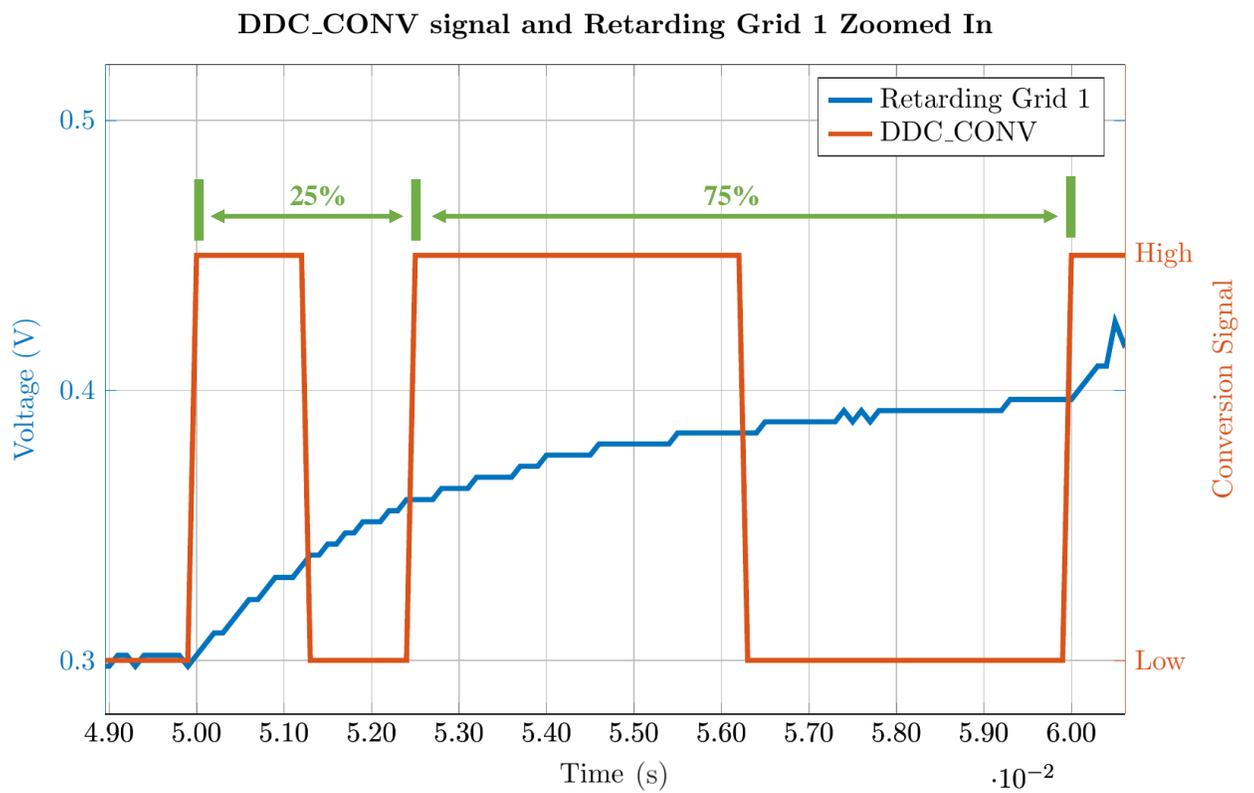


Fig. 3.5: Zoomed in plot of the same data from Fig. 3.4 with annotations added

LabView program with a packet containing IDM data is shown in Fig. 3.6. Completeness of requirement 8, which requires GRIDS data output following a defined packet structure, is demonstrated as a parsing program created to the specifications of the packet structure was able to retrieve the data embedded in the packet. Requirement 5, which requires 100 current measurements reported every second, is also shown to be completed as the packet structure defines 50 current measurements in RPA mode, and 50 current measurements in IDM mode, which each take half a second to complete. The parsing program based on this packet structure corroborates this.

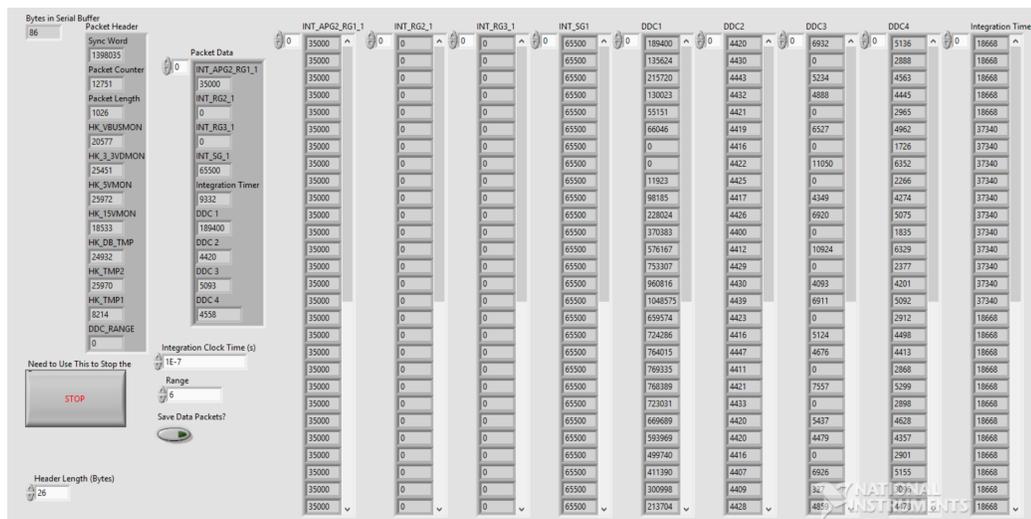


Fig. 3.6: LabView program showing data parsed from a packet containing IDM data

The packet output of GRIDS was connected to a computer running the LabView parsing program using an RS-422 to USB cable. The fact that the LabView program received the data through this cable shows completeness of requirement 9, which requires that GRIDS sends data packets using the RS-422 protocol.

3.6 10 Hz mode Testing

A plot of the grid voltages when GRIDS is in the 10 Hz mode is shown in Fig. 3.7. Because the 10 Hz mode is run on the same hardware as 50/50 mode, the aperture grid is not shown functioning properly for the same reasons the aperture grid doesn't function

properly in 50/50 mode. A more detailed view of the function of the grid voltages during 10 Hz mode is shown in Fig. 3.8. In this figure GRIDS is in IDM mode from 0.0 to 0.02 seconds, then RPA mode from 0.02 to 0.1 second, then repeats with IDM mode from 0.1 to 0.12 seconds and RPA mode from 0.12 to 0.20 seconds. This timing is consistent with the goal of requirement 11, producing 10 sets of measurements per second. However, there is a hardware issue in regards to the response time of the grid voltages as the retarding grids are supposed to be set to 0 volts for the duration of IDM mode. In Fig. 3.8 it is observable that the time it takes for the voltage to fall from 12 volts to 0 volts at the transition of RPA mode to IDM mode takes long enough to interfere with IDM mode measurements.

The packetizer system for 10 Hz mode was also tested with the LabView parsing program, which shows it is working as intended. 0.2 seconds worth of data taken while GRIDS was in 10 Hz mode is listed in appendix A.1. The rest of the function of the 10 Hz mode matches that of the 50/50 mode and has already been shown to be functional.

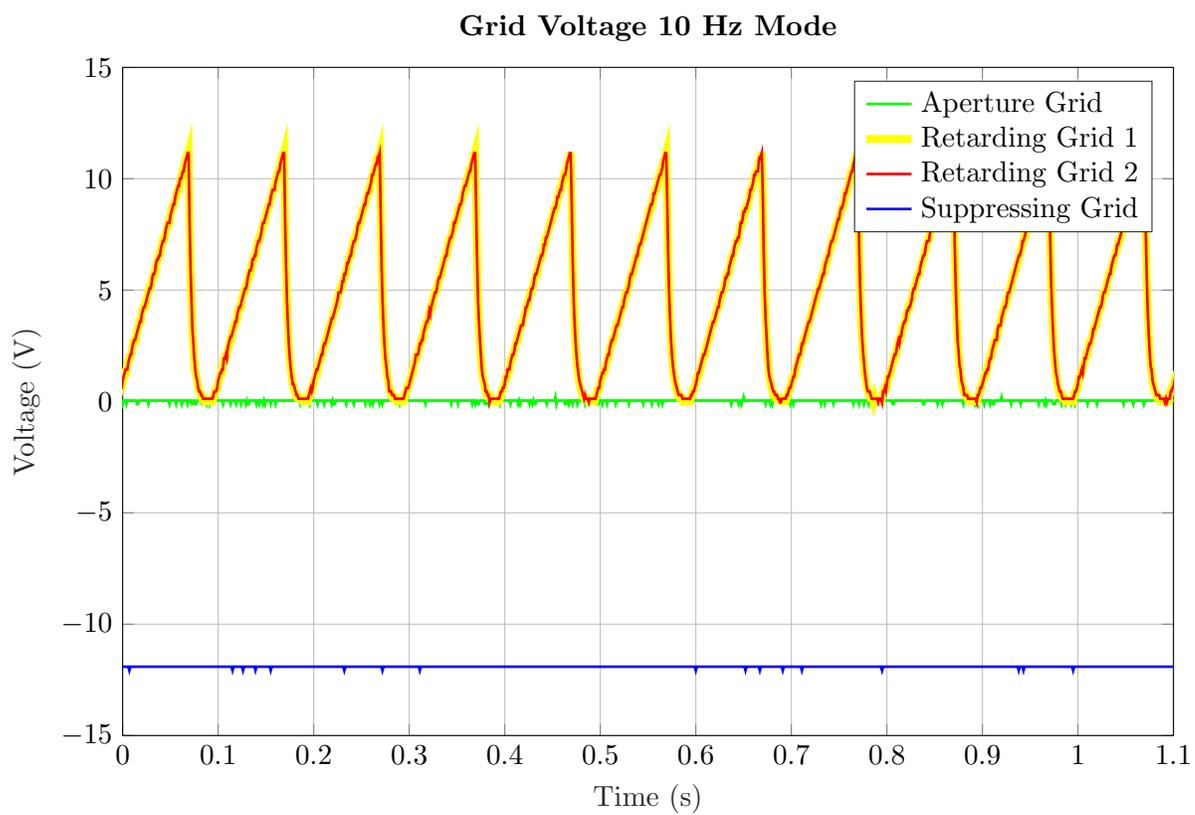


Fig. 3.7: Plot of the four grid voltages with GRIDS configured for 10 Hz mode, data recorded for 1.1 seconds

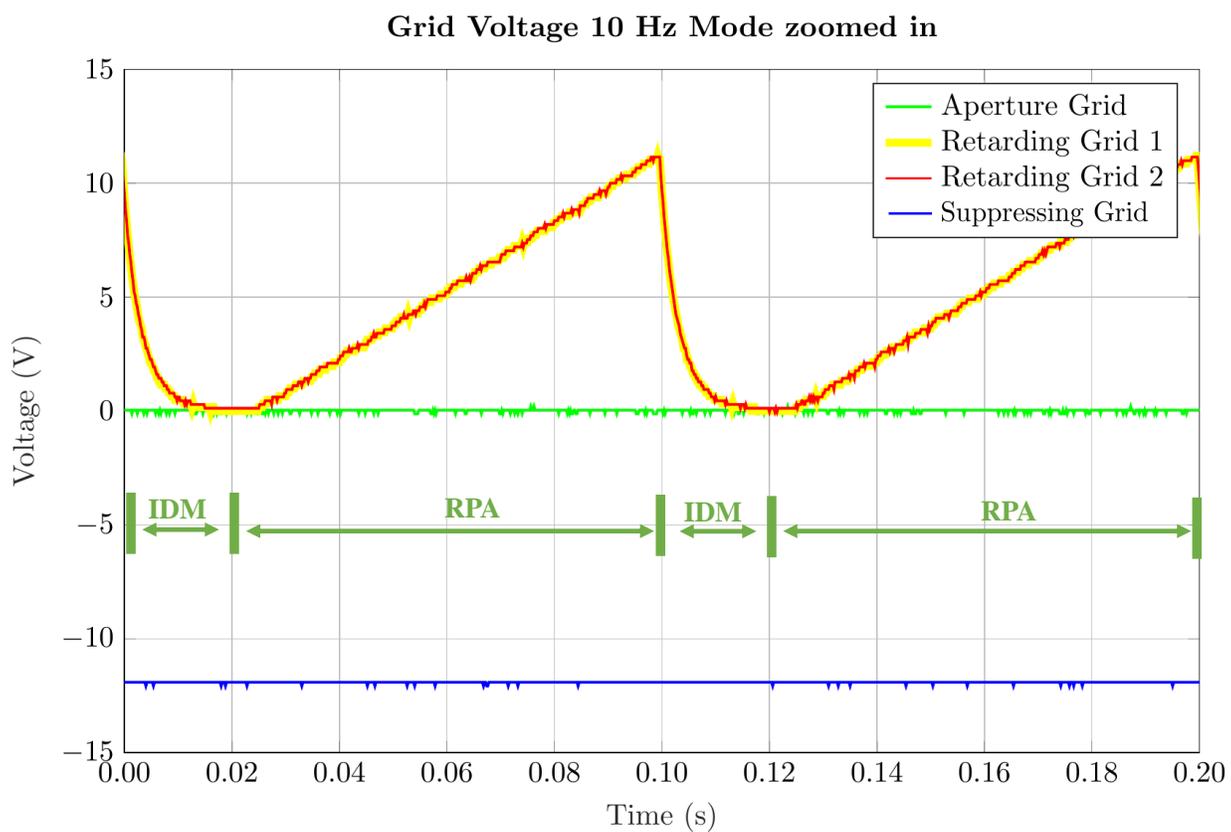


Fig. 3.8: Annotated plot of the four grid voltages with GRIDS configured for 10 Hz mode, data recorded for 0.2 seconds

CHAPTER 4

CONCLUSIONS AND FUTURE WORK

4.1 Conclusion

This thesis outlines the FPGA design and testing of the GRIDS instrument. GRIDS can perform the same measurements as both the IDM and RPA in one small, low-weight, low-power package suitable for CubeSats. The FPGA code was developed in Matlab Simulink, ported to HDL using an auto-coder, then fed into Libero to run place and route. GRIDS uses an FPGA to control a quad-channel DAC for setting grid voltages and to control a quad-channel current sensing chip, the DDC114 chip. An automatic ranging system was implemented in the current sensing part of the design. This was needed because the range of currents GRIDS is expected to encounter in normal operation is larger than the capabilities of the DDC114 chip to measure in any one configuration. A packet structure was created and used to output the data GRIDS produces through a RS422 bus. Two modes of operation were implemented, the 50/50 mode and 10 Hz mode. Through testing all of the desired functionality listed in the requirements was shown to be met with the exception of the aperture grid due to a hardware malfunction.

4.2 Future Work

The hardware that is shown in Fig. 1.5 is not the final version of the hardware. Some parts such as the FPGA, housekeeping ADC, and signal filters are going to be updated. The new FPGA should include phase-locked loops, to run the current sensing chip at it's fastest supported rate, and more RAM space to allow for implementation of packet buffering before packet output. The housekeeping ADC should have enough channels to support all housekeeping data signals without the need for a multiplexer. The new signal filters should allow the voltage to fall faster when switching from RPA mode to IDM mode, and shorten

the voltage rise time to be within the first 25% of the step time. These hardware changes will influence what future work needs to be done on the GRIDS FPGA code, along with additional desired functionality. A list of known future work for the FPGA code of GRIDS follows.

1. The FPGA code written for this thesis will need to be ported to a new FPGA other than the currently used AGLN250V5-VQG100 from Microsemi Corporation. So long as another FPGA made by Microsemi Corporation is used this hardware change should only necessitate changing pin assignments in Libero.
2. Buffer a whole packets worth of data before outputting a packet. Packet data will be able to be buffered once additional RAM space is available. The current implementation doesn't store packet data in RAM and just outputs the data as it is created. Correct implementation of packet output means that packet data will be stored in RAM until a full packets worth of data is available for output.
3. FPGA code to implement the housekeeping data needs to be written. The housekeeping data, which makes up much of the packet header, isn't working currently. The decision was made to not spend time implementing the housekeeping code because much of the hardware surrounding the housekeeping data had plans to change.
4. Implement commanding to give additional control over GRIDS while on orbit. GRIDS would receive commands through its RS-422 port, parse it, and execute the command. Some examples of desired commands include the ability to change the value of the non-zero constant that the aperture grid is set to during IDM mode, and to enable/disable automatic ranging.
5. Add additional ranges for the ranging system to increase instrument accuracy. With the addition of phase-locked loops in a new FPGA it should be possible to add additional ranges for the ranging system. Also, supposing that the new hardware can handle the calculations, averaging the multiple current measurements the DDC114

chip takes while in the high ranges during a single voltage step would be a desirable function.

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APPENDICES

Appendix A
Additional Data

A.1 10 Hz Packet Parser text output

INT_APG2_RG1.1 INT_RG2.1 INT_RG3.1 INT_SG.1 Integration Timer DDC 1 DDC
2 DDC 3 DDC 4 I1 (A) I2 (A) I3 (A) I4 (A)

0 0 0 65500 18668 0 4415 5182 4557 -6.277453E-10 4.888935E-11 1.664383E-10 7.065200E-
11

0 4090 4090 65500 18668 0 4413 0 2706 -6.277453E-10 4.858283E-11 -6.277453E-10
-2.130288E-10

0 8180 8180 65500 18668 0 4428 3365 4069 -6.277453E-10 5.088170E-11 -1.120317E-10
-4.137970E-12

0 12270 12270 65500 18668 0 4429 6560 5031 -6.277453E-10 5.103496E-11 3.776281E-10
1.432964E-10

0 16360 16360 65500 18668 0 4428 204 3119 -6.277453E-10 5.088170E-11 -5.964807E-10
-1.497332E-10

0 20450 20450 65500 18668 0 4410 953 3323 -6.277453E-10 4.812306E-11 -4.816903E-10
-1.184685E-10

0 24540 24540 65500 18668 0 4427 7472 5330 -6.277453E-10 5.072844E-11 5.173995E-10
1.891205E-10

0 28630 28630 65500 18668 0 4410 3097 3908 -6.277453E-10 4.812306E-11 -1.531049E-10
-2.881253E-11

0 32720 32720 65500 18668 0 4422 0 2847 -6.277453E-10 4.996215E-11 -6.277453E-10
-1.914194E-10

0 36810 36810 65500 18668 0 4418 5445 4707 -6.277453E-10 4.934912E-11 2.067452E-10
9.364072E-11

0 40900 40900 65500 18668 0 4420 4614 4445 -6.277453E-10 4.965564E-11 7.938772E-11
5.348709E-11

0 44990 44990 65500 18668 0 4411 0 2464 -6.277453E-10 4.827631E-11 -6.277453E-10
-2.501173E-10

0 49080 49080 65500 18668 0 4424 3855 4168 -6.277453E-10 5.026867E-11 -3.693521E-11
1.103459E-11

0 53170 53170 65500 18668 0 4409 7114 5120 -6.277453E-10 4.796980E-11 4.625331E-10
1.569363E-10

0 57260 57260 65500 18668 0 4431 55 3069 -6.277453E-10 5.134148E-11 -6.193161E-10
-1.573961E-10

0 61350 61350 65500 18668 0 4419 1961 3554 -6.277453E-10 4.950238E-11 -3.272061E-10
-8.306591E-11

35000 0 0 65500 9332 0 4411 4729 4499 -1.255760E-9 9.657332E-11 1.940664E-10
1.235525E-10

35000 0 0 65500 18668 0 4411 2803 3807 -6.277453E-10 4.827631E-11 -1.981628E-10
-4.429160E-11

35000 0 0 65500 18668 0 4426 0 2888 -6.277453E-10 5.057519E-11 -6.277453E-10 -
1.851358E-10

35000 0 0 65500 18668 0 4419 6167 4850 -6.277453E-10 4.950238E-11 3.173976E-10
1.155566E-10 0 0 0 65500 18668 0 4431 4749 4487 -6.277453E-10 5.134148E-11 1.000776E-
10 5.992393E-11

0 4090 4090 65500 18668 0 4403 0 2478 -6.277453E-10 4.705025E-11 -6.277453E-10
-2.479717E-10

0 8180 8180 65500 18668 0 4434 3394 4052 -6.277453E-10 5.180125E-11 -1.075872E-10
-6.743358E-12

0 12270 12270 65500 18668 0 4417 6445 4973 -6.277453E-10 4.919586E-11 3.600034E-10
1.344074E-10

0 16360 16360 65500 18668 0 4432 0 2979 -6.277453E-10 5.149473E-11 -6.277453E-10
-1.711893E-10

0 20450 20450 65500 18668 0 4407 1943 3570 -6.277453E-10 4.766328E-11 -3.299648E-10
-8.061378E-11

0 24540 24540 65500 18668 0 4441 7768 5389 -6.277453E-10 5.287406E-11 5.627639E-10
1.981628E-10

0 28630 28630 65500 18668 0 4411 2566 3776 -6.277453E-10 4.827631E-11 -2.344850E-10
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1.154034E-10

0 40900 40900 65500 18668 0 4436 5080 4545 -6.277453E-10 5.210777E-11 1.508060E-10
6.881290E-11

0 44990 44990 65500 18668 0 4410 0 2801 -6.277453E-10 4.812306E-11 -6.277453E-10
-1.984693E-10

0 49080 49080 65500 18668 0 4419 3933 4196 -6.277453E-10 4.950238E-11 -2.498108E-11
1.532581E-11

0 53170 53170 65500 18668 0 4430 6897 5077 -6.277453E-10 5.118822E-11 4.292760E-10
1.503462E-10

0 57260 57260 65500 18668 0 4432 328 3108 -6.277453E-10 5.149473E-11 -5.774767E-10
-1.514190E-10

0 61350 61350 65500 18668 0 4416 1078 3363 -6.277453E-10 4.904260E-11 -4.625331E-10
-1.123382E-10

35000 0 0 65500 9332 0 4428 5618 4699 -1.255760E-9 1.017852E-10 4.666178E-10
1.848689E-10

35000 0 0 65500 18668 0 4418 2571 3801 -6.277453E-10 4.934912E-11 -2.337187E-10
-4.521115E-11

35000 0 0 65500 18668 0 4411 0 2788 -6.277453E-10 4.827631E-11 -6.277453E-10 -
2.004616E-10

35000 0 0 65500 18668 0 4417 5484 4721 -6.277453E-10 4.919586E-11 2.127223E-10
9.578634E-11