PLASMA VELOCITY VECTOR INSTRUMENT FOR SMALL SATELLITES (PVVISS)

by

William Smith Hatch

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ABSTRACT

Plasma Velocity Vector Instrument for Small Satellites (PVVISS)

by

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Utah State University, 2016

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Low-earth orbit (LEO) contains plasma which can impact satellite charging and radio frequency (RF) communications. Quantifying both the composition and movement of ions in LEO can improve efficiency of the forecasting models that predict the impact plasma will have on satellite communications and accuracy of global positioning satellite measurements.

Two instruments known as the Retarding Potential Analyzer (RPA) and the Ion Drift Meter (IDM) have been used in tandem to measure ionospheric properties including ion temperature, velocity, and density. These instruments are costly and occupy large areas on a spacecraft. In recent years, space mission budgets have diminished. This change has driven innovation towards creating new instruments which are compatible with smaller and cheaper satellites yet still yield measurements of comparable quality. This thesis presents the design of a new instrument that encompasses the functionality of both the RPA and IDM, known as the Plasma Velocity Vector Instrument for Small Satellites (PVVISS). PVVISS has compact form factor and low power requirements, making it a viable option for smaller, low cost nano-satellite sized missions. Missions utilizing the PVVISS sensor will allow increased exploration of the ionospheric impact on satellite communications.

(77 pages)

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This thesis presents the design of a new instrument that encompasses the functionality of both the RPA and IDM, known as the Plasma Velocity Vector Instrument for Small Satellites (PVVISS). PVVISS has compact form factor and low power requirements, making it a viable option for smaller, low cost nano-satellite sized missions. Missions utilizing the PVVISS sensor will allow increased exploration of the ionospheric impact on satellite communications.

To my wonderful wife and friend - I couldn't have done this without you.
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William Smith Hatch

CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

Introduction and Literature Review

Ions are a prominent feature of the earth's upper atmosphere. Understanding the energy, density, and movement of ions in low earth orbit (LEO) can improve the efficiency of forecasting models that can quantify the impact ions will have on spacecraft charging, communication systems, and global satellite positioning networks [1]. Historically, ion measurements in LEO have commonly been completed using two instruments: retarding potential analyzers (RPA) and ion drift meters (IDM). Together, the RPA and IDM help space scientists gain insight into the density, temperature, velocity, and ratio of light to heavy ions based on their energy [2].

1.1 Ion Species Energy

Many ion species exist in LEO. Researchers must be able to quantify these ions based on their energies in order to assess the impact they will have on the aforementioned forecasting models. The principal ions of interest include: atomic oxygen, nitrogen, helium, and hydrogen. Each species has an energy relative to the spacecraft frame of reference. The energy of a resting ion with respect to a satellite in LEO can be defined as:

$$R = \frac{1}{2} m_i v_s^2 \tag{1.1}$$

Where m_i is the mass of the species and v_s is the spacecraft velocity [3]. The energy for each species of ion can be calculated given any spacecraft velocity. For example, the energy R for atomic oxygen (O^+) is shown to be about 5 eV for an average LEO spacecraft velocity of 7.8 km/s.

PVVISS uses the species-dependent energy to distinguish and isolate ions. The instrument repels ions that have a lower electric potential than that of the instrument measurement system, and therefore allows only ions of greater energy potential to be measured.

1.2 History of Retarding Potential Analyzers

The RPA is a proven instrument that accurately measures ion density, temperature, and the component of ion velocity vector normal to the instrument aperture (the ram direction in most satellite applications). The RPA also provides a ratio of light to heavy ions using a grid system which quantifies the known differences in the species' energy as defined in equation 1.1.

The RPA controller places a voltage on the retarding grid, which blocks ions that have less kinetic energy than the potential energy barrier presented by the grid from continuing through the system. Those ions with greater or equal energy pass through the retarding grid and impact the collector plate at the back of the instrument. As ions come into contact with the collector, a small current is produced through charge exchange and is measured using analog circuitry. The retarding grid is swept over a finite range of pre-defined voltages. The voltages and the associated currents from each retarding grid sweep are recorded, which can then be quantified into ion species, density, velocity, and temperature. This data set is known as an I-V curve. An ideal I-V curve is determined by equation 1.2 as derived by W. C. Knudsen [4]:

$$I = T_r A e v cos\theta \sum_i n_i * \frac{1}{2}[1 + erf(\kappa_i) + \frac{exp(-\kappa_i^2)}{\pi^{\frac{1}{2}} a_i}] \tag{1.2}$$

Where,

$$\kappa_i = a_i - b \tag{1.3}$$

$$a_i = \frac{v cos\theta}{\alpha_i} \tag{1.4}$$

$$\alpha_i = (\frac{2kT}{m_i})^{\frac{1}{2}} \tag{1.5}$$

$$b = (\frac{e(V + \phi)}{kT})^{\frac{1}{2}} \tag{1.6}$$

T_r is the optical transmission of the grids, A is the aperture area, e is the charge of an electron, v is the relative velocity of the ions to the aperture plane, θ is the angle between the normal to the aperture face and the relative velocity, ϕ is the potential of the spacecraft relative to the plasma, n_i is the concentration of the i^{th} ion constituent, m_i is the mass of the i^{th} ion constituent, T is the ion temperature, and k is the Boltzmann Constant.

The normalized IV curve for a plasma consisting of 85% oxygen and 15% hydrogen, for a velocity of $7.5km/s$ and temperature of 1500°K is shown in Figure 1.1.

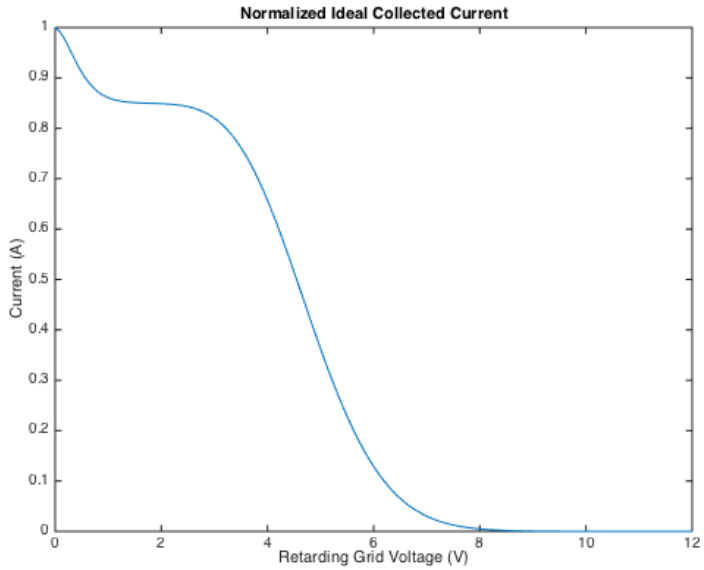

Fig. 1.1: Normalized IV Curve

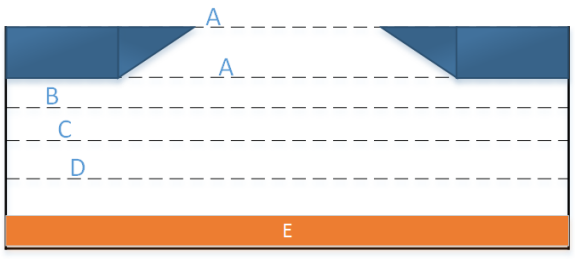

Fig. 1.2: RPA Design

Figure 1.2 illustrates the RPA grid stack layout.

- Aperture Grid (A)

  The aperture grids are held at spacecraft ground to ensure that voltages inside the sensor do not influence the ions and their energies outside the sensor.

- Retarding Grid (B)

  The retarding grid provides a sweeping positive voltage relative to spacecraft ground. This varying voltage blocks incoming ions that have less kinetic energy than the potential energy barrier produced by the retarding grid.

- Suppression Grid (C)

  The suppression grid is held at a negative voltage relative to spacecraft ground. This prevents thermal electrons from reaching the collector and suppresses any photo-electrons that are emitted from the collector.

- Ground Grid (D)

  The ground grid is used to prevent coupling between the suppression grid and the collector plate.

- Collector Plate (E)

  The ions that pass through the grid stack hit the collector plate and through charge exchange create a small current, which is then measured with analog circuitry and an analog to digital converter (ADC).

The RPA has been extensively analyzed to optimize its efficiency and accuracy [5]. Some design limitations and overall RPA improvements have been explored by the research performed by Hanson et al., Klenzing et al., and Davidson et al. [6] [7] [8].

Hanson et al. [6] mention that any physical grid system will have a non-uniform potential in the plane, which will allow some ions with less energy than the grid potential to leak through. Thus, ion leakage through the grid system is an inherent limitation in a single

retarding grid RPA design. This leakage may be mediated by using a tandem grid array as described by Klenzing et al. [7]. A tandem, four-grid system can be used which includes two retarding grids and a suppression grid. This array works to improve ion filtering and to increase RPA data accuracy.

Also, Davidson and Earl discovered that differences in grid wire thickness and wire spacing can influence the effectiveness of the grids [8]. For example, varying width and distance of the wires can change the accuracy of temperature and density measurements [8]. RPA design must consider these effects to optimize functionality.

1.3 History of Ion Drift Meters

The IDM is designed to measure the transverse velocity of ions at a given spacecraft's location. Although physically similar to the RPA design, the IDM separates the collection plate into four segments [9]. The four-segment design allows two mutually perpendicular arrival angles to be measured by alternating which collector segments are used during calculation. For example, Figure 1.3 shows a collector plate split into four segments. One arrival angle can be calculated by using the ratio of the four collector plates i.e. $\frac{A+B}{C+D}$. The perpendicular angle can be calculated by connecting alternating plate current sections i.e. $\frac{A+C}{B+D}$.

The arrival angle, α, can then be calculated using Equation 1.7.

$$\tan\alpha = \frac{W}{2D}\frac{1-\frac{I_1}{I_2}}{1+\frac{I_1}{I_2}} \tag{1.7}$$

Where W and D are the aperture width and the effective depth respectively, I_1 and I_2 are the currents from the collector plates. IDM angles can be viewed in Figure 1.4.

1.4 Combined RPA and IDM Functionality

Together, the IDM and RPA can measure estimated composition, density, temperature, and the ambient ion drift. When used in tandem, these instruments give the researcher a comprehensive understanding of these ion characteristics at a given spacecraft location [10].

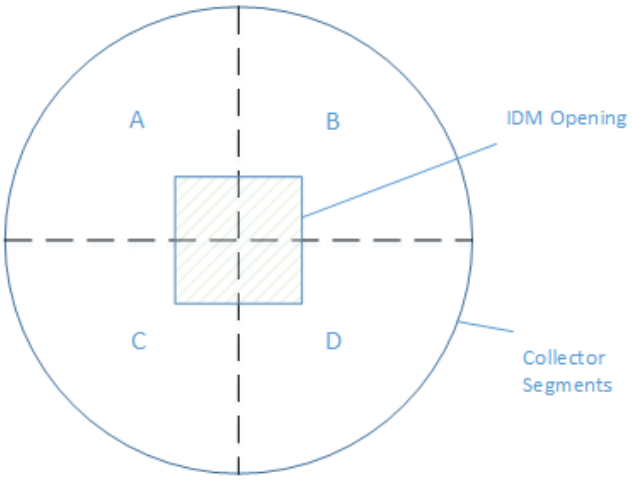

Fig. 1.3: IDM Collector Segments

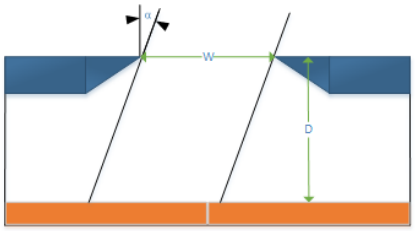

Fig. 1.4: IDM Angles

Because of the combined versatility of the RPA and IDM instruments, they have been flown on many satellite missions. Examples of these missions include: C/NOFS [11], Dynamics Explorer [12], and many Defense Meteorological Satellite Program (DMSP) satellites [13].

1.5 Spacecraft Charging

Although RPA and IDM ideal functionality has been quantified, environmental factors must also be considered to ensure optimal performance. Spacecraft charging can be a significant challenge for many space missions. Large negative potentials can build up on a spacecraft when bombarded by electron events. The sheath of between the bulk plasma and the spacecraft slows down ions as they pass through and cause the instrument to measure

ions at a reduced velocity. It can also lead to electric discharges and create data anomalies [14]. Spacecraft design must account for this discrepancy in charge across spacecraft surfaces to maintain data integrity and system functionality.

Zuccaro and Holt [15] outlined a method to mediate charge discrepancies across a spacecraft body. This method, known as the SenPot, uses a conductive reference surface in the ram direction which is insulated from the spacecraft [2]. The SenPot potential can then be used as a reference ground for an RPA or IDM instead of the spacecraft ground, thus mitigating spacecraft charge discrepancies.

1.6 Small Satellite Missions

Although RPA and IDM provide important diagnostics of the ionosphere, these legacy instruments have traditionally been designed for large satellites [16]. Large spacecraft missions are becoming increasingly unfeasible as space exploration budgets have diminished. The industry has therefore begun to shift to smaller, more compact satellite missions to conduct science missions in LEO [17].

Cube satellites (CubeSats), may be an appropriate vehicle for atmospheric and ionospheric measurements due to their small size and relatively modest cost when compared to larger satellites [17]. Due to their size and weight, they fit into the nano-satellite specification. They have been used for many space weather and atmospheric research programs, such as the Dynamic Ionosphere CubeSat Experiment (DICE) mission, Explorer [18], Osiris [19], and RAX-2 [20].

CubeSats generally weigh about one kilogram and have the physical dimensions of 10 x 10 x 10 centimeters. These spacecraft have standardized design and specifications to reduce production cost and design complexities [2]. Legacy RPA and IDM instruments are not well suited for use on smaller satellites due to their size and power requirements. To utilize the CubeSat platform, IDM and RPA instruments must be altered to be compatible with nano-satellite design. Design changes must include reduced overall size, weight, and power consumption.

1.7 Project Goals

This thesis describes the design of an instrument that encompasses the functionality of both the RPA and IDM and is compatible with CubeSat specifications. This instrument will be compact, have a lower overall power draw than previous RPA/IDM pairs, and will be modular to allow easy adaptation into many mechanical configurations. By doing so, this instrument can be used on smaller, less expensive LEO platforms and allow increased exploration of ionospheric physics.

The project goals include:

1. Create a new instrument that combines the functionality of both the RPA and IDM in one sensor that is suitable for CubeSat missions.

    - Generate grid bias voltages.

        Generate up to four different positive voltages with a magnitude of 0-12 V for use on the grids.

        Generate a negative voltage in the range of -12 V to 0 V for use on the suppression grid.

        Grid voltages must be fully programmable such that the instrument can sweep up to 128 different voltages in one second. This sweep requirement was chosen as this step size has been proven to be sufficient for a 12 volt sweep [2].

    - Measure current from collectors.

        Must be able to measure currents as low as 50 pico amps (pA) and as high as 5 micro amps (μA).

        The analog to digital converter must have sufficient resolution to measure 50pA of current.

    - Design schematics and board layout for the new instrument.

    - Verify and Test FPGA code.

        Current collection and readout.

Retarding and Suppression grid voltage generation (not implemented in this design).

2. Test new instrument capabilities.

   - Design a test procedure that will outline all tests required to verify instrument performance.
   - Design test software to automate the testing procedure.

3. Analyze the test results to confirm instrument meets specifications.

   - Review data to verify completion of requirements, that the new PVVISS instrument performs as expected, and is therefore a viable option for LEO missions.

CHAPTER 2

PVVISS Design

2.1 Requirements

Chapter 2 contains the essential components for instrument viability on LEO missions and CubeSat compatibility. Table 2.1 lists the requirements for size, power, mass, and circuit board operation. All components must be tested and confirmed.

Table 2.1: Requirements

Parameter	Requirement	Design Goals	Verification
Mass	$\leq$ 0.5 kg	0.4 kg	Test
Power	$\leq$ 0.5 Watts DC	0.4 Watts DC	Test
Size	$\leq$ 3.5" x 3.5" x 2"	3.5" x 3.5" x 2.5"	Inspection
Survival Temperature	$\leq -10°C$	$-35°C$	Datasheet
Survival Temperature	$\geq 40°C$	$80°C$	Datasheet
Operating Temperature	$\leq 5°C$	$-10°C$	Datasheet
Operating Temperature	$\geq 30°C$	$80°C$	Datasheet
Telemetry Rate	$\geq$ 2048 bits/s	115200 bits/s	Test
Min Collector Currents	$\geq 50pA$	$50pA$	Test
Max Collector Currents	$\leq 5\mu A$	$10\mu A$	Test
Retarding Grids (RGs) Bias	$\leq$ 0 V	-13.5 V	Test
Retarding Grids (RGs) Bias	$\geq$ 12 V	13.5 V	Test
Suppressor Grid Bias	$\geq$ 0 V	0 V	Test
Suppressor Grid Bias	$\leq$ -12 V	-13.5 V	Test
RG Sweep Points	$\geq$ 32 Pts	128 Pts	Test
RG Sweep Time	$\leq$ 1 s	1 s	Test
Sweep Modes	$\geq$ 1	4	Test
Collector Current Resolution	$\geq$ 16 bits	20 bits	Test

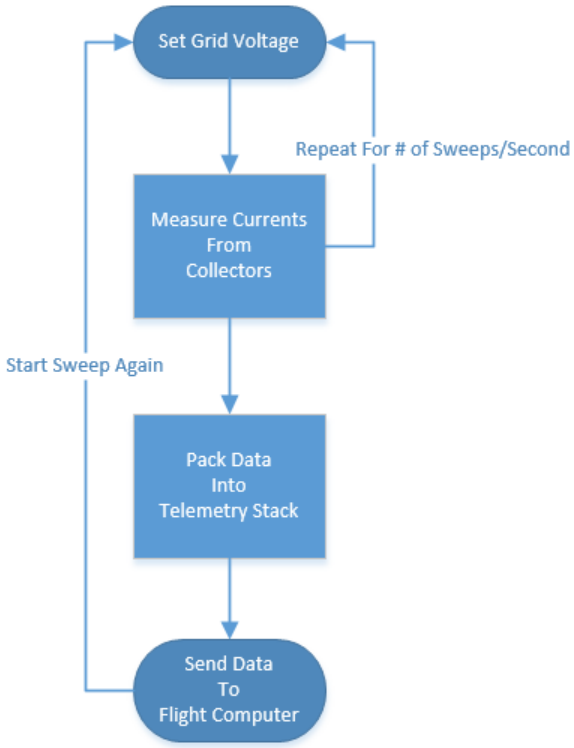

Fig. 2.1: PVVISS Measurement Flow Chart

A general flow chart of the PVVISS measurement progression is presented in Figure 2.1. A PVVISS measurement consists of a series of collected currents and their associated retarding grid voltage. The retarding grid voltage is changed for each point in the sweep, and current measurements are taken. When the number of points in the sweep is completed, PVVISS compiles all the measurements together with housekeeping data into the telemetry stack. The compiled data is then sent to the main flight computer. A new measurement set can then be collected, and the cycle repeats.

2.2 PVVISS Hardware Components

As mentioned in Chapter 1, previous RPA/IDM designs have used a combination of switches with logarithmic and difference amplifiers to both measure the ion currents and to calculate the arrival angle. PVVISS electrical components have been methodically chosen

to maintain RPA/IDM functionality while creating an instrument compatible with CubeSat missions by minimizing size and instrumentation complexity.

PVVISS employs two circuit boards: the daughter board both measures the collector currents and digitizes them, and the main board controls the daughter board, grid voltage control, communications with flight computer, and general housekeeping. A picture of the two circuit boards can be seen in Appendix H. Small connectors are used to reduce PVVISS mass and size.

2.3 Daughter Board Design

2.3.1 Circuit Design

The daughter board in the PVVISS design contains a small chip with low power draw which can replace the previously complicated and spacious circuitry into a single, more space-effective package. (See Appendix G for schematics).

The DDC114 Analog to Digital Converter (ADC) (made by Texas Instruments) is used because it has the ability to measure the small currents, as is required by RPA/IDM. The DDC114 requires a reference voltage of 4.096V, which is generated on the daughter board by a low power voltage reference chip. An op-amp is used as a buffer to supply the DDC114 with a constant voltage.

A microD connector has been chosen in place of a regular D-sub connector to reduce the overall size of the daughter board. The daughter board is also equipped with a temperature sensor to allow for temperature correction of the collected data.

As this PVVISS design is a proof of concept, test points have been added to all data lines and voltage rails to allow debugging and to ease troubleshooting. Red and Blue LEDs are added to the main power rails to visually verify the board is being powered on.

2.3.2 Part Selection

The DDC114 is a quad current input, 20-bit ADC. It combines both current-to-voltage and analog-to-digital conversions using two delta-sigma converters and digital filters, which

allows four low-current sources to be connected directly to the inputs and then be digitized. The integration time for the delta-sigma converters can be adjusted to meet design timing requirements. This ADC was specifically chosen because of its low average power usage of 13.5mW per channel while in low power mode.

The DDC114 charges one of eight internal capacitors that can be selected by the user, C_f . When a current enters the device, the DDC114 capacitor partially discharges over a user-specified integration time T_{int}. The voltage on the capacitor is then digitized by the internal ADC. The ADC counts are turned into a measured voltage by equation 2.1, and then the measured voltage is used to calculate the charge on the capacitor using equation 2.2. The average input current is calculated by dividing the charge by the integration time, as shown in Equation 2.3.

$$V_{mes} = \frac{V_{ref}}{2^{20}} * ADC_{Count} \tag{2.1}$$

$$Q = C_f * V_{mes} \tag{2.2}$$

$$I_{in} = \frac{Q}{T_{int}} \tag{2.3}$$

An accurate reference voltage is required to correctly digitize the currents for analysis. Reference voltage noise must therefore be moderated to ensure clean data. In order to minimize noise from the DDC114, Texas Instruments recommends the REF3140 as the external voltage reference chip and the OPA340 op-amp as a low noise buffer. The voltage reference has an accuracy of 0.2% and a low 20ppm/°C drift over temperature. The OPA340 is used as an operational amplifier buffer in between the REF3140 and the DDC114 to ensure the reference voltage pin on the DDC114 has sufficient input current at all times. The high accuracy temperature sensor chosen for this design is the LTC2997 from Linear Technology. It has an analog output of 4mV/°K.

Table 2.2: Daughter Board Power Budget

IC	Current		Input Voltage		Power	
REF3140	100	μA	5	V	0.0005	W
OPA340	750	μA	5	V	0.00375	W
LTC2997	150	μA	5	V	0.00075	W
DDC114 Analog	10.5	mA	5	V	0.525	W
DDC114 Digital	0.67	mA	3.3	V	0.02211	W
Total Power					55.211	mW
Total Power/Channel					13.80275	mW

Table 2.2 shows the typical power consumption of each component on the daughter board as well as a total power per channel.

As PVVISS is intended to measure small currents, parasitic capacitance must be minimized to reduce measurement error; therefore, an insulating terminal and wire system is used to remove the trace from the board. Wire leads are soldered to the input pins of the DDC114 and then to a polytetrafluoroethylene (PTFE) insulating solder terminal. Another wire is attached to the solder terminal and connected to the respective collector segment in the sensor head.

2.3.3 Part Simulation

Some output voltage drift is inherent in all voltage reference circuits, and Integrated Circuits (IC) are greatly influenced by temperature changes, which can amplify voltage drift. Designers must therefore select a reference chip and op-amp buffer which is minimally impacted by temperature changes. Also, researchers must be able to quantify the effects of temperature on the circuitry due to the temperature variability during spacecraft missions.

Figure A.1 shows the OPA340 op-amp output voltage variation as a function of temperature using Texas Instruments simulation software.

This analysis shows small deviations from the regulated output voltage of 4.096V over a range of temperatures typical to the LEO space environment. The simulation shows the OPA340 is a good candidate for buffering the precision reference voltage chip.

The LTC2997 is a high-accuracy analog output temperature sensor. It converts the temperature of an external sensor or its own temperature to an analog voltage output. For the PVVISS design, the internal temperature sensor is used. To ensure that the LTC2997 performs as expected, a simulation was run in LTSpice, as shown in Appendix A.2. The temperature simulation goes from 223.15°K to 348.15°K. The results are displayed in Appendix A.3.

DDC114 signal simulations were attempted to verify output data and signal integrity prior to designing the daughter board circuitry. This analysis was not possible, however, as the only simulation file provided by the manufacturer did not allow for SPICE simulation as they consider these details to be proprietary information. Although this analysis would have been favorable, researchers were able to continue design knowing the expected functionality of DDC114 based on manufacturer specifications.

2.3.4 Daughter Board Printed Circuit Board

The printed circuit board (PCB) layout was done by VPI PCB Design. The 2 layer PCB layout design is shown in Appendix A.4. All components, red pads, and traces are on the top layer as shown in Appendix A.4. The bottom layer is used for routing; the blue routing traces are also shown in AppendixA.4. The blue circular pads represent through hole components that have solder pads on both the top and bottom layers.

Once the layout was completed, the PCB files were sent to Quick Turn Circuits to fabricate the boards, and an engineer at the Center for Space Engineering was contracted to populate the components on two daughter board PCBs. The final printed circuit board assembly (PCBA), which includes the PCB and all of the components, can be seen in Appendix C.

2.4 Main Board

2.4.1 Circuit Design

The main board of the PVVISS circuit performs many functions including DDC114 control, power generation, grid voltage generation, conditioning, and control, and spacecraft communication over RS422 protocol. The board will control the individual retarding, suppression, and aperture grid voltages. It will report both grid voltage and current on each collector segment and general housekeeping numbers that include power rail voltages, and temperatures from both boards.

2.4.2 Part Selection

The main board electronics were based off the robust and versatile RPA designed by Lucy K. Fanelli et al [2]. The power budget for the main board excluding the 71% efficient DC/DC conversion is shown in Table 2.3.

The IGLOO FPGA has been selected as the main controller because of its small size, low power, and large amount of system gates in relation to its size. The IL3222 chip and the RS422 driver chip magnetically isolates the main PVVISS board from the spacecraft computer to ensure that spacecraft and PVVISS grounds do not connect. It interfaces with the FPGA over a basic Universal Asynchronous Receiver/Transmitter (UART) at 115,200 baud.

Separate Molex MicroD connectors were chosen for the RS422 port and instrument grid connection. These connectors were chosen for their compact size and pin number density. Instrument grid voltages are generated by the LTC2604 16 bit Digital to Analog Converter (DAC). This component can control up to four output channels. The FPGA interfaces to the LTC2604 over Serial Peripheral Interface (SPI).

The voltages generated by the LTC2604 are filtered to remove any high-frequency noise, which helps to maintain a clean DC voltage on the grids. An op-amp stage amplifies the voltage with a gain of 2.4 to have an output voltage range of 0 to +12 volts on the retarding grids.

Table 2.3: Main Board Power Budget

Main Board Power Budget			
Integrated Circuit	Typical Current	Input Voltage	Power
IL3122	25 mA	3.3 V	0.0825 W
AGLN250V5-VQG100	44 μA	1.5 V	0.000066 W
NC7WP14	2.6 mA	3.3 V	0.00858 W
FOX924B-10.000	6 mA	3.3 V	0.0198 W
OP497 (U8)	580 μA	15 V	0.0087 W
OP497 (U16)	580 μA	15 V	0.0087 W
LTC2604	1 mA	5 V	0.005 W
LTC2997	170 μA	5 V	0.00085 W
74LVC1T	2 μA	3.3 V	0.0000066 W
OP184 (U12)	1.45 mA	15 V	0.02175 W
LTC2997	170 μA	5 V	0.00085 W
OP184 (U14)	1.45 mA	15 V	0.02175 W
OP184 (U15)	1.45 mA	15 V	0.02175 W
OP497	580 μA	15 V	0.0087 W
ADS8343	1.5 mA	5 V	0.0075 W
DG406	21.5 μA	3.3 V	0.000071 W
SN74LVC2T45	24 mA	3.3 V	0.0792 W
Total Main Board Power			0.2957494 W
			295.7404 mW

A simulation was created to test the DAC, low pass filter, and gain stages to measure rise times based on points per sweep. This was done to find the integration time available to the DDC114 to collect data. The rise time is decided when the output voltage has reached 95% of its maximum. The simulation results are shown in Figure 2.2. The total rise time is calculated by multiplying the rise time from the simulation by how many points are in the sweep. As each sweep is performed in one second, the time left over for integration is found by Equation 2.6.

$$Total\ Rise\ Time = Rise\ Time * Points\ in\ Sweep \tag{2.4}$$

$$Time\ Left\ Over = 1 - Total\ Rise\ Time \tag{2.5}$$

$$Integration\ Time = \frac{Time\ Left\ Over}{Points\ in\ Sweep} \tag{2.6}$$

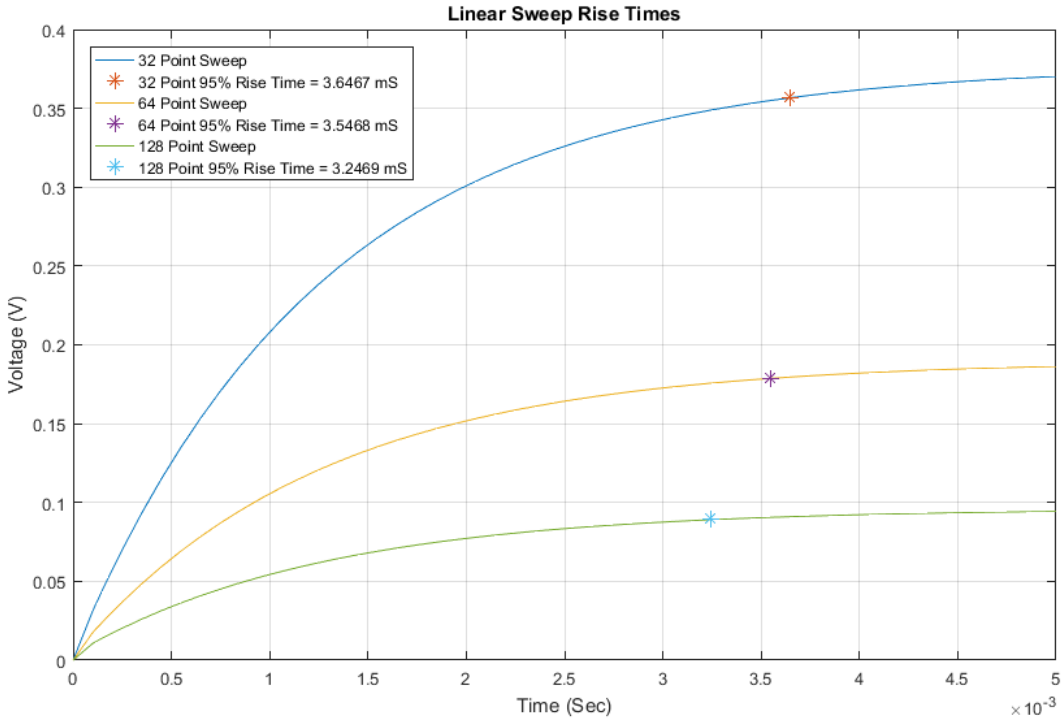

Fig. 2.2: Rise Times

Table 2.4 shows the rise time, total rise time, time left over, and integration time.

The frequency response of the op-amp stage is given in Figure B.5. The suppression grid drive has an extra op-amp stage to invert the voltage to produce a 0 to -12 volt output range. The frequency response of the op-amp stage for the suppression grid drive is given in Figure B.6.

Both the grid and system rail voltages are monitored using a combination of a multiplexer and an analog-to-digital converter (ADC). The ADS8343 runs on five volts; therefore, a voltage level translator is needed to lower the logic levels of the digital output to be 0 to +3.3 volts. The multiplexer selects from a one of eight possible housekeeping inputs to allow multiple functions on one ADC channel.

A highly accurate and low drift voltage reference chip is needed as a voltage reference

Table 2.4: Rise Time Table

	Rise Time (mS)	Rise Time * Points (mS)	Time Left Over (mS)	Integration Time (mS)
32 Point Linear Sweep	3.65	116.7	883.3	13.8
64 Point Linear Sweep	3.55	227	773	6.04
128 Point Linear Sweep	3.25	415.6	584.4	2.28

for the ADS8343. The LT1790 was found to be a suitable reference chip for this instrument. The initial accuracy of the output voltage is 0.05% and has a drift of 10ppm/°C. The power rail voltage monitors are created by using a simple voltage divider that brings them into the voltage range of the ADC (between 0 and 3.3 Volts).

The main board creates its own regulated power supplies from the spacecraft power system. The PVVISS design requires five different voltages for analog and digital circuitry. Four electrically isolated DC/DC converters are employed to generate four main power rails. A single DC/DC converter creates both positive and negative 15 V. By using isolated converters noise on the power system is reduced by breaking any potential ground loops.

2.4.3 Part Simulation

The voltage generation circuit is simulated using Tina-TI to quantify the noise generated by the output filter and gain stages of the grid voltage generation. Appendix B.1 shows the resulting simulation.

The grid voltage generation circuit was also simulated to verify its response to temperature. The same circuit model was used from the output noise simulation, with the exception of replacing the input voltage to be a constant 1 V DC. Figure B.2 shows the output voltage as a function of temperature. The intent of the simulation is to understand worst case scenarios, going from 223.15°K to 348.15°K.

An accurate and low-drift voltage reference is needed for PVVISS to provide a constant 2.5 volt reference since all of the analog to digital conversions use this reference voltage for the conversions. To ensure the output noise would not affect the ADC conversion and to quantify the voltage drift due to temperature, simulations were run using LTspice. Figure B.3 shows the noise on the output voltage as a function of frequency. Figure B.4 shows the output voltage as a function of temperature.

2.5 Design Wrap Up

This chapter has discussed the design for the PVVISS daughter board and main board. Each component in the circuit design has been examined and explanations are given as to why they were chosen. In-depth simulations and analyses have been introduced and discussed to verify full functionality of the instrument over the lifetime of the mission. Design testing and resulting conclusions can be found in subsequent chapters.

CHAPTER 3

PVVISS Testing

3.1 PCB Checkout and Verification

The PVVISS instrument underwent systematic verification to validate device functionality. Pictures of the test setup can be seen in Appendix D. Main board and daughter board testing procedures are outlined below.

3.1.1 Daughter Board Checkout and Verification

The daughter board checkout can be found in Appendix I. The tests include:

1. Component Layout
    - Verify orientation of all Integrated Circuts (ICs), polarized capacitors, and connectors on board prior to applying power.
    - Verify all passive components are populated correctly.
2. Power Checkout
    - Verify there is adequate resistance between each voltage and ground.
    - Supply board with power and verify all regulated output voltages before any additional components are connected to the board.
3. Signal Verification
    - Connect the communications cable to the main board or testing equipment.
    - Verify that the digital signals exist on their lines including the system clock.

4. Collector Currents

   - Connect the current source to one of the input terminals.
   - Set the current source to the reference range and record the output.

3.1.2 Main Board Checkout and Verification

The Main Board Checkout includes a section to program and verify the FPGA. This must be done before Signal and Collector Currents Verification on the daughter board can be completed.

3.2 Noise

Testing was performed to quantify the noise floor of the DDC114 and the daughter board circuity. The minimum measurable current requirement of 50pA was generated by a remote current source.

The mean and standard deviations for each integration time and capacitor range are shown in Figures E.1. The mean values for each integration time and capacitor range are shown in Tables E.1 and E.2. Figure E.2 shows the RMS values of the noise. The RMS noise values show the minimum threshold the instrument is able to measure. Based on this data, PVVISS is able to measure $50pA$ of current to varying degrees of accuracy given a long enough integration time and capacitor range (e.g. 13.583 mS and capacitor ranges 1-6).

The signal to noise ratio (SNR) is shown in Figure E.3. A SNR greater than one signifies more signal than noise. To calculate SNR, data was collected with fixed integration time and capacitor range. The difference of measured and expected values is used to calculate the noise value. The SNR in decibels is the ratio of the signal squared to that of the noise squared.

The collected data show that with 6mS integration time and the eighth capacitor range, the SNR increases as input signal increases. The data also indicates that the SNR increases after calibration.

3.3 Calibration

The data collected for each capacitor range and integration time are linear with a given slope and intercept. Based on the collected data, calibration equations were made and applied to further testing.

Calibration slope plots can be found in Figures F.1 and F.2. Calibration intercept plots can be found in Figures F.3 and F.4.

3.4 Mass

The mass of the completed circuit boards was measured using a gram scale to verify weight requirements. The daughter board has a mass of 11.8 grams, and the main board has a mass of 64.4 grams. The combined mass of the PVVISS electronics is 76.2 grams.

3.5 Power

The PVVISS was designed to be relatively low power. Based on initial simulations and data sheet specifications, it was determined that PVVISS would use at most 492 mW including a DC/DC conversion efficiency of 71%. During testing, however, it was found to use 1.38 W of power. This excessive power use was due to a number of factors including lower efficiency of the DC/DC converters than expected and minor design flaws. The DC/DC isolating converters have efficiency curves as a function of current draw, therefore when little current is drawn the conversion is inefficient and wastes 400.2 mW of power.

Design errors occurred during PVVISS development, which also impacted power draw. The clamping diodes for the grid drive circuits were designed incorrectly, and the wrong pins were connected to ground and the voltage rail, which wasted 192.15 mW of power. Also, the feedback resistors in the grid drive amplification stage were found to leak current. The resistors waste 125 mW of power; current leakage would not occur if feedback resistors were 100 times greater than originally designed. The RS422 chip control lines were also found to be floating, as the FPGA was not controlling them, thereby wasting 211.86 mW of power within the chip and with a 100 ohm load.

Table 3.1 shows the power consumed by components on each voltage rail after the DC/DC converter. The RS422 chip and clamping diodes were taken out of the circuit since these issues are easy to correct. Based on the data collected, this PVVISS design does not meet the power design requirements.

Table 3.1: Power Table

	Part Number	**Max Current**	**Measured Current**	**Total Output Current**	**Efficiency based on TOC**	**Power**
Analog 5V	RS0-1205SZ	83 mA	31mA	37%	67%	155 mW
Digital 3.3 V	NCS1S1203SC	303 mA	7.8 mA	3%	8%	25.74 mW
Digital 5V	NCS1S1205SC	200 mA	0.01 mA	0.01%	1%	0.05 mW
Analog ±15V	TDR 3-1223WISM	100 mA	18 mA	18%	70%	270 mW
					Total Power	450.79 mW

3.6 Telemetry Rate

The PVVISS instrument was designed for a baud rate of 115200 over RS422. Communication between the computer and PVVISS hardware is done with a USB to UART controller. This meets the telemetry rate requirement.

3.7 Retarding Grid Sweep Modes and Points

There are four sweep modes that the instrument can perform. The sweep modes are programmable in the firmware and include:

1. 32 point linear sweep
2. 64 point linear sweep
3. 128 point linear sweep
4. Constant voltage

The number of sweep modes and sweep points satisfy the requirement.

3.8 Collector Current Resolution

The DDC114 has two output resolutions: 16 and 20 bits. PVVISS uses the 20 bit resolution, which satisfies the design requirement.

3.9 Temperature

All temperatures for critical components were verified against design requirements, and are recorded in Table 3.2. Overall, all components met both high and low temperature requirements, and high temperature design goal. Only two ICs (the FPGA and external oscillator for the FPGA) do not meet the design goal of a minimum operating temperature of −35°C.

Table 3.2: Temperatures

Main Board				
Designator	Manufacturer	MPN	Operating Temperature	Survival Temperature
U1	NVE	IL3222-3E	−40°C to +85°C	−65°C to +150°C
U4	ACTEL	AGLN250V5-VQG100	−20°C to +85°C	−65°C to +150°C
U5	Fairchild	NC7WP14P6X	−40°C to +85°C	−65°C to +150°C
U6	Fox	FOX924B-10.000	−30°C to +85°C	−40°C to +85°C
U7,U8,U16	Analog Devices	OP497FS	−40°C to +85°C	−65°C to +150°C
U9	Linear Tech	LTC2604IGN#PBF	−40°C to +85°C	−65°C to +150°C
U10,U13	Linear Technology	LTC2997HDCB#TRMPBF	−40°C to +125°C	−65°C to +150°C
U11	TI	SN74LVC1T45MDCKREP	−55°C to +125°C	−65°C to +150°C
U12,U14,U15	Analog Devices	OP184ES	−40°C to +125°C	−65°C to +150°C
U17	TI	ADS8343EB	−40°C to +85°C	−65°C to +150°C
U18	Maxim	DG406EUI+	−40°C to +85°C	−65°C to +150°C
U19	TI	SN74LVC2T45DCUR	−40°C to +85°C	−65°C to +150°C
U24	Linear Tech	LT1790ACS6-2.5#TRMPBF	−40°C to +85°C	−65°C to +150°C

Daughter Board				
Designator	Manufacturer	MPN	Operating Temperature	Survival Temperature
U1	Texas Instruments	DDC114IRTCT	−40°C to +85°C	−60°C to +150°C
U2	Texas Instruments	OPA340NA/3K	−55°C to +125°C	−55°C to +125°C
U3	Texas Instruments	REF3140AIDBZT	−40°C to +125°C	−65°C to +150°C
U4	Linear Technology	LTC2997HDCB#TRMPBF	−40°C to +125°C	−65°C to +150°C

DC/DC				
Designator	Manufacturer	MPN	Operating Temperature	Survival Temperature
U20	Traco Power	TDR 3-1223WISM	−40°C to +85°C	−55°C to +125°C
U21	Murata	NCS1S1203SC	−40°C to +105°C	−50°C to +125°C
U22	Murata	NCS1S1205SC	−40°C to +105°C	−50°C to +125°C
U23	Recom Power	RSO-1205SZ	−40°C to +85°C	−10°C to +85°C
U25	Murata	LXDC2HL15A-051	−40°C to +85°C	−55°C to +125°C

3.10 IV Curve Simulation

IV curve simulation was based on anticipated environmental factors. For example, ionospheric densities can be small, only a few 100 *ions per* cm^3, but the average lowest measurement expected for instrumentation is $500 - 1000$ *ions per* cm^3. The high end of

measurement density is on the order of 10^6 *ions per* cm^3. Plasma temperatures are usually somewhere in the range of 800 k $-$ 2000 k.

Using an optical transparency of the grid stack of 50%, collector plate area of 6.75 cm^2, a spacecraft velocity of 7500 *meters per second* and a total ion density consisting of 85% Oxygen and 15% Nitrogen of $5,000$ *ions per* cm^3, a simulation was run to test the performance of PVVISS near the low end of the expected ion densities. The RMS deviation for the measured from ideal is 197 pA. The RMS deviation for the calibrated from ideal 8.07 pA The results of the simulation are shown in Figure 3.1.

Normal ionospheric densities are in the range of $100,000$ *ions per* cm^3. Figure 3.2 shows the simulation results of $100,000$ *ions per* cm^3. The RMS deviation for the measured from ideal 1.21 nA. The RMS deviation for the calibrated from ideal 205 pA.

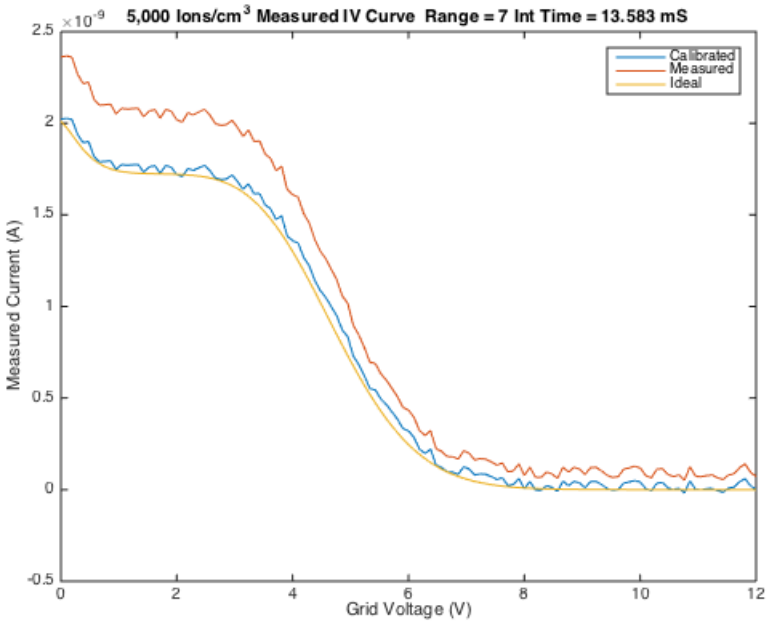

Fig. 3.1: IV Curve Simulation A

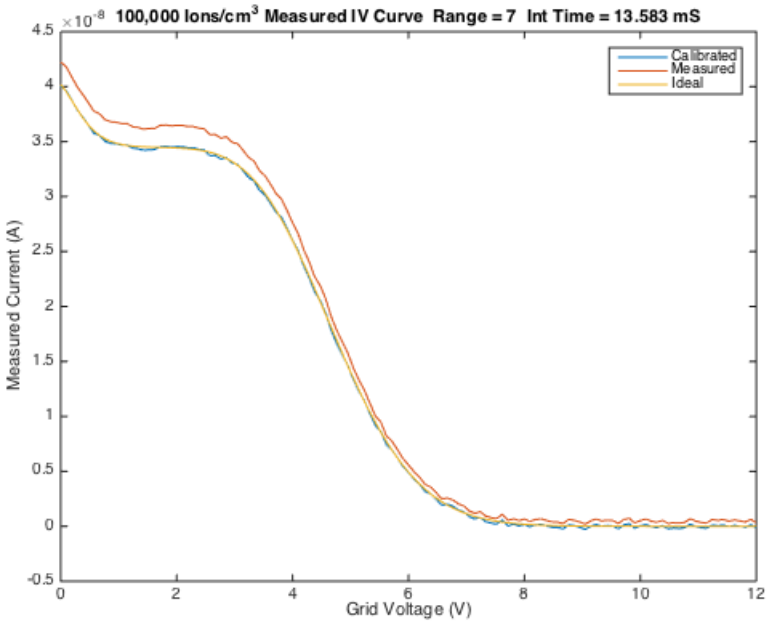

Fig. 3.2: IV Curve Simulation B

CHAPTER 4

Conclusions

This thesis outlines the design, testing, and verification of an instrument that encompasses the functionality of both the RPA and IDM and is compatible with CubeSat specifications. The PVVISS successfully meets CubeSat parameters for mass and size. Initial testing also shows that selected components are compatible with LEO environment including temperature. In addition to meeting size and environmental specifications, testing revealed that PVVISS is able to successfully meet most electrical requirements, including demonstrating that the DDC114 is a feasible option for measuring collector currents. Although additional testing and design clean-up is warranted, successful grid bias, sweep time and modes, and appropriate current resolution simulations show the instrument has the potential to successfully perform as an RPA/IDM. As mentioned in Chapter 3, PVVISS did not meet power specifications. The power components could be altered to meet specifications, which are outlined in Section 4.1. Table 4.1 gives the Pass/Fail results of the requirements.

4.1 Future Work

Although this preliminary instrument showed the PVVISS design to be a viable option for continued study and flight, testing revealed a number of components that could be improved when updating the design.

These fixes include:

- Design alterations to improve power consumption:
  - Design grid amplification stage clamping diodes to have the correct pin and net connections.

Table 4.1: Requirements Pass/Fail

Parameter	**Requirement**	**Pass/Fail**
Mass	$\leq$ 0.5 kg	Pass
Power	$\leq$ 0.5 Watts DC	Fail
Size	$\leq$ 3.5" x 3.5" x 2"	Pass
Operating Temperature	$\leq -10°C$	Pass
Operating Temperature	$\geq 40°C$	Pass
Science Temperature	$\leq 5°C$	Pass
Science Temperature	$\geq 30°C$	Pass
Telemetry Rate	$\geq$ 2048 bits/s	Pass
Min Collector Currents	$\geq 50pA$	Pass
Max Collector Currents	$\leq 5\mu A$	Pass
Retarding Grids (RGs) Bias	$\leq$ 0 V	Pass
Retarding Grids (RGs) Bias	$\geq$ 12 V	Pass
Suppressor Grid Bias	$\geq$ 0 V	Pass
Suppressor Grid Bias	$\leq$ -12 V	Pass
RG Sweep Points	$\geq$ 32 Pts	Pass
RG Sweep Time	$\leq$ 1 s	Pass
Sweep Modes	$\geq$ 1	Pass
Collector Current Resolution	$\geq$ 16 bits	Pass

  - Increase grid amplification stage feedback resistors by two orders of magnitude to reduce resistor power consumption.
  - Reevaluate the DC/DC converters, and consider using a single DC/DC converter for digital and another for analog. Linear regulators would then be used to step down both the main digital and analog voltages to the other needed voltage levels.

- FPGA selection:
  - If possible, future researchers should consider using an FPGA that is radiation tolerant.

- Consider use of a multiplexer:
  - Instead of using a multi-channel ADC together with a multiplexer, future design may be improved if a single channel ADC was used in combination with a

multiplexer. This would allow the device to switch between all the housekeeping inputs on the multiplexer and simplify control of the ADC.

- Alternative communication chip:
  - Although the RS422 interface adequately functioned in the PVVISS design, future works may consider using more common interface such as LVDS or RS232. This would allow the design to be more compatible with a variety of flight computers.
- Noise reduction
  - PVVISS test data had excessive noise, which was likely due to the laboratory testing environment. Ideally, future testing would include instrument shielding from all RF interference.

4.2 Adaptability and Future Feasibility

PVVISS a great candidate for a variety CubeSat missions with varying flight parameters. Initially, PVVISS can perform as an RPA/IDM instrument. It can change current range, retarding grid sweep points, sweep time, sweep modes, retarding grid maximum and minimum voltages, and DDC114 resolution.

PVVISS also met most crucial temperature parameters. With small modifications, this instrument is compatible with temperatures to be seen on spacecraft missions.

PCB sizes are compatible with CubeSat size requirements. Future designs will require small changes to include components of required power draw, which will allow future revisions to be compatible with CubeSat specifications.

Even with the shortcomings of the initial design and test structure, the PVVISS design encompasses components with high adaptability to potential flight parameters. This flexibility, in combination with its reduced size when compared to historical instruments, proves PVVISS to have been a successful preliminary testing instrument which may be further

improved with future design and testing work. A mock-up of the 3D structure for the next revision of PVVISS is shown in Appendix J.

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APPENDICES

APPENDIX A

Daughter Board Simulation Plots

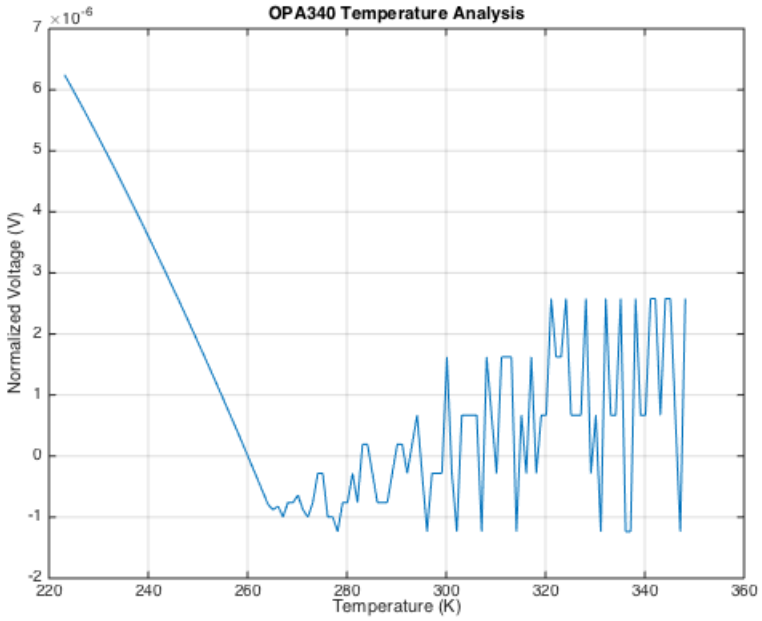


Fig. A.1: OPA340 Temperature Analysis

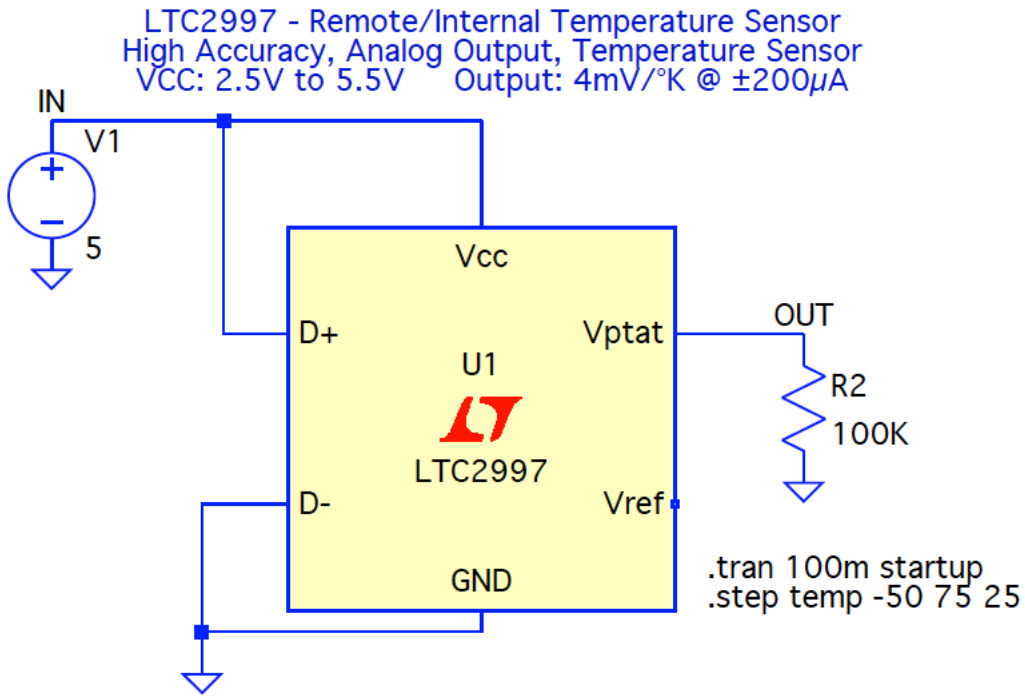


Fig. A.2: LTC2997 Simulation Circuit

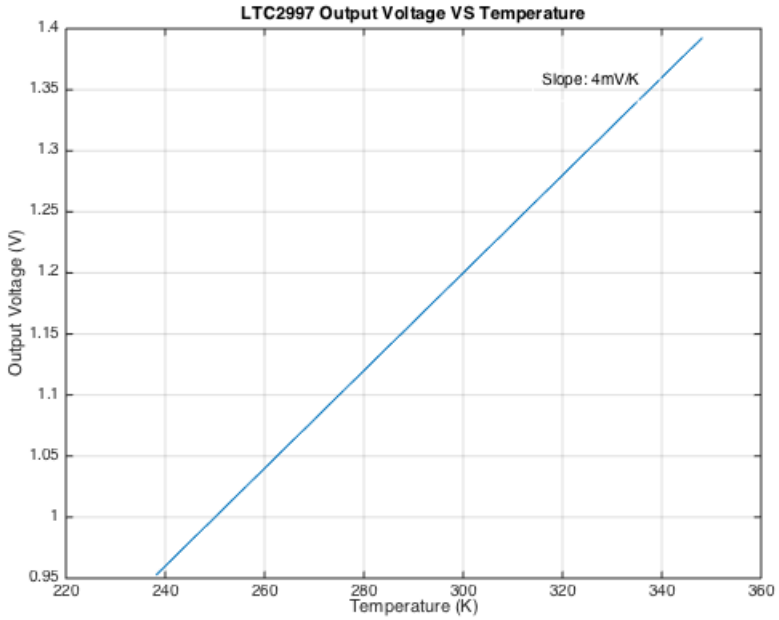


Fig. A.3: LTC2997 Temperature Simulation

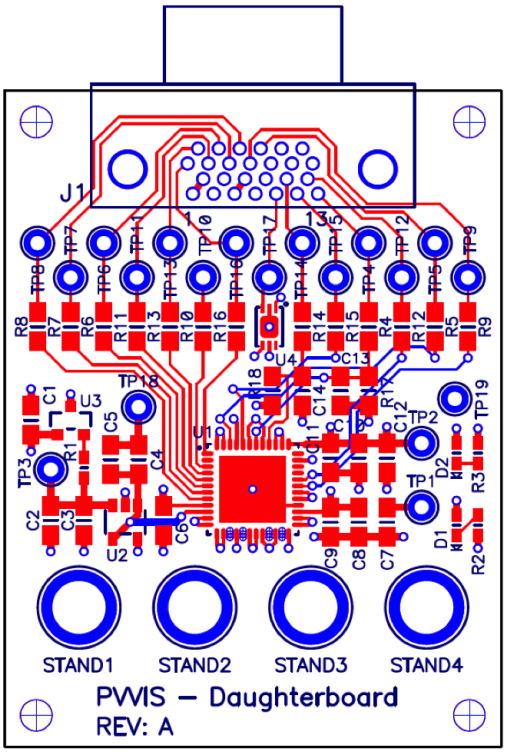


Fig. A.4: Daughter Board PCB Layout

APPENDIX B

Main Board Simulation Plots

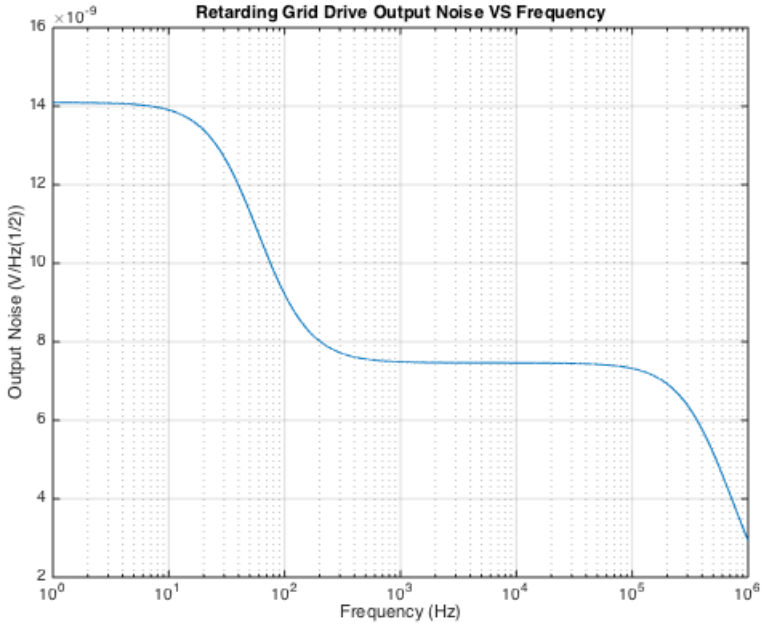


Fig. B.1: Retarding Grid Drive Output Noise VS. Frequency

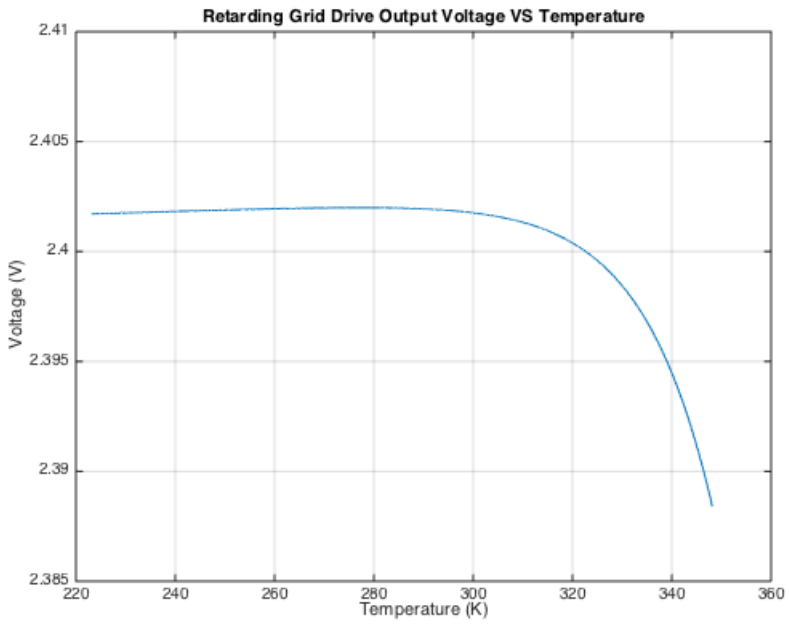


Fig. B.2: Retarding Grid Drive Output Voltage VS. Temperature

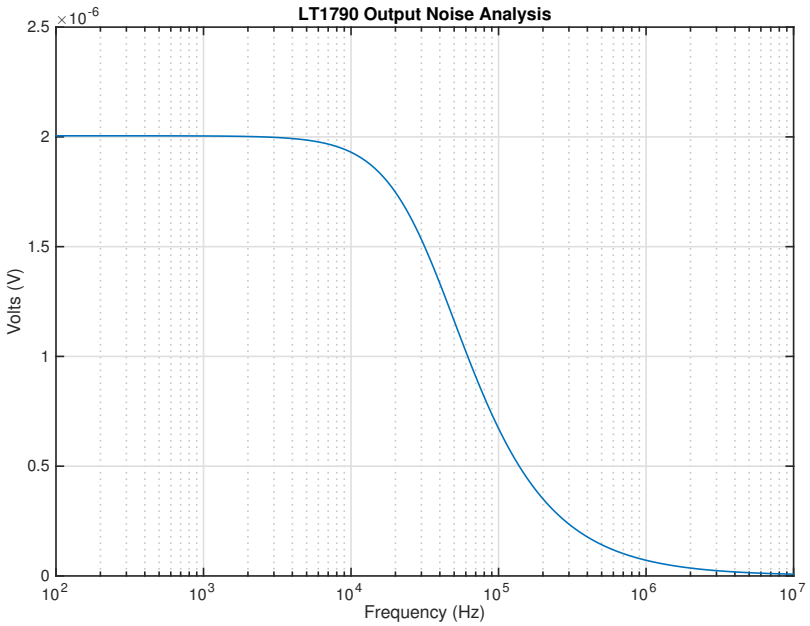


Fig. B.3: LT1790 Output Voltage Noise VS. Frequency

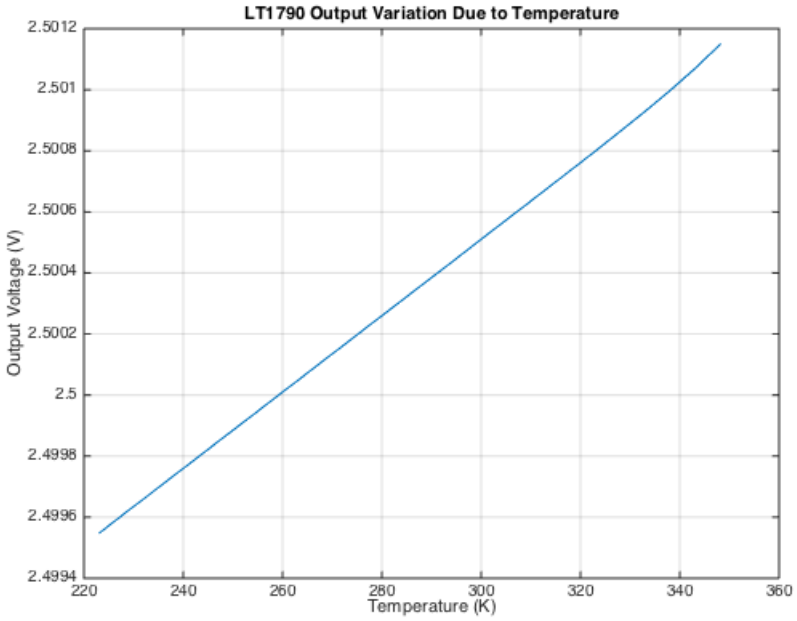


Fig. B.4: LT1790 Output Voltage VS. Temperature

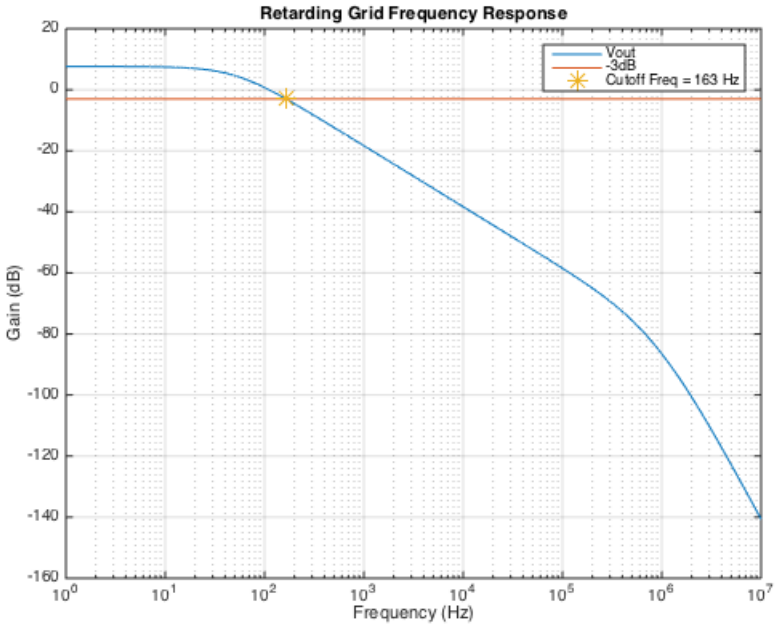


Fig. B.5: Retarding Grid Frequency Response

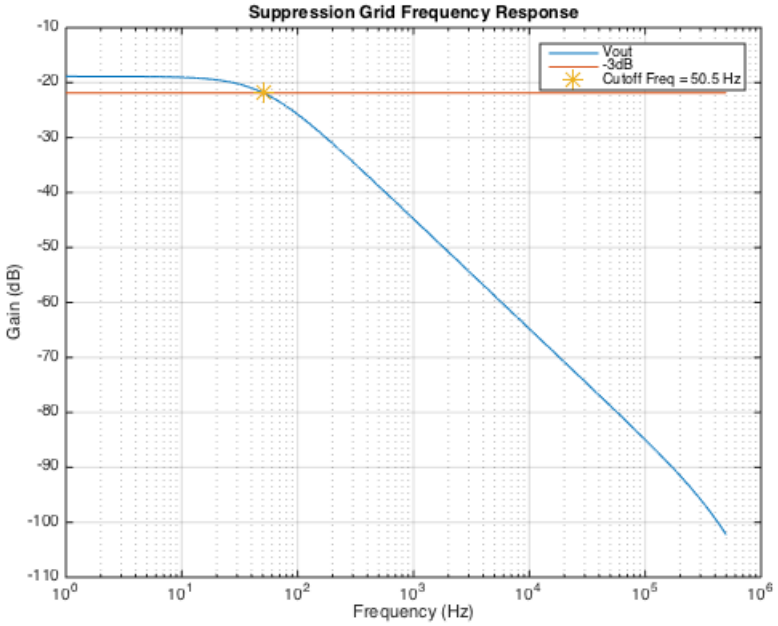
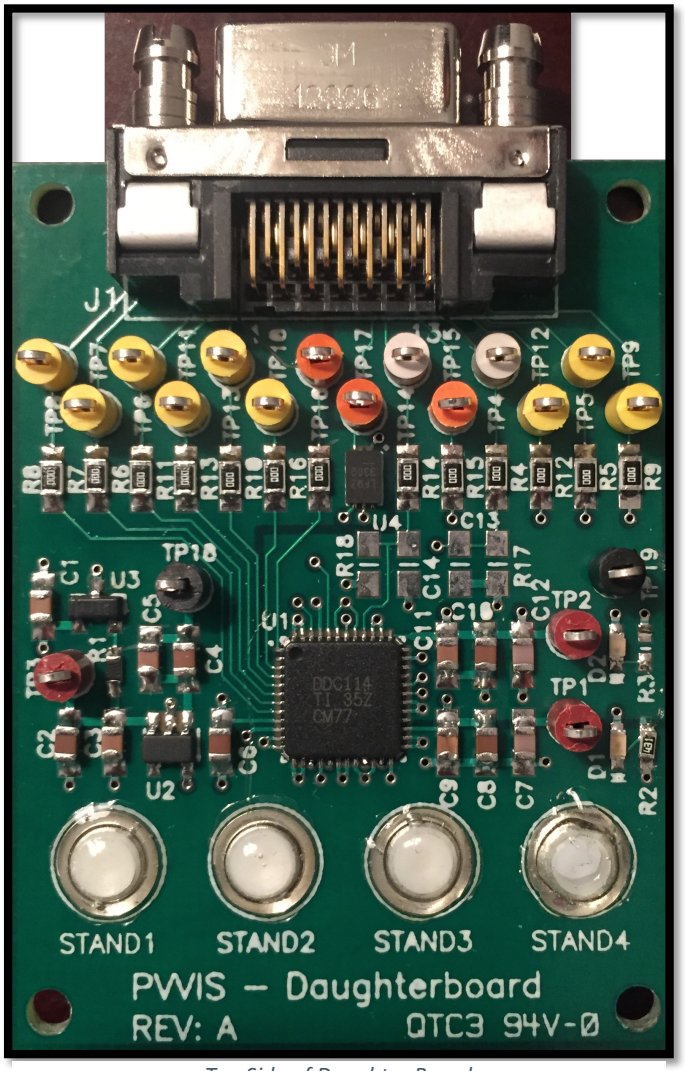


Fig. B.6: Suppression Grid Frequency Response

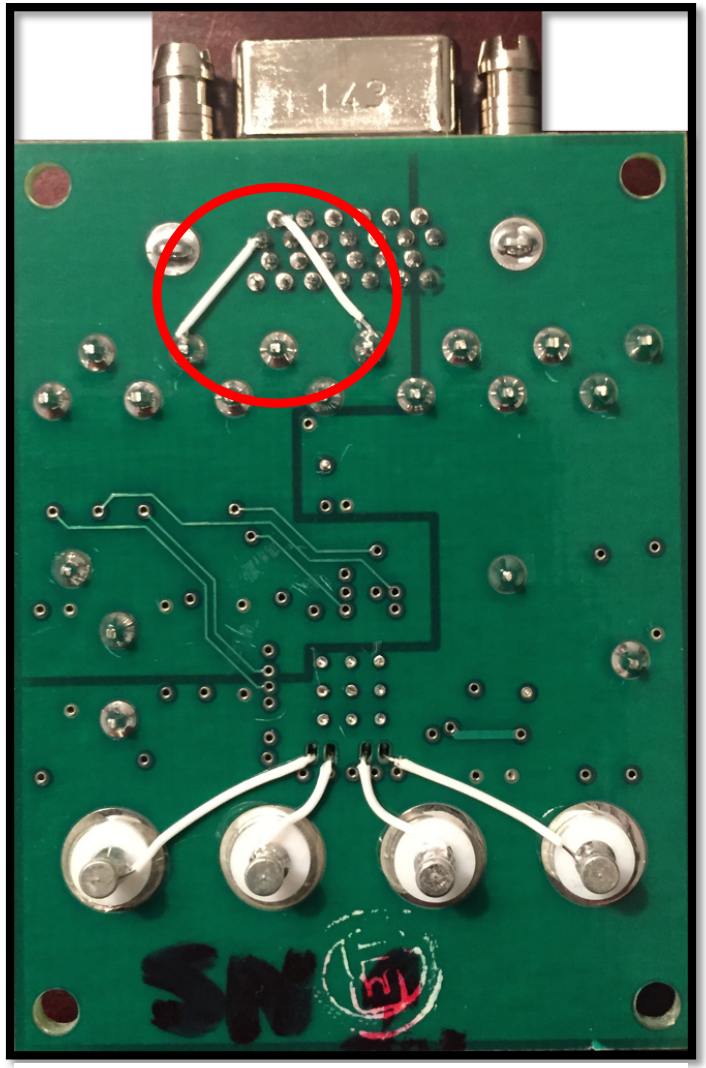
APPENDIX C

Daughter Board PCBA

White jumpers implemented to fix cameralink spec incompatibility with PVVISS design



Top Side of Daughter Board



Bottom Side of Daughter Board

APPENDIX D

PVVISS Test Setup

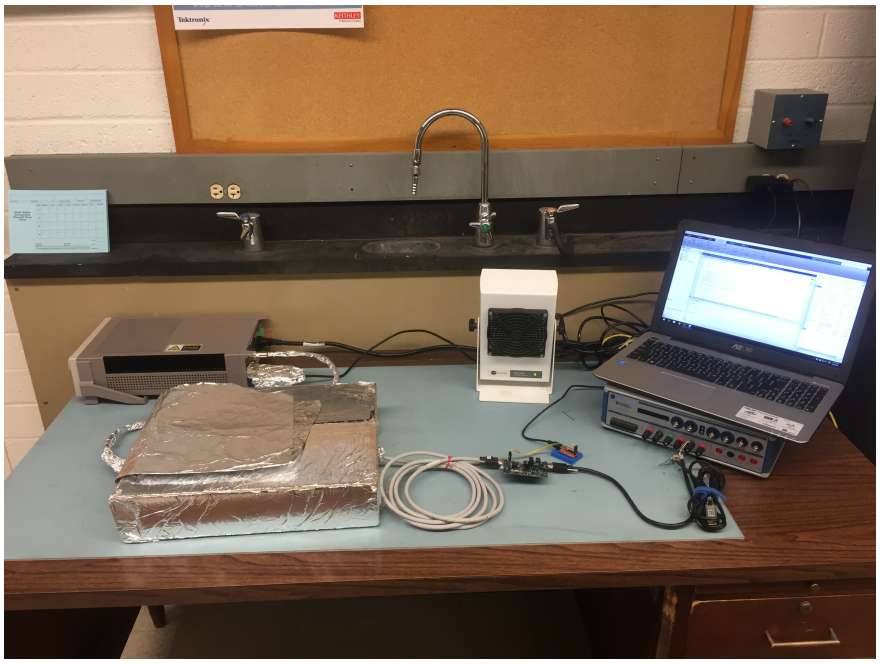


Fig. D.1: PVVISS Test Setup

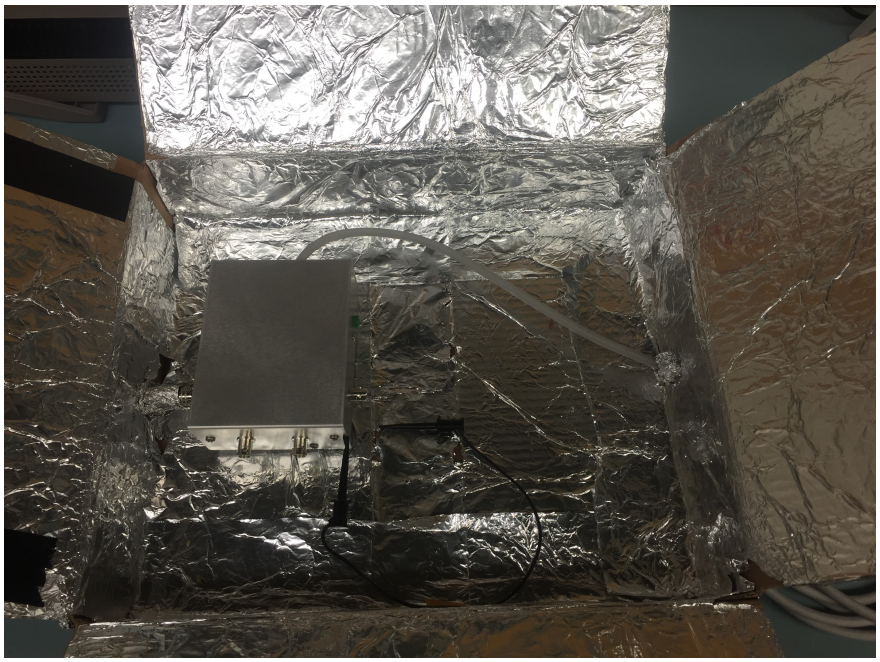


Fig. D.2: Inside Foil Box

APPENDIX E

PVVISS Noise

Table E.1: Mean Table A

	Capacitor Range 1	**Capacitor Range 2**	**Capacitor Range 3**	**Capacitor Range 4**
2.2668 mS	33.85pA	41.11pA	55.24pA	40.6pA
6.8064 mS	-39.73pA	-7.99pA	-2.45pA	12.8pA
13.583 mS	1.79pA	26.6pA	16.18pA	18.89pA

Table E.2: Mean Table B

	Capacitor Range 5	**Capacitor Range 6**	**Capacitor Range 7**	**Capacitor Range 8**
2.2668 mS	36.39pA	48.56pA	41.13pA	19.59pA
6.8064 mS	34.07pA	76.94pA	8.69pA	16.67pA
13.583 mS	18.35pA	24.42pA	24.42pA	24.93pA

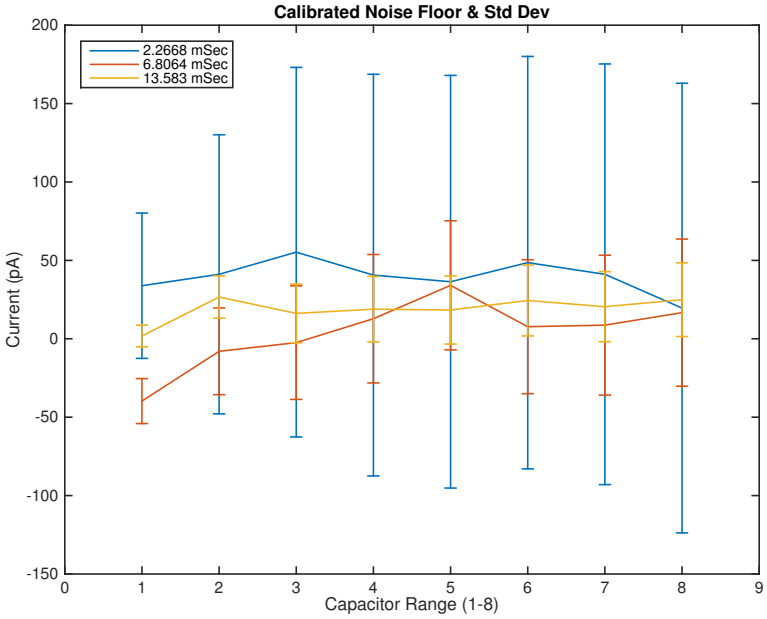


Fig. E.1: PVVISS Noise Floor

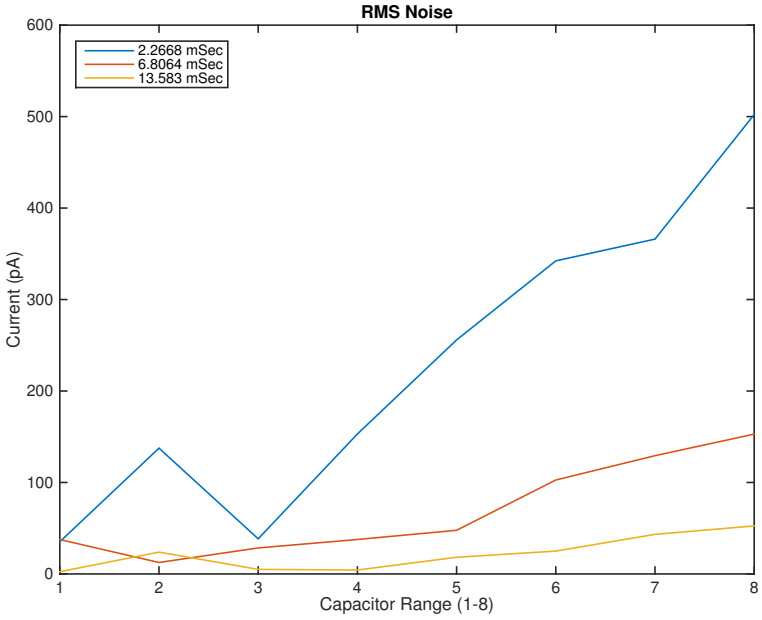


Fig. E.2: PVVISS RMS Noise Values

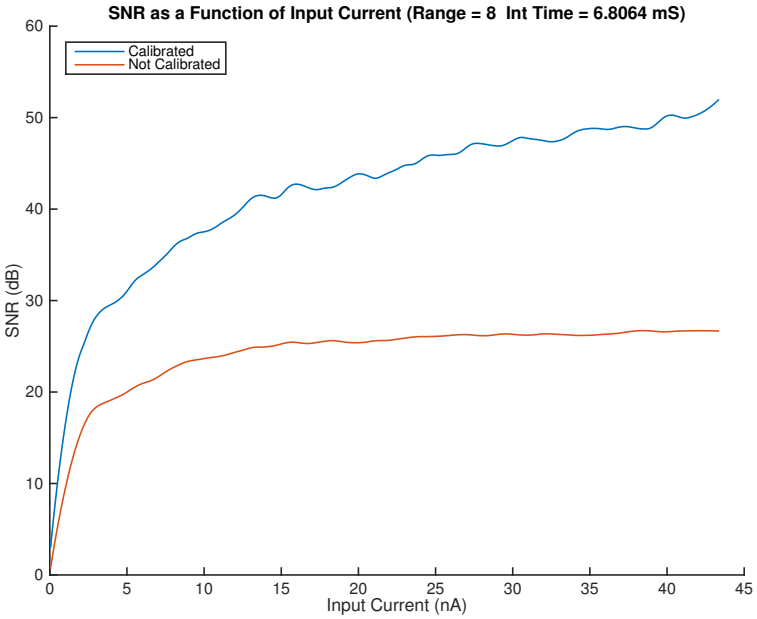


Fig. E.3: Signal to Noise Ratio

APPENDIX F

PVVISS Calibration

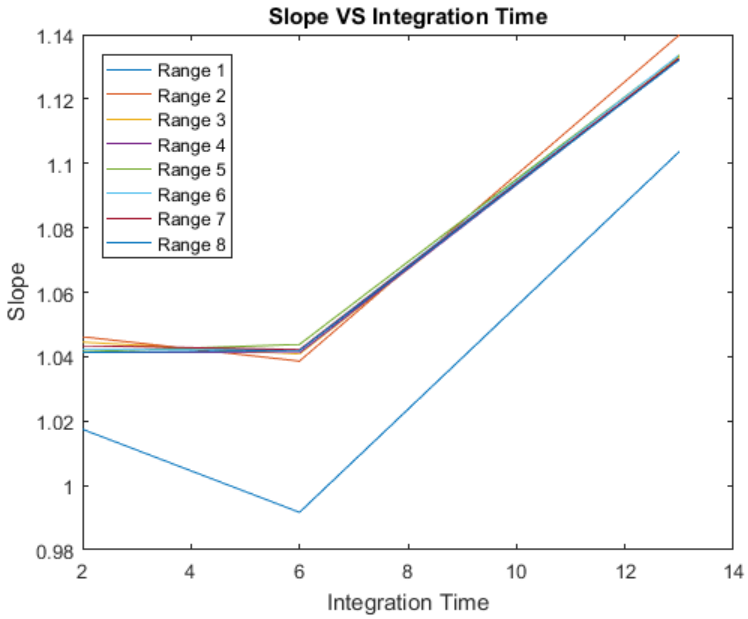


Fig. F.1: Calibration Equation Slope Based on Integration Time

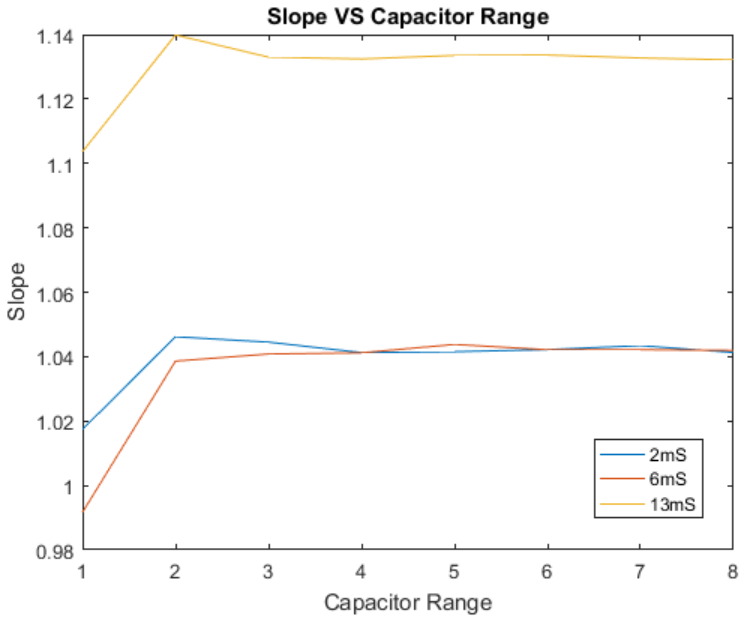


Fig. F.2: Calibration Equation Slope Based on Capacitor Range

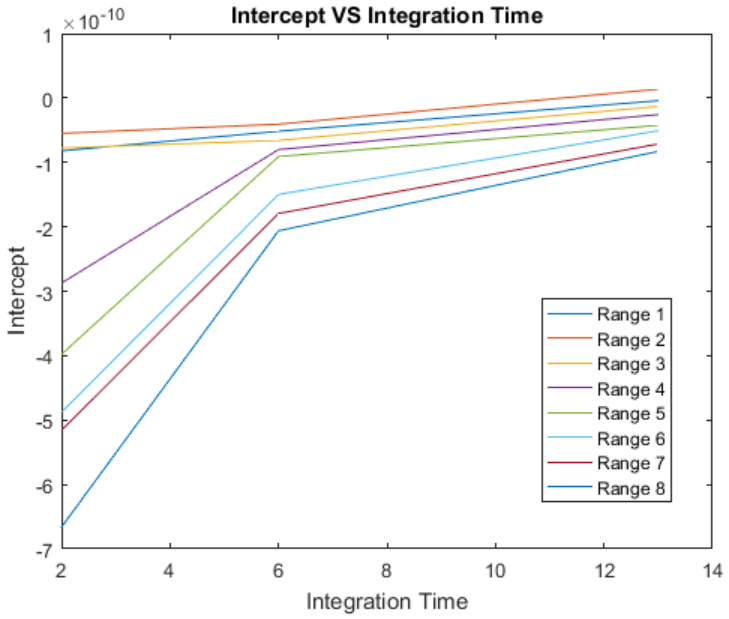


Fig. F.3: Calibration Equation Intercept Based on Integration Time

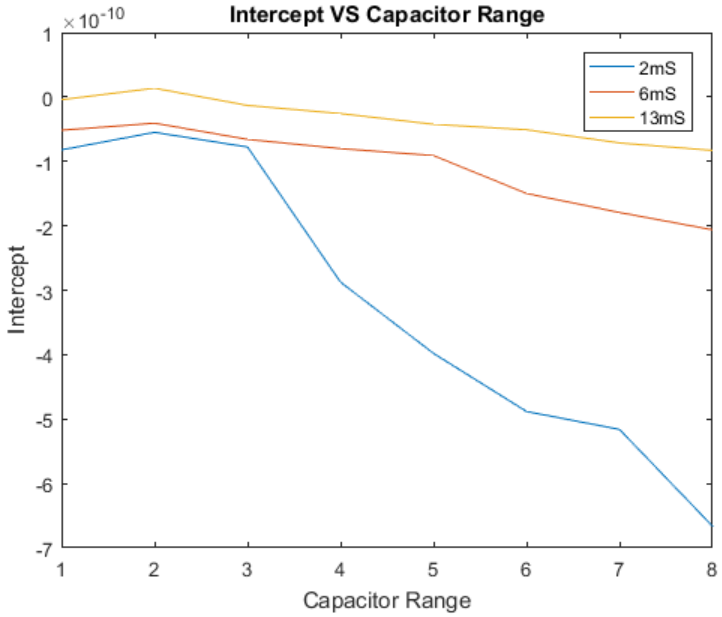


Fig. F.4: Calibration Equation Intercept Based on Capacitor Range

Table F.1: Calibration Slopes

Slope Table			
Range	2mS Int Time	6mS Int Time	13mS Int Time
1	1.017437529	0.991660761	1.103631447
2	1.046175533	1.038614251	1.139873371
3	1.044500842	1.040818584	1.132998053
4	1.041260568	1.04117947	1.132437081
5	1.041530922	1.043797133	1.133525633
6	1.042181595	1.042138948	1.133648787
7	1.043414997	1.042160134	1.13272876
8	1.041289807	1.041937368	1.132151564

Table F.2: Calibration Intercepts

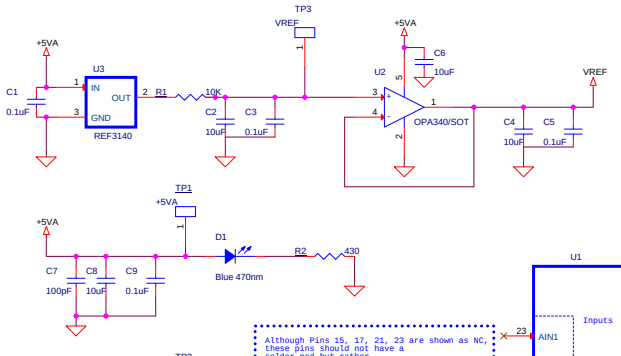
Intercept Table			
Range	2mS Int Time	6mS Int Time	13mS Int Time
1	-8.21248E-11	-5.1609E-11	-4.21E-12
2	-5.49E-11	-4.07E-11	1.37E-11
3	-7.77E-11	-6.58E-11	-1.31E-11
4	-2.87E-10	-8.02E-11	-2.57E-11
5	-3.98E-10	-9.10E-11	-4.23E-11
6	-4.88E-10	-1.50E-10	-5.09E-11
7	-5.16E-10	-1.79E-10	-7.14E-11
8	-6.66E-10	-2.06E-10	-8.29E-11

APPENDIX G

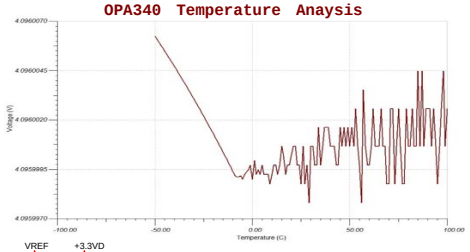
Schematics

G.1 Daughter Board

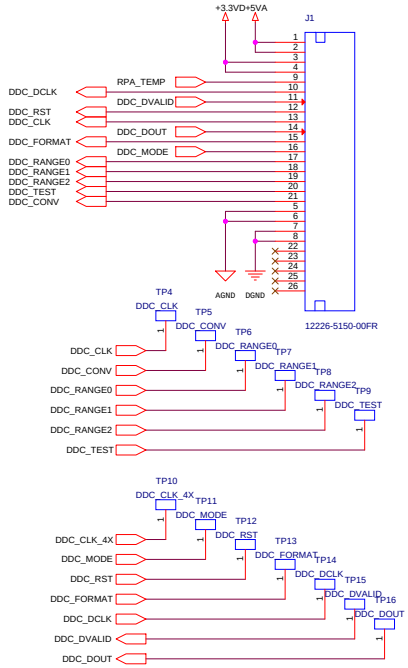
Power Conditioning



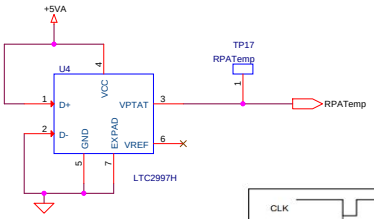
OPA340 Temperature Anaysis

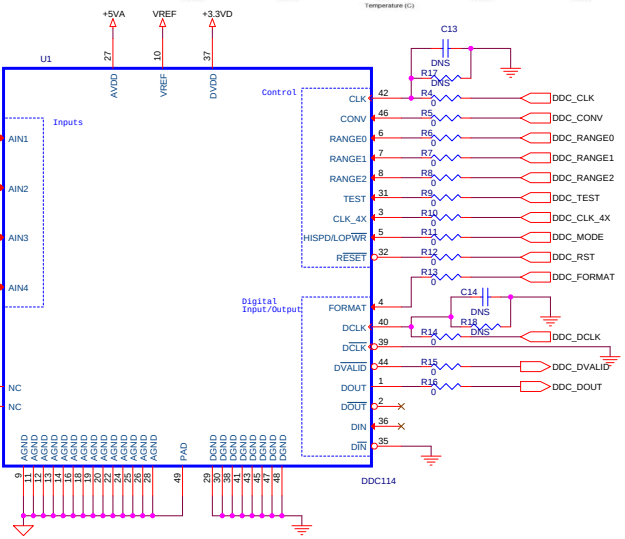


Power and Signal Connector Interface



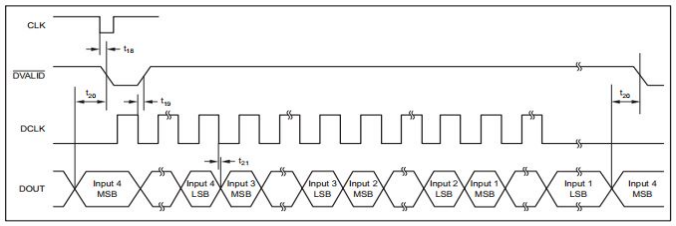
Temperature Sensor

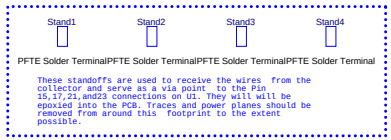


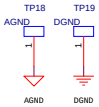


Although Pins 15, 17, 21, 23 are shown as NC, these pins should not have a solder pad but rather, a through-hole beneath it to keep it separate/isolated from the PCB.

DDC114 Timing Diagram

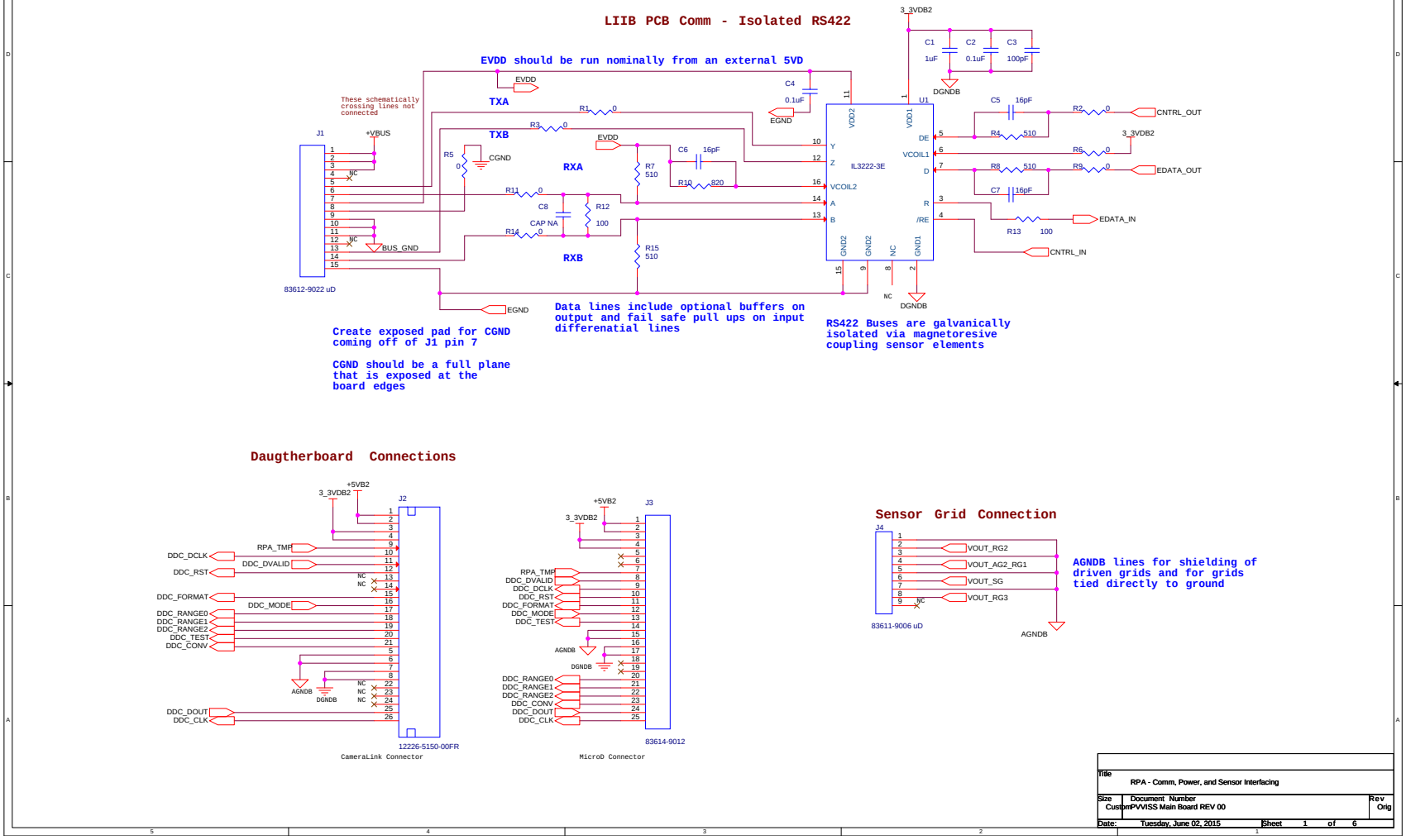


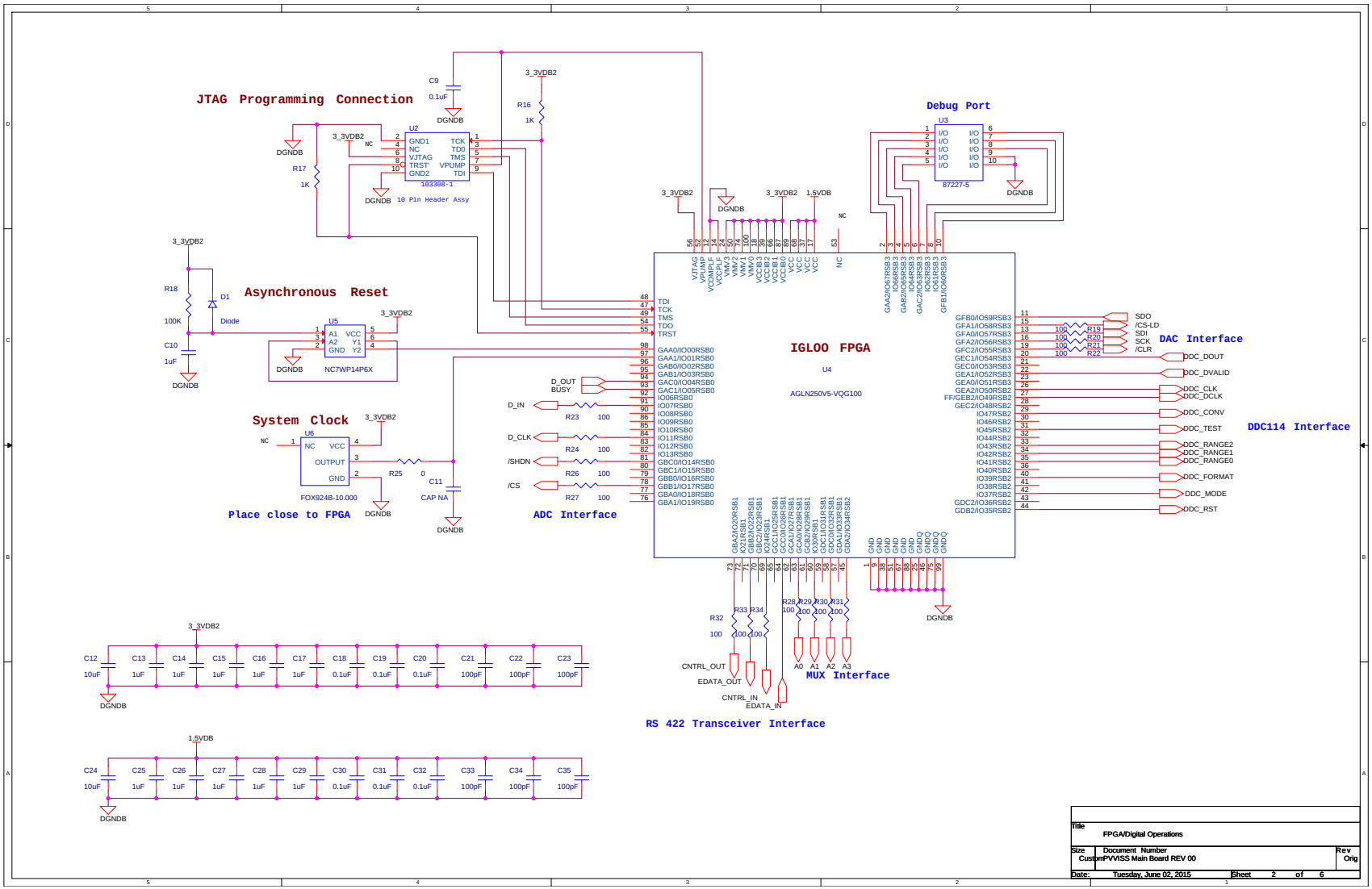


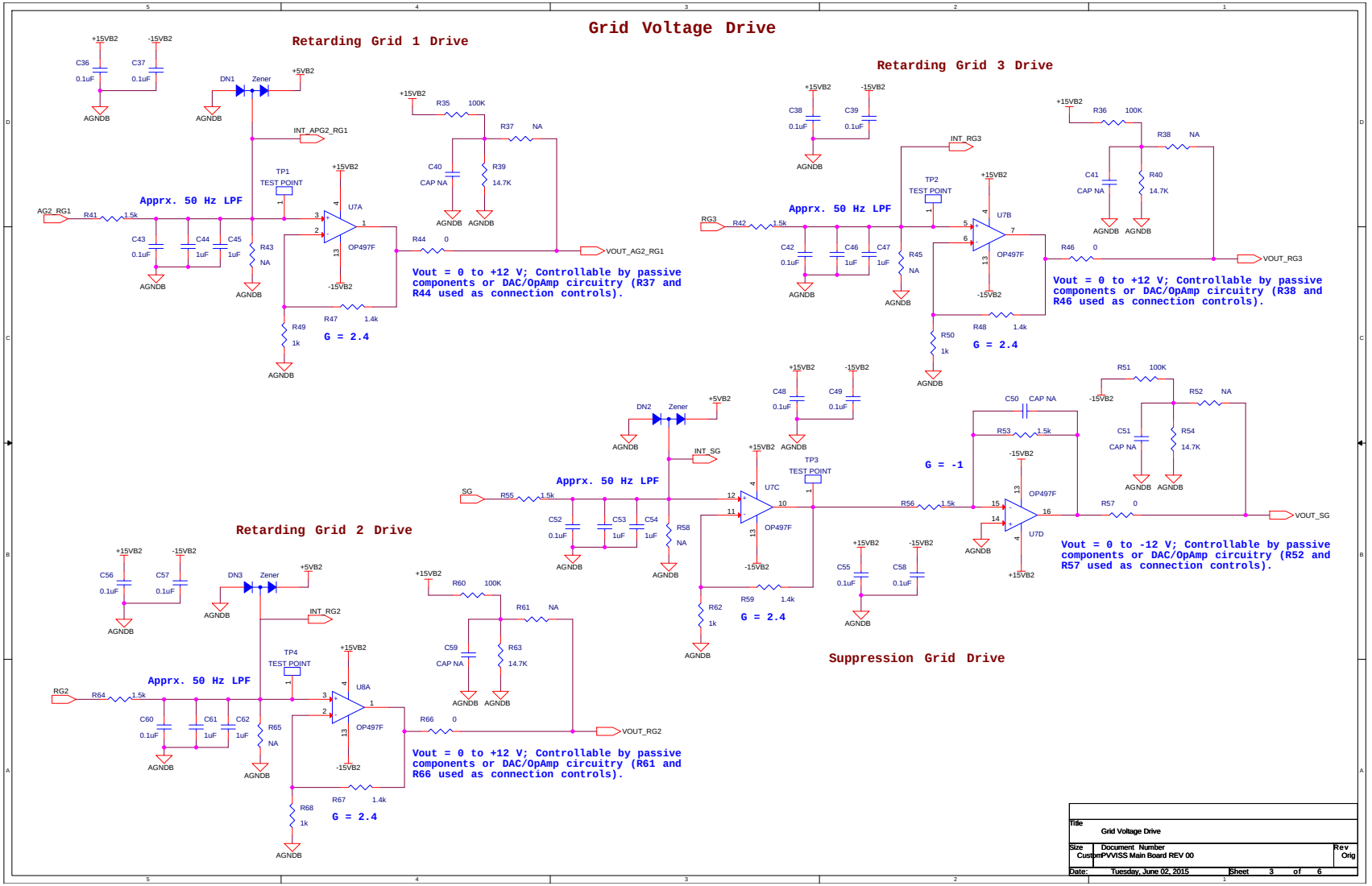


Title: PVVIS Daughter Board		
Size	Document Number <Doc>	Rev 00
Date: Friday, January 30, 2015	Sheet 1 of 1	

G.2 Main Board

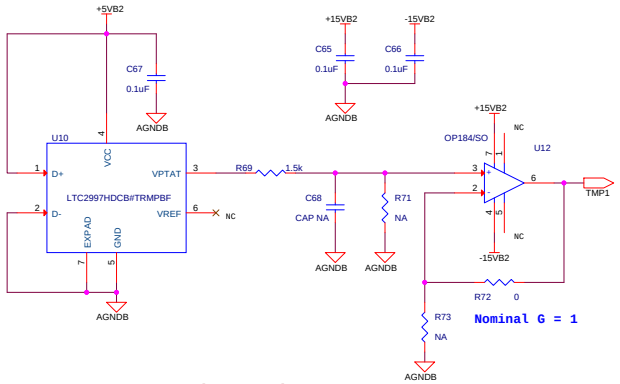

LIIB PCB Comm - Isolated RS422
EVDD should be run nominally from an external 5VD
These schematically crossing lines not connected
TXA
TXB
RXA
RXB
J1
+VBUS
BUS_GND
83612-9022 uD
EVDD
EGND
CGND
R1
R3
R5
R7
510
R10
820
C6
16pF
R11
R12
100
R14
R15
510
C8
CAP NA
C4
0.1uF
U1
IL3222-3E
VDD2
VDD1
GND2
GND2
NC
GND1
VCOIL2
VCOIL1
DE
D
R
/RE
3_3VDB2
C1
1uF
C2
0.1uF
C3
100pF
DGNDB
C5
16pF
R2
CNTRL_OUT
R4
510
R6
R8
510
R9
EDATA_OUT
C7
16pF
R13
100
EDATA_IN
CNTRL_IN
Create exposed pad for CGND coming off of J1 pin 7
CGND should be a full plane that is exposed at the board edges
Data lines include optional buffers on output and fail safe pull ups on input differenatial lines
RS422 Buses are galvanically isolated via magnetoresive coupling sensor elements
Daugtherboard Connections
+5VB2
3_3VDB2
J2
RPA_TMP
DDC_DCLK
DDC_DVALID
DDC_RST
DDC_FORMAT
DDC_MODE
DDC_RANGE0
DDC_RANGE1
DDC_RANGE2
DDC_TEST
DDC_CONV
DDC_DOUT
DDC_CLK
AGNDB
DGNDB
12226-5150-00FR
CameraLink Connector
J3
83614-9012
MicroD Connector
Sensor Grid Connection
J4
VOUT_RG2
VOUT_AG2_RG1
VOUT_SG
VOUT_RG3
83611-9006 uD
AGNDB lines for shielding of driven grids and for grids tied directly to ground
Title
RPA - Comm, Power, and Sensor Interfacing
Size
Custom
Document Number
PVVISS Main Board REV 00
Rev
Orig
Date:
Tuesday, June 02, 2015
Sheet
1
of
6


JTAG Programming Connection
Asynchronous Reset
System Clock
Place close to FPGA
ADC Interface
IGLOO FPGA
U4
AGLN250V5-VQG100
Debug Port
DAC Interface
DDC114 Interface
MUX Interface
RS 422 Transceiver Interface
10 Pin Header Assy
Diode
NC7WP14P6X
FOX924B-10.000
CAP NA
87227-5
Title
FPGA/Digital Operations
Size
Custom
Document Number
PVISS Main Board REV 00
Rev
Orig
Date:
Tuesday, June 02, 2015
Sheet
2
of
6

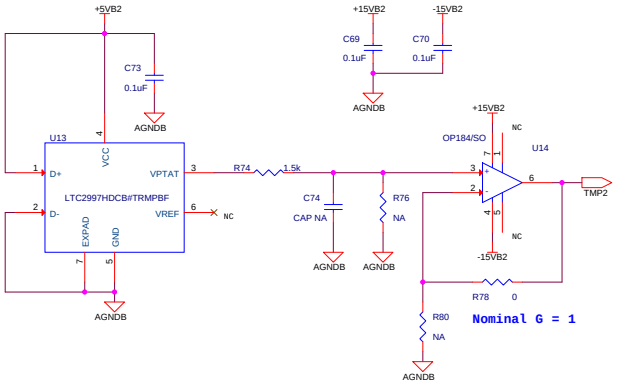

Grid Voltage Drive
Retarding Grid 1 Drive
Retarding Grid 3 Drive
Retarding Grid 2 Drive
Suppression Grid Drive
Apprx. 50 Hz LPF
Vout = 0 to +12 V; Controllable by passive components or DAC/OpAmp circuitry (R37 and R44 used as connection controls).
Vout = 0 to +12 V; Controllable by passive components or DAC/OpAmp circuitry (R38 and R46 used as connection controls).
Vout = 0 to -12 V; Controllable by passive components or DAC/OpAmp circuitry (R52 and R57 used as connection controls).
Vout = 0 to +12 V; Controllable by passive components or DAC/OpAmp circuitry (R61 and R66 used as connection controls).
G = 2.4
G = -1
+15VB2
-15VB2
+5VB2
AGNDB
OP497F
TEST POINT
CAP NA
Title
Grid Voltage Drive
Size
Custom
Document Number
PVVISS Main Board REV 00
Rev
Orig
Date:
Tuesday, June 02, 2015
Sheet
3
of
6

Temperature Sensors

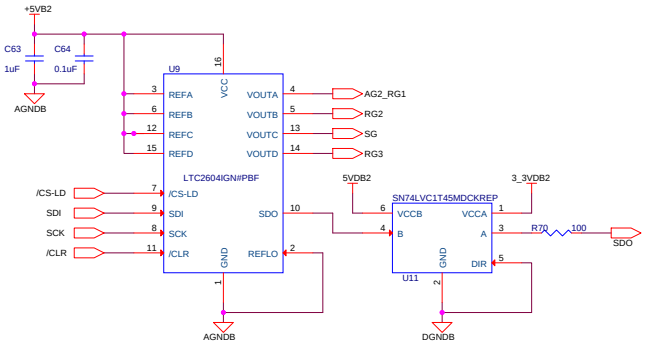
Main Board Temp



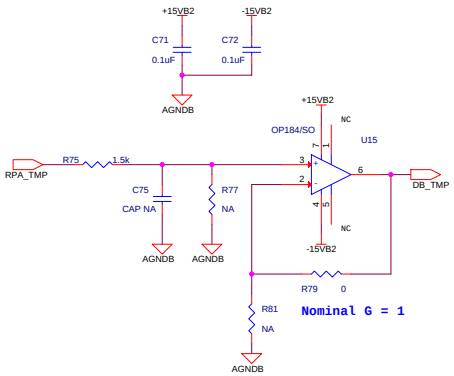
Main Board Temp



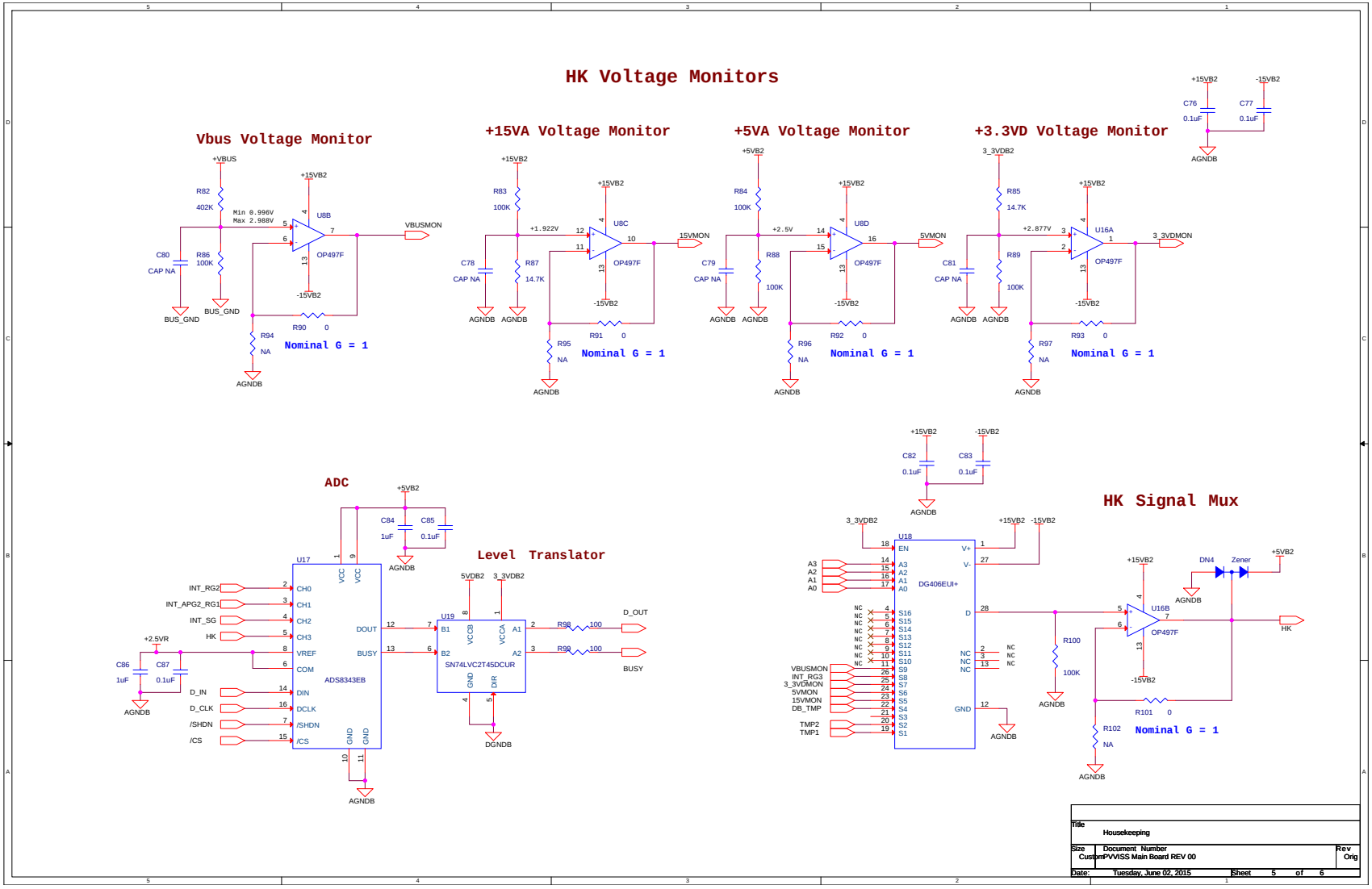
Grid Voltage Generation

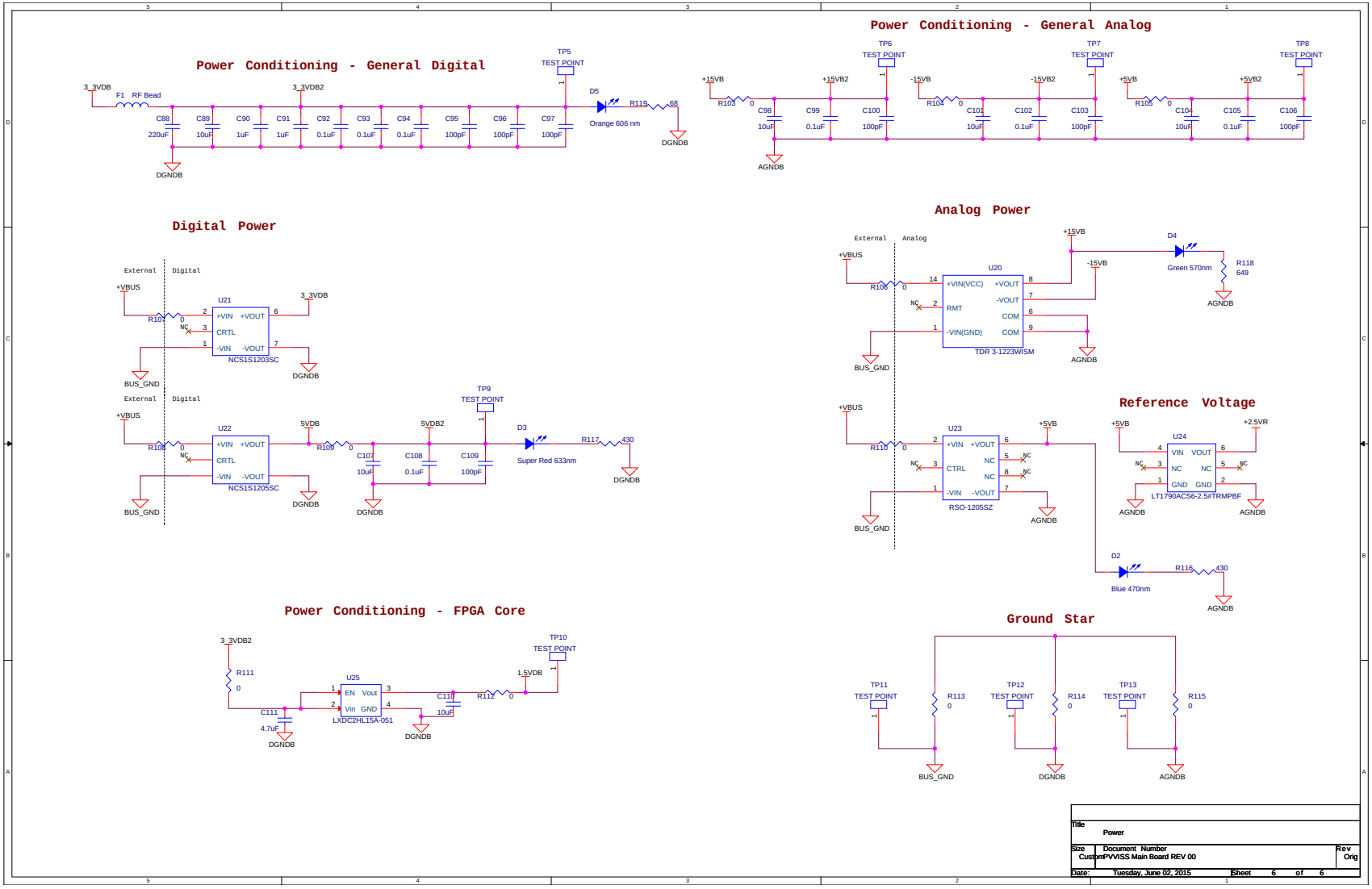


Daughter Board Temp



Title	Temperature Sensors	
Size: Custom	Document Number: PVVISS Main Board REV 00	Rev: Orig
Date: Tuesday, June 02, 2015	Sheet 4 of 6	


HK Voltage Monitors
Vbus Voltage Monitor
+15VA Voltage Monitor
+5VA Voltage Monitor
+3.3VD Voltage Monitor
+VBUS
R82
402K
Min 0.996V
Max 2.988V
U8B
OP497F
VBUSMON
C80
CAP NA
R86
100K
BUS_GND
R90
0
R94
NA
AGNDB
Nominal G = 1
+15VB2
-15VB2
R83
100K
+1.922V
U8C
15VMON
C78
R87
14.7K
R91
R95
R84
100K
+2.5V
U8D
5VMON
C79
R88
R92
R96
R85
14.7K
+2.877V
U16A
3_3VDMON
C81
R89
R93
R97
3_3VDB2
C76
0.1uF
C77
ADC
+5VB2
C84
1uF
C85
U17
ADS8343EB
INT_RG2
INT_APG2_RG1
INT_SG
HK
+2.5VR
C86
C87
D_IN
D_CLK
/SHDN
/CS
VREF
COM
DIN
DCLK
DOUT
BUSY
Level Translator
5VDB2
U19
SN74LVC2T45DCUR
D_OUT
BUSY
DGNDB
C82
C83
HK Signal Mux
U18
DG406EUI+
EN
V+
V-
D
GND
A3
A2
A1
A0
VBUSMON
INT_RG3
3_3VDMON
5VMON
15VMON
DB_TMP
TMP2
TMP1
R100
100K
U16B
DN4
Zener
HK
R101
R102
Title
Housekeeping
Size
Custom
Document Number
PVVISS Main Board REV 00
Rev
Orig
Date:
Tuesday, June 02, 2015
Sheet
5
of
6


Power Conditioning - General Digital
3_3VDB
F1 RF Bead
3_3VDB2
C88 220uF
C89 10uF
C90 1uF
C91 1uF
C92 0.1uF
C93 0.1uF
C94 0.1uF
C95 100pF
C96 100pF
C97 100pF
DGNDB
TP5 TEST POINT
D5
Orange 606 nm
R119 68
DGNDB
Power Conditioning - General Analog
+15VB
R103 0
+15VB2
C98 10uF
C99 0.1uF
C100 100pF
AGNDB
TP6 TEST POINT
-15VB
R104 0
-15VB2
C101 10uF
C102 0.1uF
C103 100pF
TP7 TEST POINT
+5VB
R105 0
+5VB2
C104 10uF
C105 0.1uF
C106 100pF
TP8 TEST POINT
Digital Power
External
Digital
+VBUS
R107 0
NC
U21
+VIN +VOUT
CRTL
-VIN -VOUT
NCS1S1203SC
3_3VDB
BUS_GND
DGNDB
R108 0
U22
NCS1S1205SC
5VDB
R109 0
C107 10uF
5VDB2
C108 0.1uF
C109 100pF
TP9 TEST POINT
D3
Super Red 633nm
R117 430
Analog Power
External
Analog
+VBUS
R106 0
U20
+VIN(VCC) +VOUT
RMT
-VIN(GND)
-VOUT
COM
TDR 3-1223WISM
+15VB
-15VB
D4
Green 570nm
R118 649
AGNDB
BUS_GND
Reference Voltage
R110 0
U23
RSO-1205SZ
+5VB
U24
VIN VOUT
NC
GND
LT1790ACS6-2.5#TRMPBF
+2.5VR
D2
Blue 470nm
R116 430
Power Conditioning - FPGA Core
3_3VDB2
R111 0
U25
EN Vout
Vin GND
LXDC2HL15A-051
C111 4.7uF
C110 10uF
R112 0
1_5VDB
TP10 TEST POINT
Ground Star
TP11 TEST POINT
R113 0
TP12 TEST POINT
R114 0
TP13 TEST POINT
R115 0
Title
Power
Size
Custom
Document Number
PVVISS Main Board REV 00
Rev
Orig
Date:
Tuesday, June 02, 2015
Sheet
6
of
6

APPENDIX H

PVVISS Circuit Boards

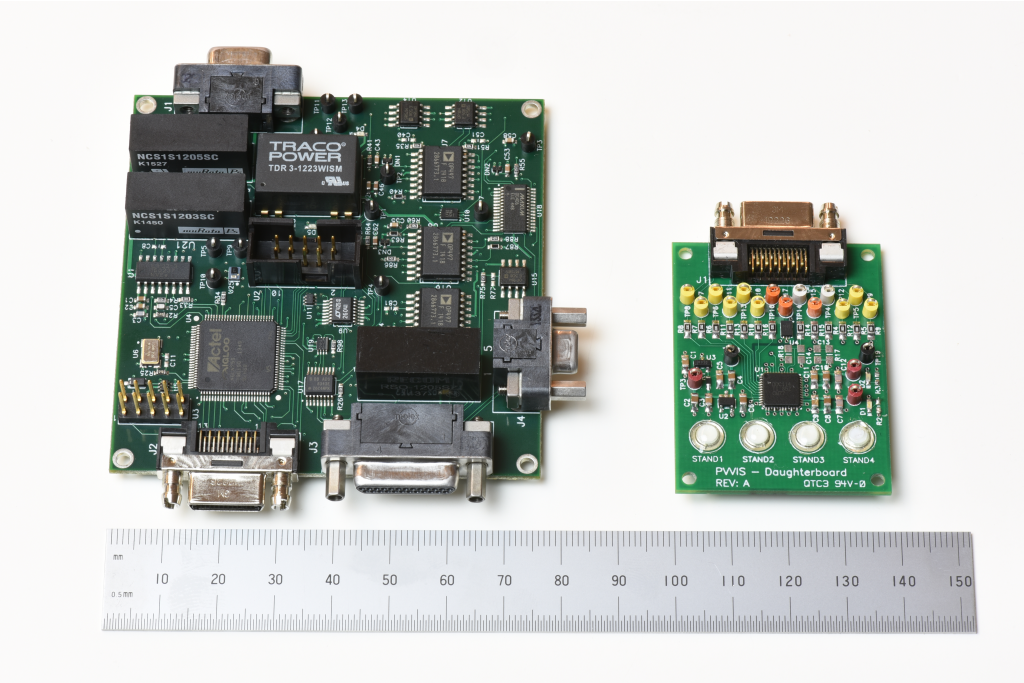


Fig. H.1: PVVISS Circuit Boards

APPENDIX I

Test Procedures

PVVIS Daughter Board Test Procedure

FOUO DATA NOTICE

REVISION: -
DATE: FEB 20, 2015

1. INTRODUCTION

The Center for Space Engineering is designing, fabricating, and testing the PVVIS Daughter Board (###-####). This document outlines the testing to occur on the board.

2. COMPONENT LAYOUT CHECKOUT

- Verify orientation of all ICs, polarized capacitors, and connectors on board. This is performed before any power is applied to the board Initial_____ Date_____
- Verify all passive components are populated correctly Initial_____ Date_____

3. POWER CHECKOUT

- Verify there is adequate resistance between each voltage and ground

Table 1: Power Resistances

Voltage	Resistance
+5VA	
+3.3VD	
VREF	

Initial_____ Date_____

- Supply board with +5V and +3.3V through microD Connector. Verify all regulated output voltages shown in Table 22. This is performed before anything is connected to the board.

Table 2: Power Voltages

Voltage	Test Point	Measured Voltage
+5VA	TP1	
+3.3VD	TP2	
+4.096V_REF	TP3	

Initial_____ Date_____

4. SIGNAL VERIFICATION

- Connect the rest of the communications cable to the main board or testing equipment.
- Verify that the following signals exist on their lines

Signal	Test Point	Type of Signal
DDC_CLK	TP4	Continuous Clock (Square wave)
DDC_CONV	TP5	Conversion Control Input: 0 = Integrate on Side B 1 = Integrate on Side A
DDC_RANGE0	TP6	Range Control
DDC_RANGE1	TP7	Range Control
DDC_RANGE2	TP8	Range Control
DDC_TEST	TP9	Test Mode Control (should be low)
DDC_CLK_4X	TP10	Master Clock Divider Control (should be low)
DDC_MODE	TP11	Mode Control (should be low)
DDC_RST	TP12	Resets the Digital Circuitry, Active Low
DDC_FORMAT	TP13	Digital Output Word Format 0 = 16 Bits, 1 = 20 Bits

Initial_____ Date_____

5. COLLECTOR CURRENTS

- Follow the table below.
- Connect the Current Source to the indicated input terminal
- Set the current source to the current in the table below and record the output

Current Source Setting (Amps)	Input Terminal	Output
1.0x10^-10	**1**	
1.0x10^-8	**1**	
1.0x10^-6	**1**	
1.0x10^-5	**1**	
1.0x10^-10	**2**	
1.0x10^-8	**2**	
1.0x10^-6	**2**	
1.0x10^-5	**2**	
1.0x10^-10	**3**	
1.0x10^-8	**3**	
1.0x10^-6	**3**	
1.0x10^-5	**3**	
1.0x10^-10	**4**	
1.0x10^-8	**4**	
1.0x10^-6	**4**	
1.0x10^-5	**4**	

Initial_____ Date_____

APPENDIX J

Next Revision 3D Mock-pp

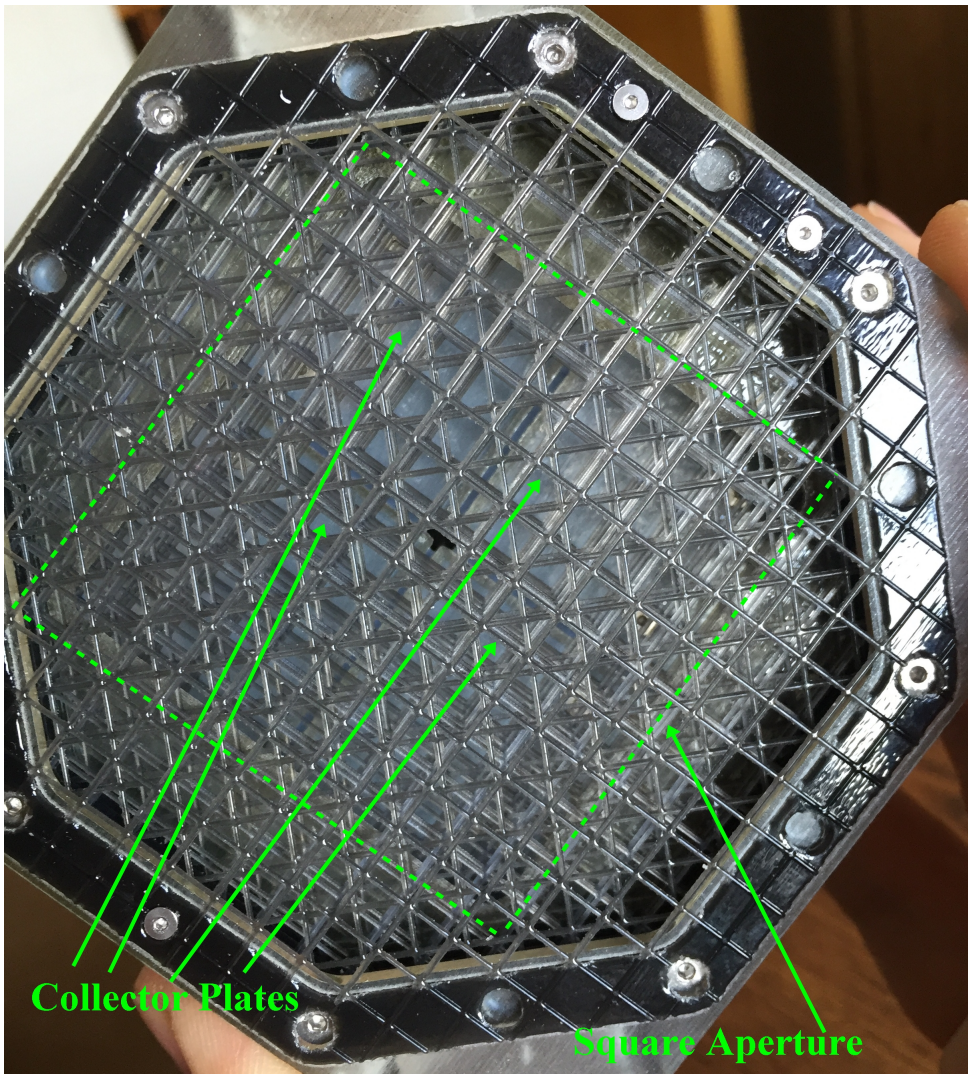


Fig. J.1: 3D Mock-up of Next PVVISS Design (Front)

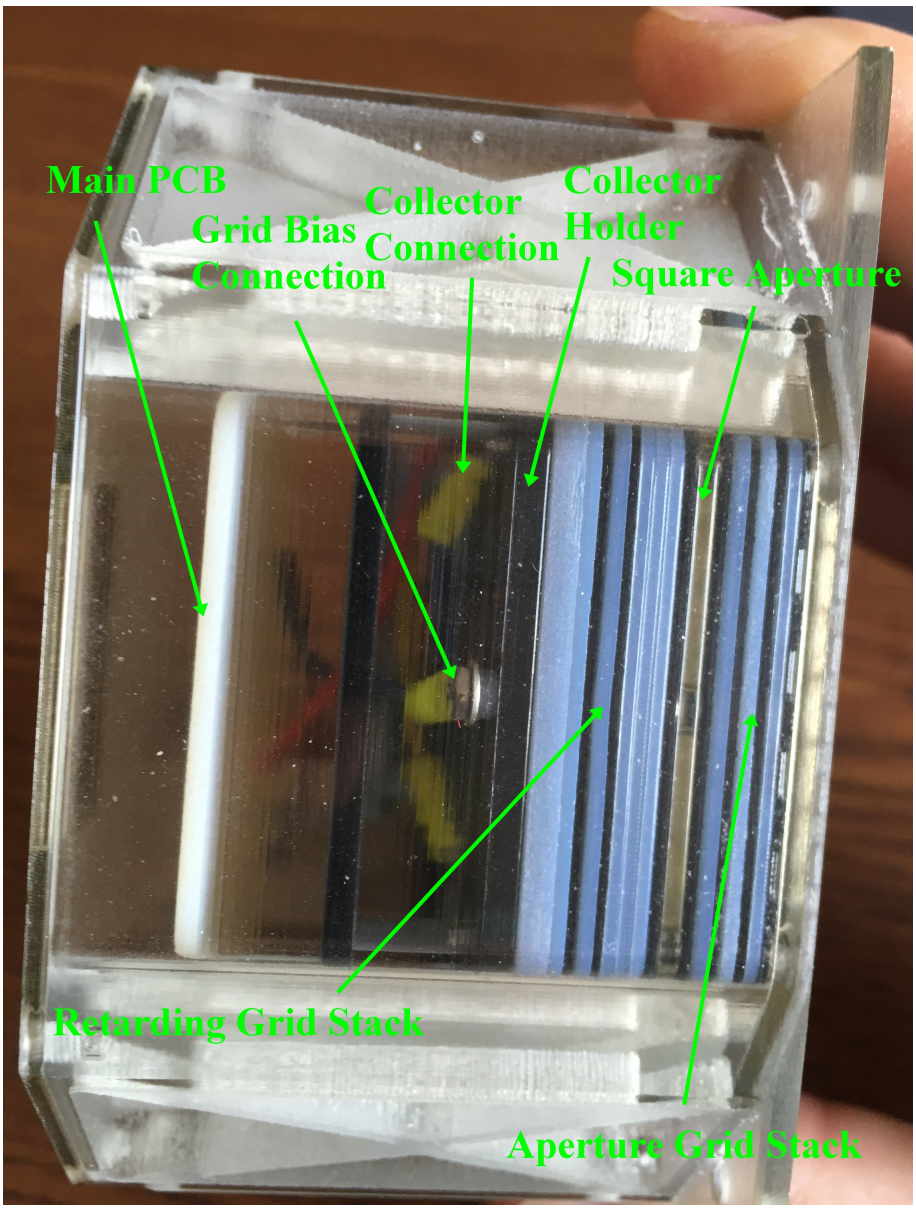


Fig. J.2: 3D Mock-up of Next PVVISS Design (Grid Stack)