ANALOG FRONT-END DESIGN USING THE G_M/I_D METHOD FOR A PULSE-BASED PLASMA IMPEDANCE PROBE SYSTEM

by

Arun J Rao

A thesis submitted in partial fulfillment
of the requirements for the degree

of

MASTER OF SCIENCE

in

Electrical Engineering

Approved:

Dr. Edmund Spencer Major Professor	Dr. Chris Winstead Committee Member
Dr. Bedri Cetiner Committee Member	Dr. Byron R. Burnham Dean of Graduate Studies

UTAH STATE UNIVERSITY
Logan, Utah

2010

Abstract

Analog Front-End Design Using the g_m/I_D Method for a Pulse-Based Plasma Impedance Probe System

by

Arun J Rao, Master of Science

Utah State University, 2010

Major Professor: Dr. Edmund Spencer
Department: Electrical and Computer Engineering

The Plasma Impedance Probe (PIP) is an electronic instrument that measures the impedance of a dipole antenna immersed in a plasma environment. Measurements made by the PIP provide valuable information regarding the plasma environment. Knowledge of ionospheric plasma density and density disturbances is required to understand radio frequency communication with satellites. The impedance curve provides us with significant plasma characteristics such as the electron-neutral collision frequency and plasma electron density.

The work proposed here is a transistor-level implementation of the analog front-end, the non-inverting amplifier that is used to drive the antenna. The antenna immersed in plasma is excited with a sinusoidal/pulse stimulus and the output from the non-inverting configuration is fed into the difference amplifier. In the difference amplifier the output signal from the non-inverting amplifier is subtracted from the original stimulus and then fed into a high-speed pipeline data converter. The entire analog and mixed signal components are integrated on a single chip. The obvious advantages with this design are that it eliminates several sources of analog signal processing errors, thereby improving stability. A Fast Fourier Transform (FFT) is then applied on the sampled input stimulus as well as the processed signal. The

input voltage FFT is then divided by the current FFT to obtain the antenna impedance. The FFT method helps in reducing transient errors and improves noise immunity of the system. The antenna impedance span curves over the frequency range from 100 kHz to 20MHz.

The approach for the tranistor-level design is implementing short-channel design techniques using the g_m/I_D method. This is the primary focus of the thesis where the emphasis has been on using a simple and intuitive method to design the front-end amplifier in the TSMC .35μm technology. The design specifications for this amplifier are derived from the system-level simulations. The transition from a Printed Circuit Board (PCB)-based design to System on Chip (SOC) implementation is explored. This makes the design components highly specific to the application.

The following are the design approaches used for the analog front-end design.

- A detailed study of the various factors affecting the PIP instrument measurement capabilities from the previous works.
- System-level simulation of the the entire PIP system to completely characterize the analog front-end.
- Exploration of the possible design topologies for the transistor-level implementation.
- A novel method of analog amplifier design using the g_m/I_D methodology.

Miniaturization of the instrument and using a pulse-based measurement scheme also offer an immediate benefit to sounding rocket missions. The reduction of power, mass, and volume will enable the instrument to be flown on many more sounding rockets than at present. The faster measurement is especially valuable since the ionospheric plasma changes in character most rapidly with altitude.

(83 pages)

To my loving parents, my twin
and dearest tona...

Acknowledgments

The journey to complete my thesis has been very challenging as well as fun. I finally had an opportunity to work in the space-related field that has always fascinated me. I was exposed to a variety of different projects, which helped me gain a broader perspective in the technicalities involved.

All this was made possible by the guidance of Dr. Edmund Spencer, my major professor. He always guided me in every aspect and supported me in every possible way he could. I extend very sincere thanks to him for infusing me with the enthusiasm and providing me a very positive perspective regarding my work. Dr. Chris Winstead's courses rekindled my passion for electronics design, which was always my dream to work on. I thank him for his valuable inputs to my projects and helping me become a more organized person.

My loving parents and my twin brother were always providing me the encouragement I needed during my entire course of study. Special thanks to my friend, Tona, for providing me her everlasting support and care.

I would like to thank Anju for dragging me to all the outdoor excursions to national parks, which really helped me take a break from the normal routines. Sudheer made sure that my wireless carrier free minutes were fully utilized. I am also very grateful to Swadesh, Tushar, Sanyogita, and Keyur for all their help, which made my stay in Logan a memorable experience.

Arun J Rao

Contents

List of Tables

List of Figures

Acronyms

PIP	Plasma Impedance Probe
FFT	Fast Fourier Transform
SIP	Swept Impedance Probe
SAL	Sudden Atomic Layer
PCB	Printed Circuit Board
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
GA	Genetic Algorithm
OTA	Operational Transconductance Amplifier
OPAMP	Operational Amplifier
UGF	Unity Gain Frequency
PM	Phase Margin
CMIR	Common Mode Input Range
ODR	Output Dynamic Range
SR	Slew Rate
RHP	Right Half Plane
LHP	Left Half Plane
FOM	Figure Of Merits

Chapter 1

Introduction

1.1 Background

Plasma is considered the fourth state of matter and is defined as quasi-neutral collection of charged particles. The entire universe is composed of the matter plasma. As we move higher into the earth's atmospheric layers we are actually passing into layers of plasma. The study of the plasma characteristics of the earth's atmosphere is an important field in space physics. There have been various instruments devised to measure the characteristics of the plasma. The Plasma Impedance Probe (PIP) is an electronic instrument that measures the impedance of an antenna immersed in a plasma environment (the environment here referring to the ionosphere). Important characteristics of the plasma can be obtained by studying the plasma impedance curve. Knowledge of ionospheric plasma density and density disturbances is required to understand radio frequency communication with satellites. The impedance curve provides us with significant plasma characteristics such as the electron-neutral collision frequency and plasma electron density. The PIP is an instrument based on self-impedance technique where no cross calibration is required to obtain absolute electron densities. An extensive study on the previous PIP designs on various rocket missions was done by Sanderson [1]. This instrument has been developed over the past five decades with constant modifications and improvements to the measuring techniques.

1.1.1 Plasma Characteristics

The parameters, such as electron density and electron neutral collision frequency, determine the ionospheric plasma characterization. Electron densities and density gradients determine the ionospheric plasma properties whereas the electron neutral collision frequency v_{en}, particularly the ratio of electron-neutral collision frequency to electron cyclotron fre-

quency f_{ce}, is used to determine the dominant ionospheric conductivities and energy conversion processes at different ionospheric lattitudes as studied by Steigies [2]. As mentioned earlier, the method of employing an electrically short antenna to obtain plasma parameters is essentially a Radio Frequency (RF) technique. The primary advantage of using such a method is that the RF response is not susceptible to spacecraft charging problems above the plasma frequency, where ion sheath effects are negligible [3].

A plasma is a quasi-neutral gas of charged and neutral particles which exhibits collective behavior. The Swept Impedance Probe (SIP) sweeps a sinusoidal voltage over the desired frequency range and measures the small signal RF impedance of an electrically short dipole antenna immersed in plasma. In this thesis we propose to use a wideband Gaussian derivative pulse covering the desired frequency range as the input stimulus to the PIP which eliminates the need of sweeping through the frequencies. The measured plasma impedance curves has distinct resonant regions that are related to plasma frequency f_{pe}, the electron cyclotron frequency f_{ce}, and the upper hybrid frequency f_{uh}. These resonant regions are approximately analogus to resonances of series and parallel Resistor-Inductor-Capacitor (RLC) circuits. The impedance of antenna in a plasma is normalized by dividing it with its impedance under free-space conditions, which is capacitive at wavelengths much longer than the antenna dimensions. On a normalized impedance plasma impedance curve, the series resonance f_{ce} gives the minimum impedance magnitude, while the parallel resonance at f_{uh} gives a maximum of the impedance magnitude. The impedance curve for a particular combination of f_{pe}, f_{ce}, and f_{uh} is unique. Figure 1.1 shows an unnormalized imedance curve and its phase response. It illustrates the magnitude and phase response corresponding to the series and parallel resonances from Balmain theory [3]. Figure 1.2 shows the comparison of the Impedance curve in the presence and absence of plasma. The absence of plasma indicates a capacitive nature for the antenna impedance.

1.1.2 Dipole in Unmagnetized Plasma

C-probe theory (Pfister's theory) [4]: An electrically short antenna (physical lengths much smaller than the free-space electromagnetic wavelength) can be treated very much like

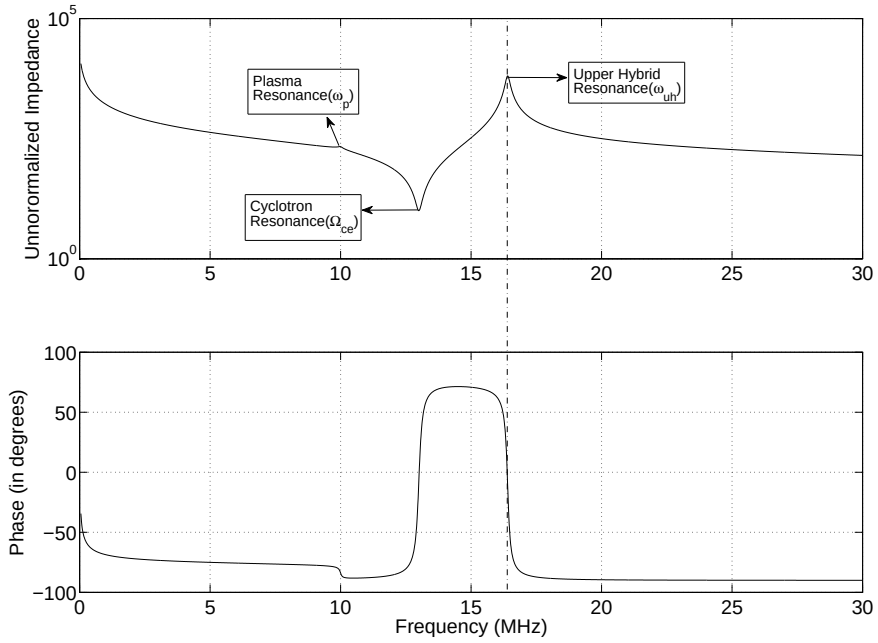


Fig. 1.1: Unnormalized impedance magnitude and phase of a dipole antenna in a cold magnetoplasma.

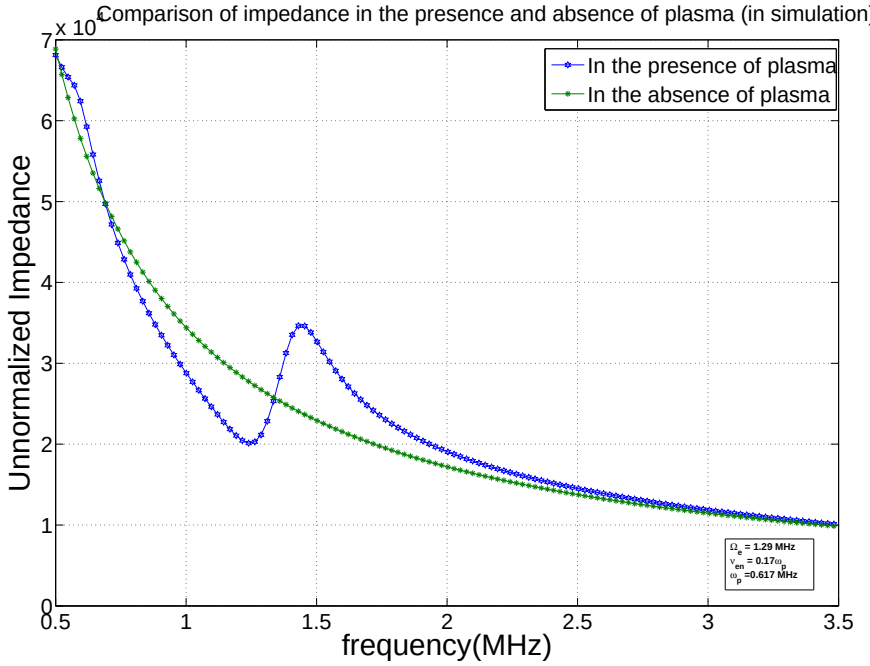


Fig. 1.2: Impedance comparison in the presence and absence of plasma.

a capacitor. This is shown in fig. 1.3. The antenna probe used in our missions is a dipole antenna, in which both conductor ends are immersed in plasma where one side is connected to ground and the other is fed to the input voltage on the generator end. Because of the low frequency of operation compared to a wavelength, the antenna can be regarded as a simple capacitor. The current in the dipole varies linearly from maximum at the midpoint of the antenna to zero towards the conductors.

$$Z_{antenna} = \frac{-j}{\omega C_0} \tag{1.1}$$

$$C = \epsilon_r C_0 \tag{1.2}$$

$$\epsilon_r = \left(1 - \frac{\omega_p^2}{\omega^2 - j\omega\mu_{en}}\right) \tag{1.3}$$

1.1.3 Dipole in Magnetized Plasma

For a cold collisional, non-drifting plasma of electrons and immobile ions, the following equations depict the prominent characteristics of the curve shown in fig. 1.4.

$$\text{Plasmafrequency} = \omega_{\text{pe}}^2 = \frac{\eta_{\text{e}} \text{e}^2}{\epsilon_0 \text{m}_{\text{e}}}, \tag{1.4}$$

where η_e is the plasma electron density, e is the electron charge, m_e is the lectron mass, and ϵ_0 is the free-space permittivity. The cyclotron frequency for a given magnetic field B is given by

$$\text{Cyclotronfrequency} = \omega_{\text{ce}} = \frac{\text{eB}}{\text{m}_{\text{e}}}. \tag{1.5}$$

The parallel RLC like resonance, which characterizes maximum impedance, occurs at the upper hybrid frequency and is denoted as

$$\text{UpperHybridfrequency} = \omega_{\text{uh}}^2 = \omega_{\text{pe}}^2 + \omega_{\text{ce}}^2. \tag{1.6}$$

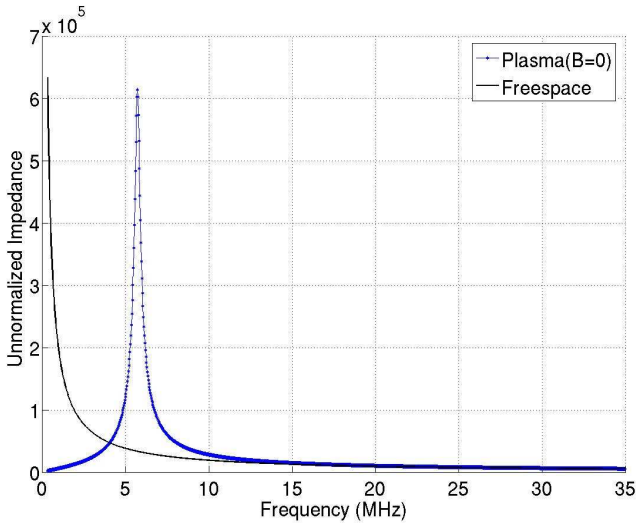


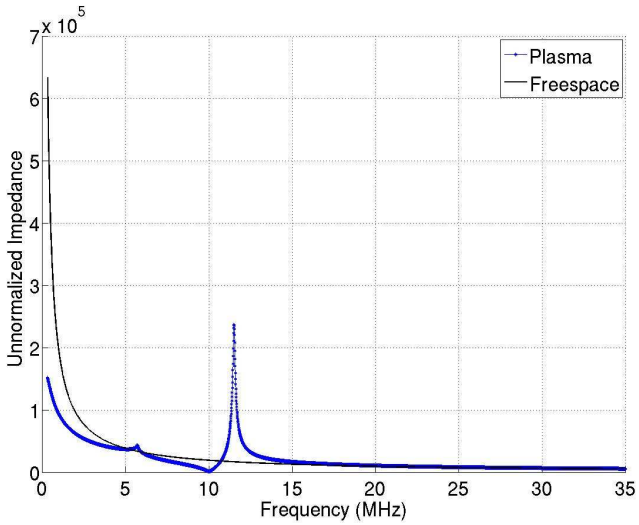
Fig. 1.3: Comparison between impedance of dipole in free-space and in an unmagnetized plasma.

1.2 Errors in Impedance Measurements

The PIP is an instrument flown in a highly dynamic environment where the composition of the environment is continuously changing. The instrument should be able to make accurate measurments in spite of the myriad factors affecting it. The complete analysis of errors encountered because of the environment, the spacecraft, velocity, spacecraft charging, and the wake is beyond the scope of this thesis. We concentrate only on the potential causes of errors in the impedance magnitude data which may occur due to the electronics of the PIP. A study of the impedance curves at various upleg and downleg altitudes has been done by analyzing Sudden Atom Layer (SAL) mission data by Patra [5].

Some of the key factors affecting impedance measurements are:

- The radial variation in particle density caused by the payload wake, affects magnitude of electron density;
- If the frequencies are not swept fast enough then the density gradients will affect the impedance measurements;



[b]

Fig. 1.4: Comparison between impedance of dipole in free-space and in cold magnetized plasma.

- Impedance data is affected by the resolution of data converters and the inherent noise in the dynamic environment. The noise is an important factor in consideration as it is difficult to separate the noise contributed by the instrument and the environment in which it is flown;

- The theory of the ionosphere from models cannot be accurately matched at low frequencies, at various altitudes in the upleg and downleg.

A typical flow diagram of a Printed Circuit Board (PCB)-based PIP electronics designed is shown in fig. 1.5. The electronics uses a quadrature sampling technique for impedance measurements proposed by Hummel [6].

1.3 Motivation for PIP Miniaturization

The present space technology is moving towards miniaturization with emphasis on reducing costs for missions. It is currently an era of cubesats, microsatellites, and nanosatellites which are frontrunners in studying the characteristics of the earth's atmosphere. These small satellites can be flown as constellations in the earth's atmosphere. With the reduction in size of the satellites, the resources available on-board the satellites are also limited in

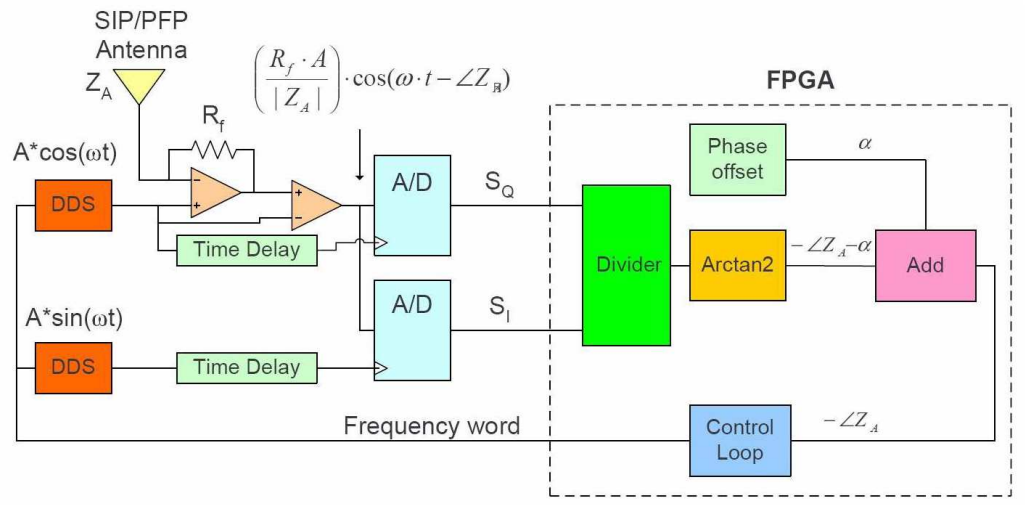


Fig. 1.5: Quadrature sampling technique for plasma impedance measurements.

terms of area, power, and time slices for data transmission to the ground stations available for each instrument. Flying multiple instruments on a single mission is always economical. The above constraints call for miniaturization of the electronics used for various experiments. The PIP until now was a PCB design and the feasibility of using this instrument on cubesat missions inherently called for an Application Specific Integrated Circuit (ASIC) design. More recently such a design for miniaturization using Complementary Metal Oxide Semiconductor (CMOS) technology was proposed by Jayaram et al. [7].

1.4 Proposed Design

The design proposed here will use short-channel design technique called the g_m/I_D methodology to arrive at the transistor specifications. Also the system will be tested for both sinusoidal and pulse-based inputs. System level characterization is done using pulse-based stimulus. The proposed design is shown in fig. 1.6.

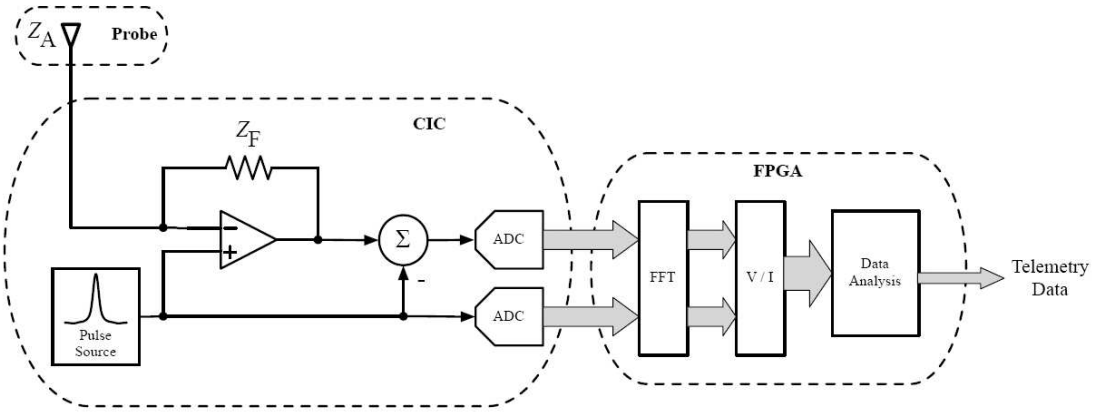


Fig. 1.6: Signal flow of the proposed PIP using a pulse.

Table 1.1 shows a summary of comparison between the quadrature sampling design and the present design.

1.5 Research Contributions

The proposed research contributions in the present thesis are:

- Develop a pulsed-based methodology for the PIP electronics;
- Carry out a system-level simulation of the entire PIP design and verify the feasability of using a pulse stimulus;
- Complete a transistor level implementation of the analog front-end, using short-channel g_m/I_D method, satisfying the system for a Gaussian derivative input;
- A comparative study of the above developed system with respect to the other conventional designs.

Table 1.1: Comparison between the quadrature sampling technique and the Finite Fourier Transform (FFT) method proposed for on-chip implementation.

PIP I-Q	PIP I-V
This method verified on various missions.	Not affected by the non-linearities in the system as the fundamental frequency can easily be identified.
Does not require high computational resources.	Precise sinusoid generation not required.
Presence of DDS provides accurate sinusoids and hence sampling for A/D conversion can be done with reference to the DDS.	Constant sampling done in the A/D converter.
Requires precise DDS which consumes more power.	Relaxation on DDS precision and works well with a noisy system.
Sensitive to noise and non-linearities.	Needs high computational capabilities and a new design approach.

1.6 Thesis Outline

The main emphasis in this thesis is on the short-channel g_m/I_D-based design technique. Also, the system-level simulation results for pulse-based stimulus is shown. The flow of the thesis is as mentioned below.

- In Chapter 2 a detailed system-level simulation of the PIP with a pulse-based system is done on MATLAB/SIMULINK. The purpose and necessity of this new design is explored with quantifying results and graphs.

- Chapter 3 mainly deals with the basics in the transistor level design. It gives an insight to the various possible configurations that can be used for designing the op-amp in the analog front-end. Also the specifications needed to satisfy the design criteria are discussed.

- Chapter 4 concentrates on the g_m/I_D methodology. It gives us an insight into the procedures involved in using this approach and illustrates the design using simple circuit examples.

- In Chapter 5 design of a two-stage amplifier for the analog front-end using the new methodology is discussed. Frequency compensation techniques and results of the amplifier in various configurations are shown.

- Chapter 6 summarizes the key aspects of the work and points out the limitations in the present design. Also, a discussion on possible explorations in the area of transistor-level design for the PIP using the g_m/I_D method is mentioned.

Chapter 2

Pulse-Based System

2.1 Why a Pulse?

The antenna immersed in a plasma environment needs to be excited by a stimulus. Conventionally the excitation is done using a sinusoidal voltage source and sweeping through the desired frequencies to obtain the impedance curve. The current work proposes that the antenna be excited with a wideband Gaussian derivative pulse. This wideband pulse must contain the entire frequencies of interest, specifically it must cover the frequencies from 100KHz to 20MHz. Also, the magnitude of the pulse must be such that the current levels from the antenna must be well above the noise floor of the electronics used. Some of the obvious advantages of using a pulse waveform as the stimulus are:

- Eliminates the need to sweep through frequencies;
- Improves the spatial resolution of the obtained signal;
- Eradicates the need to produce extremely precise sinusoids;
- In sounding rocket missions, the plasma environment is highly dynamic due to the spacecraft's velocity. The pulse method captures a rapid snapshot of the plasma density, thereby improving the instrument's capability in highly dynamic environments. The new pulse method will also provide better correspondence between the measurement technique and ground-based computational analysis. The increased speed of the measurement using the new pulse-based technique will increase the instrument's capability of measuring local densities with high accuracy. The spacecraft will not have moved far during a single pulse when compared to sweeping through multiple sinusoidal waveforms.

The following sections further explore and analyze the pulse stimulus when applied to the PIP based on system-level simulation results.

2.1.1 Gaussian Pulse

The input voltage expression in time domain and its Fourier transform for a Gaussian pulse given by Taflove [8] is as follows:

$$V_{gauss}(t) = V_0 exp\big[(-t/\tau_p)^2/2\big], \tag{2.1}$$

$$V_{gauss}(\omega) = \sqrt{2\pi}\tau_p V_0 exp\big[(-\omega\tau_p)^2/2\big]. \tag{2.2}$$

The time domain and frequency domain plots for the Gaussian pulse are as shown in fig. 2.1. When the antenna is to be analyzed over a band of frequencies, it is efficient to excite the antenna with a pulsed signal and then use the Fourier transform to get the desired frequency-domain response.

2.1.2 Gaussian Derivative or Monocycle Pulse

The spectrum of the Gaussian pulse has significant low-frequency content as shown in the frequency spectrum of fig. 2.1. Since the purpose of the the pulse stimulus to the antenna is to provide a quick measurement of the antenna impedance, the presence of low-frequency components can cause longer settling time for the PIP electronics. Thus a Gaussian derivative pulse (also called the monocycle pulse) is used for the antenna excitation. The time domain voltage and the corresponding Fourier transform expressions are given as follows:

$$V_{mono}(t) = -V_0 \left(\frac{t}{\tau_p}\right) exp\big(-\left[(t/\tau_p)^2 - 1\right]/2\big), \tag{2.3}$$

$$V_{mono}(\omega) = -\mathrm{j}\omega\sqrt{2\pi}(\tau_p)^2 V_0 exp\big(-\left[(\omega\tau_p)^2 - 1\right]/2\big). \tag{2.4}$$

The time and frequency domain plots for the Gaussian derivative pulse are shown in fig. 2.2.

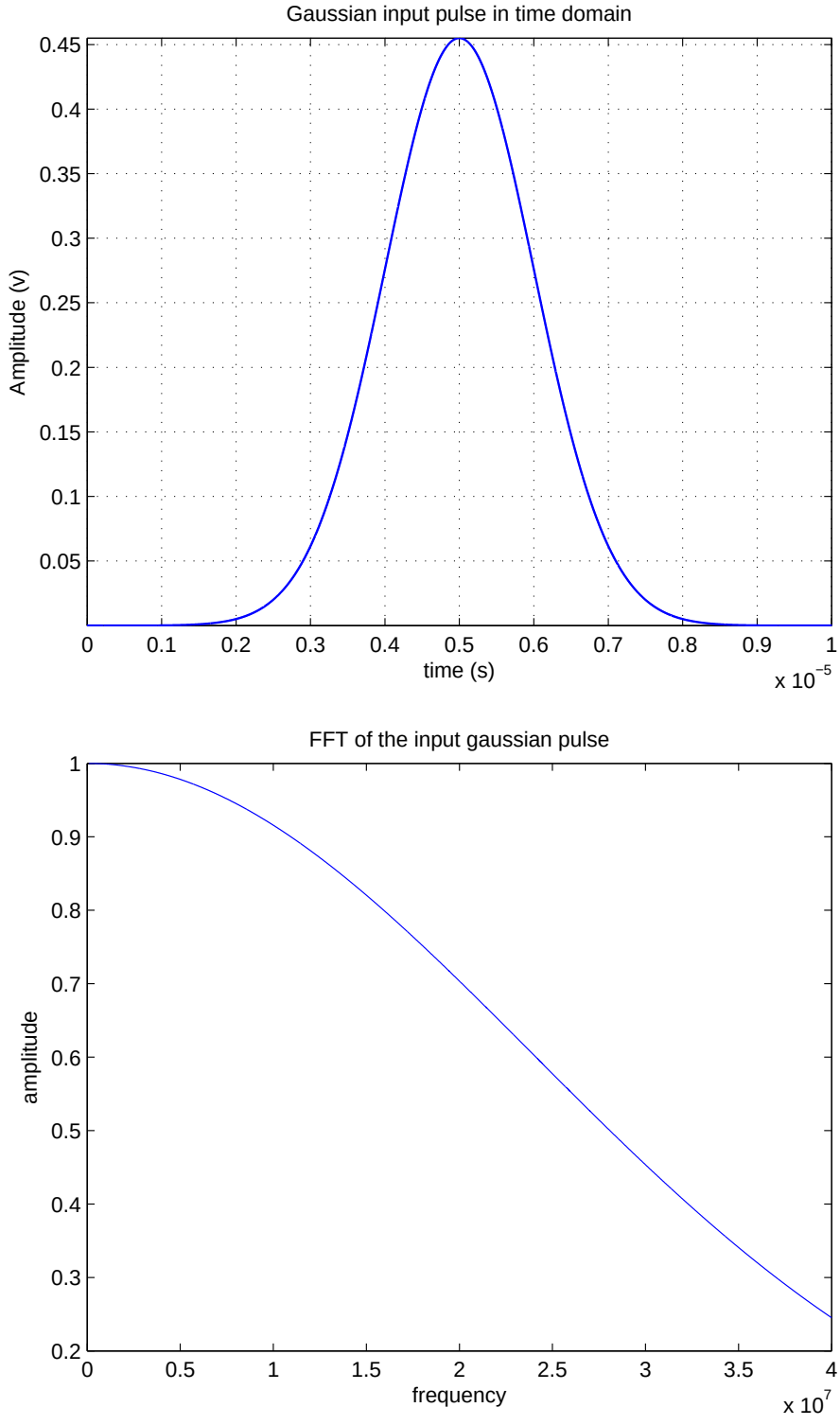


Fig. 2.1: The time domain and FFT plots of input Gaussian pulse.

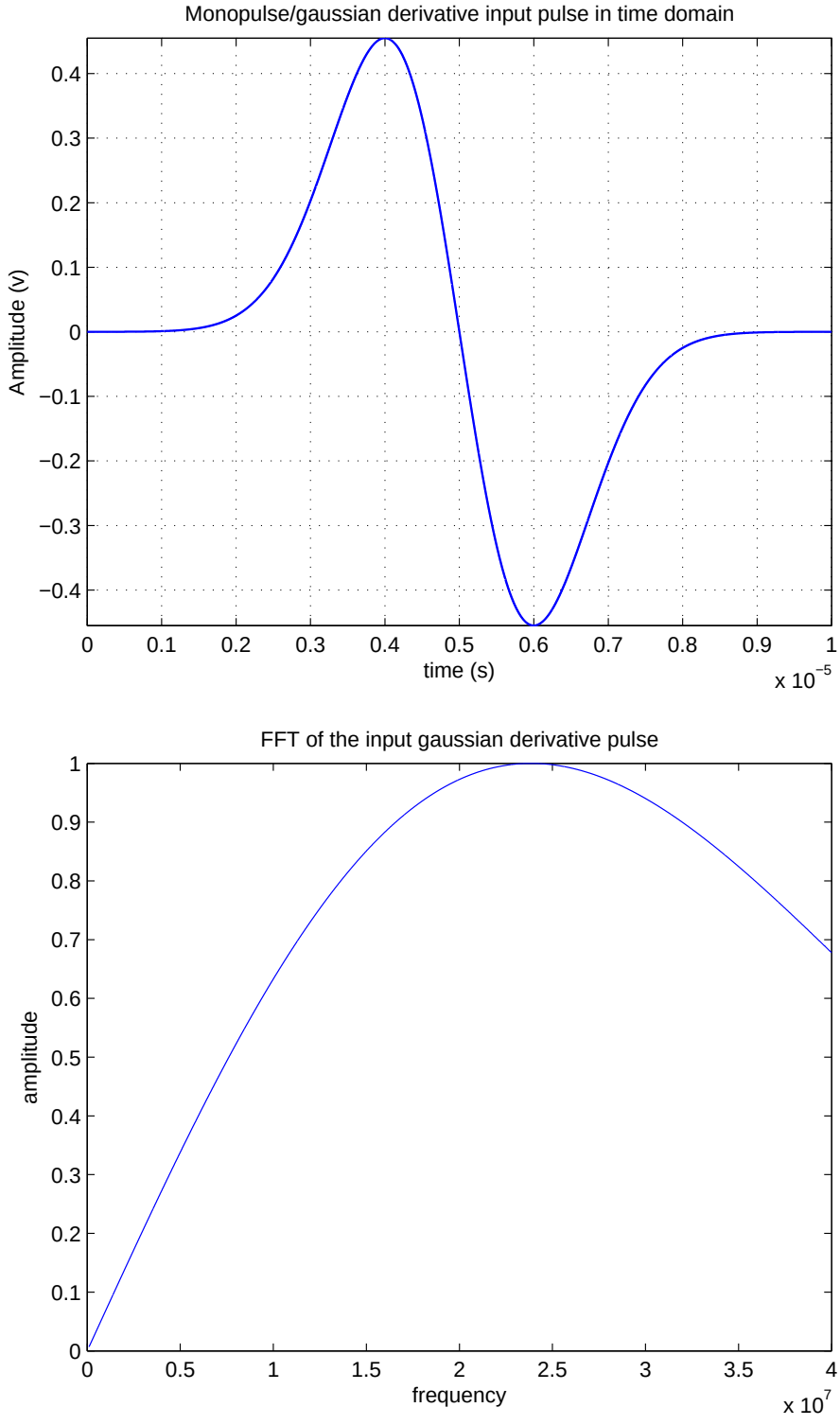


Fig. 2.2: The time domain and FFT plots of input Gaussian derivative pulse.

2.2 The Antenna Model

As mentioned previously, the ionospheric impedance can be visualized to be a combination of series and parallel RLC resonances corresponding the cyclotron f_{ce} and upper hybrid f_{uh} points on the plasma impedance curve. We use the following formula as a model for the antenna impedance:

$$Z_a(s) = \frac{1}{s}\left(\frac{s^2 + as + b}{s^2 + cs + d}\right). \tag{2.5}$$

The Genetic Algorithm

The antenna model in s-domain is used in the system level simulations to quantify the impedance curve. The resonances from the s-domain equation are matched to the actual Balmain theory [3]. For the purpose of obtaining this impedance curve we use an optimization algorithm. A brief description of the genetic algorithm using the Balmain theory as the fitness function is given below. Also a typical impedance curve obtained by using the genetic algorithm optimization technique is shown in fig. 2.3.

- Initialization of the population (bits, parameters, and population count).
- Specify the ranges for the coefficients in the s-domain impedance equation. (i.e., specify values for a, b, c, d).
- Balmain fitness function. This is the fitness function against which the s-domain impedance curve will be evaluated.
- Iterate through the population and fitness function according to the values set initially.
- Choose the best population matching the fitness function.
- Create a new population from the best matching elements.
- Iterate for the desired number of generations depending on the accuracy required.

As can be seen, the plasma resonance is not modeled in our s-domain antenna equation. For all practical pursposes it is sufficient if we can reproduce the cyclotron and upper hybrid resonances from our simulations and design.

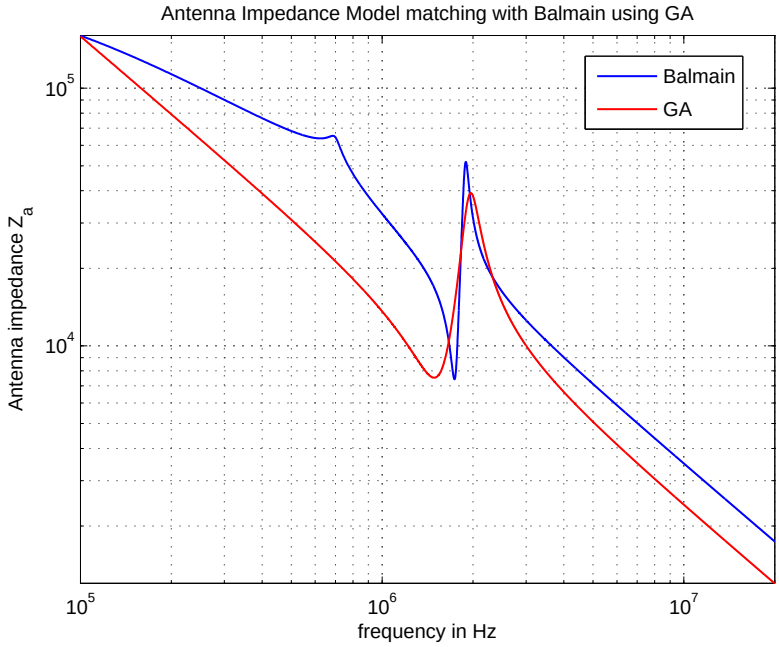


Fig. 2.3: Impedance curve obtained by matching with Balmain fitness function using genetic algorithm.

2.3 System-Level Simulation of PIP

In this section we perform the system-level simulation of the PIP electronics when excited by a pulse stimulus using MATLAB/SIMULINK. The entire PIP is broken into the analog front-end modeled using the amplifier and feedback system transfer functions. A pipeline analog-to-digital converter from the work of Hamoui [9] has been used for the system level simulations.

Analysis of the Amplifier with Finite K in Non-Inverting Configuration

We proceed with the analysis of an amplifier in the non-inverting configuration. Amplifier is assumed to have finite open-loop gain. The amplifier in non-inverting configuration used for analysis is as shown in fig. 2.4.

$$(V_i - V_x)K = V_0 \tag{2.6}$$

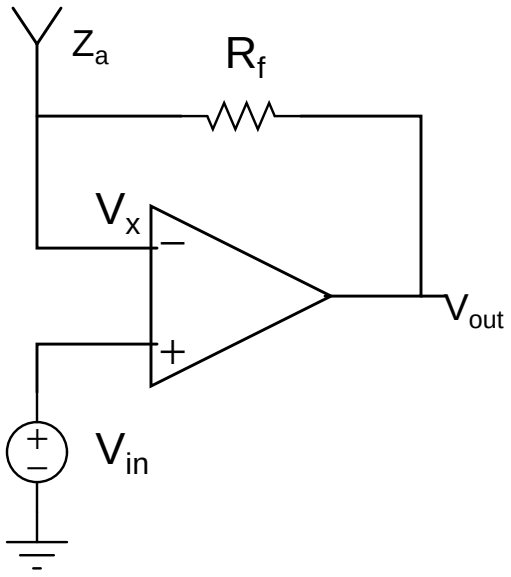


Fig. 2.4: Amplifier in non-inverting configuration.

$$V_x = \frac{Z_a}{Z_a + R_f} V_0 \tag{2.7}$$

Solving for the overall transfer function of the amplifier in closed-loop we have the following:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{K(Z_a + R_f)}{(1+K)Z_a + R_f}. \tag{2.8}$$

We model our antenna as a simple capacitance and then the overall transfer function can be written as follows:

$$Z_a = \frac{1}{sC_a}, \tag{2.9}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{K(1 + sC_aR_f)}{(1+K) + sC_aR_f}. \tag{2.10}$$

Rearranging the terms to obtain pole and zero locations, we have the following equation:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{k}{1+k} \frac{(1 + sC_aR_f)}{(1 + s\frac{C_aR_f}{1+k})}. \tag{2.11}$$

From the above equation we can infer the following:

$$\text{Zerolocation} = \omega_{\text{z}} = \frac{1}{\text{C}_{\text{a}}\text{R}_{\text{f}}}, \tag{2.12}$$

$$\text{Polelocation} = \omega_{\text{p}} = \frac{1+\text{K}}{\text{C}_{\text{a}}\text{R}_{\text{f}}}. \tag{2.13}$$

The Bode plot with the pole and zero locations for the amplifier is as shown in fig. 2.5.

Analysis

The Bode plot gives us some very interesting properties of the amplifier. The presence of a capacitor at the negative end of the amplifier shows us a high pass response (like a differentiator). This can be easily verified by the zero and pole locations as derived from the equations above.

- At low frequencies C_a is open, therefore, $\frac{V_{out}}{V_{in}} = \frac{K}{1+K}$. If K tends to infinity, this is a unity gain follower as expected.
- At intermediate frequencies, and K = infinity, we have, $\frac{V_{out}}{V_{in}} = 1 + sC_aR_f$, a high pass response.
- The finiteness of K puts the pole into the picture so that the final response we obtain is $\frac{V_{out}}{V_{in}} = \frac{K}{1+K}(1+K) = K$ as $s = j\omega$ tends to infinity.

This theory can be extended to further analysis in the following sections where it can be clearly seen from the transfer function in closed-loop that a zero is present which occurs before the poles. And the zero is predominantly due to the antenna capacitance. A thorough understanding of the results obtained in this section is required which will aid us in the selection of topology for the transistor level implementation developed in further sections.

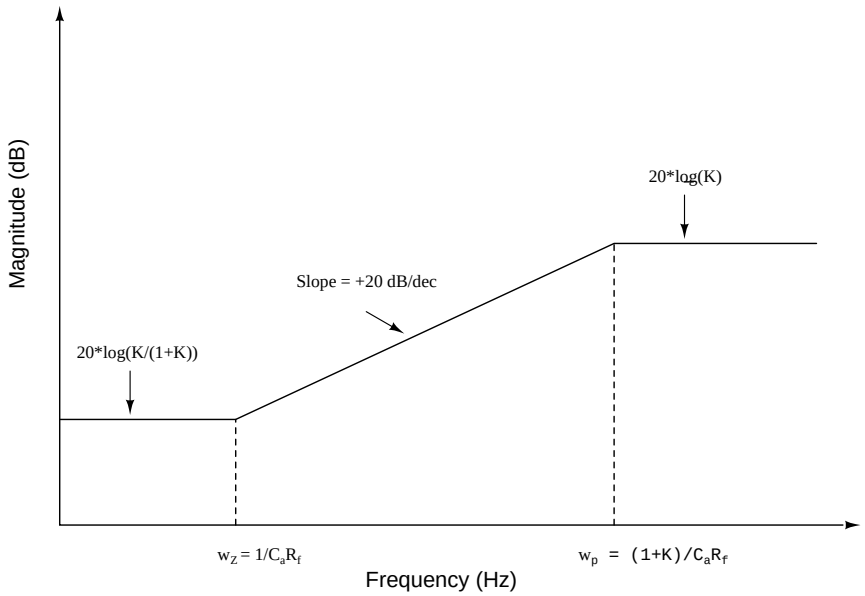


Fig. 2.5: Bode plot showing the pole and zero locations.

Amplifer with Single Dominant Pole, KG

Assuming the amplifier has a single dominant pole

$$G = K\left(\frac{a}{s+a}\right), \tag{2.14}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{Ka(1+sC_aR_f)}{a(1+k)+s(1+aC_aR_f)+s^2C_aR_f}. \tag{2.15}$$

Characteristic equation

$$s^2 + s\left(\frac{1+aC_aR_f}{C_aR_f}\right) + \frac{a(1+K)}{C_aR_f} = 0. \tag{2.16}$$

Amplifier with Double Pole Response

Assuming an amplifier with complex conjugate poles we have the following equation for G:

$$G = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{2.17}$$

Overall transfer function of amplifier in closed-loop is given as follows:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{K\omega_n^2(1+sC_aR_f)}{\omega_n^2(1+K)+s(C_aR_f\omega_n^2+2\zeta\omega_n)+s^2(1+2C_aR_f\zeta\omega_n)+s^3(C_aR_f)}. \tag{2.18}$$

Characteristic equation is given by:

$$s^3+s^2\left(\frac{1+2C_aR_f\zeta\omega_n}{C_aR_f}\right)+s\left(\frac{C_aR_f\omega_n^2+2\zeta\omega_n}{C_aR_f}\right)+\frac{\omega_n^2(1+K)}{C_aR_f}=0. \tag{2.19}$$

2.4 Proof of Concept

The MATLAB simulation for the above analysis and results are shown below: The amplifer transfer function considered is mentioned below. Also the actual antenna transfer function as mentioned in the previous section is used instead of a simple capacitor.

Amplifier with a Zero and Two-Complex Pole Response

The following equation governs the amplifier transfer function:

$$G=\frac{s+\frac{\omega}{\omega_{z1}}}{1+\frac{2\zeta s}{\omega_n}+\frac{s^2}{\omega_n^2}}. \tag{2.20}$$

The simulink model used is shown in fig. 2.6.

Results: The graphs obtained are as shown in the fig. 2.7 and fig. 2.8. The simulations are done assuming complex conjugate poles for the first two plots. Again in the first simulation, the location of zero is before the pole, and in the second result we see the zero location after the pole location. The third simulation shows the presence of two separate poles and a zero after the poles. In general, a thorough system-level analysis is done to study the impact of pole-zero locations (amplifier transfer function) in obtaining the antenna impedance curve. These simulations give us a better understanding of the analog front-end behavior when designing actual topologies in cadence. The simulations help us in arriving at the following specifications which the amplifier has to satisfy. Table. 2.1 shows the specifications to be achieved from the transistor-level implementation in cadence.

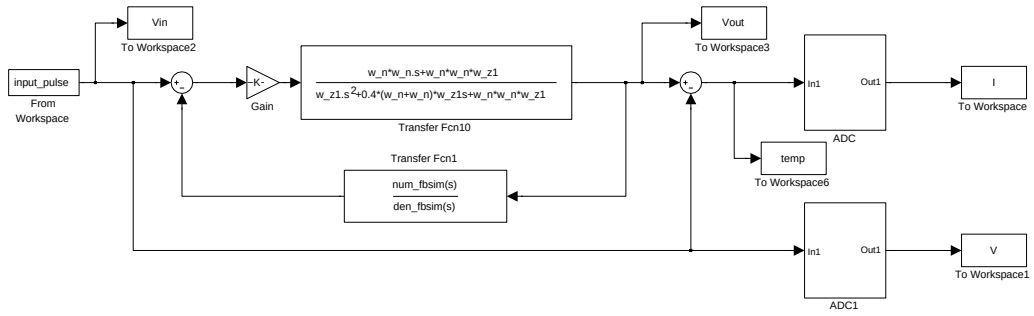


Fig. 2.6: The simulink model used to simulate results for amplifier with zero and complex poles combination.

Table 2.1: Amplifier specifications to be achieved from the transistor-level design, obtained from extensive matlab simulations.

A_v : DC Gain	$60 - 70dB$
f_u	$100MHz$
ϕ_M : Phase Margin	$45^\circ - 60^\circ$
ODR	$2.0V$
Slew Rate	$50V/\mu s$

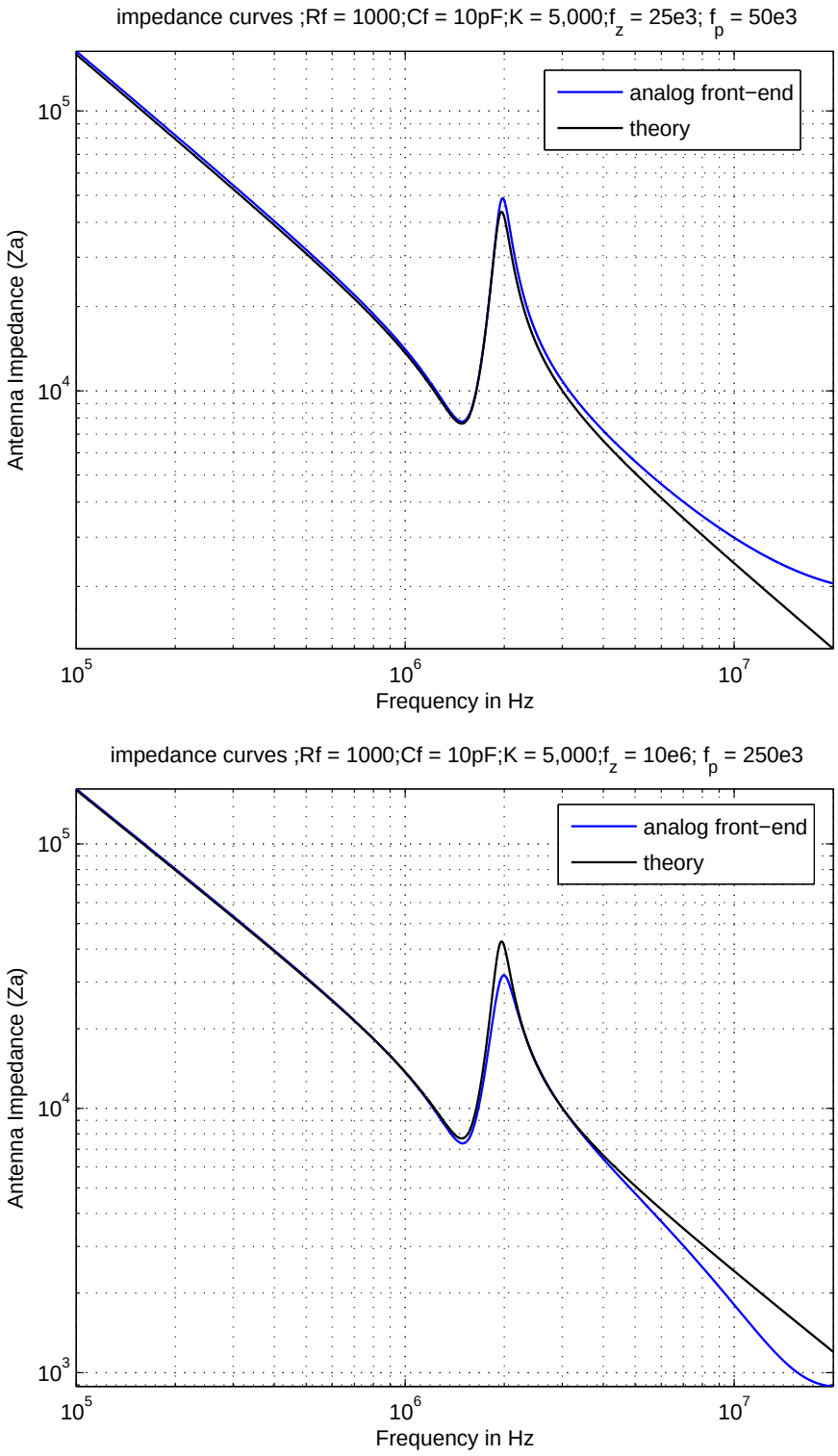


Fig. 2.7: Complex conjugate pole in amplifier transfer function.

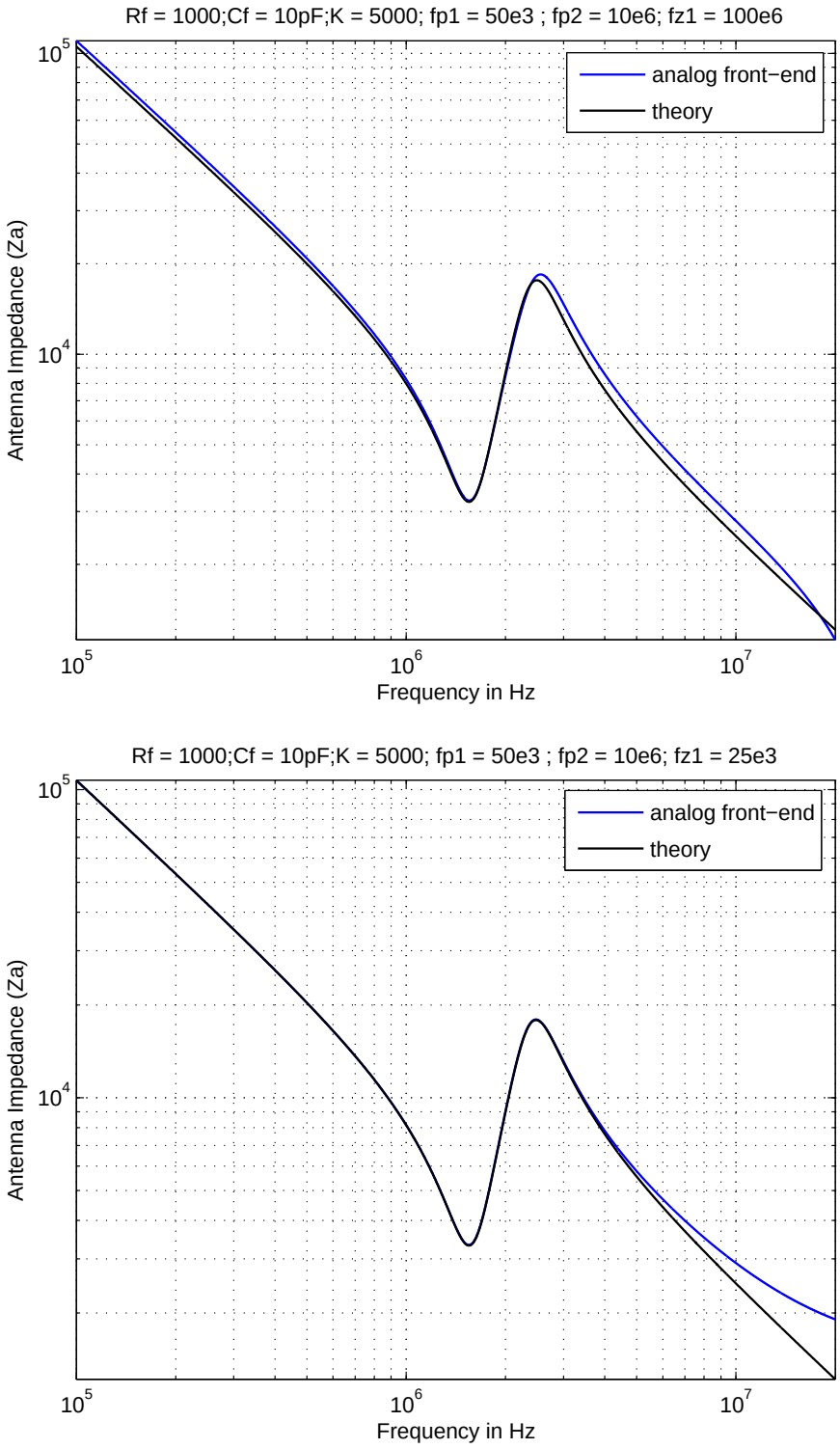


Fig. 2.8: Discrete poles in amplifier transfer function.

Chapter 3

The Analog Front-End Design

Operational amplifiers are amplifiers (various forms of controlled sources) with a very large forward gain (gain $> 10^5$ volts/volts), the closed-loop transfer function is independent of the gain of the amplifier. For CMOS on-chip designs we conventionally design an Operational Transconductance Amplifier (OTA) as opposed to the discrete operational amplifier design used in the bi-polar counterpart. Table 3.1 gives a summary on some of the basic differences between the two configurations.

3.1 Operational Amplifier (OPAMP) vs Operational Transconductance Amplifier (OTA)

We proceed to design the amplifier used in the non-inverting configuration as an OTA for the on-chip design. The following sections describe the various configurations of the OTA that can be used and the use of conventional and specialized design techniques to arrive at the desired specifications.

3.2 Topologies

The nature of OTA topology used is tied to the desired specifications and the application of the amplifier. In general, the amplifiers can be broken down into basic analog structures or blocks. Furthermore the design can be classified according to the various stages of conversion. Figure 3.1 shows the classification of various stages.

3.3 Amplifier Specifications

Any amplifier design requires a set of specifications which it has to meet. It may not be possible to satisfy all the specifications, and thus there is always a trade-off in any amplifier

Table 3.1: Comparison of OPAMP vs OTA.

OPAMP	OTA
high input impedance and low output impedance.	high input impedance and high output impedance.
Modeled as a voltage controlled voltage source because of the above property.	Modeled as voltage controlled current source.
Used with external feedback for creating circuits. Used as an output buffer. Contains compensation capacitor in its circuitry between the 2 stages (Miller compensation).	All nodes are at low impedance except for the input and the output nodes.
Op-amp becomes unstable with larger load capacitances.	Better frequency capabilities than op-amp. As load capacitance increases the phase margin increases and the OTA is stable.
An OTA with output buffer is an op-amp.	Generally a single stage design.
	For most on-chip applications as loads are capacitive the design of op-amp is essentially design of an OTA.

design. The following sections briefly give an insight into each of the specifications needed in an amplifier design [10–14].

Gain: For any CMOS topology the gain of the circuit is given by the the product of its transconductance structure and the output resistance of the load structure. The gain is strongly dependent on frequency of the input signal. At higher frequencies the inherent parasitic capacitances of the circuit reduce the gain. The gain expression can be given as:

$$A_v(gain) \quad = \quad g_m * R_{out}. \tag{3.1}$$

Unity Gain Bandwidth: This specifies the frequency at which the open-loop gain of the amplifier is unity. The maximal capacitance at the output node defines this specification. There is always a trade-off in achieving high gain and high bandwidth as the gain-bandwidth

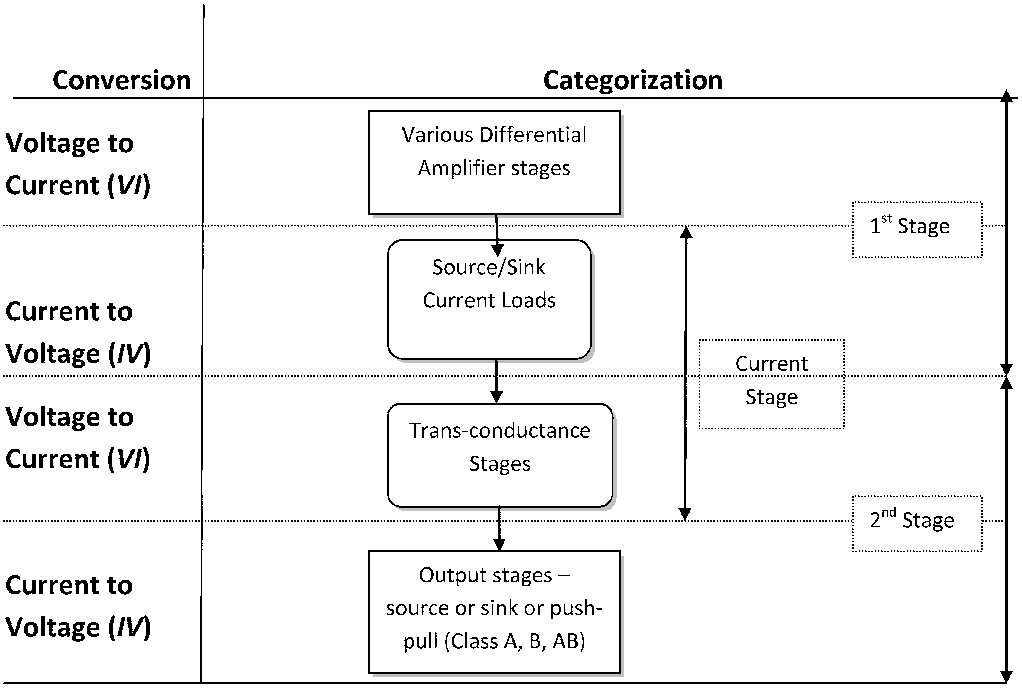


Fig. 3.1: Single-ended or fully-differential single-stage amplifier or the first stage of a two-stage amplifier.

product for any amplifier is constant for a particular design.

$$f_u = \frac{g_m}{2\pi C_L} \tag{3.2}$$

Phase Margin: The Phase Margin (PM) will determine the stability of an amplifier. Higher values of PM will allow the output signal to achieve steady state without much ringing. Lower values will cause ringing at the output. The value of Phase Margin depends on the application. In our design we require a $PM > 60°$.

$$PM = 108° - \arctan\left(\frac{f_u}{f_{dp}}\right) - \Sigma \arctan\left(\frac{f_u}{f_{ndp}}\right), \tag{3.3}$$

where f_{dp} is the dominant pole and f_{ndp} are the non-dominant poles in the amplifier transfer function. This equation has ignored the zeros in the amplifier transfer function.

Common Mode Input Range (CMIR): This is an important parameter at the

input of the circuit. The saturation voltage of the bias structure, the saturation voltage, and V_{GS} voltage headroom of the transconductance structure define the CMIR. An approximate expression can be given as

$$CMIR = V_{DD} - V_{GS} - V_{Dsat}. \tag{3.4}$$

Similarly the differential mode input range (DMIR) is the V_{GS} in the circuit. The available supply voltage V_{DD} defines the type of configuration which can be used for obtaining the highest CMIR.

Output Swing: This specification relates to the output of the amplifier. The saturation voltage of the load structure mainly defines the output swing of the amplifier. In general the use of cascoded load structures results in lower output swing as more number of transistors are stacked under each other and the V_{DSsat} subtracted from the V_{DD} provides the output voltage swing.

$$ODR = V_{DD} - \Sigma V_{DSsat} \tag{3.5}$$

Static Current Consumption: The product of current in all the amplifier branches and the supply voltage defines this specification. Careful design needs to be done if the power budget allocated is very low. Such a scenario exists in our design as the PIP instrument is allocated a certain power on the satellite.

Slew Rate: The output capacitance and the current flowing in the output branch define this parameter. High slew rate designs require using high values of current which may affect other specifications in the amplifier design.

$$SR = \frac{I_{out}}{C_L} \tag{3.6}$$

The speed of an amplifier is dependent on the equivalent RC constant at the output node. It also depends on the current sourcing/sinking capability at the output. Thus it is a strong function of the internal capacitances and currents in the amplifier branches.

3.4 The Two-Stage Op-Amp

The following section describes the two-stage op-amp shown in fig. 3.2 with its small signal-analysis and design using the conventional design technique. The overall transfer function is derived and the approximate location of poles and zeros is given. Then we proceed to design this particular configuration in virtuoso cadence using a set of equations from the following papers [15,16]. The bias circuit is known as the robust bias as mentioned by Johns and Martins [14]. The small signal equivalent circuit of the two-stage amplifier is shown in fig. 3.3.

Nodal Equations:

$$gm_1 V_{id} + V_A \left(\frac{1}{R_A} + sC_A \right) + (V_A - V_0) \left(\frac{1}{R_z + \frac{1}{sC_c}} \right) = 0 \tag{3.7}$$

$$gm_6 V_A + V_0 \left(\frac{1}{R_B} + sC_B \right) + (V_0 - V_A) \left(\frac{1}{R_z + \frac{1}{sC_c}} \right) = 0 \tag{3.8}$$

Solving the above two equations, we obtain the overall transfer function represented by the following polynomial:

$$\frac{V_0}{V_{id}} = \frac{a \left(1 - s \left(\frac{1}{gm_6} - R_z C_c \right) \right)}{1 + bs + cs^2 + ds^3}. \tag{3.9}$$

where

$$a = gm_1 gm_6 R_A R_B, \tag{3.10}$$

$$b = R_z C_c + R_A (C_A + C_c) + R_B (C_B + C_c) + gm_6 R_A R_B C_c, \tag{3.11}$$

$$c = R_A R_B (C_A C_B + C_B C_c + C_A C_c) + R_z C_c (C_B R_B + C_A R_A), \tag{3.12}$$

$$d = R_A R_B R_z C_A C_B C_c. \tag{3.13}$$

If R_z is assumed to be less than R_A and R_B (which usually is the case), the approximate locations of poles and zeros can be given by dominant pole as ω_{p1}, RHP zero as ω_{z1}, and

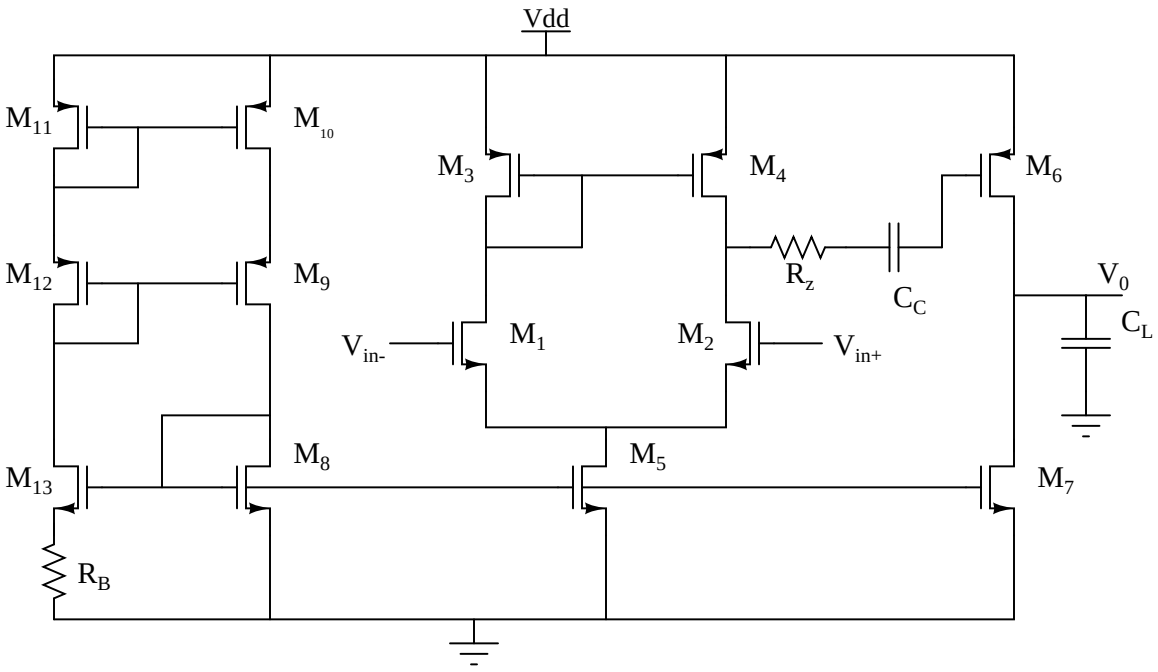


Fig. 3.2: Schematic shows a two-stage op-amp with the nulling resistor and the robust bias circuitry.

the unity gain bandwidth as ω_u. The higher order poles are neglected for simplicity.

$$\omega_{p1} = -\frac{1}{gm_6 R_A R_B C_c} \tag{3.14}$$

$$\omega_{z1} = \frac{1}{C_c\left(\frac{1}{gm_6} - R_z\right)} \tag{3.15}$$

$$\omega_{p2} = -\frac{gm_6}{C_B} \tag{3.16}$$

$$\omega_u = \frac{gm_1}{C_c} \tag{3.17}$$

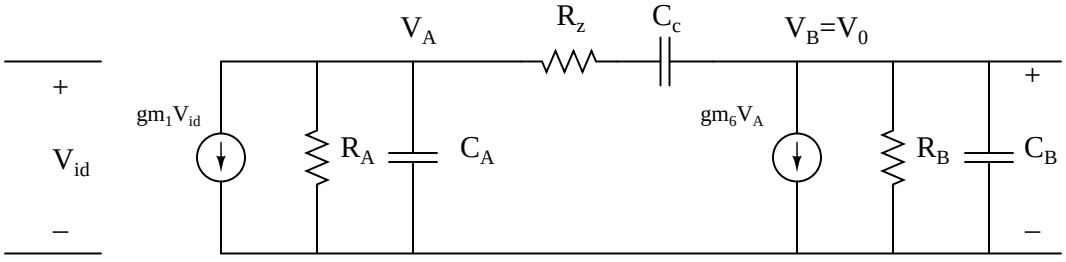


Fig. 3.3: Small-signal equivalent circuit of the two-stage amplifier.

3.4.1 High Bandwidth Design (Long-Channel Design)

The above two-stage configuration using a nulling resistor introduces a zero in the right half plane. As can be seen, the right half plane (RHP) zero is an important aspect to consider as it causes instability in the amplifier. The resistor R_z allows independent control over the placement of zero. It can be seen that the value of R_z if set to $\frac{1}{g_{m6}}$ eliminates the right half plane (RHP) zero. Also, another method is to place the RHP zero on top of the left half plane (LHP) pole location ω_{p2} which eliminates the output loading capacitance inferred from the above equations. This gives us the value of R_z as follows:

$$R_z = \left(\frac{C_c + C_B}{C_c}\right)\left(\frac{1}{g_{m6}}\right). \tag{3.18}$$

The on-chip implementation of the nulling-resistor R_z is a transistor operating in the triode (linear) region. We proceed to design the two-stage op-amp with design equations developed by Holberg [12]. The design approach is inherently different and currents are assumed in the two stages because of the nature of high bandwidth design. We emphasize the fact that the amplifier is able to supply sufficiently high value of currents to drive the antenna. Figure 3.4 shows the schematic of the amplifier in virtuoso cadence. The bias current is generated using an ideal current source.

Results: This section shows the results obtained by using a combination of design techniques mentioned by Holberg and Mahattanakul [12, 15]. The results provide a clear indication that using long-channel design techinque it is very difficult to achieve desired results without tweaking of the transistor dimensions. Here the results are presented without any tweaking of the dimensions. Figure 3.5 shows the open-loop frequency response in the presence of a source-follower output buffer. The design specifications we are trying to achieve are as follows: $A_v = 60dB$, $f_u = 100MHz$ and PhaseMargin = 60°. We also test the configuration of the two-stage op-amp in a unity gain configuration. This configuration provides us very important information regarding the stability of the op-amp. Figure 3.6 shows the frequency response in the unity gain configuration. As can be seen from the frequency response plots the amplifier fails to achieve the desired specifications. The long

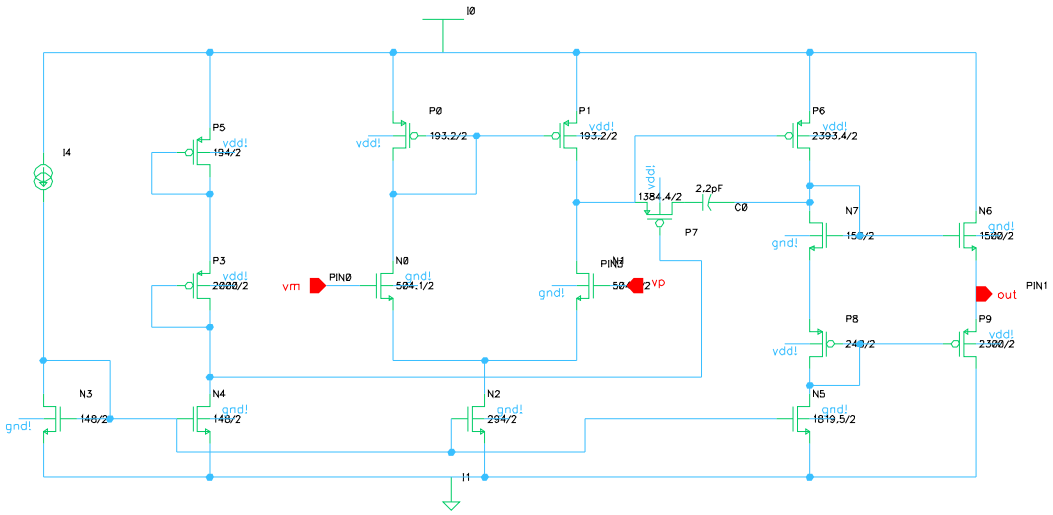


Fig. 3.4: Schematic of the two-stage amplifier with output buffer.

channel equations cannot provide us the results without iterations and tweaking for various parameters. Thus the process of iteration is not always intuitive and can quickly become a tedious task.

3.4.2 Source-Follower Output Buffer

The design of CMOS amplifiers is essentially an OTA design because of the nature of its on-chip implementation unlike a general purpose design for the bipolar counterparts. Most of these amplifiers see a capacitve load at the output stage so the high output resistance at the output stage does not have a significant impact on the performance. Our current design of the analog front-end amplifier requires an output buffer as it is implemented in the non-inverting configuration with feedback resistors and capacitors. In the previous section, we designed a two-stage amplifier followed by a source-follower buffer. We now do a study on the frequency response of the source-follower. A source-follower ideally provides a gain of unity and has a low-output resistance which is an important property for buffers. Figure 3.7 shows a source follower with its equivalent small-signal circuit. The following equations

govern the gain and output resistance of a source follower:

$$Av = \frac{g_m}{g_m + g_{mb}}, \tag{3.19}$$

$$R_{out} = \frac{1 + s.R_S.C_{GS}}{g_m + s.C_{GS}}, \tag{3.20}$$

where g_{mb} is the body-effect and R_S is the resistance of the input source (it could be the output resistance of an OTA design). As can be seen from the gain equation, the gain is always less than unity. We are interested in the output resistance as it will achieve a lower resistance in our amplifier circuit while providing an approximate gain of unity (neglecting body-effect). We can incur the following:

- At low frequencies (i.e., @DC) $R_{out} = \frac{1}{g_m}$;
- At high frequencies $R_{out} = R_S$.

Plotting the output resistance with respect to the analysis above gives us the graph as shown in fig. 3.8. The graph clearly indicates that as frequencies increase the output resistance may be equal to its preceding stage output impedance. It also causes ringing in its output response. Hence, source-followers are a poor choice as output buffers in the present design of the analog front-end amplifier.

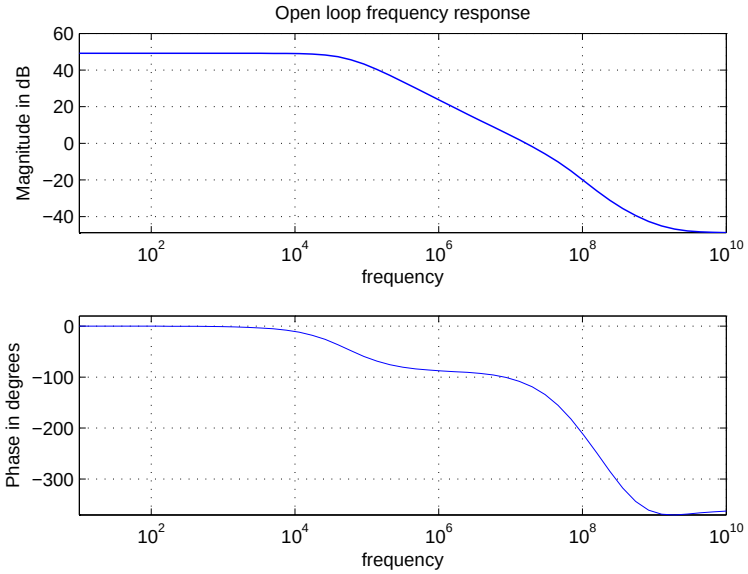


Fig. 3.5: Open-loop response of two-stage op-amp designed using long-channel equations.

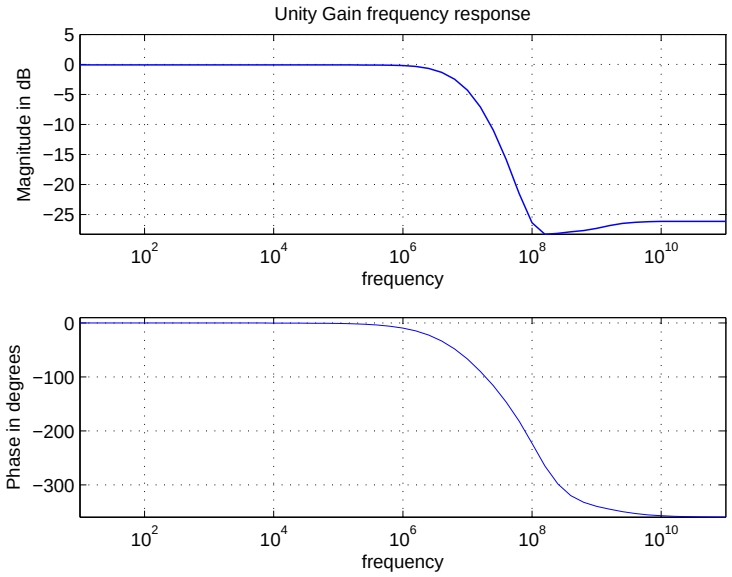


Fig. 3.6: Unity gain response indicating that the op-amp is stable because of a good phase margin.

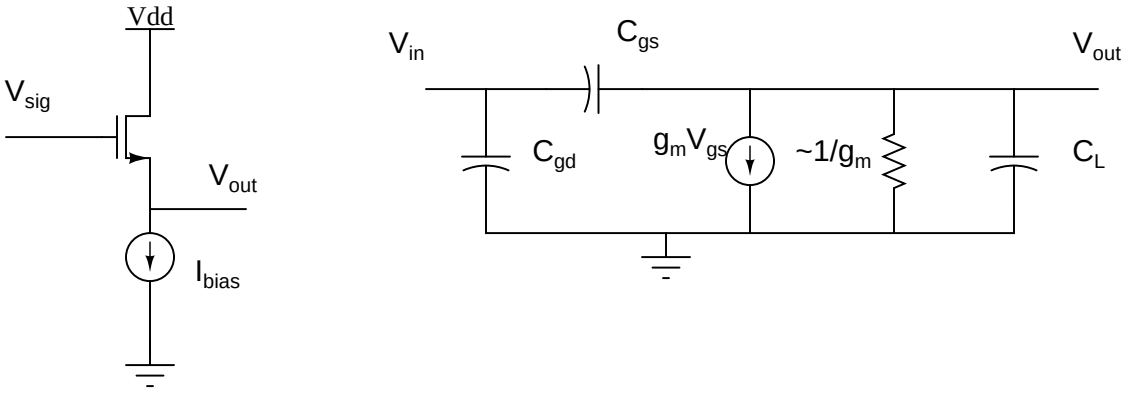


Fig. 3.7: Source-follower configuration with its equivalent small-signal circuit.

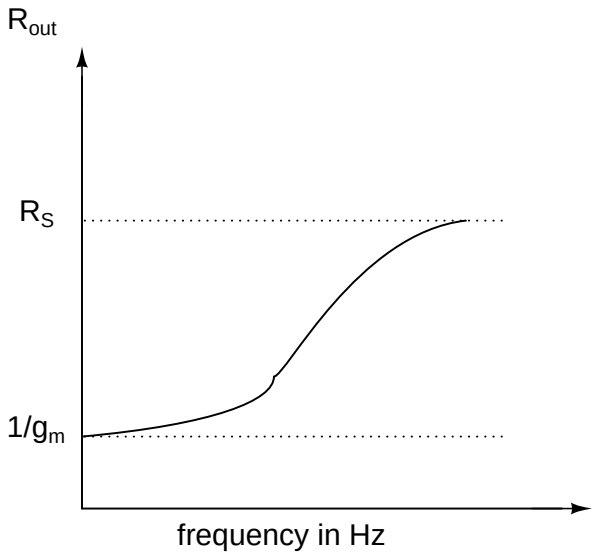


Fig. 3.8: Output resistance of source-follower with respect to frequency.

Chapter 4

The g_m/I_D Methodology

With the advent of advanced fabrication processes the transistor dimensions have reduced drastically. Although the trend towards miniaturization has helped digital circuitry with densely packed transistors, the analog counterpart had to pay the price with decreasing supply voltage headroom, reduced dynamic range, lower gain, and similar other attributes. As a consequence the conventional long-channel equations employed in the analog design were no longer producing desired results. We have already shown the design of OTAs in the previous chapters using the conventional design technique. The short-channel effects combined with the need for precise and intuitive design procedure called for a complete characterization of the process technology. A methodology is devised where currents are fixed to arrive at the transistor dimensions to satisfy specifications like the gain-bandwidth, low power, area, etc. The g_m/I_D is a ratio obtained by complete characterization of the process for the PMOS and NMOS transistors. The following sections further elaborate the g_m/I_D design approach.

4.1 Introduction

The long-channel design has different set of equations which govern each region of operation. The overdrive voltage V_{ov} is a key parameter which defines the region the device is operating in. The g_m/I_D method characterizes the performance of a transistor in all regions of operation [17, 18]. The following section develops the long-channel equations of the transistor. From these equations we derive the figure of merits for the g_m/I_D method.

Triode Region

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) - \frac{V_{DS}}{2} \right] . V_{DS} \tag{4.1}$$

Saturation Region

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS}-V_t\right)^2 \tag{4.2}$$

Transconductance

$$g_m = \frac{dI_D}{dV_{GS}} = \mu C_{ox}\frac{W}{L}\left(V_{GS}-V_t\right) = \mu C_{ox}\frac{W}{L}V_{ov} \tag{4.3}$$

$$g_m = \sqrt{2I_D\mu C_{ox}\frac{W}{L}} = \frac{2I_D}{V_{ov}} \tag{4.4}$$

Output Conductance with Channel Length Modulation (CLM)

$$g_{ds} = \frac{dI_D}{dV_{DS}} = \frac{d}{dV_{DS}}\left[\frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS}-V_t\right)^2\left(1+\lambda V_{DS}\right)\right] \tag{4.5}$$

$$g_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS}-V_t\right)^2\lambda = \frac{\lambda I_D}{1+\lambda V_{DS}} \simeq \lambda I_D \tag{4.6}$$

Intrinsic Gate Capacitances

$$C_{gg} \triangleq C_{gs}+C_{gb}+C_{gd} \tag{4.7}$$

The performance of any analog circuit can be broadly divided into its large signal and small signal characteristics. The current I_D determines the power dissipation; voltage V_{DS} the available signal swing (both the ICMR and ODR); transconductance g_m signifies speed and voltage gain; the intrinsic capacitances C_{GS}, C_{GD}, C_{DB} determine the speed and the output impedance; r_0 the voltage gain of the circuit. Summarizing the above we have

DC Voltage Gain

$$A_{DC} = g_m * r_o \tag{4.8}$$

Bandwidth

$$f_{transit} = \frac{1}{2\pi R_{in}C_{gg}} \tag{4.9}$$

Power Dissipation

$$P = V_{DD} * I_D \tag{4.10}$$

4.1.1 Figure of Merits (FOM)

We can now define certain figure of merits for the technology characterization in the g_m/I_D-based method.

Transconductor Efficiency

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}} \tag{4.11}$$

Transit Frequency

$$\frac{g_m}{C_{gg}} \simeq \frac{3}{2}\frac{\mu V_{ov}}{L^2} \tag{4.12}$$

Intrinsic Gain

$$\frac{g_m}{g_{ds}} \simeq \frac{2}{\lambda V_{ov}} \tag{4.13}$$

The equations on the right hand side are derived from the square law equations.

4.1.2 g_m/I_D Graphs

The next step in the technology characterization is the generation of plots in accordance with the Figure of Merits (FOM). Figure 4.1 shows an N-Channel Metal Oxide Semiconductor (NMOS) transistor setup in cadence which is used for generating the plots. In a similar manner a P-Channel Metal Oxide Semiconductor (PMOS) transistor is setup to obtain its FOM. A typical comparison between the values of an NMOS and PMOS transistor is shown in fig. 4.2. For this simulation transistor dimensions of $\frac{W}{L} = \frac{50\mu m}{2\mu m}$ is chosen.

A family of curves for PMOS and NMOS transistors are obtained for various transistor lengths. L_{min}, $2.5 * L_{min}$, $5 * L_{min}$, and $10 * L_{min}$ are the lengths of transistors chosen for

simulation in the TSMC $0.35\mu m$ process. We obtain plots for the following:

- g_m/g_{ds} vs g_m/I_D graph. Figure 4.3 shows the plot for both NMOS and PMOS devices;
- f_T vs g_m/I_D graph. Figure 4.4 shows the plot for both NMOS and PMOS devices;
- I_d/W vs g_m/I_D graph. Figure 4.5 shows the plot for both NMOS and PMOS devices;
- I_D/W vs V_{ov} graph. Figure 4.6 shows the plot for both NMOS and PMOS devices.

4.2 Design Illustration of a Common-Source Amplifier

In this section, a simple common-source amplifier is designed which allows us to get an insight into the utilization of the graphs generated for the g_m/I_D method [19, 20]. Figure 4.7 shows a simple common source amplifier. The target specifications for this amplifier are: $f_u = 100MHz$, $C_L = 5pF$, and $I_D \leqslant 1mA$.

Method 1 In this we primarily assume a current of $I_D = 1mA$ and proceed with our design,

$$\begin{aligned} g_m &= 2\pi f_u C_L = 2\pi * 100 * 10^6 * 5 * 10^{-12} = 3.141mS, \\ \frac{g_m}{I_D} &= \frac{3.141m}{1m} = 3.141. \end{aligned}$$

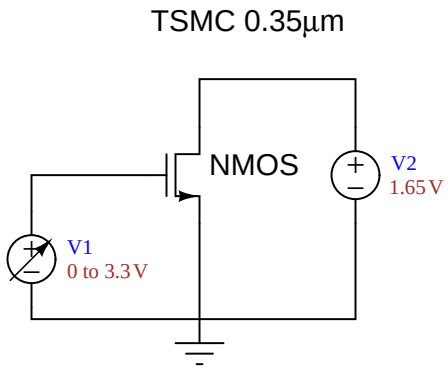


Fig. 4.1: Schematic of the NMOS transistor setup in cadence.

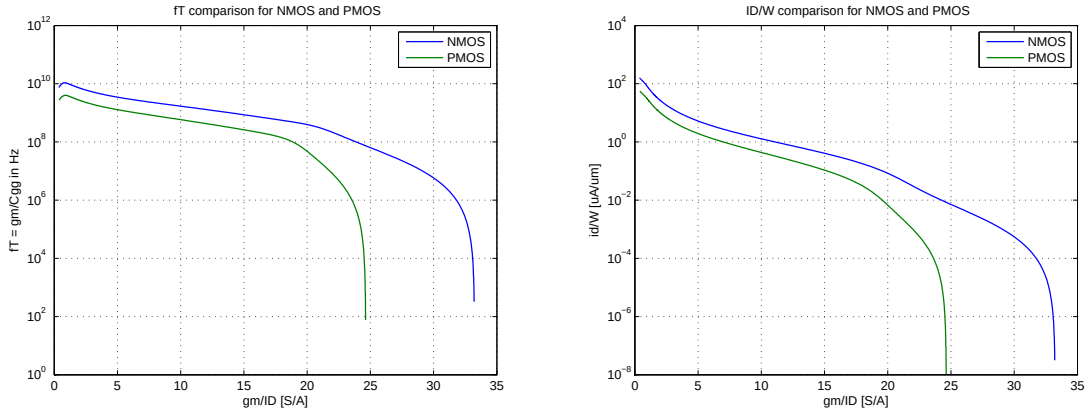


Fig. 4.2: Comparison of PMOS and NMOS transistors for f_T vs g_m/I_D and I_D/W vs g_m/I_D.

We then use the I_D/W vs g_m/I_D graph in fig. 4.8. Corresponding to the g_m/I_D value we obtain $I_D/W = 10^{1.0895} = 12.288$.

$$W = \frac{I_D}{I_D/W} = \frac{1m}{12.288} = 81.37\mu m$$

The Bode plot in fig. 4.9 shows us that we achieve the desired bandwidth without much effort.

Method 2 In this method, instead of assuming the current we assume the overdrive voltage V_{ov} in which the transistor is operating. Assume $V_{ov} = 250mV$.

$$\begin{aligned} g_m &= \frac{2I_D}{V_{ov}} \\ g_m &= 2\pi f_u C_L = 2\pi * 100 * 10^6 * 5 * 10^{-12} = 3.141mS \\ I_D &= \frac{g_m.V_{ov}}{2} = \frac{3.141 * 10^{-3} * 250 * 10^{-3}}{2} = 392.625\mu A \end{aligned}$$

We use the I_D/W vs V_{ov} graph in fig. 4.10. Corresponding to the V_{ov} we obtain $I_D/W = 2.1$.

$$W = \frac{I_D}{I_D/W} = \frac{392.625 * 10^{-6}}{2.1} = 186.96\mu m$$

The Bode plot in fig. 4.11 shows us the magnitude plot. It is interesting to note that there

is a mismatch in the results obtained by the two design methods. We can observe that the assumption of higher values of curent in the previous method gave us a more accurate result. Thus for a high bandwidth design it can be seen that assumption of a higher value of current gives us more accurate results. This observation will be used in the development of further designs as our main emphasis is obtaining a high bandwidth amplifier to be used in the analog front-end of the PIP.

4.3 Key Features of the g_m/I_D Method

Some of the key features with a g_m/I_D based design are as follows [21, 22]:

- This method gives us an idea of the device operating regime. The set of curves generated for a particular technology is continuous and there are no transition in equations from various regions of operation. Thus we can conveniently select the device operation as per our needs;

- Using a pre-generated set of graphs for a particular technology we can easily arrive at the transistor dimensions meeting the specifications by breaking the amplifier into its basic constituent structures;

- The amount of iteration required in designing complex analog circuits is greatly reduced. Since there is complete characterization of the technology, additional graphs which completely characterize the parasitics can be generated. The use of approximate equations determining the device behavior is eliminated.

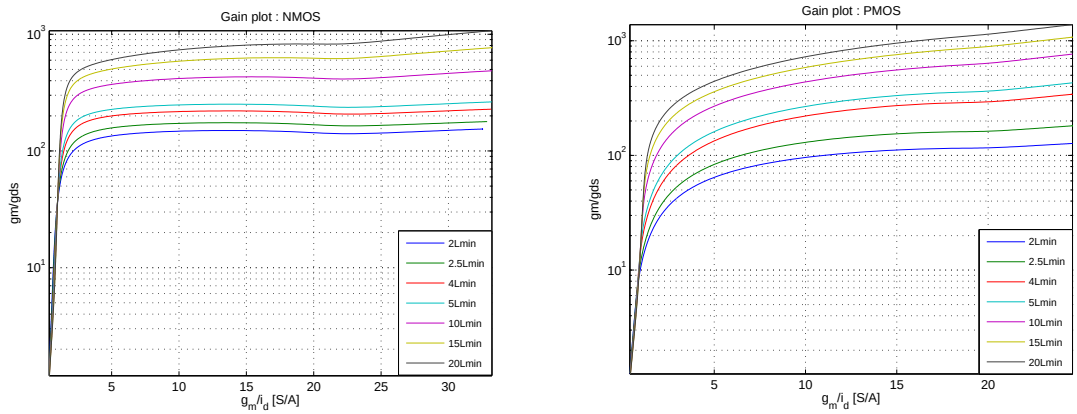


Fig. 4.3: g_m/g_{ds} vs g_m/I_D plot for NMOS and PMOS device.

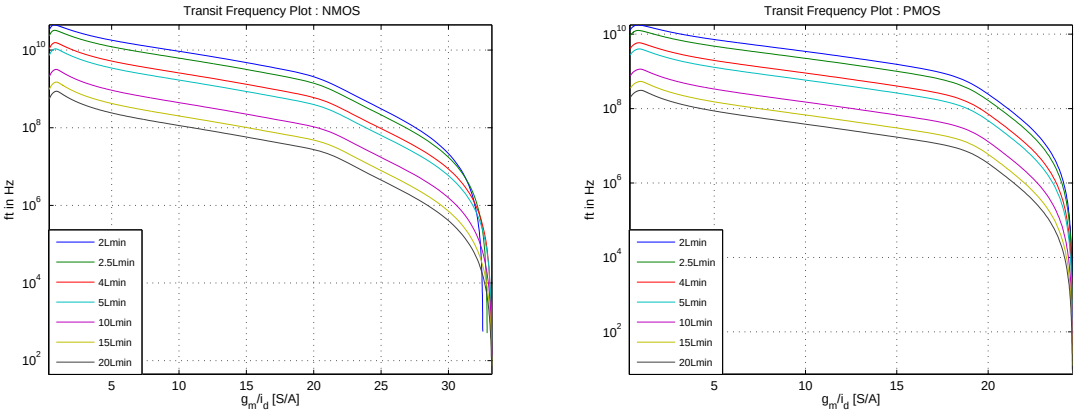


Fig. 4.4: f_T vs g_m/I_D plot for NMOS and PMOS device.

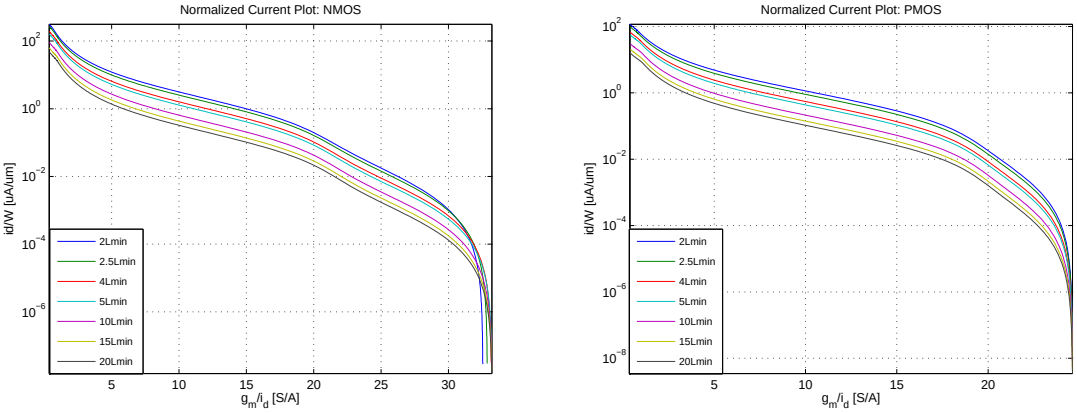


Fig. 4.5: I_D/W vs g_m/I_D plot for NMOS and PMOS device.

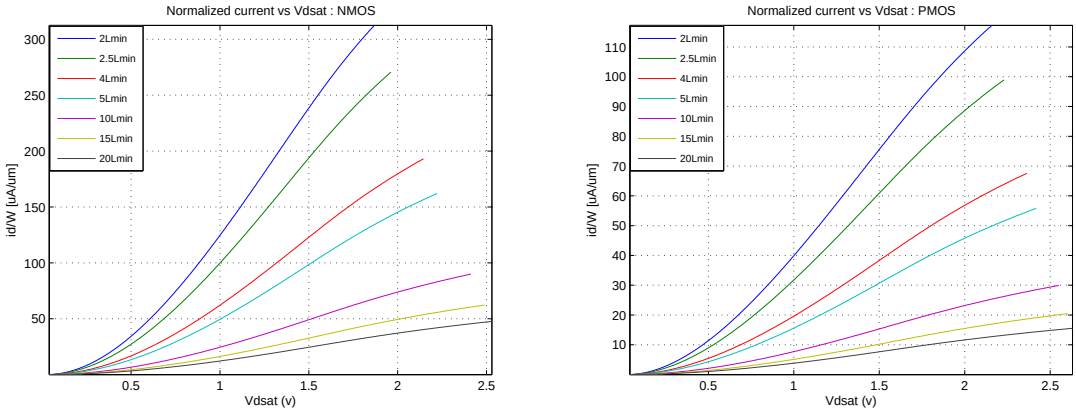


Fig. 4.6: I_D/W vs V_{ov} plot for NMOS and PMOS device.

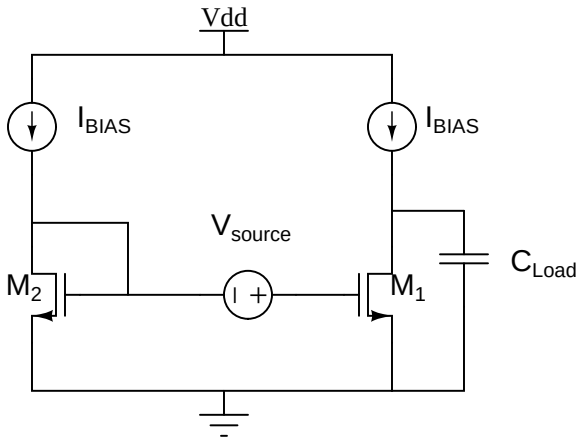


Fig. 4.7: Schematic of the common-source amplifier.

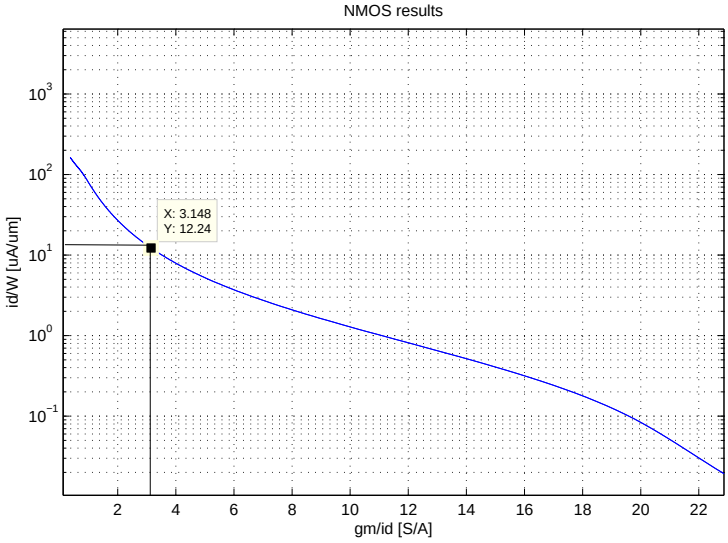


Fig. 4.8: I_D/W vs g_m/I_D plot.

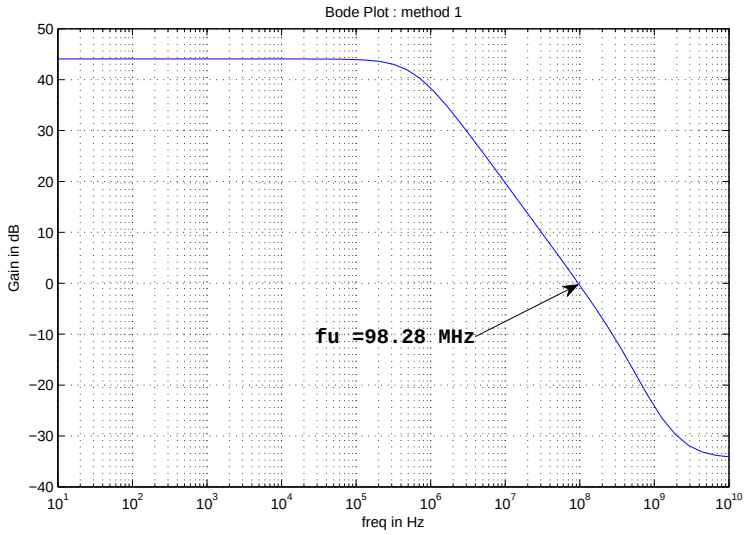


Fig. 4.9: Gain plot from method 1.

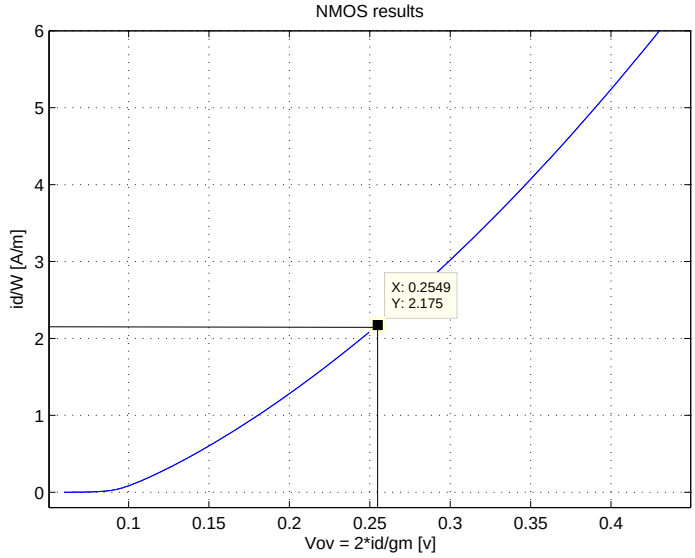


Fig. 4.10: I_D/W vs V_{ov} plot.

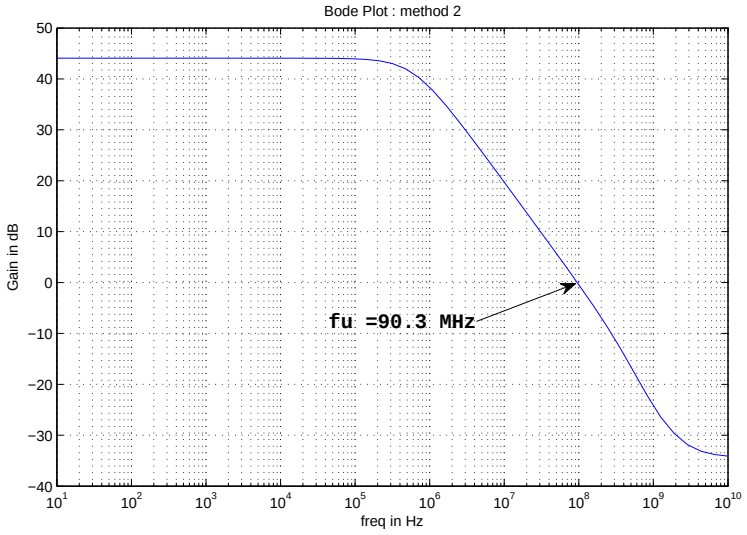


Fig. 4.11: Gain plot from method 2.

Chapter 5

OTA Design Using the g_m/I_D Method

5.1 Two-Stage OTA Design

In this section we design a two-stage operational transconductance amplifier using a procedural design approach [17]. The entire op-amp is broken down into its constituent parts and then the transistor dimensions are obtained by the g_m/I_D method to meet the target specifications.

5.2 Specifications

The following are the circuit-level design parameters.

Static Current Consumption

$$\Sigma = I_{D5} + I_{D7} + I_{bias} \tag{5.1}$$

Gain and Output Resistance

$$A_v = A_{v1}.A_{v2} \tag{5.2}$$

$$A_{v1} = g_{m1,2}.R_{01}; R_{01} = \frac{1}{g_{ds1,2} + g_{ds3,4}} \tag{5.3}$$

$$A_{v1} = g_{m6}.R_{02}; R_{02} = \frac{1}{g_{ds6} + g_{ds7}} \tag{5.4}$$

Common Mode Input Range [CMIR]

$$V_{iCM,max} = V_{DD} - \mid V_{GS3,4} \mid - \mid V_{DSsat1,2} \mid - \mid V_{GS1,2} \mid \tag{5.5}$$

$$V_{iCM,min} = V_{DSsat5} + V_{GS1,2} \tag{5.6}$$

Output Dynamic Range [ODR]

$$V_{o,max} = V_{DD} - V_{DSsat6} \tag{5.7}$$

$$V_{o,min} = V_{DSsat7} \tag{5.8}$$

Slew Rate

$$SR = min\left\{\frac{I_{D5}}{C_c}, \frac{I_D7}{C_L}\right\} \tag{5.9}$$

Input Referred Equivalent Noise

$$v_n^2 = 2.v_{n1,2}\left(\frac{g_{m3,4}}{g_{m1,2}}\right)^2.v_{n3,4}^2 + \frac{v_{n6}^2 + \left(\frac{g_{m7}}{g_{m6}}^2.v_{n7}\right)^2}{A_{v1}^2} \tag{5.10}$$

Gain Bandwidth and Phase Margin

$$f_{GBW} = \frac{g_{m1}}{2\pi C_c} \tag{5.11}$$

$$PM = 180^\circ - \arctan\left(\frac{\omega}{f_{p1}}\right) - \arctan\left(\frac{\omega}{f_{p2}}\right) - \arctan\left(\frac{\omega}{f_{z1}}\right) \tag{5.12}$$

Pole Zero Locations: We have already determined the pole-zero locations of the two-stage OTA in Chapter 3. The summary is given below.

$$\omega_{p1} = -\frac{1}{g_{m6}R_{01}R_{02}C_c} \tag{5.13}$$

$$\omega_{z1} = \frac{1}{C_c\left(\frac{1}{g_{m6}} - R_z\right)} \tag{5.14}$$

$$\omega_{p2} = -\frac{g_{m6}}{C_L} \tag{5.15}$$

$$\omega_u = \frac{g_{m1}}{C_c} \tag{5.16}$$

$$\omega_{p3} = \frac{g_{m3,4}}{\Sigma C_{G3,4}} \tag{5.17}$$

5.3 Circuit Partition

The two-stage Miller OTA can be partitioned into the following basic analog structures.

5.3.1 Compensation Capacitor

The compensation capacitor determines the location of the poles and zeros of the amplifier transfer function. It also determines the transconductance of the input pair differential transistors. We adopt the approach in Holberg [12] for determining the value of compensation capacitor. Assumption that for a two-pole and one-zero system, the zero location is at least 10 times greater than the value of the unity gain frequency is made. It may always not be the case for a high-bandwidth design. Illustration for a phase margin $PM = \phi_{PM}$:

$$\phi_{PM} = 180^\circ - \arctan\left(\frac{\omega}{|p_1|}\right) - \arctan\left(\frac{\omega}{|p_2|}\right) - \arctan\left(\frac{\omega}{|z_1|}\right), \quad (5.18)$$

$$180^\circ - \phi_{PM} = \arctan\left(\frac{f_u}{|p_1|}\right) + \arctan\left(\frac{f_u}{|p_2|}\right) + \arctan\left(\frac{f_u}{|z_1|}\right), \quad (5.19)$$

$$180^\circ - \phi_{PM} = \arctan\left(A_v\right) + \arctan\left(\frac{f_u}{|p_2|}\right) + \arctan 0.1, \quad (5.20)$$

$$\phi_{PM} = 90 - \arctan 0.1 - \arctan\left(\frac{f_u}{|p_2|}\right). \quad (5.21)$$

Calculate the location of the pole p_2. The equation will be of the form $p_2 \geq x.f_u$. From the assumption $\frac{g_{m6}}{C_c} > 10 * \frac{g_{m2}}{C_c}$ we arrive at the following equation.

$$C_c > \frac{x.C_L}{10}, \quad (5.22)$$

where C_L is the load capacitance, g_{m2} transconductance of the differential pair transistor, and g_{m6} transconductance of the common source stage transistor.

5.3.2 Differential Pair

This basic structure determines the gain of the first stage, the gain-bandwidth, CMIR,

and noise specifications as can be seen from the equations developed earlier. The Transconductance efficiency g_m/I_D can be determined as follows:

$$g_{m1,2} \geq 2\pi C_c f_{GBW} \longrightarrow \frac{g_{m1,2}}{\frac{I_{D5}}{2}} = \left(\frac{g_m}{I_{Dsat}}\right)_{1,2}. \tag{5.23}$$

The value of the compensation capacitor significantly determines the specifications of this analog block. Sometimes it is necessasry to re-calculate the figure of merits to satisfy the value of compensation capacitor used. Another point to be noted is that the gain of the first stage is determined by $\frac{1}{g_{DS1,2}+g_{DS3,4}}$. Thus the lengths of the transistors determine the gain of this stage. In our design we select a transistor length and use it throughout our design.

5.3.3 Load Structure

The PMOS transistors M_3, M_4, and M_6 form the load structure of the two stages. This structure is responsible for fixing the stability, offset, and most importantly the output dynamic range (ODR) of the system. It is necessary that the g_m/I_D ratio of transistors $M_{3,4}$ and M_6 are the same for perfect matching (to avoid offset) at the output of the first stage. The output stage has currents several times the current flowing at the input stage.

$$\frac{g_{m3,4}}{\frac{I_{D5}}{2}} = \frac{g_{m6}}{I_{D7}} = 2.x.g_{m3,4}, \tag{5.24}$$

where x is the scaling factor of current in the second satge $x = \frac{I_{D7}}{I_{D1}}$. In general, the IF for the load structures can be determined by the output range specification. Generally the load structures are operated from moderate to strong inversion. The g_m/I_D vs V_{DSsat} curve will determine the g_m/I_D for the load structures. $V_{DSsat} \longrightarrow (g_m/I_D)_{3,4} = (g_m/I_D)_6$ as the load structures of the two stages need to be matched.

5.3.4 Common Source Stage

The current flowing in the second stage determines the transconductance of the transistor M_6.

$$g_{m6} \quad > \quad 2\pi.y_{pm}.f_{GBW}.C_L \tag{5.25}$$

The factor y_{pm} is determined from the phase margin specification. The non-dominant poles ω_{p2} and ω_{p3} need to be farther apart from each other in order to achieve an acceptable phase margin. $f_{p3} >> f_{GBW}$.

$$f_{p2} \quad = \quad \frac{g_{m5}}{2\pi C_L} = \frac{2.x.g_{m3,4}}{2\pi C_L} \tag{5.26}$$

The transistor length L_6 determines the gain of this stage since the output resistance $R_{02} = \frac{1}{g_{ds6}+g_{ds7}}$. For our design the transistor dimensions of the common source stage is determined by the current flowing through this stage. Usually it is equal to 8 - 12 times the current provided by the bias circuitry. The advantage of this method is that the required transconductance factor mentioned earlier is easily satisfied. Higher values of current at the output help in achieving the desired bandwidth and slew rate specifications at the cost of increased power consumption.

5.3.5 Bias Circuit Design

The transistor M_5 supplies the current to the differential pair. It mirrors the current supplied by the bias circuitry. An ideal matching should exist between all the transistors that form the bias circuitry.

- Select an appropriate V_{Dsat} voltage for the tail transistor and determine the normalized current using the I_D/W vs V_{ov} curve.
- Determine the g_m/I_D ratio and use the same ratio for the PMOS transistors in the bias circuitry. This is done to ensure better matching.

The tail transistor determines the Power Supply Rejection ration (PSRR) of the op-amp. Thus it is an important consideration while designing op-amps. In our design, as previously mentioned, we pick a single length and use it throughout our design.

$$PSRR = \frac{A_v}{g_{m5}.R_{02}} \tag{5.27}$$

5.4 Frequency Compensation Techniques

This section describes the frequency compensation techniques that can be used for the two-stage op-amp. We explore the methods applicable to our design as mentioned by Holberg and Mahattanakul [12, 15, 16].

The selection of compensation capacitor derived earlier in the chapter assumes the presence of zero at least 10 times greater than the unity gain frequency. Although this approximation may hold good for low-bandwidth op-amp design, the condition may not satisfy high-bandwidth requirements. Thus in our design we select a sufficiently high value of compensation capacitor and then design using the frequency compensation techniques mentioned below. If the value of compensation capacitor selected is high, it can also be implemented off-chip to reduce the area of the main amplifier.

5.4.1 Nulling Resistor Approach

- The transfer function for the two-stage op-amp derived earlier clearly indicates the location of the poles and zeros. We see the presence of the output pole and the RHP zero. The RHP zero can cause significant stability problems for high bandwidth design as its location may not be sufficiently far in the frequency regime of interest. The location of zero as derived earlier is as follows:

$$\omega_{z1} = \frac{1}{C_c\left(\frac{1}{g_{m6}} - R_z\right)}. \tag{5.28}$$

  By setting the value of $R_z = 1/g_{m6}$ we effectively remove the zero in the transfer function. This method is not very effective for high-bandwidth applications due to

reasons mentioned earlier.

- Another approach is to place the zero on top of the output pole location so that there is a pole zero cancellation. Consider the zero and the output pole location given by the equations:

$$\begin{aligned} \omega_{z1} &= \frac{1}{C_c\left(\frac{1}{g_{m6}} - R_z\right)}, \\ \omega_{p2} &= -\frac{g_{m6}}{C_L}. \end{aligned}$$

Solving for R_z using the above two equations we obtain the following:

$$R_z = \left(\frac{C_c + C_L}{C_c}\right).\left(\frac{1}{g_{m6}}\right). \tag{5.29}$$

The presence of a resistor on-chip can significantly increase the parasitics and the area of the chip. It can also bring about a temperature dependence. Thus we implement the on-chip resistor using a transistor operating in the linear region. But the g_m/I_D method of implementation poses a challenge in obtaining the figure of merits for such a design. A g_m/I_D method for such an implementation still needs to be explored. In the current design a trial and error method is employed to achieve the desired deisgn goal for the tranistor operating in the linear region.

5.4.2 Current Buffer Method

The Miller capacitor with a common gate current buffer helps in realizing a single dominant pole behavior for a two-stage op-amp. A typical implementation of such a circuit is given in fig. 5.1. Again we encounter limitations to its use for high bandwidth design. An attempt has been made in the following section to realize such a circuit using the g_m/I_D method. A more elaborate analysis of this technique has been explained and implemented by Holberg and Mahattanakul [12, 16]. The design procedure for the two-stage design essentially remains the same and in this method a common-gate transistor is designed using

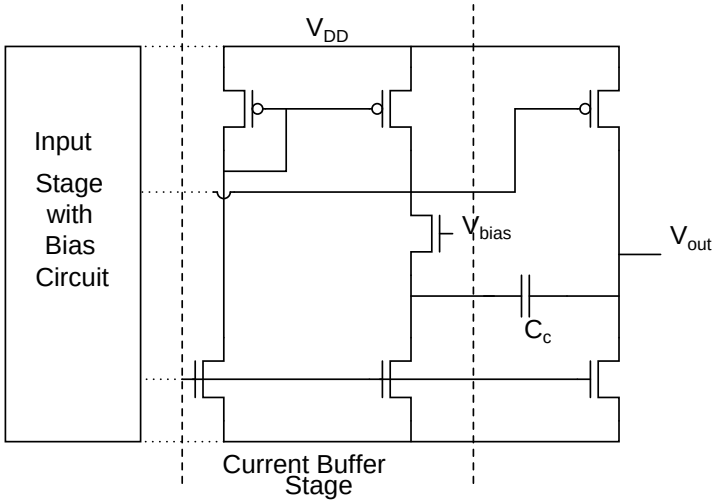


Fig. 5.1: Frequency compensation technique implemented using a current buffer technique.

the g_m/I_D method.

5.5 Design Illustration

We proceed to design our two-stage amplifier implementing frequency compensation techniques and output buffer implementation with a robust bias circuit satisfying the following specifications. $A_v > 60dB$, $f_u = 100MHz$, $PM > 45^\circ$, $SR > 50V\mu s$.

5.5.1 Test Benches

The following test benches help us in the complete characterization of the amplifier we design. Figure 5.2 is used to test the amplifier in unity gain configuration and its output dynamic range. A square input indicated can either be a sinusoidal or pulse stimulus depending on the parameter to be measured. Figure 5.3 measures the common mode rejection ratio of the amplifer, and fig. 5.4 measures the open-loop response of the amplifer.

5.5.2 Two-Stage Amplifier with Nulling Resistor Implementation

The circuit of a two-stage op-amp using the nulling resistor is shown in fig. 5.5. An on-chip implementation of a resistor can be done by using a transistor operating in the linear region as it helps in the reduction of area and parasitics. Thus the practical implementation of a two-stage amplifier is shown in fig. 5.6. Table 5.1 summarizes the specifications achieved for the amplifier design and Table 5.2 indicates the dimensions of the transistors used in the amplifier design.

Figures 5.7 and 5.8 show the open-loop and unity gain frequency response of the amplifier, respectively. The amplifier stability is analyzed in the most unfavorable case, that is when the negative feedback factor is equal to one.

5.5.3 Setup Measuring Antenna Impedance

The following section shows the test benches used to test the amplifier measuring antenna impedance. An actual circuit setup to measure the antenna impedance is not implemented, instead we setup a test circuit measuring the capacitance which represents the antenna. The frequency response of such a test indicates the high pass (differentiator) type of response of the ampilifier when the negative terminal is connected to the antenna (or a capacitor). Figure 5.9 shows the setup of the circuit in cadence and fig. 5.10 shows the frequency response of the test set-up. The range of frequencies measuring antenna impedance is clearly shown.

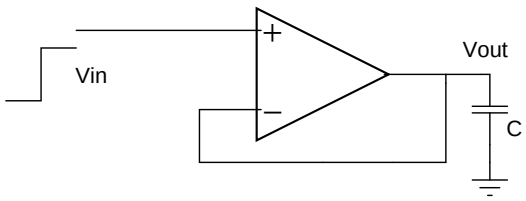


Fig. 5.2: An input square or sinusoidal stimulus to measure the slew rate, frequency response in unity gain configuration, and the output dynamic range of the amplifier.

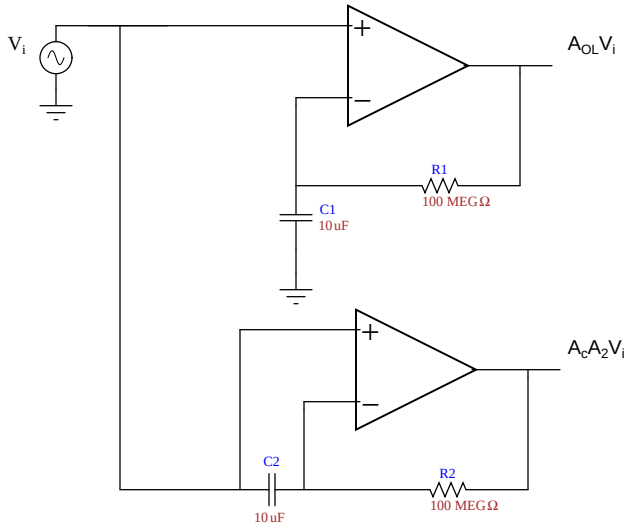


Fig. 5.3: Common mode rejection ratio measurement.

5.5.4 Two-Stage Amplifier with Current Buffer for Frequency Compensation

The two-stage amplifier is designed to have a single dominant pole response by using the current buffer frequency compensation technique. The circuit with the common-gate design in the current buffer is shown in fig. 5.11. Table 5.3 shows the specifications obtained after simulation on test benches in cadence. Comparison with the previous design seen in Table 5.1 we can infer that the unity gain bandwidth has significantly improved with a slight reduction in gain. The single dominant pole behavior can also be verified in the cadence simulations. Table 5.4 show the dimensions of the components for the two-stage amplifier with current buffer.

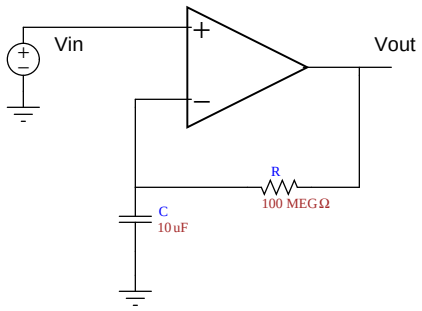


Fig. 5.4: Test bench to measure the open-loop frequency response of the amplifier.

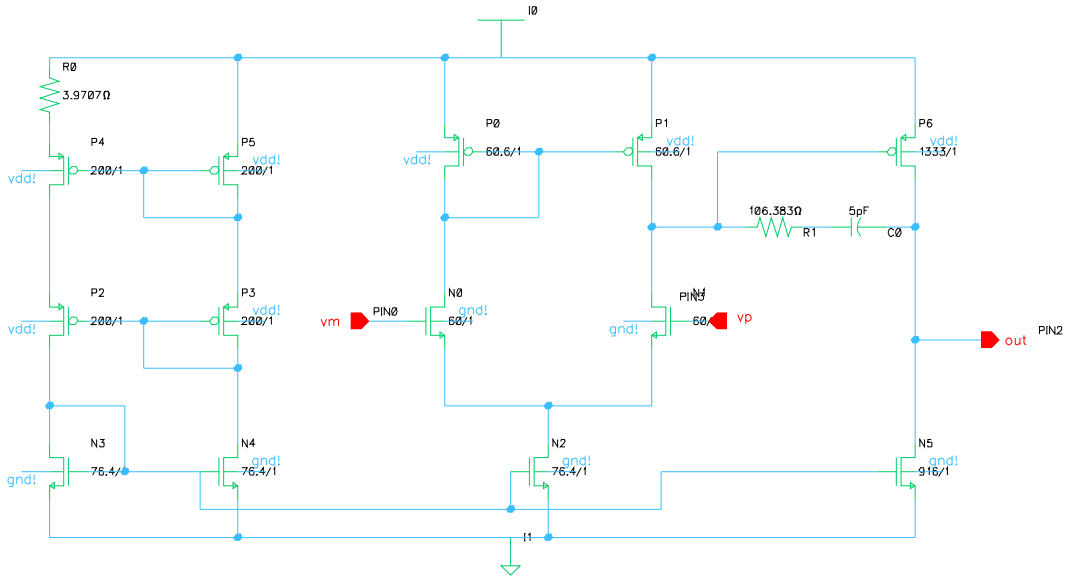


Fig. 5.5: Two-stage amplifier with nulling resistor and robust bias circuit.

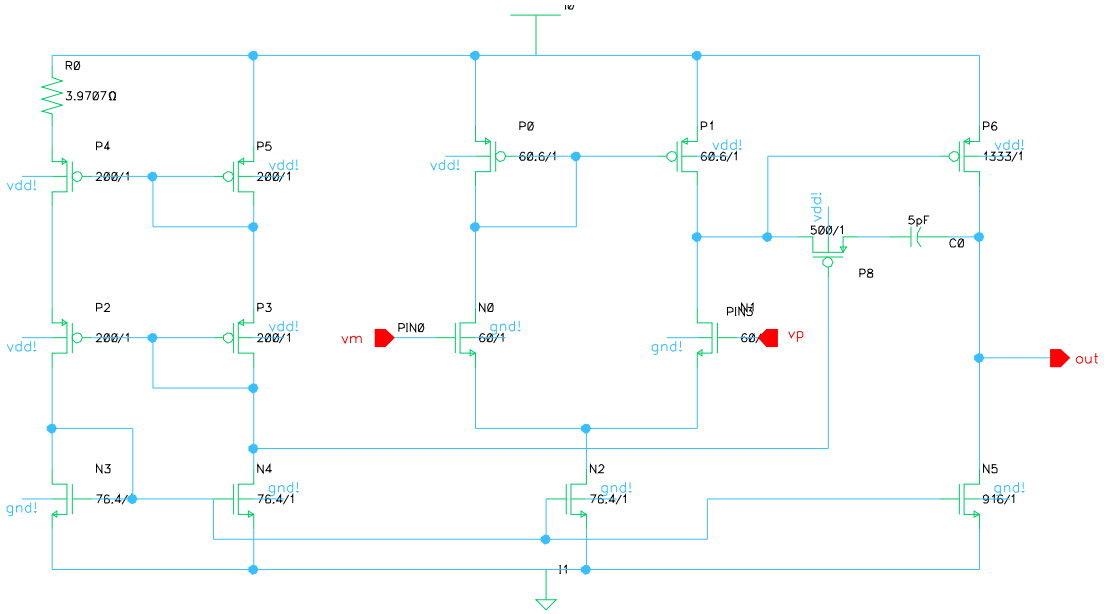


Fig. 5.6: Two-stage amplifier with nulling resistor implemented as a transistor operating in the linear region.

Table 5.1: Simulated results for the two-stage amplifier with the nulling resistor approach in TSMC 0.35μm technology.

A_v : DC Gain	$76.13dB$
f_u	$100.8MHz$
ϕ_M : Phase Margin	55.01°
Power	$23.1mW$
ODR	$2.67V$
CMRR	$118.3dB$
Slew Rate	$86.55V/\mu s$
Noise @ 1MHz	$354nV/\sqrt{Hz}$
Noise @ 5MHz	$97nV/\sqrt{Hz}$
Noise @ 10MHz	$50nV/\sqrt{Hz}$

Table 5.2: Design parameters for the two-stage amplifier with nulling resistor approach in TSMC 0.35μm technology : $Length = 1\mu m$.

Diff Pair : W_{diff}	$60\mu m$
Current mirror load : W_{load}	$60.6\mu m$
Diff Pair Tail: W_{tail}	$76.4\mu m$
Common source stage : $W_{P,out}$	$1333\mu m$
Common source stage : $W_{N,out}$	$916\mu m$
Bias Circuit,NMOS : $W_{N,bias}$	$76.4\mu m$
Bias Circuit,PMOS : $W_{N,bias}$	$200\mu m$
Compensation Capacitor : C_c	$5pF$
Transistor in linear: W_{R_z}	$500\mu m$
Bias Resistor : R_{bias}	3.9707Ω

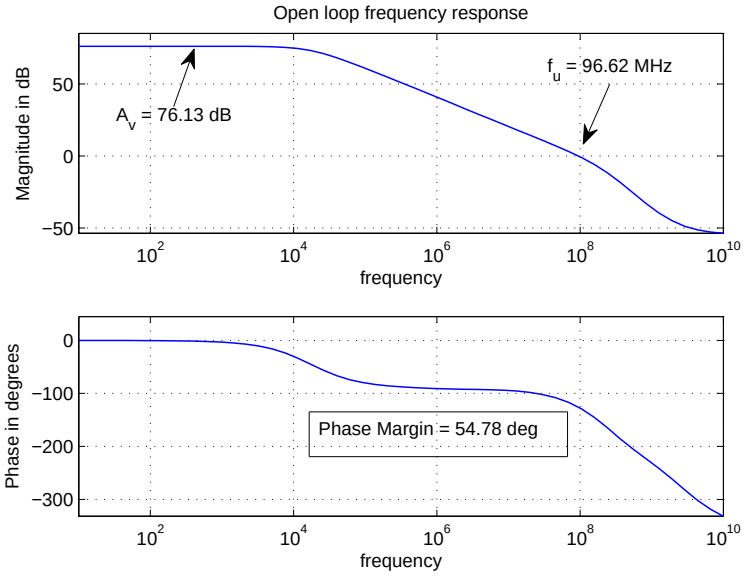


Fig. 5.7: The open-loop frequency response of the amplifier indicating the achieved gain and bandwidth.

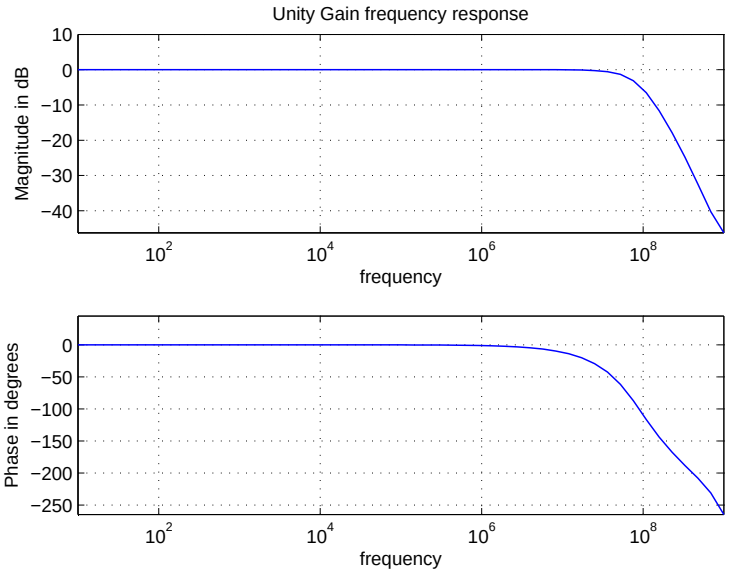


Fig. 5.8: The frequency response in unity gain configuration.

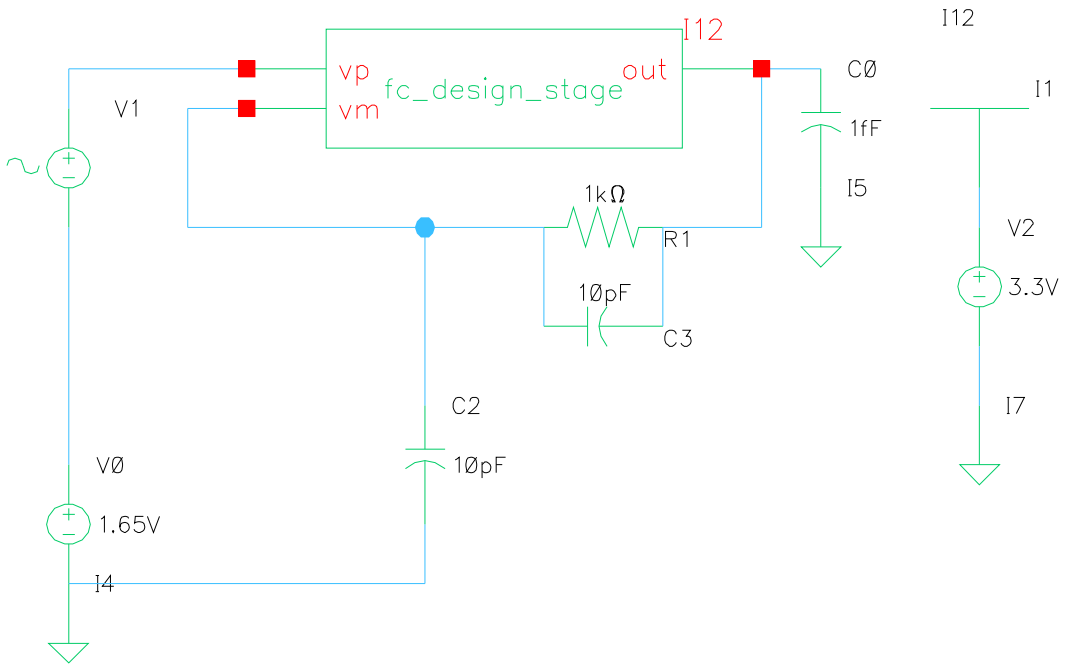


Fig. 5.9: Test setup in cadence to measure antenna impedance.

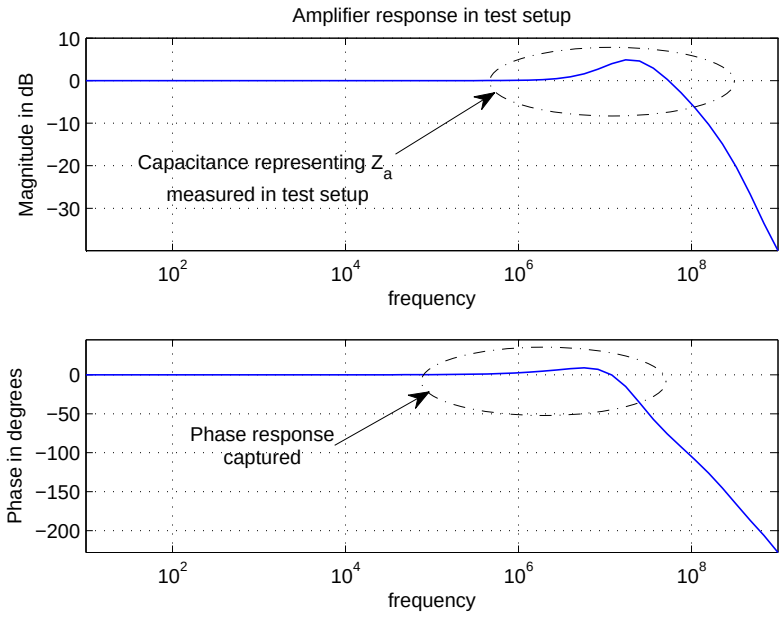


Fig. 5.10: Frequency response of the test circuit.

5.5.5 Two-Stage Amplifier with Output Buffer Implementation

An output buffer capable of driving resistive and capacitive loads for the previously designed two-stage amplifier with current buffer is implemented. It consists of a common source stage with a diode connected PMOS load to achieve low-output resistance. Figure 5.12 shows such an implementation. The use of a diode connected load at the output reduces the output dynamic range which can be seen in Table 5.5. Table 5.6 shows the dimensions of the amplifier configuration.

5.5.6 Impedance Curves for Two-Stage Amplifier Design Verification

To verify the amplifier design we generate a set of theoritical impedance curves, where the resonances in the s-domain equations developed earlier are varied over the frequency ranges of interest (between $500KHz$ to $10MHz$). Two significant poles and a zero are identified from the cadence simulations and then inserted back into the system level simulations earlier. The output after the analog front-end is verified with the theory and results of these simulations are shown in fig. 5.13.

5.6 Folded Cascode Amplifier Design

In this section we present the design results for a folded cascode amplifier designed using the g_m/I_D methodology. The procedure in which the amplifier is partitioned into its constituent analog blocks remains essentially the same. Figure 5.14 shows the implemented folded cascode amplifier with the bias circuitry. The op-amp specifications of the folded cascode amplifier are shown in Table 5.7. The final dimensions of the amplifier using the g_m/I_D method is given in Table 5.8.

5.7 Impedance Curves for Folded Cascode Amplifier Design Verification

The theoritical impedance curves generated in the previous sections are similarly employed in the verification of the folded cascode OTA design. Figure 5.15 shows the performance of the the folded cascode amplifier verified with the theoritical impedance curves.

5.8 Design Challenges

The miniaturization of the PIP instrumentation by proposing to implement all the analog and mixed-signal components on-chip posed a lot many challenges which had to be overcome. Some of the main aspects encountered when implenmenting the design in the TSMC 0.35μm CMOS technology were as follows:

- The electronics design for the PIP required a transition from PCB-based architecture low to a system on chip (SOC) implementation;
- The immediate consequence of such a transition was the reduction in available resources like the voltage headroom, area, supply voltage, and the current sourcing/sinking capabilities of the electronics;
- Even though CMOS technology is well suited for on-chip applications, designing an amplifier to match the performance of a discrete opamp was indeed a great challenge. Also, the transconductances for devices in the CMOS technology are lower than that provided by the BJT counterpart.

Thus, taking into account the above points, the designed amplifiers achieve satisfactory results in the analog front-end design. From the results obtained in the preceding sections it is clear that desired results are easily achieved using the structural design approach in the g_m/I_D methodology with minimal effort. The high-bandwidth nature of the design still necessitates the use of novel methods for frequency compensation. Thus, the g_m/I_D method with the associated graphs provide us an intuitive and precise approach in designing analog circuits. The design technique can be further extended to other areas such as switched capacitor circuits for data converters, ultra wideband communication circuits, complex analog structures, and fully differential circuits.

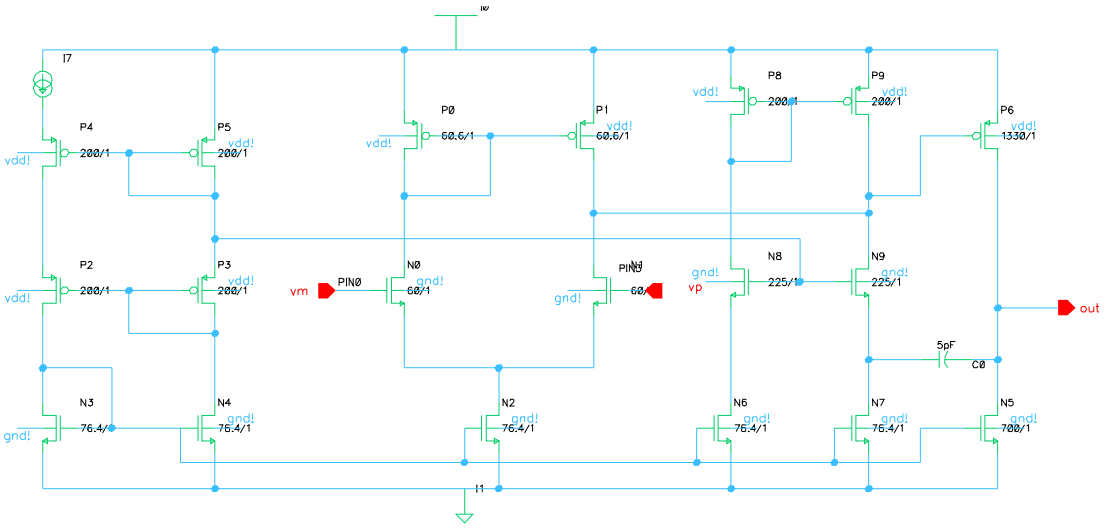


Fig. 5.11: Two-stage amplifier with current buffer using common-gate transistor to obtain a single dominant pole response.

Table 5.3: Simulated results for the two-stage amplifier with current buffer in TSMC 0.35μm technology.

A_v : DC Gain	$70.1dB$
f_u	$150.9MHz$
ϕ_M : Phase Margin	$54.6°$
Power	$25.4mW$
ODR	$2.69V$
CMRR	$110.5dB$
Noise @ 1MHz	$373nV/\sqrt{Hz}$
Noise @ 5MHz	$96nV/\sqrt{Hz}$
Noise @ 10MHz	$48nV/\sqrt{Hz}$

Table 5.4: Design parameters for two-stage amplifier with current buffer in TSMC 0.35μm technology : $Length = 1\mu m$.

Diff Pair : W_{diff}	$60\mu m$
Current mirror load : W_{load}	$60.6\mu m$
Diff Pair Tail: W_{tail}	$76.4\mu m$
Common source stage : $W_{P,out}$	$1330\mu m$
Common source stage : $W_{N,out}$	$700\mu m$
Bias Circuit,NMOS : $W_{N,bias}$	$76.4\mu m$
Bias Circuit,PMOS : $W_{N,bias}$	$200\mu m$
Compensation Capacitor : C_c	$5pF$
Common Gate Transistor : W_{CG}	$225\mu m$

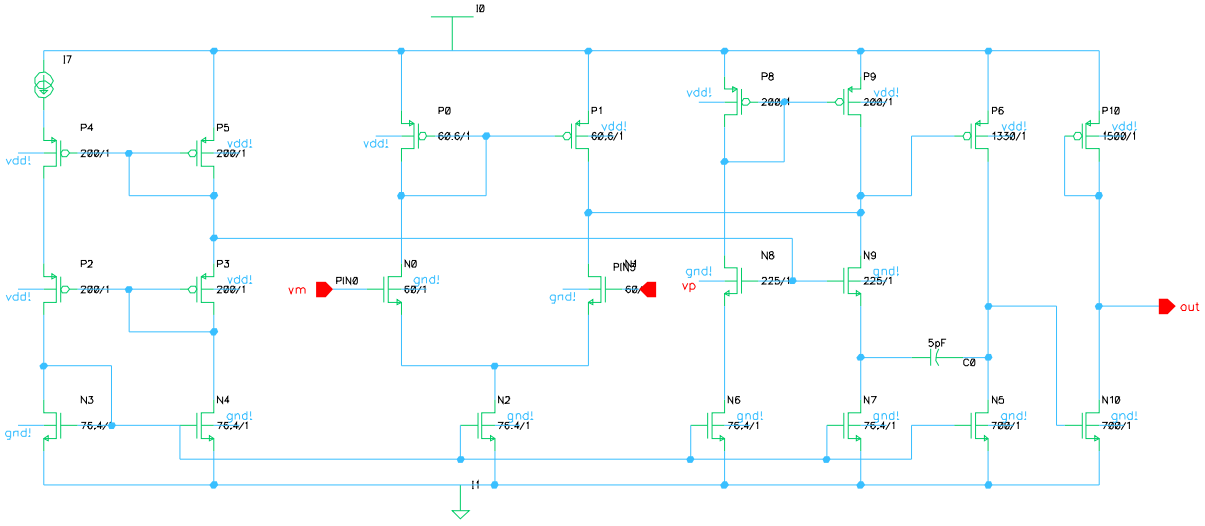


Fig. 5.12: Two-stage amplifier with common source output buffer with diode connected load.

Table 5.5: Simulated results for the two-stage amplifier with common source output buffer in TSMC 0.35μm technology.

A_v : DC Gain	$70.3dB$
f_u	$156.8MHz$
ϕ_M : Phase Margin	54.83°
ODR	$2.25V$
CMRR	$120.3dB$
Noise @ 1MHz	$517nV/\sqrt{Hz}$
Noise @ 5MHz	$105nV/\sqrt{Hz}$
Noise @ 10MHz	$52nV/\sqrt{Hz}$

Table 5.6: Design parameters for two-stage amplifier with common source output buffer in TSMC 0.35μm technology : $Length = 1\mu m$.

Diff Pair : W_{diff}	$60\mu m$
Current mirror load : W_{load}	$60.6\mu m$
Diff Pair Tail: W_{tail}	$76.4\mu m$
Common source stage : $W_{P,out}$	$1330\mu m$
Common source stage : $W_{N,out}$	$700\mu m$
Bias Circuit,NMOS : $W_{N,bias}$	$76.4\mu m$
Bias Circuit,PMOS : $W_{N,bias}$	$200\mu m$
Compensation Capacitor : C_c	$5pF$
Common Gate Transistor : W_{CG}	$225\mu m$
Output Buffer PMOS : W_{Pbuf}	$1500\mu m$
Output Buffer NMOS : W_{Nbuf}	$700\mu m$

Table 5.7: Simulated results for the folded cascode amplifier in TSMC 0.35μm technology.

A_v : DC Gain	$61.28dB$
f_u	$118.6MHz$
ϕ_M : Phase Margin	61.25°
Power	$16.5mW$
ODR	$2.57V$
CMRR	$98.2dB$
Slew Rate	$97V/\mu s$
Noise @ 1MHz	$350nV/\sqrt{Hz}$
Noise @ 5MHz	$71nV/\sqrt{Hz}$
Noise @ 10MHz	$35nV/\sqrt{Hz}$

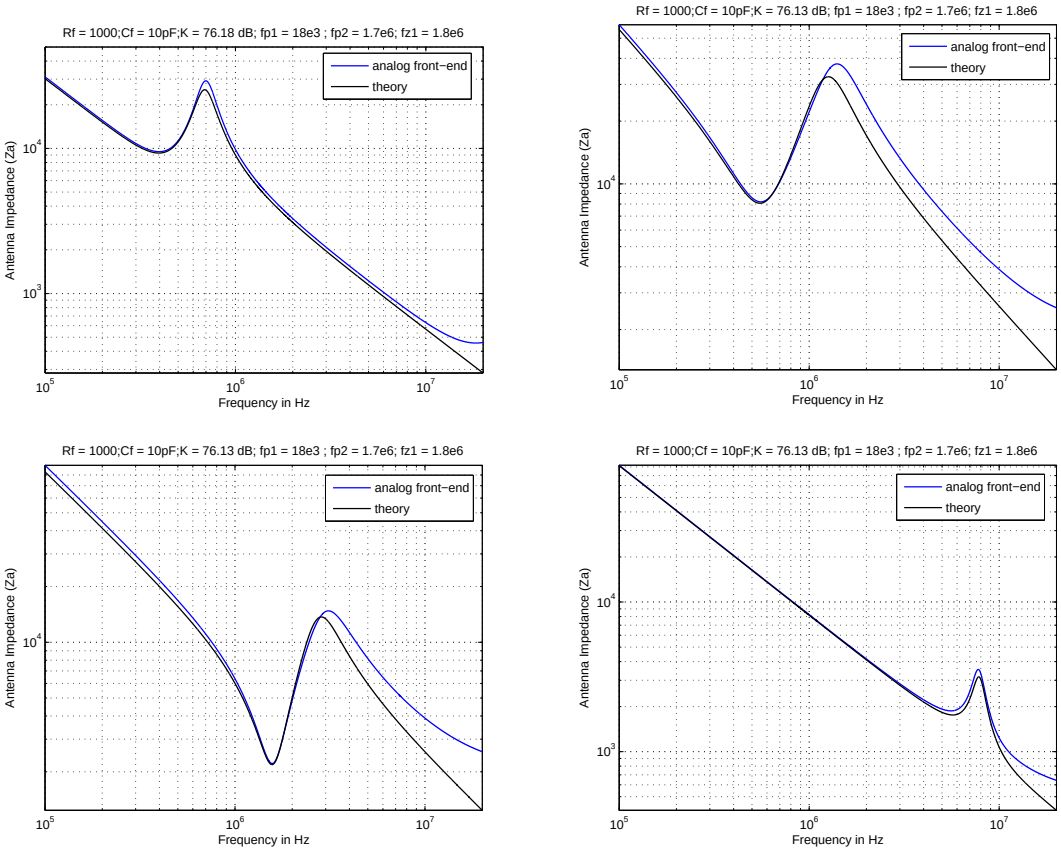


Fig. 5.13: Impedance curves reproduced by the two-stage amplifier verified against the theoritical curves after the analog front-end.

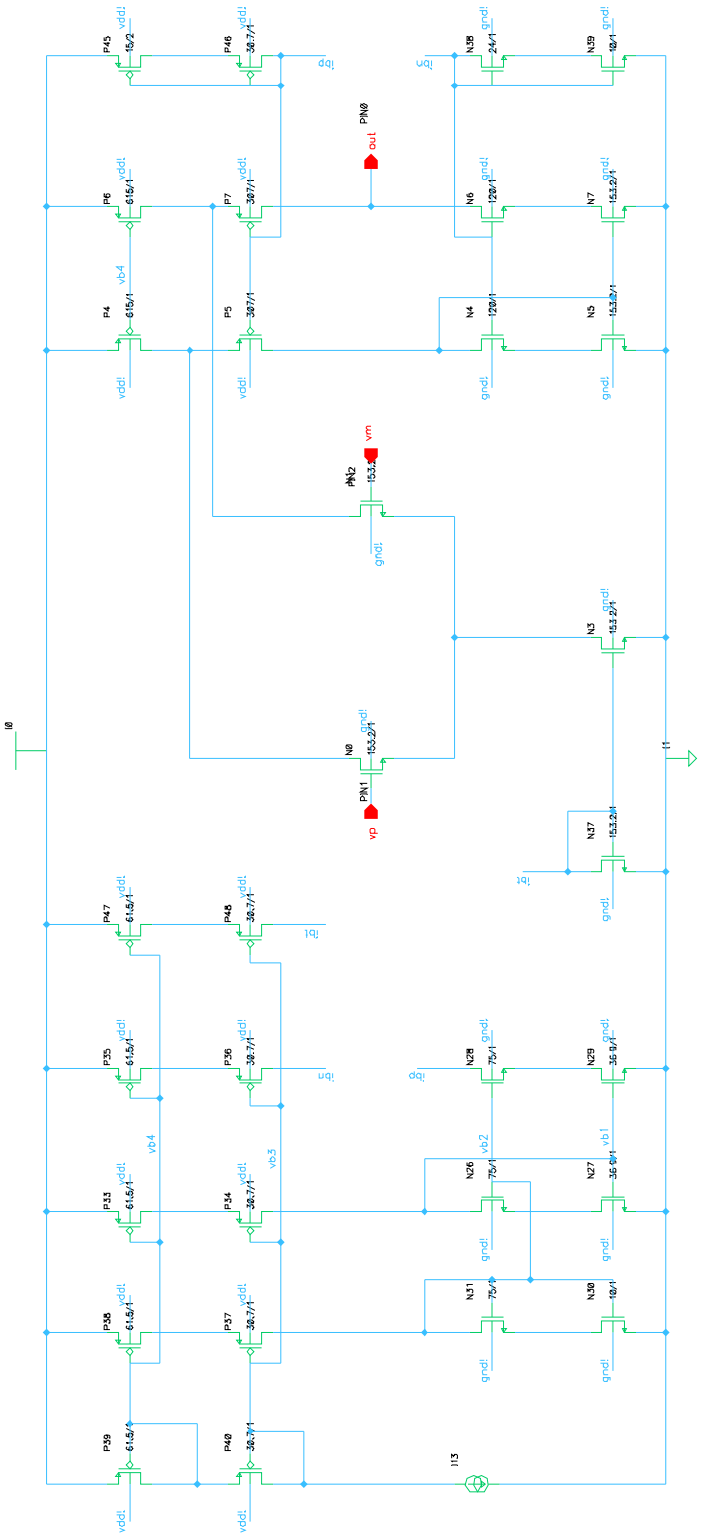


Fig. 5.14: Single-ended folded cascode amplifer with bias circuitry.

Table 5.8: Design parameters of the folded-cascode amplifier in TSMC $0.35\mu m$ technology : $Length = 1\mu m$.

Diff Pair : W_{diff}	$140\mu m$
Transistor supplying current to cascode load: $W_{curr,cas}$	$815\mu m$
Diff Pair Tail: W_{tail}	$153.2\mu m$
Cascode PMOS load : $W_{P,cas,out}$	$461.5\mu m$
Cascode NMOS load : $W_{N,cas,out}$	$180\mu m$
Cascode NMOS load : $W_{N,cas}$	$244\mu m$
Votage Bias, NMOS : $W_{N,bias}$	$24\mu m$
Voltage Bias PMOS : $W_{N,bias}$	$61.5\mu m$
Main Bias, NMOS : $W_{N,bias,up}$	$75\mu m$
Main Bias, NMOS : $W_{N,bias,down}$	$30.6\mu m$
Main Bias, PMOS : $W_{N,bias,up}$	$61.5\mu m$
Main Bias, PMOS : $W_{N,bias,down}$	$46.2\mu m$

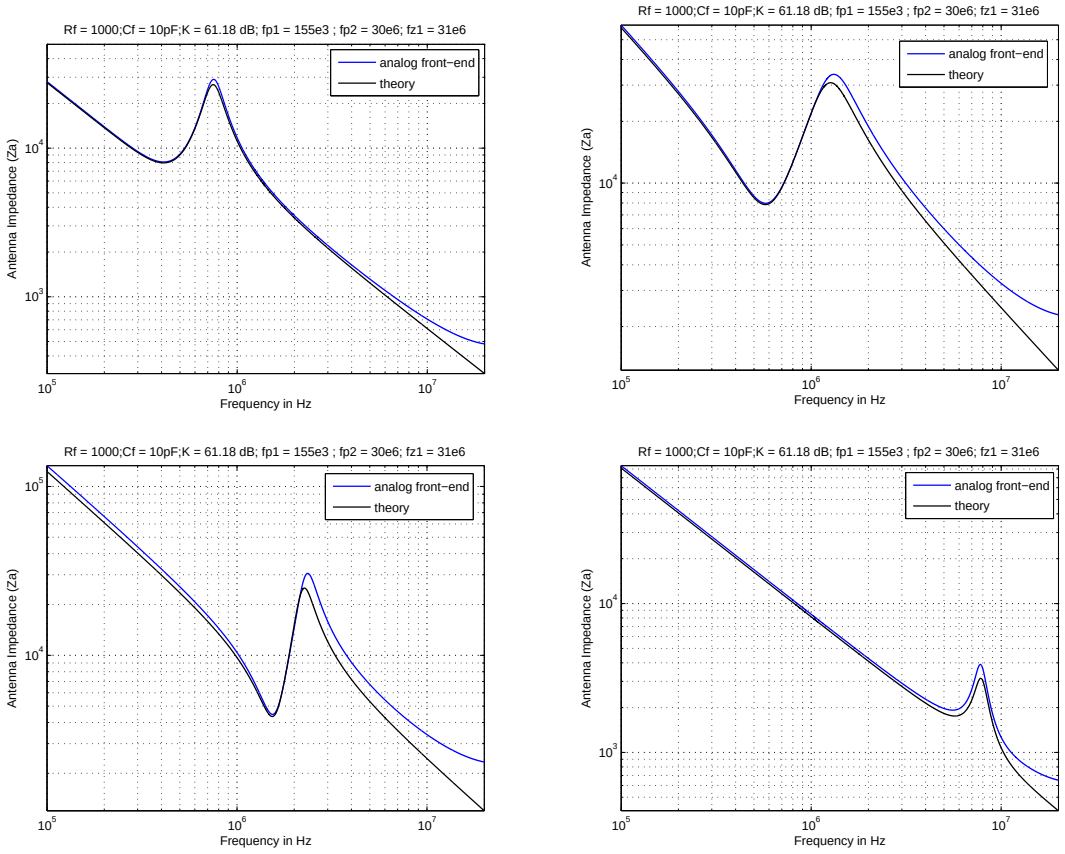


Fig. 5.15: Impedance curves reproduced by the folded cascode amplifier verified against the theoritical curves after the analog front-end.

Chapter 6

Summary and Future Work

6.1 Summary

The work in the thesis mainly focusses on the analog front-end design of the PIP using the g_m/I_D design technique for a pulse-based excitation. Some of the contributions from this work are listed below.

- A study of the wideband pulse excitation to the PIP instrument for the impedance probe measurement is explored by studying the various available pulse sources.
- The analog front-end amplifier is analyzed by deriving the transfer function in closed-loop and the behavior of such a configuration is studied. A Simulink model is created to model the amplifier for a complex s-domain antenna and feedback elements and the entire flow of PIP electronics on a system level is verified.
- The extensive simulations help us in arriving at the amplifier specifications. The designed transistor-level amplifier needs to satisfy these specifications.
- The short channel design technique using the g_m/I_D method for transistor-level analog design is introduced with design illustrations.
- A structured design approach for designing complex analog structures by breaking it down into its constituent elements and design of each element using the g_m/I_D method is implemented for different OTA configurations.
- A two-stage amplifier with various frequency compensation techniques like the Miller capacitor, nulling resistor, and current buffer using the common gate configuration is designed to achieve high-bandwidth specifications. Also, a simple output buffer is

implemented for the two-stage with current buffer configuration such that it can drive resistive and capacitive loads.

- Finally, a folded cascode OTA is also implemented using the g_m/I_D technique which can be a possible configuration to implement the on-chip amplifiers in the data converters.

6.2 Future Work

The g_m/I_D technique can be extended in the design of the amplifiers on the proposed on-chip implementation. A procedure to implement the nulling resistor using a device operating in the linear region in the g_m/I_D method needs to be explored. Pulse generation circuits to generate a wideband monocycle pulse needs to be explored and implemented in cadence. The effects of slewing of the pulse input to the analog front-end amplifiers also need to be studied. A bias circuitry, independent of temperature variations and other elements needs, to be designed. After the complete analog and mixed-signal components of the PIP have been designed the layout of the entire chip needs to be done and fabricated so that the PIP can be tested in an actual environment.

References

[1] W. Sanderson, "The history and dynamics of the plasma impedance probe," Master's thesis, Utah State University, Logan, UT, 2007.

[2] C. T. Steigies, D. Block, M. Hirt, A. Piel, and H. Thiemann, "Electron density measurements with impedance and langmuir probes in the deos campaign," *Advances in Space Research*, vol. 25, no. 1, pp. 109–112, 2000.

[3] K. G. Balmain, "The Impedance of a Short Dipole Antenna in a Magnetoplasma," *IEEE Transactions on Antennas and Propagation*, vol. 12, no. 5, pp. 605–617, Sept. 1964.

[4] W. Pfister, "Survey of RF impedance probes," Direct Aeronic Measurements in Lower Ionosphere, Aeronomy Report 1. University of Illinois, Urbana, IL, Dec. 1963.

[5] S. Patra, "Electron density and electron neutral collision frequency in the ionosphere using plasma impedance probe measurements on sounding rockets," Master's thesis, Utah State University, Logan, UT, 2009.

[6] A. Hummel, "The plasma impedance probe: A quadrature sampling technique," Master's thesis, Utah State University, Logan, UT, 2006.

[7] M. Jayaram, M. E. Hamoui, S. Patra, C. Winstead and E. Spencer, "Fully-integrated electronic system for a plasma impedance probe," *22nd Annual American Institute of Aeronautics and Astronautics/Utah State University Conference on Small Satellites*, vol. SSC08-VI-2, 2008.

[8] A. Taflove and S. Hagness, *Computational Electrodynamics: The Finite-Difference Time-Domain Method*. Norwood, MA: Artech House, 2005.

[9] M. Hamoui, "A pipeline analog-to-digital converter for a plasma impedance probe," Master's thesis, Utah State University, Logan, UT, 2009.

[10] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw Hill, 2005.

[11] J. Baker, *CMOS Design, Layout and Simulation*. New York: Wiley-IEEE Press, 2005.

[12] P. Allen and D. Holberg, *CMOS Analog Circuit Design*. UK: Oxford University Press, 2002.

[13] P. Gray, S. Lewis, P. Hurst, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley-IEEE Press, 2001.

[14] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley-IEEE Press, 1997.

[15] J. Mahattanakul and J. Chutichatuporn, "Design procedure for two-stage cmos opamp with flexible noise-power balancing scheme," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 8, pp. 1508 – 1514, Aug. 2005.

[16] J. Mahattanakul, "Design procedure for two-stage cmos operational amplifiers employing current buffer," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 11, pp. 766 – 770, Nov. 2005.

[17] D. Stefanovic and M. Kayal, *Structured Analog CMOS Design*. Dordrecht, Netherlands: Springer, 2008.

[18] P. Jespers, *The g_m/I_D Methodology, a sizing tool for low-voltage analog CMOS Circuits*. Boston, MA: Springer, 2009.

[19] B. Murman, *Analog Integrated Circuit Design*, Stanford University, Autumn 2007/2008.

[20] B. Boser, *Analog Circuit Design with Submicron Transistors*, Class Notes, University of California, Berkeley, 2004.

[21] F. Cortes and S. Bampi, "Anaysis and Design of Amplifiers and Comparators in CMOS $0.35\mu m$ Technology," *Microelectronics Reliability*, vol. 44, no. 4, Sept. 2004.

[22] H. Dammak, S. Bensalem, and M. Loulou, "Design of Folded Cascode OTA in Different Regions of Operation Through g_m/I_D Methodology," *World Academy of Science, Engineering and Technology*, 2008.