MODELING POWER DISTRIBUTION ARCHITECTURES AND MAINTAINING CONSTANT POWER WITH MISALIGNMENT IN DYNAMIC WIRELESS CHARGING SYSTEMS FOR ELECTRIC VEHICLES

by

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ABSTRACT

Modeling Power Distribution Architectures and Maintaining Constant Power with Misalignment in Dynamic Wireless Charging Systems for Electric Vehicles

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Wireless inductive power transfer (IPT) is widely used for applications ranging from phone charging and implantable medical devices to electric vehicle charging. Roadway electrification with in-motion wireless charging of Electric Vehicles (EVs), one of the applications of IPT, represents a promising solution to support the widespread adoption of EVs with reduced battery size and cost. However, there are numerous challenges involved with Dynamic Wireless Power Transfer (DWPT) systems, including associated infrastructure and misalignment tolerances. This dissertation addresses approaches to solving problems in practical high-power in-motion wireless charging systems.

First, it provides a comparative analysis of DC current- and voltage-distribution architectures for large-scale DWPT systems. It also provides mathematical loss models to evaluate power distribution system efficiency as a function of traffic volumes and corresponding EV loads on the roadway. A case study for a 1-mile wireless charging roadway at 1 MW has also been presented in this thesis. Second, the power regulation with misalignment using a soft switching DC-DC converter and system-level controls for one of the most commonly used topologies, double-sided LCC tuning, is analyzed and experimentally verified at 50 kW. Soft switching of the DC-DC converter is optimized and improved, and,

compared with conventional soft-switching approaches, offers significant reductions in losses, achieving peak efficiency of 99% at 50 kW, which is also experimentally verified at 50 kW. Third, it proposes a parallel resonant series-series (PRSS) tuning, which is a novel design methodology for tuning IPT systems to maintain constant power across a range of coupling coefficients. With PRSS tuning, the need for additional DC-DC stage and any controls is eliminated, thereby reducing the system cost and complexity. Zero-voltage switching (ZVS) for the primary switches is also analyzed for this tuning to maintain high efficiencies of the IPT system in the entire range of nearly constant power regions.

(271 pages)

PUBLIC ABSTRACT

Modeling Power Distribution Architectures and Maintaining Constant Power with Misalignment in Dynamic Wireless Charging Systems for Electric Vehicles

Mayank Chawla

With increasing demand for wireless power transfer systems from phone charging and medical devices, in-motion wireless charging of electric vehicles offers a unique advantage of charging the vehicle while in motion on an electrified roadway. Compared to the stationary or wired charging, electric vehicle users can significantly save time and cost with a reduction in the battery size. However, with large-scale infrastructure required for a wireless charging roadway and the driver's ability to align with the electrified roadway, come significant challenges for the practical implementation of in-motion wireless charging systems. This dissertation aims to solve some of the problems associated with high-power in-motion wireless charging systems.

First, for the practical implementation of large-scale in-motion wireless charging systems, mathematical models and loss comparisons are provided for DC current- and voltage-distribution architectures for deciding the architecture to be efficiently utilized depending on traffic conditions. Second, to prevent the power loss and efficiency when the driver is not perfectly aligned with the wireless charging roadway, an efficient power converter and control scheme are designed to maintain constant power with misalignment up to a certain level. Third, to further reduce the system's complexity and cost for maintaining nearly constant power with misalignment, a novel design methodology called parallel resonant series-series (PRSS) tuning is proposed.

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ACRONYMS

IPT	Inductive Power Transfer
ZVS	Zero Voltage Switching
EV	Electric Vehicle
EVs	Electric Vehicles
HEVs	Hybrid Electric Vehicles
PHEVs	Plug-in Hybrid Electric Vehicles
BEVs	Battery Electric Vehicles
WPT	Wireless Power Transfer
DWPT	Dynamic Wireless Power Transfer
SS	Series-Series
SP	Series-Parallel
SiC	Silicon Carbide
PRSS	Parallel Resonant Series-Series
PCB	Printed Circuit Board
QSW	Quasi Square Wave
FPGA	Field Programmable Gate Arrays
MSB	Most Significant Bit
LSB	Least Significant Bit
B2C	Binary Two's Complement
EMI	Electromagnetic Interference
ZCS	Zero Current Switching
CO2	Carbon Dioxide
DC	Direct Current
AC	Alternating Current
A/D	Analog-to-Digital Converter
LCC	Inductor-Capacitor-Capacitor

DC-DC	Direct Current-Direct Current
AC-DC	Alternating Current-Direct Current
DC-AC	Direct Current-Alternating Current
PFC	Power Factor Correction
PID	Proportional–Integral–Derivative
PI	Proportional–Integral
PL	Power Loss
LD	Light-duty
HD	Heavy-duty
ZVS-QSW	Zero Voltage Switching-Quasi Square Wave
AWG	American Wire Gauge
GK	Gustav Klein
NHR	NH Research
PWM	Pulse Width Modulator
DPWM	Digital Pulse Width Modulator
nA/D	Number of bit for Analog-to-Digital Converter
DR	Dynamic Range
Q	Quantization
RMS	Root Mean Square
SAE	Society of Automotive Engineers
LCR	Inductance, Capacitance, and Resistance

CHAPTER 1

INTRODUCTION

Over the last few years, there has been a significant change in climate conditions, ranging from heatwaves, wildfires, floods, tropical storms, and hurricanes throughout the world [3]. The transportation sector is one of the major contributors to climate change. The transportation sector accounts for almost 30% of all energy consumption globally, and 37% of global CO2 emissions come from transport [4]. To reduce the dependency on fossil fuels for transportation, all forms of electric vehicles, including Hybrid vehicles(HEVs), Plug-in hybrid electric vehicles (PHEVs), and all-electric vehicles, also referred to as battery electric vehicles (BEVs), have emerged as a possible solution [5]. According to the global EV outlook 2024, nearly one in five cars sold in 2023 was electric [6]. The increasing demand for electric vehicles creates a need for developing a charging infrastructure to support the present demand for EVs [7]. There have been a lot of developments recently in wired charging infrastructure, which includes Level 1 charging, Level 2 charging, and DC Fast charging. However, range anxiety in electric vehicles, having a large power distribution infrastructure, and using heavy charging cables for EV charging are some of the major challenges that need to be solved.

1.1 Wireless Charging Systems for Electric Vehicles

Wireless inductive power transfer (IPT) systems have numerous industry applications today, which include charging portable devices, electric vehicle charging, biomedical implants, and various other applications. There are several companies working on IPT systems, such as Apple, WiTricity, Wave IPT, Qualcomm, and many other companies that work on different IPT applications. One of the emerging applications of WPT is EV charging [8], [9], which can be of two types, stationary or dynamic. Dynamic charging is an attractive solution to combat the range anxiety of electric vehicles.

Wireless power transfer was demonstrated by Nikola Tesla in the twentieth century. It can be of two types: non-radiative or near-field wireless power transfer that uses inductive or capacitive coupling to transfer power over short distances, and radiative wireless power transfer that uses microwaves or lasers to transfer power wirelessly over long distances. Developments and recent progress in near field inductive wireless power transfer have been summarized in [10], [11]. There have been some developments in capacitive wireless power transfer in recent years. The maximum power level reported is up to 44.3 kW [12] [13], [14]. However, due to high power transfer capabilities, reliability, and thermal stability of IPT systems that have been demonstrated in the recent literature, they are generally preferred over capacitive systems for EV charging applications.

This proposal presents some challenges associated with practical dynamic wireless charging systems and new methods to overcome these challenges for the large-scale implementation of dynamic wireless charging systems.

1.2 Research Objectives

The objectives of this research are as follows:

(i) Modeling and analysis of power distribution architectures for large-scale in-motion wireless charging infrastructures to evaluate the performance of different power distribution architectures, considering the complexity in system wiring, voltage drop along the cables, and resistive losses from cables and connectors.

(ii) Designing a soft-switched DC-DC converter and system-level controls for power regulation on the receiver side of dynamic wireless charging systems for one of the most commonly used topologies, such as double-sided LCC tuning, so that constant power can be maintained over a range of misalignment. For double-sided LCC tuning, the power can also be regulated to a lower power level when the battery is close to being fully charged.

(iii) Designing a novel tuning method for IPT systems to deliver nearly constant power from primary to secondary for a range of coupling coefficients k without any external controls and a DC-DC converter required. The design of the tuning method is based on k between the primary and secondary coils and can be used for any type of coil. Moreover, the range

of coupling coefficient over which nearly constant power is desired can be selected by the designer for comparison with commonly used IPT tuning methods.

1.3 Dissertation Organization

- Chapter 2 provides an overview of large-scale dynamic wireless power transfer systems, misalignment challenges in IPT systems, soft switching of DC-DC converters, and synchronization and control techniques for dynamic wireless charging systems.

- Chapter 3 provides mathematical models for large-scale DC voltage and DC current distribution architectures and efficiency curves as the number of primary pads is activated from 1 to 20 for a 1-mile, 1 MW section of the wireless charging roadway.

- Chapter 4 provides a detailed design methodology for a soft-switched ZVS-QSW DC-DC converter for WPT systems. Comparison of proposed soft switching with traditional soft switching with internal capacitance of the module and hard switching DC-DC converter is also provided, achieving peak efficiency of 99% with proposed soft switching. EMI comparisons of the proposed soft switching, traditional soft switching technique, and hard switching case are also provided in this chapter. Experimental results at 50 kW, 40 kW, 30 kW, and 20 kW are provided in this chapter for the DC-DC converter.

- Chapter 5 provides system-level controls design for power regulation of WPT systems using phasor modeling and discrete time modeling techniques. System-level stability is also determined in this chapter for designing the control systems. Experimental Results for 50 kW and 8 kW for the full WPT system with a DC-DC converter are provided in this chapter.

- Chapter 6 proposes a single-stage architecture to achieve nearly constant power without any external controls and the DC-DC converter. A novel tuning methodology, Parallel Resonant Series-Series (PRSS) tuning, is proposed in this chapter. Detailed design methodology for PRSS tuning is provided in this chapter. Simulation Results

for PRSS tuning at 10 KW and comparisons with conventional and most commonly used tuning topologies, series-series and double-sided LCC tuning topologies have also been provided in this chapter. Hardware Setup for future testing at 10 kW is also provided in this chapter.

- Chapter 7 provides the conclusions and future work for this dissertation.

CHAPTER 2
LITERATURE REVIEW: DYNAMIC WIRELESS CHARGING FOR ELECTRIC VEHICLES

While the development of electrified transportation systems utilizing Electric Vehicles (EVs) is gaining close attention for the benefits of improving air quality, reducing carbon footprint, noise levels, and petroleum consumption [15], a few limiting factors that impact the widespread adoption of EVs still exist, including range anxiety, long refueling times, and a high purchase price [16]. The in-motion wireless charging technology that allows EVs to be charged while traveling represents a promising solution to facilitate the widespread adoption of EVs by overcoming the above-mentioned limitations and allowing reduced battery size and cost.

This chapter highlights some of the developments that have been done for dynamic wireless charging systems, common architectures that have been suggested till now for implementing large-scale dynamic wireless charging systems, misalignment problems in the current dynamic wireless charging systems, and control methods currently being used for these systems to handle misalignment tolerances for achieving constant power.

2.1 Large Scale Dynamic Wireless Charging Systems for Electric Vehicles and their architectures

A conceptual illustration of the in-motion wireless charging technology, which is also referred to as dynamic wireless power transfer (DWPT), for EVs is shown in Fig. 2.1. As illustrated in Fig. 2.1, the system consists of two main components: (i) primary pads and the associated power electronics, which are integrated with the roadway, (ii) secondary pad(s) and the necessary power electronics, which are mounted on the vehicle [17]. In order to achieve a broader impact on EV adoption and maximize the benefits introduced by in-motion wireless charging technology, the development and deployment of large-scale

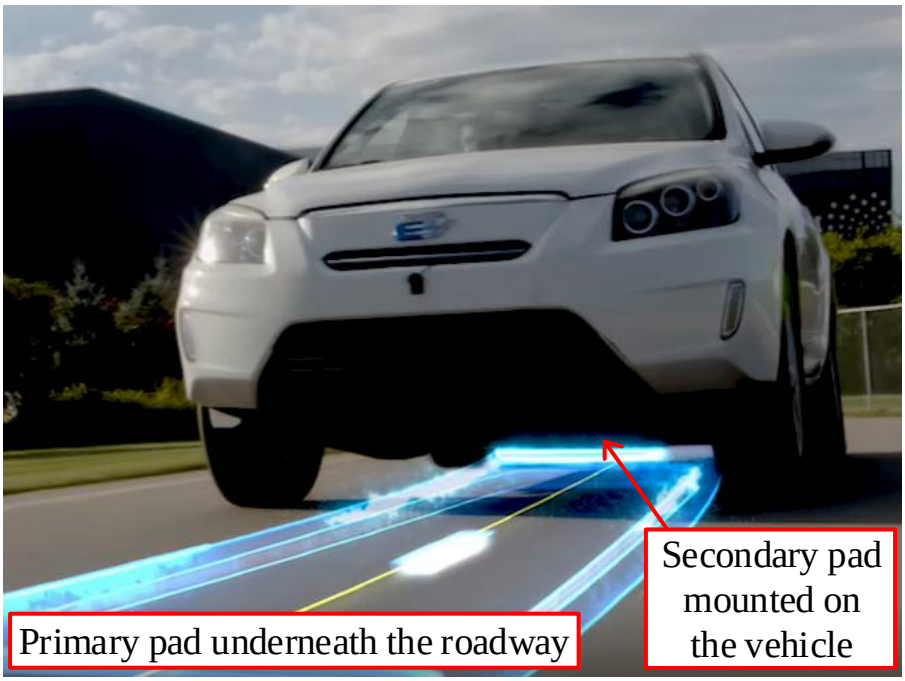


Fig. 2.1: System concept for the integration of DWPT into an electrified transportation system.

infrastructures are required. Future large-scale in-motion wireless charging infrastructures will include thousands of primary pads covering tens of miles of roadway and providing services to a wide range of EV classes from light-duty (LD) passenger vehicles to heavy-duty (HD) trucks, with grid connections in the multi-megawatt to tens or even hundreds of megawatt range. To achieve that, it is worth noting that significant technical gaps and design challenges exist between small-scale systems and large-scale infrastructures. The critical and unique challenges associated with large-scale in-motion wireless charging infrastructures have not been studied in the literature yet.

Some of the recent developments in track-based dynamic wireless charging systems include the designs from [18], [19], and [20] where a single track serves as the primary and could supply power to multiple secondary circuits that are coupled to the primary track. These primary tracks could have large self-inductance, resulting in large voltage across the primary track and high losses at high frequencies due to the long length of the primary track. Therefore, these systems are not favorable for large-scale deployment

of wireless charging systems. The University of Auckland, New Zealand, has proposed a double-coupled system [21] where an intermediary coupler circuit could be added between the power supply primary track and secondary circuit. The intermediary coupler circuit could operate at high frequencies and reduce losses on the primary track, which could operate at a lower frequency, thus improving the efficiency of the system. A laboratory-based prototype was demonstrated for [21]. However, this scheme increases the cost and complexity of having an additional intermediary coupler circuit for large-scale dynamic wireless charging systems.

Dynamic wireless charging systems where individual primary pads that have a size close to the size of the secondary pads have been proposed and developed in [22], [23], [24] [25], [26]. Each primary pad could be turned on separately when the vehicle is passing, resulting in more efficient utilization of the system. These systems may have different power distribution architectures to distribute electric power to each primary pad.

One of the common architectures that could be used for individual primary pads is an AC power distribution architecture presented in Fig. 2.2(a), where a grid-tied AC-DC converter and a high-frequency DC-AC inverter are typically required for energizing each individual primary pad. The other kind of architecture that could be used for these types of systems would be centralized architecture, where a single high-power AC-DC converter unit is used for grid integration, as shown in Fig. 2.2(b). In Fig. 2.2(b), the grid-tied AC-DC converter provides a constant DC voltage source, which is then used to distribute power to individual primary pads through a high-frequency DC-AC converter. Recently, a new centralized architecture has been proposed in [27], [28] by the Utah State University power electronics group, where a DC current source is used for power distribution after the grid-tied DC-AC converter, as shown in Fig. 2.2(c) to power individual primary pads through a high-frequency DC-AC converter.

Dynamic wireless charging systems, where individual primary pads are more favorable for large-scale systems, would require miles of roadway to be electrified to mitigate the problem of range anxiety of electric vehicles. However, there is no significant literature

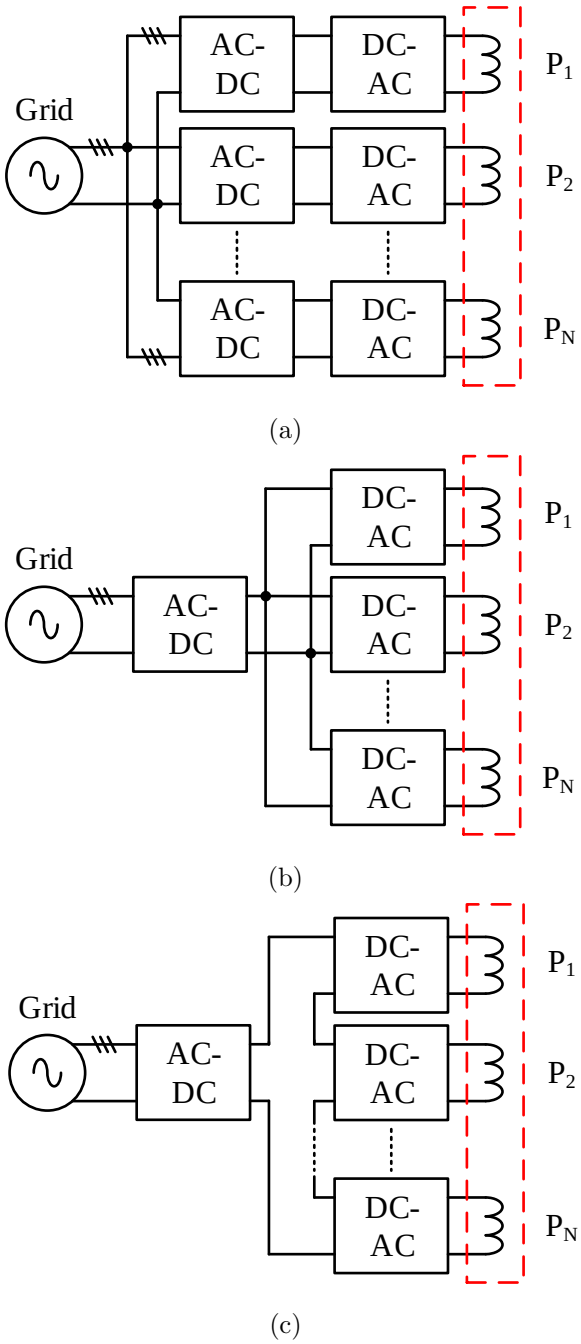


Fig. 2.2: Different power distribution architectures to energize the primary pads: (a) ac distribution, (b) dc voltage distribution, (c) dc current distribution.

for the selection of the type of distribution architecture for large-scale in-motion wireless charging systems, considering the variation in traffic volumes, EV loads on the roadway, complexity in system wiring, and losses across the cables and connectors. There is scope for mathematical models and comparison of the power distribution architectures that could provide insights to the researchers and engineers for implementing large-scale dynamic wireless charging systems.

2.2 Misalignment Challenge in Dynamic Wireless Charging Systems

There have been significant developments in dynamic wireless charging systems for individual coil-based systems [29], [30]. The most common compensation topologies for dynamic wireless charging systems include series-series compensation [31] and double-sided LCC compensation [32]. However, one of the challenges of misalignment between the primary coil and secondary coil still remains significant in dynamic wireless charging systems due to the difficulties in communication between the primary and secondary sides, where the secondary side or vehicle is generally moving at very high speeds. Misalignment between the primary and secondary coils causes a decrease in coupling between the primary and secondary coils, which often leads to a drop in power transferred or an increase in power transferred to the secondary [33] for the commonly used compensation topologies. However, it is desirable to have a relatively constant output power regardless of the misalignment. Therefore, to compensate for the misalignment and maintain constant power, system designers often use complex coil structures and complicated controls on the secondary side, which generally require synchronization techniques and extra DC-DC converters with standard compensation topologies.

Coil design techniques have been explored in [34], [35] to reduce the effects of misalignment on the coupling coefficient, which increases the complexity of the coil design for IPT systems. Synchronization techniques have been developed in [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48] to detect the phase of the primary circuit using active rectifiers which can then be used to regulate power. An active impedance compression network approach has been developed in [49] to achieve constant power delivered to

the secondary side, which is based on controlling a semi-active rectifier. However, achieving both synchronization and power regulation on the active or semi-active rectifier complicates the secondary side controls, which require additional controllers and sophisticated control algorithms, which not only increase the cost of the secondary side electronics but also make it difficult to achieve soft switching for the constant power regulation range with misalignment in the primary and secondary coils. Additional DC-DC converters on the secondary side have been used in [50], [51], [52], [53], [54] to maintain constant power with misalignment between the primary and secondary coils. The extra DC-DC converters can provide good regulation of output power with additional weight on the vehicle side, and increase the cost of the wireless charging system.

The above-mentioned techniques create a need to have a compensation topology for the dynamic wireless charging system, which can maintain constant power for a certain range of misalignment without any complicated controls, complex coil structures, and additional electronics on the vehicle or the primary side. A series hybrid topology to improve the misalignment tolerance of Inductive Power Transfer (IPT) systems is proposed in [55], which can maintain constant power for a certain range of misalignment without any controls or additional electronics. This topology works only for a polarized magnetic coupler, such as DD pads on both sides. A series-parallel-series topology for an IPT system has been proposed in [56]; the layout of the pad helped in reducing changes in self and mutual inductances, which further helped in uniform power flow as mentioned in [55]. Also, in the proposed topology of [56], ZVS analysis is not considered, which is an important factor for high-power IPT systems. Thus, there is scope for a compensation topology for a dynamic wireless charging system that can achieve a nearly constant power for a certain range of misalignment without any complicated controls or additional electronics, and is independent of the coil topology used for the system.

2.3 DC-DC Converters for Power Regulation of Dynamic Wireless Charging Systems

A complete wireless charging system with a DC-DC converter included is shown in

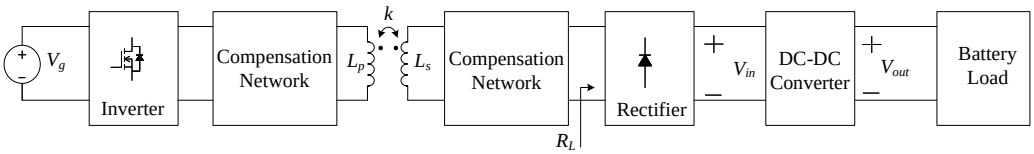


Fig. 2.3: Complete Wireless Charging system.

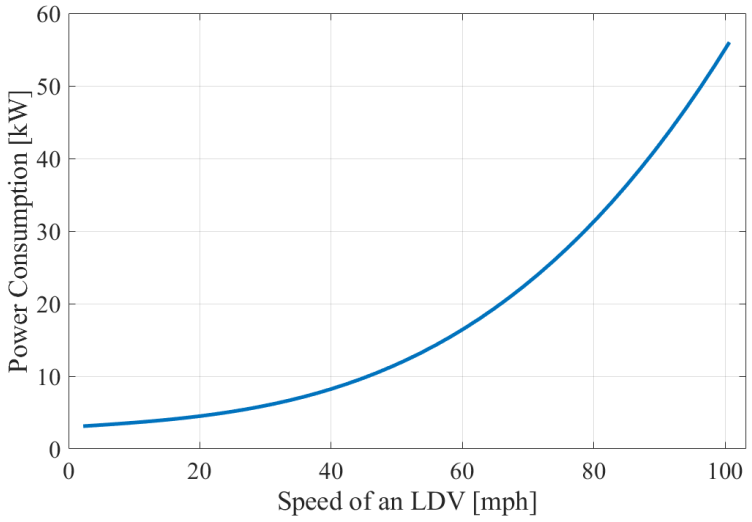


Fig. 2.4: Average power consumption of a light-duty vehicle at different constant speeds on a flat roadway.

Fig. 2.3. The power rating of each primary and secondary pad for an individual coil system in dynamic wireless charging systems depends on the charging required by the battery to maintain a constant speed on a flat roadway, as mentioned in [57], shown in Fig. 2.4. It can be seen from Fig. 2.4 that the preferable rating for power electronics for each primary and secondary pad would be between 10 kW and 60 kW for light-duty vehicles. The design considerations for the DC-DC converter on the receiver side of the dynamic wireless charging system are reviewed in terms of the power range given in Fig. 2.4. Since a wireless charging system can be considered to be a type of resonant converter, the concept of adding a DC-DC converter on the receiver side for power regulation comes from the literature of resonant converter design principles [58]. The power transferred to the secondary depends on the equivalent load resistance seen from the diode bridge rectifier circuit, as shown in Fig. 2.3. The equivalent load resistance is a function of the DC voltage at the output of the rectifier circuit, as mentioned in [58]. Thus, by changing the equivalent load resistance seen from the rectifier or the DC voltage at the output of the rectifier, power delivered to the secondary circuit or the battery can be controlled.

In [59], [60] dc-dc converters for wireless charging systems have been used to maximize efficiency of the systems. In [59], three types of dc-dc converters, buck, boost, and buck-boost, have been proposed for different applications depending on the load resistance seen from the rectifier that is required for a specific application. For the buck converter, the equivalent load resistance can be varied from a specific value up to ∞. For a boost type converter, the equivalent load resistance can be varied from zero up to a specific value. For the buck-boost converter, the equivalent load resistance can be varied from zero up to ∞. Since, for the application of dynamic wireless charging systems, the power has to be regulated from zero up to the maximum value as mentioned in the objective (iii) of chapter 1, a boost converter is preferred for this particular application. In [61], [62], a buck converter at the receiver side has been used for a dynamic wireless charging application to maintain constant power with misalignment. However, low-power lab-based prototypes of 2 kW to 3 kW have been developed in both these systems. Moreover, soft switching analysis

or loss analysis of DC-DC converters has not been considered in either of these systems. According to the Fig. 2.4, for high power dynamic wireless charging systems up to 50 kW power level, there is a need for loss analysis and soft switching analysis so that a DC-DC converter can be added to the wireless charging systems without having large losses in the DC-DC converter.

Zero-voltage switching quasi-square wave (ZVS-QSW) operation of pulsewidth-modulated dc-dc converters has been introduced in [63] and [64], which can achieve zero voltage switching during the turn-on transitions of the SiC switch due to the high ripple and negative current of the inductor as explained in [65] and [66]. In [66], silicon carbide-based ZVS-QSW boost converters have been designed with an efficiency optimization strategy by adjusting the switching frequency and dead times for power levels between 2 kW and 8 kW. In [67], a ZVS-QSW boost converter with a zero voltage detection circuit and tuning the switching frequency, which results in a 90-degree valley resonant transition, is designed to reduce the peak currents and losses in the circuit. The output capacitance of the switch is used to form the ZVS-QSW circuit. 5 kW hardware results are presented for this scheme. In [68], a ZVS control scheme to improve ZVS time margin for a MHz ZVS Gan totem-pole PFC rectifier for a 3 kW prototype is presented. In [69], a ZCS boost converter with peak efficiency of 97% for an 80 kW prototype is presented; there is still scope for improving the efficiencies at high power with ZVS circuits. The turn-on losses of the half-bridge module can be drastically reduced using the above-mentioned approaches; however, for high power designs in the range of 10 kW to 50 kW, the turn-off losses become significantly large as explained in [70]. Therefore, there is scope for finding solutions to improve efficiencies for DC-DC converters for high-power designs using soft switching techniques. Also, the control of the DC-DC converter will depend on the soft switching topology used and the wireless power transfer compensation network, which requires further analysis.

In [71], controls for the IPT system using series-series compensation with a buck converter are shown. Input to the buck converter, that is, the IPT system, is assumed to be a current source. The impedance interaction of the buck converter and IPT system is not

analyzed for stability. An average small signal model is used for the buck converter for designing the controls. Experimental results with a 1 A amplitude of ac input for a static IPT system are provided. Proportional and PI compensators are used for the control of the buck converter. In [72], model predictive control for a DC-DC converter with double-sided LCC tuning is presented for a 2 kW DWPT system. The system-level stability and the interaction of the WPT system with the DC-DC converter are not presented. The comparison of model predictive control with PID control is presented; the comparisons with higher-order compensators are not provided, which can significantly improve the dynamic response. In [73], receiver side power control for a 200 kW DWPT system using a DC-DC converter is presented; however, system-level stability analysis is not provided, and a PI compensator is used to design control for the DC-DC converter. The response time and startup time are approximately 20 ms. Therefore, there is scope for improvement for designing controls with faster response time using advanced control techniques and higher-order compensators, and analyzing system-level stability for WPT systems for high-power DWPT systems.

CHAPTER 3

MATHEMATICAL MODELS FOR DISTRIBUTION ARCHITECTURES

The design of an in-motion wireless charging system requires (i) the rated power of each secondary pad and (ii) the number of electric vehicles that are being charged on the roadway at any instance.

The power rating of the secondary pad can be designed based on sustained charging of the EV battery, and at the same time, providing the vehicle tractive energy [15]. A light-duty passenger vehicle cruising on a flat roadway is used as a design example in this paper to calculate the average power consumption of an EV using

$$P(v) = \frac{C_r M_v g}{\eta_{tw}} v + \frac{C_d A_v \rho}{2\eta_{tw}} v^3 + P_{aux}. \tag{3.1}$$

The parameters used in (6.5) for the average power consumption calculation are mentioned in [74,75]. The resultant power consumption of a light-duty vehicle, while cruising, is given in Fig. 3.1. For the case study, the power level of each secondary pad is considered to be 50 kW based on the power consumption shown in Fig. 3.1, and an excess power required to maintain the sustained charging of the battery.

The expected number of EVs that could be on the DWPT roadway at any instance is determined by a historical data-based traffic prediction algorithm using hourly traffic counts collected from the Texas Department of Transportation for a highway system near Dallas, Texas. The case study considers 10% EV injection and a 1-mile roadway and is based on the sales projections of EVs for the year 2025 [76]. The forecasted hourly traffic flow represented by the number of EVs is presented in Fig. 3.2. As shown in Fig. 3.2, the maximum number of EVs estimated to be on the 1-mile in-motion wireless charging roadway is 20. Assuming one secondary pad per light-duty passenger vehicle, with the power rating of 50 kW per secondary pad, the total maximum power demand from this 1-mile roadway is 1 MW.

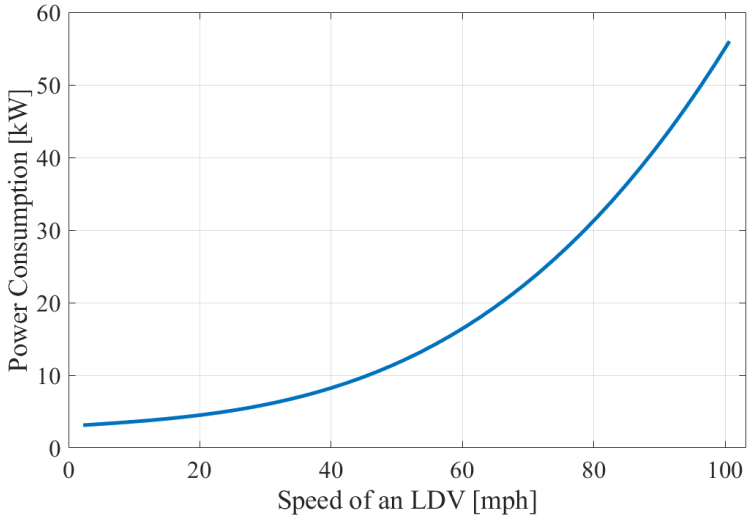


Fig. 3.1: Average power consumption of a light-duty vehicle at different constant speeds on a flat roadway.

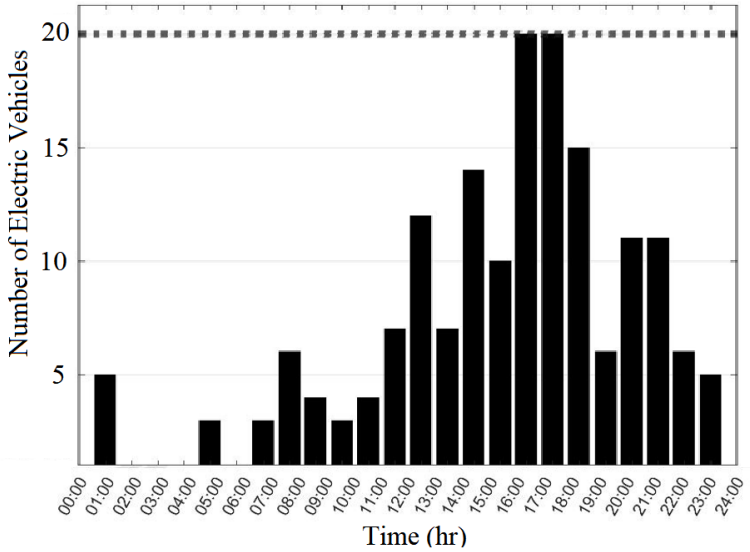


Fig. 3.2: Hourly EV traffic counts assuming 10% injection [1].

3.1 DC Voltage Distribution

For the mathematical loss analysis of the DC voltage distribution, a roadway of length L is considered, where the primary pads are spread out throughout the roadway, as shown in Fig. 3.3. The length of the main cable extending through one pad (L_{seg}) is equal to the length of the primary pad, which is denoted as L_{pad}. The length of the cable that connects the DC-AC inverter to the main cable is denoted as L_m. Moreover, the total number of

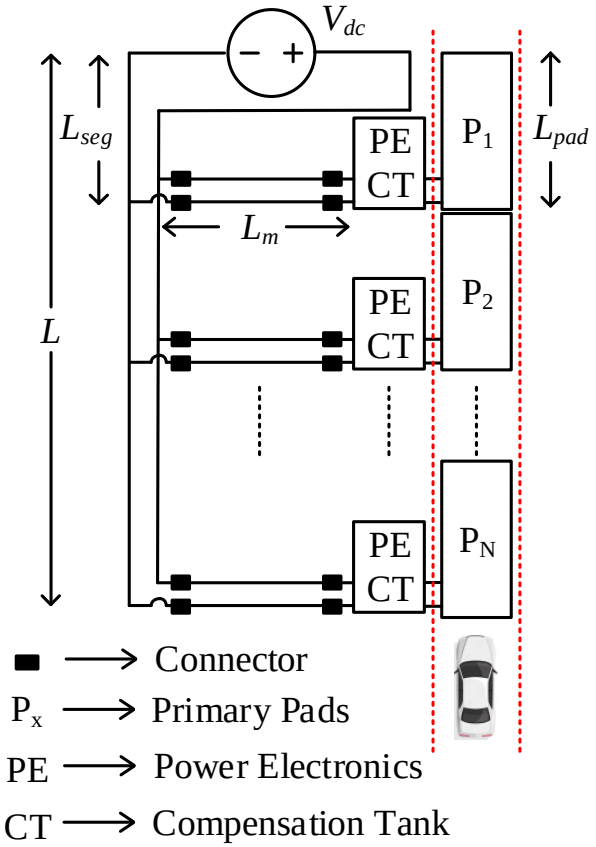


Fig. 3.3: DC voltage distribution architecture with primary pads connected in parallel.

pads (N) integrated with the roadway is given as L/L_{seg}. The power transmitted by each primary pad to the secondary pad mounted on the vehicle is denoted as P_{pad}. I_{seg} represents the current entering the DC-AC inverter of a single primary pad. The maximum current drawn by the main cable from the voltage source is I_{max}, which is directly proportional to I_{seg}, and is determined by the maximum power transfer capability of the roadway. The resistance of the L_{seg} portion of the main cable is denoted as R_{seg}. For the calculation of the resistance of this segment, the copper area of the cable is determined in terms of I_{max} and the maximum current density of the main cable. The resistance of the cable used to connect the DC-AC inverter to the main cable is calculated in a similar manner and is denoted as R_{mod}. In addition, the resistance of the connector that connects the main cable to the DC-AC inverter is denoted as $R_{connector}$.

Efficiency and power loss equations are derived for the voltage distribution architecture when the k number of primary pads are activated. The worst-case scenario is considered in which these k number of pads are present at the farther end of the roadway from the DC voltage source. Power loss in the distribution network shown in Fig. 3.3 consists of: (i) power loss in the main cable ($PL_{maincable}$), (ii) power loss in the cables that connect dc-ac inverter, which are of length L_m (PL_{mod}), (iii) power loss in the connectors ($PL_{connectors}$), and (iv) power loss in the wireless power transmission and the associated power electronics with it (PL_{ind}), which is calculated with the help of efficiency number (η_{ind}). Expressions for all these losses are given in (3.2)-(3.6).

$$PL_{maincable} = I_{seg}^2 R_{seg} + (2I_{seg})^2 R_{seg} + ...+ ((k-1)I_{seg})^2 R_{seg} + (kI_{seg})^2 R_{seg} \frac{(L-(k-1)L_{seg})}{L_{seg}} \quad (3.2)$$

The above equation can be simplified as

$$PL_{maincable} = I_{seg}^2 R_{seg} \frac{k(k-1)(2k-1)}{6} + (kI_{seg})^2 R_{seg} \frac{(L-(k-1)L_{seg})}{L_{seg}} \quad (3.3)$$

$$PL_{mod} = \ kI_{seg}^2 R_{mod} \quad (3.4)$$

$$PL_{connectors} = \ kI_{seg}^2 \times 4R_{connector} \quad (3.5)$$

The power at the input of the DC-AC inverter is considered as P_{dc}. The loss in the DC-AC inverter, compensation network, and wireless power transfer from the primary pad to the receiver pad are all combined into one component denoted as PL_{ind}, which is given by

$$PL_{ind} = \frac{(100-\eta_{ind})}{\eta_{ind}} \times P_{pad} \quad (3.6)$$

where η_{ind} is defined as P_{pad}/P_{dc}. Considering all power loss components, the overall efficiency of the system with k primary pads energized is given in (3.7), where $PL_{grid-tied}$ is the power loss of the grid-tied ac-dc converter and PL_{system} is the overall power loss of the distribution network which is given by $PL_{maincable} + PL_{mod} + PL_{connectors} + PL_{ind}$.

$$\eta(k) = \frac{kP_{Pad}}{kP_{Pad} + PL_{system} + PL_{grid-tied}} \times 100. \tag{3.7}$$

3.1.1 DC Current Distribution

For the mathematical loss analysis of the DC current distribution architecture, two roadways of combined length L are considered with series-connected primary pads integrated with the roadways, as shown in Fig. 3.4. Total N number of primary pads, each having a length of L_{pad}, is spread over these roadways of length L. Consequently, N is calculated as L/L_{pad} considering the primary pads are distributed densely. Also, the primary pads that are not active or energized are bypassed by a MOSFET that has an ON resistance of R_{ds}.

Power loss in this distribution architecture consists of four components: (i) power loss in the cables (PL_{cables}), (ii) power loss in the connectors ($PL_{connectors}$), (iii) power loss in the bypass MOSFETs ($PL_{MOSFETs}$), and (iv) power loss in the wireless power transmission and associated power electronics (PL_{ind}), calculated with the help of efficiency number (η_{ind}). Expressions for all these components are given by (3.8) - (3.11).

$$PL_{cables} = I_{dc}^2 R_{cables} \tag{3.8}$$

R_{cables} in (3.8), is given by $\rho_{cable}L/A_{cable}$, where ρ_{cable} is the resistivity of the cable and A_{cable} is the cross-section area of the cable.

$$PL_{connectors} = NI_{dc}^2 \times 2R_{connector} \tag{3.9}$$

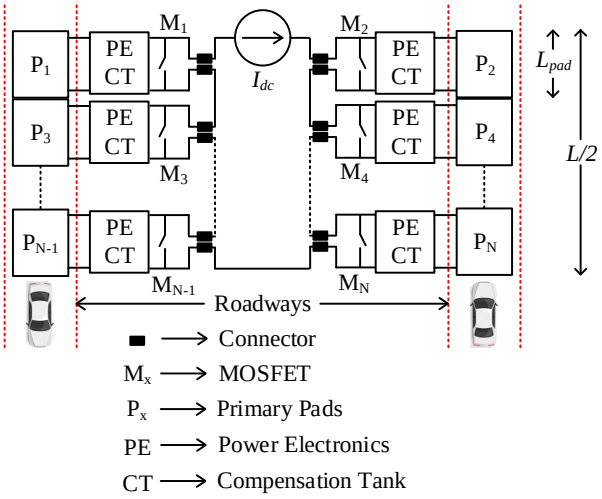


Fig. 3.4: DC current distribution architecture with primary pads connected in series.

Considering k primary pads are energized, the number of MOSFETs used to bypass the remaining primary pads would be $N - k$.

$$PL_{MOSFETs} = (N - k)I_{dc}^2 R_{ds} \tag{3.10}$$

PL_{ind} is calculated using the power transmitted by each primary pad, which is considered as P_{pad}.

$$PL_{ind} = \frac{(100 - \eta_{ind})}{\eta_{ind}} \times P_{pad} \tag{3.11}$$

Considering all the power loss components, overall efficiency of the system with k energized primary pads is given in (3.12), where $PL_{grid-tied}$ is the power loss of the grid-tied AC-DC converter and PL_{system} is the overall power loss of the distribution network which is given by $PL_{cables} + PL_{connectors} + PL_{MOSFETs} + PL_{ind}$.

$$\eta(k) = \frac{kP_{pad}}{kP_{pad} + PL_{system} + PL_{grid-tied}} \times 100. \tag{3.12}$$

3.2 Simulation Results and Discussion

3.2.1 Efficiency Curves and Results

This section provides simulation results for the centralized architecture scheme based on the mathematical model developed in Section III, which includes both DC voltage distribution and DC current distribution. Efficiency curves are plotted considering the electrified roadway has a maximum of 20 pads integrated with the roadway, with a power transfer capability of 1 MW. This is based on the analysis of the traffic data presented in Section II. Moreover, the length of the primary pad, denoted by L_{pad}, is constrained to 2 m.

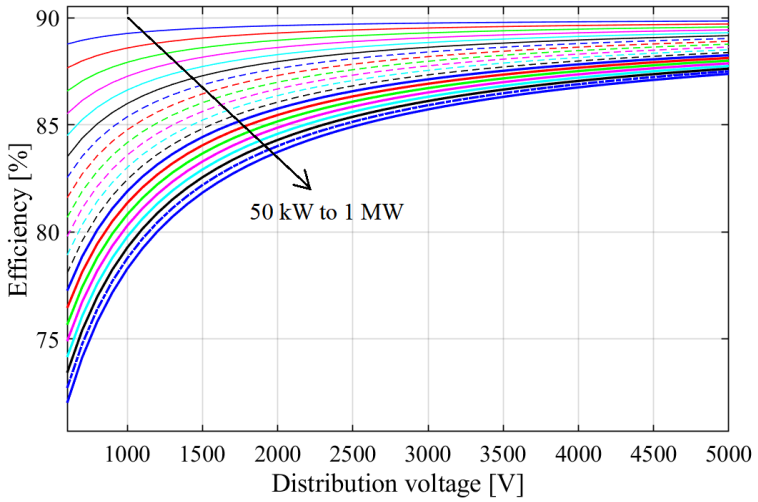


Fig. 3.5: Efficiency vs DC voltage levels for DC voltage distribution architecture. The number of energized primary pads varies from 1 to 20.

For the voltage distribution-based architecture, the maximum current I_{max} from the DC voltage source is calculated considering all 20 primary pads are energized at a time. On the other hand, for the current distribution architecture, a constant DC current is passed through the series-connected primary pads. The parameters used to calculate the efficiencies for both cases are tabulated in Table 3.1. For both analyses, the number of pads energized at a time, denoted by k, is varied from 1 to 20, which is based on the number of vehicles passing through the roadway. This corresponds to the change in the transferred power level from 50 kW to 1 MW. The efficiency curves for the different distribution voltages and currents for 1 mile of roadway are shown in Figs. 3.5 and 3.7, respectively. In addition to

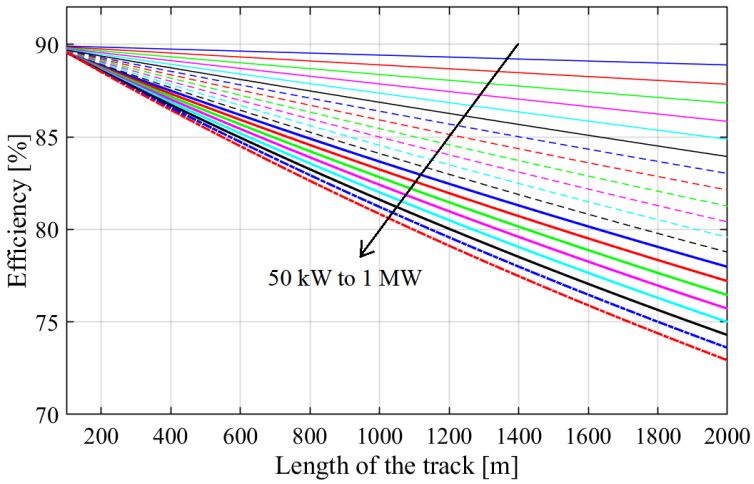


Fig. 3.6: Efficiency vs length of the roadway with 800 V distribution voltage. The number of energized primary pads varies from 1 to 20.

that, the efficiency curves for the different roadway lengths for DC voltage and DC current distribution architectures are shown in Figs. 3.6 and 3.8, respectively.

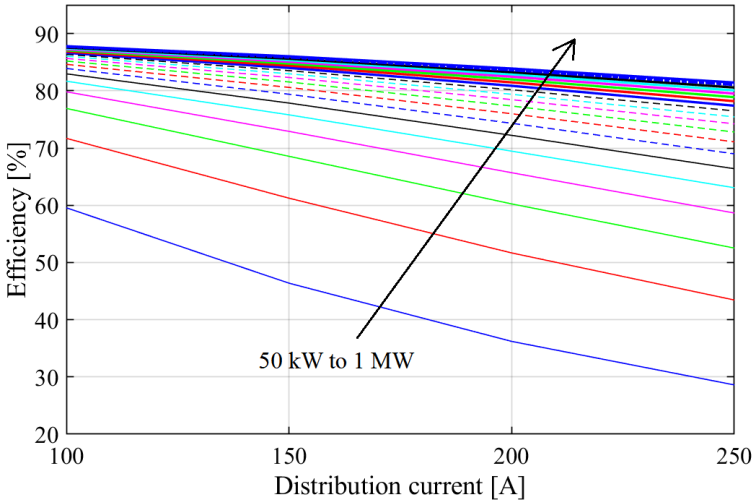


Fig. 3.7: Efficiency vs DC current levels for DC current distribution architecture. The number of energized primary pads varies from 1 to 20.

From the efficiency curves, it can be observed in the case of the voltage distribution architecture that efficiency declines as the power transfer level increases, mainly caused by the rise in cable losses. On the contrary, for the current distribution architecture,

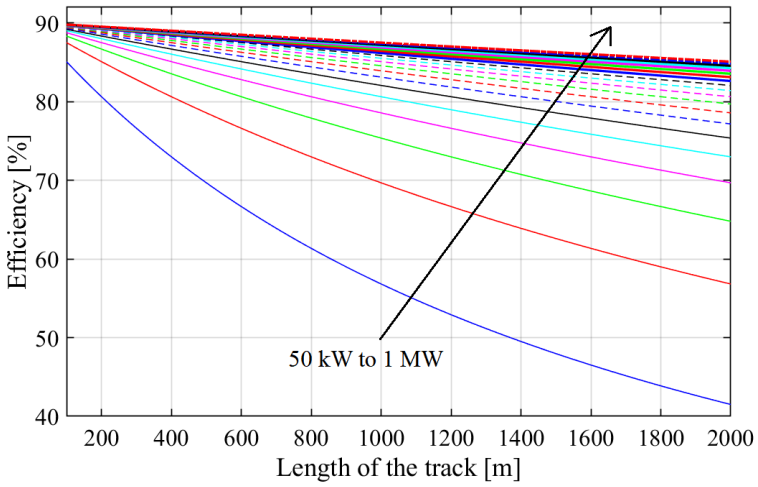


Fig. 3.8: Efficiency vs length of the roadway with 100 A of distribution current. The number of energized primary pads varies from 1 to 20.

Table 3.1: Parameters used in the simulations for Power Distribution Architectures.

Parameter	**Value**
$\eta_{grid-tied}$	97% [77]
P_{pad}	50 kW
L	1600 m
L_{seg}	2 m
L_m	1 m
$R_{connector}$	1 mΩ
R_{ds}	2 mΩ

an increase in efficiency can be observed with the increment in the number of energized primary pads because of the increment in the utilization of the current flowing through the series-connected primary pads. Moreover, in both architectures, the efficiency is higher for the shorter lengths of the roadway, as can be seen in the efficiency versus length of the roadway curves. Even though shorter lengths of the roadways seem advantageous in terms of efficiency, a larger number of grid-tied AC-DC converters will be required to electrify the roadway, which will increase the cost and complexity of the overall design.

3.2.2 Discussion

The proposed modeling and analysis count the number of secondary pads that are

being charged, which can be applied to various scenarios covering vehicle classes from LD to HD. For HD vehicles, it can be assumed that multiple secondary pads are mounted on the vehicle to receive a higher amount of power. Both the DC voltage and DC current distribution architectures can have renewable energy and energy storage integrated with the roadside AC-DC power converter to reduce the peak power drawn from the grid and the electricity cost. The DC current distribution architecture allows upgrading the roadside AC-DC power converter with higher power and voltage capability, up to the voltage rating of the system cables and connectors, as the power demand of the roadway increases. The design of +/- voltage output can be applied to the roadside AC-DC power converter in the DC current distribution architecture for achieving the high voltage due to the series connection of the primary pads. For example, +/- 5 kV can be used to achieve 10 kV.

Additional parameters could potentially be included in the proposed modeling and analysis to account for factors related to implementation and construction practices. For example, one parameter could be how distribution lines are integrated with the roadway. These types of implementation details could impact the cost and complexity, and thus impact the decision-making of power distribution architectures for large-scale in-motion wireless charging infrastructures.

3.3 Conclusion

This chapter provides guidelines and models to researchers and engineers for designing power distribution architectures for large-scale in-motion wireless charging infrastructures. A new DC current distribution architecture that has the potential to achieve efficient, reliable, and low-cost power distribution for large-scale infrastructures is analyzed in this chapter. This chapter also provides comments and discussions to further guide people on considering various trade-offs in power distribution architecture design and decision-making. In future work, the traffic prediction could be integrated further with the modeling and analysis to show the voltage/power demand on the roadside AC-DC power converter for over one day, peak efficiency at peak load in the day, and average efficiency over the day. More quantified parameters that reflect practical implementation and construction

factors could be included in the modeling and analysis for more informed decisions while implementing the large-scale in-motion wireless charging infrastructures.

CHAPTER 4

SiC-BASED ZERO VOLTAGE SWITCHING QUASI SQUARE WAVE DC-DC CONVERTER DESIGN AND ANALYSIS

4.1 System Overview

4.1.1 Background of double-sided LCC compensation

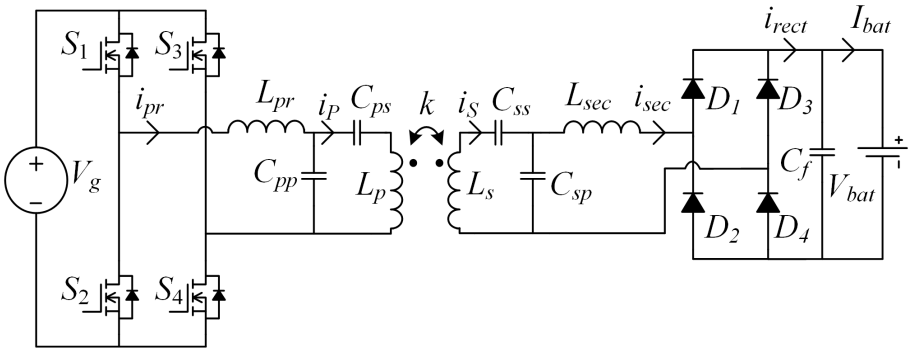


Fig. 4.1: Double-sided LCC compensation.

Fig. 4.1 shows the circuit for double-sided LCC compensation. L_p and L_s are the self-inductances of primary and secondary coils, respectively. C_{ps}, C_{pp}, and L_{pr} are the elements of the compensation network on the primary side. C_{ss}, C_{sp}, and L_{sec} are the elements of the compensation network on the secondary side. k is the coupling coefficient between the primary and secondary sides of the IPT system. M is the mutual inductance between the primary and secondary coil given in (6.1). On the primary side, L_{pr} is tuned to C_{pp} at operating frequency of the system w_s as given in (4.2), L_{pr} is also tuned to L_p and C_{ps} as given in (4.3). On the secondary side, L_{sec} is tuned to C_{sp} at operating frequency of the system ω_s as given in (4.4), L_{sec} is also tuned to L_s and C_{ss} as given in (4.5). When the circuit is tuned in this way of double-sided LCC tuning, the power transferred to the

secondary P_s given in (4.6), which is nearly equal to the output power P_{bat}, is given in (6.6). The R_L used in (4.6) is defined as the reflected load resistance of the passive rectifier, which is given in (6.19).

$$M = k\sqrt{L_p L_s} \tag{4.1}$$

$$\omega_s L_{pr} = \frac{1}{\omega_s C_{pp}} \tag{4.2}$$

$$\omega_s L_{pr} = \omega_s L_p - \frac{1}{\omega_s C_{ps}} \tag{4.3}$$

$$\omega_s L_{sec} = \frac{1}{\omega_s C_{sp}} \tag{4.4}$$

$$\omega_s L_{sec} = \omega_s L_s - \frac{1}{\omega_s C_{ss}} \tag{4.5}$$

$$P_s = \frac{\omega_s^2 M^2 i_{P_{rms}}^2 R_L}{\omega_s^2 L_{sec}^2} \tag{4.6}$$

$$P_{bat} = V_{bat} I_{bat} \tag{4.7}$$

$$R_L = \frac{8 V_{bat}^2}{\pi^2 P_{bat}} \tag{4.8}$$

The rms value of the open circuit voltage V_{OC} induced on the secondary coil is given in (4.9). The current i_{sec}, if the secondary is tuned as LCC tuning mentioned in (4.4) and (4.5), acts as a current source. The open circuit voltage V_{OC} induced on the secondary coil is represented as norton equivalent with $i_{sec_{rms}}$ given in (4.11). The $i_{sec_{rms}}$ can also be represented in terms of I_{bat}, which is also the average value of i_{rect} as given in (4.12). Since V_{OC} depends on M, ω and i_{Prms} and since i_{Prms} is a constant value as given in (4.10), it

can be observed from (4.11), that $i_{sec_{rms}}$ is a current source which has a constant value at certain value of k and $i_{P_{rms}}$ and the value of i_{SECrms} changes as k changes. Also, from equation (4.12), which shows the dependence of I_{bat} on $i_{sec_{rms}}$, it can be said that the value of I_{bat} will change as the coupling k changes. From equations (6.6) and (4.13), it can be observed that to regulate power delivered to the battery for this tuning with change in k or at constant k, V_{bat} can be changed or regulated since $i_{P_{rms}}$ and L_{sec} will remain constant and are independent of the coupling k.

$$V_{OC} = \omega M i_{P_{rms}} \tag{4.9}$$

$$i_{P_{rms}} = \frac{4V_g}{\sqrt{2}\pi\omega L_{pr}} \tag{4.10}$$

$$i_{sec_{rms}} = \frac{V_{OC}}{\omega L_{sec}} \tag{4.11}$$

$$i_{sec_{rms}} = \frac{\pi I_{bat}}{2\sqrt{2}} \tag{4.12}$$

$$P_{bat} = \frac{V_{bat}\omega M i_{P_{rms}} 2\sqrt{2}}{\omega L_{sec}\pi}. \tag{4.13}$$

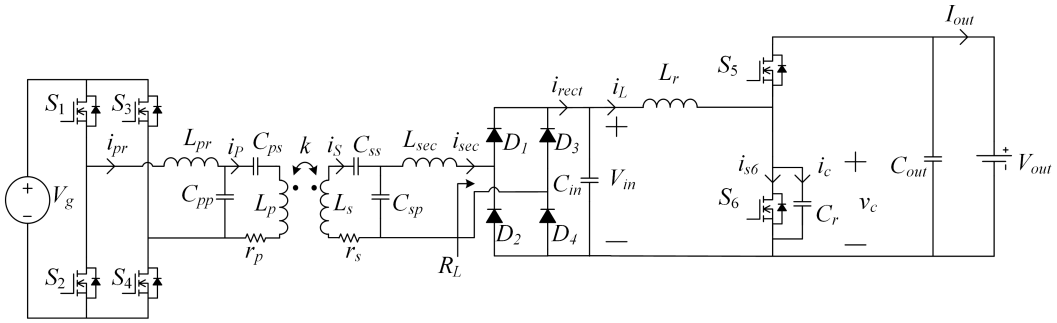


Fig. 4.2: Double-sided LCC compensation with boost converter.

4.1.2 Double-sided LCC compensation with boost converter

Fig. 4.2 shows the full WPT system with double-sided LCC tuning with a boost converter as a DC-DC converter for power regulation. In Section 4.1.1, it is shown that the output power or power transferred to the secondary can be changed by changing V_{bat} in Fig. 4.1, which is the output voltage of the rectifier circuit. Therefore, dc-dc converters can be used to regulate power transfer to the system, where the voltage V_{in} in Fig. 4.2 can be adjusted when the system's coupling coefficient k changes or when a different power is demanded from the system's battery. In [78], three types of DC-DC converters, buck, boost, and buck-boost, have been proposed for different applications depending on the load resistance seen from the rectifier that is required for a specific application. For the buck converter, the equivalent load resistance can be varied from a specific value up to ∞. For a boost type converter, the equivalent load resistance can be varied from zero up to a specific value. For the buck-boost converter, the equivalent load resistance can be varied from zero up to ∞. Since, for the application of dynamic wireless charging systems, the power has to be regulated from zero up to the maximum value that is demanded from the battery system, a boost converter is selected for this application. The power P_{out} given as $V_{out}I_{out}$ from Fig. 4.2 vs voltage V_{in} curves at three different values of k are given Fig. 4.3 where 125 A of current from the output of WPT system is considered at a coupling k of 0.2 and output battery voltage V_{out} is considered to be 600 V. It can be seen from Fig. 4.3 that V_{in} has to be changed at different couplings to achieve different power transferred to the secondary circuit and since output battery voltage is 600 V, V_{in} values are achievable by

using a boost converter at the output.

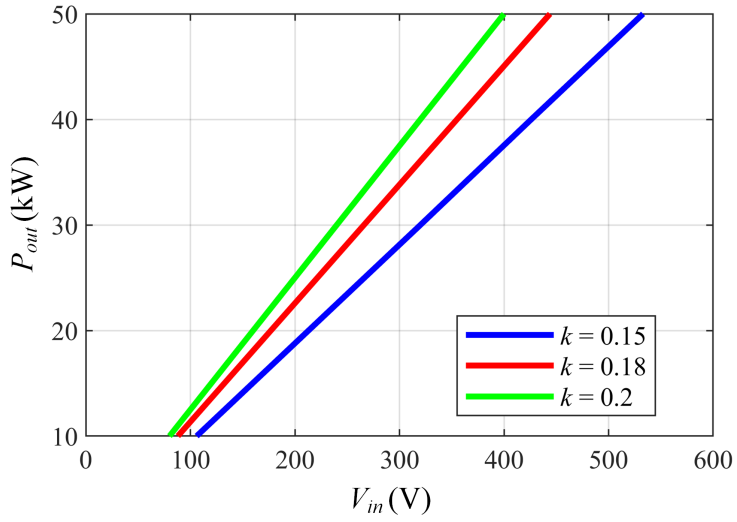


Fig. 4.3: Power Vs Voltage curves.

For high-power dynamic wireless charging systems up to 50 kW power level, there is a need for loss analysis and soft switching analysis so that a DC-DC converter can be added to the wireless charging system without having large losses in the DC-DC converter. High-power designs for DC-DC converters typically use silicon carbide (SiC) switches. There could be two approaches to using the SiC switches for this type of converter. The first would be to use individual SiC switches and parallel these switches to achieve high current capabilities of the DC-DC converters. The other option would be using SiC power modules, which are rated for much higher currents than the individual switches. The individual SiC switch approach leads to complexities in PCB designs where identical layouts are required to achieve proper current sharing in the switches. The SiC power module-based approach could reduce the complexities in paralleling SiC switches and PCB designs to achieve high-power designs. However, soft switching of these modules becomes extremely important to achieve high efficiencies for high-power designs. Therefore, this work considers soft switching converter design for the DC-DC stage. For this design, Wolfspeed power module CAB450M12XM3 [2] is used, which has a V_{ds} rating of 1200 V and an I_{ds} rating of 450A.

For soft switching analysis, a 2-transistor ZVS-QSW boost converter is considered due to the following reasons: (i) ZVS operation is feasible over conversion ratios greater than 0.5 and less than 0.5, (ii) constant frequency duty-cycle control, similar to PWM operation, is feasible, (iii) peak switch voltages during resonant ZVS transitions remain the same as hard-switched PWM.

For designing a 2-transistor ZVS-QSW boost converter, there could be two ways of designing the resonant elements L_r and C_r of the switch cell. For the selection of C_r, either the internal charge equivalent capacitance as given in [79], [80] of power modules could be used, or an external capacitance including a snubber circuit given in [81] could be used for C_r. Both options will be explored for designing the ZVS-QSW converter, and comparisons of the two cases with hard switching are also required to decide the best approach for implementing the DC-DC stage for this system.

4.2 ZVS-QSW Boost Design for Double Sided LCC Compensation

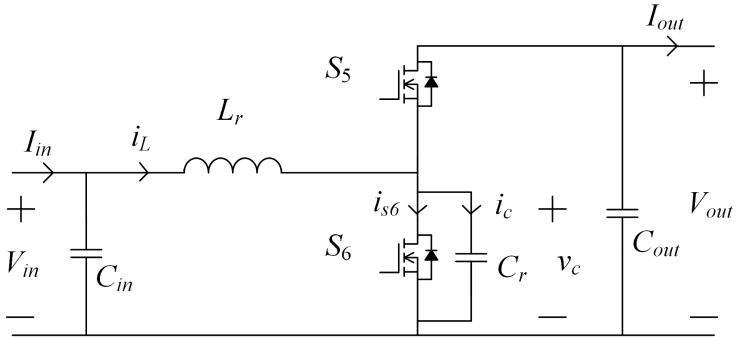


Fig. 4.4: 2-transistor ZVS-QSW boost converter for DC-DC stage.

The waveforms and normalized state plane diagram of the 2-transistor ZVS-QSW boost converter are shown in Fig. 4.5. For selecting the resonant elements L_r and C_r, certain parameters and state plane equations that are used are given in (4.14)-(4.26). The voltage conversion ratio $M(\mu)$, where μ is the conversion ratio of the switch cell, is given in equation (4.14), and the voltage conversion ratio $M(\mu)$ of the boost converter is given in equation (4.15). The center of the state plane diagram shown in Fig. 4.5(b) is $\frac{1}{M}$ or $1-\mu$. I_{on}

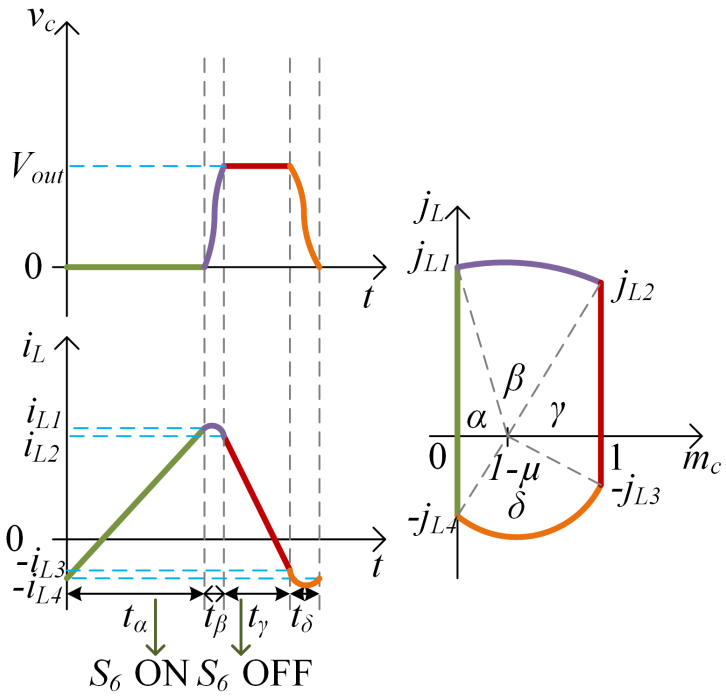


Fig. 4.5: 2-transistor ZVS-QSW boost converter (a) operating Waveforms (b) normalized state-plane diagram.

and V_{base} for boost converter are I_L and V_{bat}, and J is the normalized value of I_L. f_s is the switching frequency of operation and f_o is the resonant frequency of L_r and C_r. F is the normalized switching frequency. J_{L1}, J_{L2}, J_{L3} and J_{L4} are the normalized value of the currents I_{L1}, I_{L2}, I_{L3} and I_{L4} respectively. α, β, γ, and δ are the angles shown in the state plane diagram representing the time intervals t_α, t_β, t_γ, and t_δ. The definition of duty cycle for the ZVS-QSW converter is given in equations (4.27) and (4.28), where β and δ represent the dead times of this converter.

$$M(\mu) = \frac{V_{out}}{V_{in}} \tag{4.14}$$

$$M(\mu) = \frac{1}{1-\mu} \tag{4.15}$$

$$J = \frac{I_{on}}{V_{base}} R_o \tag{4.16}$$

$$F = \frac{f_s}{f_o} \tag{4.17}$$

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{4.18}$$

$$R_o = \sqrt{\frac{L_r}{C_r}} \tag{4.19}$$

$$J_{L4} = \sqrt{J_{L3}^2 - 1 + 2\mu} \tag{4.20}$$

$$J_{L2} = \sqrt{J_{L1}^2 + 1 - 2\mu} \tag{4.21}$$

$$J_{L1} = -J_{L4} + (1-\mu)\alpha \tag{4.22}$$

$$-J_{L3} = J_{L2} - \mu\gamma \tag{4.23}$$

$$\beta = \tan^{-1}(\frac{1-\mu}{J_{L1}}) + \tan^{-1}(\frac{\mu}{J_{L2}}) \tag{4.24}$$

$$\delta = \tan^{-1}(\frac{1-\mu}{J_{L4}}) + \tan^{-1}(\frac{\mu}{J_{L3}}) \tag{4.25}$$

$$\frac{2\pi}{F} = \alpha + \beta + \gamma + \delta \tag{4.26}$$

$$\frac{2\pi}{F} D = \alpha + \delta \tag{4.27}$$

$$\frac{2\pi}{F}(1-D) = \beta + \gamma. \tag{4.28}$$

The following design procedure is followed using the above equations to design a ZVS-QSW converter for double-sided LCC tuning.

1. Decide the peak power level of the IPT system that is to be regulated by the DC-DC converter.

2. Select the battery voltage V_{out} as the base voltage, and since the battery voltage is constant, the resonant elements could be designed corresponding to that base voltage.

3. Find maximum value of I_L, where I_L is the average value of i_L, at the maximum average value of i_{rect} for the misalignment range of the IPT system.

4. Find the value of the conversion ratio μ at the operating point calculated from steps 1, 2, and 3 and using the equations (4.14) and (4.15).

5. Select the value of f_s, the switching frequency of the system, and also the normalized value of switching frequency F.

6. Plot the μ vs J characteristics at the value of F for a 2-Transistor ZVS-QSW converter using the state plane equations given in (4.20)-(4.26).

7. Find J_{max} from μ vs J curves at the value of μ calculated in step 4.

8. Solve for R_o and f_o from equations (4.16), and (4.17), and calculate L_r and C_r using these equations.

4.3 ZVS-QSW Boost with Internal and External Capacitance

4.3.1 Design for ZVS-QSW with Internal and External Capacitances

As mentioned in Section 4.1.2, there could be two ways of designing a ZVS-QSW boost converter, where C_r could be the internal capacitance of the module or an external capacitance.

For designing a ZVS-QSW boost with internal capacitance, the C_{oss} data of XM3 module is obtained from the datasheet [2] as shown in Fig. 4.6. Since the C_{oss} capacitance of any MOSFET is nonlinear and a function of the drain-source voltage across the switch, as shown in Fig. 4.6, the charge equivalent capacitance of the half bridge module given in equation (4.29), obtained from [79], [80] is used to design the ZVS-QSW boost.

$$C_{eq,Q} = \frac{1}{V_{out}} \int_0^{V_{out}} \left(C_{oss}(v_{ds}) + C_{oss}(V_{out} - v_{ds}) \right) dv_{ds}. \tag{4.29}$$

The procedure in Section 4.2 is then followed to design the ZVS-QSW Boost with internal capacitance. The peak power level of the IPT system is selected as 50 kW, which is decided according to the power consumption for a dynamic IPT system at highway speed for a Light Duty Vehicle [1]. The battery voltage selected is 600 V. The maximum value of I_L, which is the average value of the inductor current obtained from the IPT system, is approximately 125 A. The value of μ calculated at this operating point is 0.33. The

switching frequency f_s selected for this system is 70 kHz. The value of C_r is selected according to the charge equivalent capacitance of the half bridge module given in equation (4.29), at V_{out} of 600 V. The value of C_r calculated is 6.66 nF. Since C_r is first selected, L_r, J, and F are calculated from steps 6, 7, and 8 of the design procedure in Section 4.2. Similarly, for C_r as external capacitance, the total capacitance of C_r including the charge equivalent capacitance and external capacitance C_{ext} is selected to be 50 nF, and L_r, J, and F are calculated from steps 6, 7, and 8 of the design procedure in Section 4.2. The calculated values of L_r, J, and F for the two cases of internal and external capacitance are given in Table 4.1.

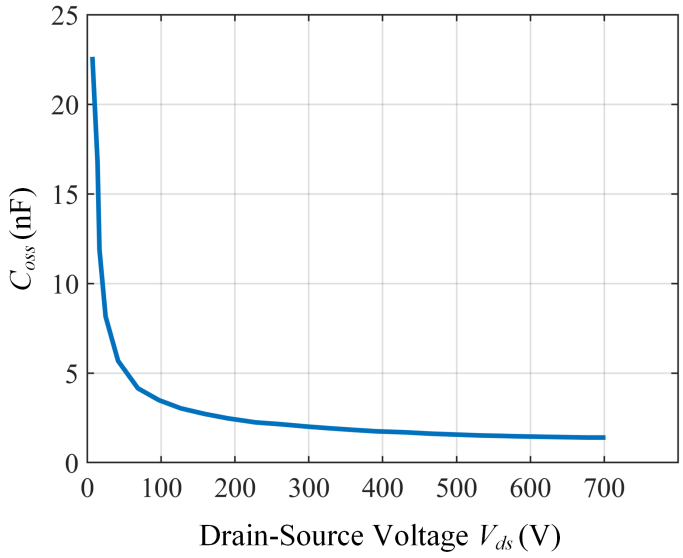


Fig. 4.6: C_{oss} vs V_{ds} plot for CAB450M12XM3 module.

The μ vs J characteristics for $F = 0.09$ and $F = 0.22$ for a 2-Transistor ZVS-QSW boost converter are shown in Fig. 4.7. It can be seen that for almost the entire range of μ less than 0.5 and greater than 0.5, ZVS turns on due to the negative currents, which can be achieved for currents I_L, when J is inside these curves for $F = 0.08$ and $F = 0.21$.

Table 4.1: Parameters used for the design of the 2-Transistor ZVS-QSW boost.

Parameter	F **= 0.09**	F **= 0.22**
f_s	70 kHz	70 kHz
I_L	125 A	125 A
P_{out}	50 kW	50 kW
V_{out}	600 V	600 V
μ	0.33	0.33
J	6.6	2.1
C_r	6.66 nF	50 nF
L_r	6.8 μH	5.1 μH

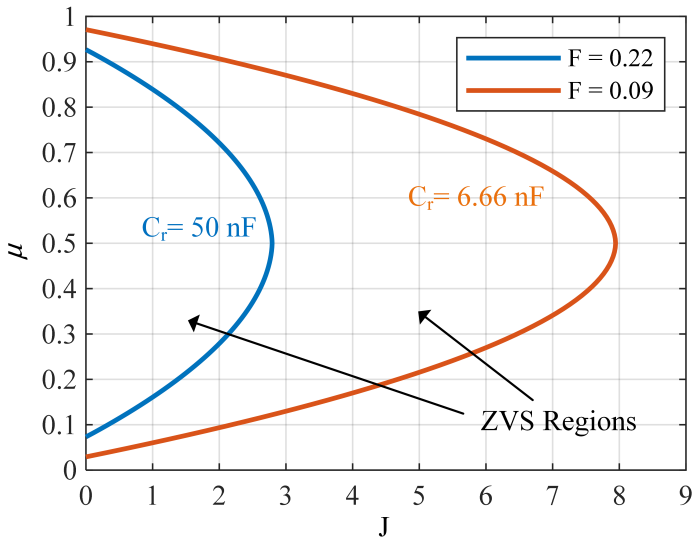


Fig. 4.7: 2-Transistor ZVS-QSW Characteristics for $F = 0.09$ and $F = 0.22$.

4.3.2 Loss Analysis using LTspice models

To verify the functionality of the ZVS-QSW converter at 50 kW for both internal capacitance and external capacitance cases, simulation analysis of CAB450M12XM3 power modules in LTspice has been done. The LTspice model of the CAB450M12XM3 half-bridge module has been obtained from the Wolfspeed website [2]. LTspice models of CAB450M12XM3 power modules to replicate the exact models provided by Wolfspeed, which can be used to see internal capacitance current, drain current, and several other waveforms of the power module, have also been developed and simulated. The losses for the hard switching case

with an inductance of 10.5 μH are also shown in this section.

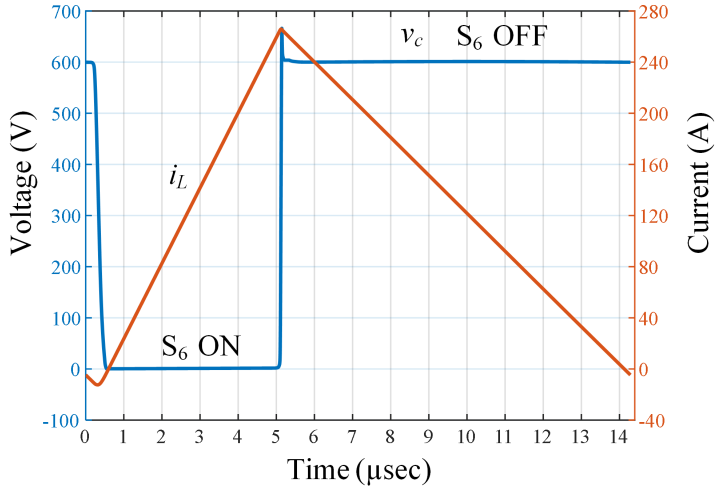


Fig. 4.8: i_L and v_c waveforms for 2-Transistor ZVS-QSW boost for $F = 0.09$.

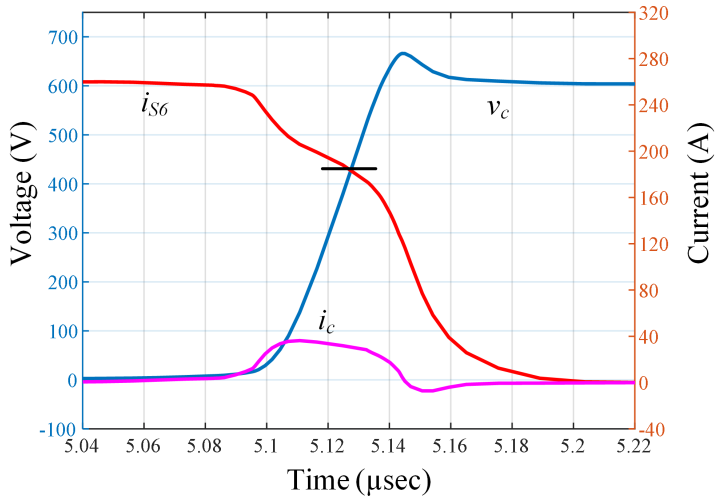


Fig. 4.9: i_{s6}, i_c and v_c waveforms for 2-Transistor ZVS-QSW boost during turn off of S_6 for $F = 0.09$.

The simulated waveforms showing resonant capacitance current, drain current, and resonant capacitor voltage for a 2-Transistor ZVS-QSW boost converter for $F = 0.09$ and $F = 0.22$ are shown in Fig. 4.8, Fig. 4.9, Fig. 4.10, and Fig. 4.11. It can be seen from

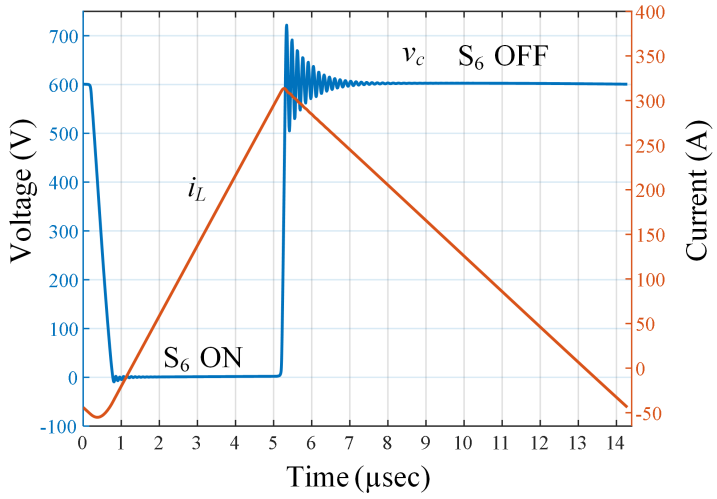


Fig. 4.10: i_L and v_c waveforms for 2-Transistor ZVS-QSW boost for $F = 0.22$.

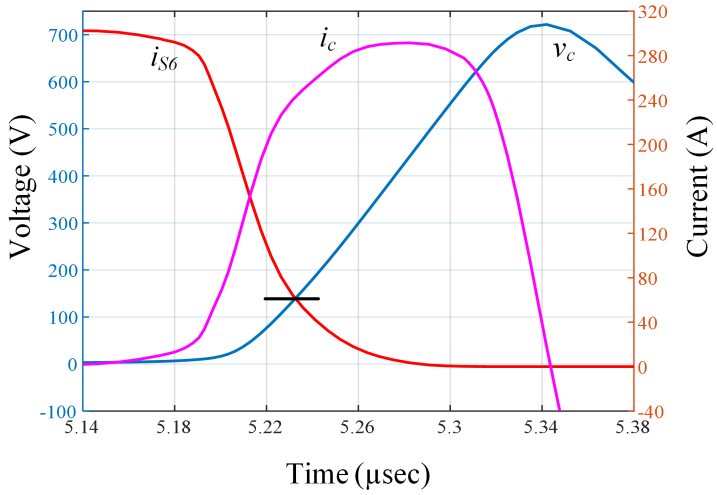


Fig. 4.11: i_{s6}, i_c and v_c waveforms for 2-Transistor ZVS-QSW boost during turn off of S_6 for $F = 0.22$.

Fig. 4.8 and Fig. 4.10 that the turn-on transitions are soft switching due to the negative value of inductor current, which helps in the discharge of C_r during the turn-on transition. For the external capacitance case, a parallel combination of 6 snubber resistors, each having a value of 200 mΩ, is added in series with C_r to mitigate the ringing due to the resonance between parasitic inductances of the module and external C_r as shown in Fig. 4.10. Fig. 4.9 and Fig. 4.11 show the turn off transition of S_6 for $F = 0.09$ and $F = 0.22$, respectively. In

Fig. 4.9, it can be observed that there is a large overlap between the drain current of s_6, i_{s6}, and the drain voltage of s_6, v_c, since it takes less time to charge C_r, which is just 6.66 nF for $F = 0.09$. Therefore, this transition almost loses soft switching for $F = 0.09$, and the turn-off losses become large. However, in Fig. 4.11, it can be observed that there is less overlap between drain current of s_6, i_{s6} and drain voltage of s_6, v_c since it takes much longer time to charge C_r with external capacitance where the total capacitance is 50 nF for F=0.22 due to which turn off losses can be reduced for $F = 0.22$. However, due to complexities in the parasitic inductances and capacitances and obtaining exact timing parameters from the datasheet of the module, hardware results are required to have accurate loss results for two designs of soft-switched boost converter and hard-switched boost converter.

For both cases of the ZVS-QSW converter with internal and external capacitance, the turn-on transition of S_6 is soft switching, and losses in S_5 and S_6 are negligible during this transition. However, the turn-off transition of S_6 is not completely soft switching, since there is overlap in the drain current of S_6 and the drain voltage across S_6, due to which the turn-off losses in S_6 contribute most to the switching losses of the ZVS-QSW boost converter. The turn-off losses for S_6 can also be estimated by equation (4.30), for soft switching with internal capacitance, and by equation (4.31) for soft switching with external capacitance, where C_{ext} is the external capacitance added to the circuit. From (4.31), it can be observed that turn-off losses for S_6 can be further reduced as compared to equation (4.30), given in [81], by adding external capacitance to a ZVS-QSW boost converter. The E_{off} for S_6 for soft switching with internal capacitance, estimated from the datasheet, is approximately 4.8 mJ. The power loss during this transition, calculated from the datasheet, is 336 W. Considering the maximum R_{dson} of 3.4 mΩ from the datasheet, the total conduction losses for the top and bottom switch are around 76 W. The total module loss estimated from the datasheet for the soft switching with internal capacitance is around 412 W, which is close to the losses calculated from the simulation of the actual module. However, due to changes in the turn-off times when external capacitance is added to the module, it is not possible to predict the losses from the datasheet. For the external capacitance from the datasheet,

the E_{off} from the datasheet is approximately 5.8 mJ, and the energy from $0.5C_{ext}V_{out}^2$ is approximately 7.8 mJ, which is not correct since the difference of two would be negative. Therefore, to predict the approximate losses, spice models of actual modules have been used. The losses obtained from the spice model for the two cases of soft switching and hard switching have been provided in Table 4.2.

$$E_{off,i} = \frac{1}{2}V_{out}i_{Lmax}t_{off} - \int V_{out}\, dQ_{oss} \tag{4.30}$$

$$E_{off,e} = \frac{1}{2}V_{out}i_{Lmax}t_{off} - \int V_{out}\, dQ_{oss} - \frac{1}{2}C_{ext}V_{out}^2 \tag{4.31}$$

Table 4.2: Estimated Module Losses for 3 cases.

Parameter	**ZVS-QSW External**	**ZVS-QSW Internal**	**Hard Switching**
P_{out}	50 kW	50 kW	50 kW
V_{out}	600 V	600 V	600 V
μ	0.33	0.33	0.33
Module Loss	282 W	401 W	458 W

4.3.3 Capacitor and Resistor Design for External Circuit of ZVS-QSW Converter

Fig. 4.12(a) shows the equivalent circuit diagram during the turn-off transition of S_6, and Fig. 4.12(b) shows the waveform of current in S_6 during the turn-off transition, where time $t_{off,i}$ is shown in the waveform. The current I_L represents the peak value of Inductor current during turn-off transition. For selecting the external capacitance, the initial approximation of the peak inductor current can be determined from the design of the ZVS-QSW converter with internal capacitance. From Fig. 4.9, it can be seen that the peak inductor current during the turn-off interval is approximately 270 A and the time $t_{off,i}$ is

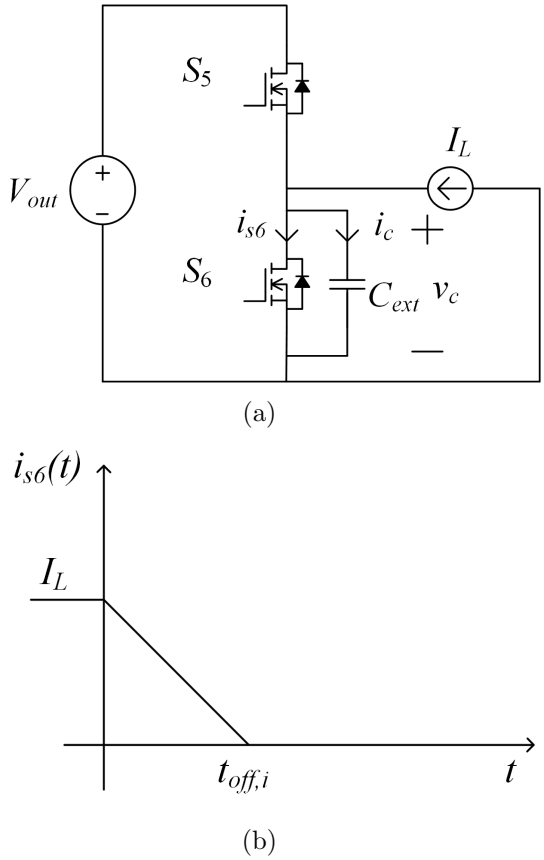


Fig. 4.12: (a) Equivalent circuit diagram of Boost Converter with inductor current during turn off of S_6, (b) Waveform showing current in S_6 during turn off transition.

approximately 100 ns. The time taken to charge this capacitance is approximately 50 ns, which is very fast, resulting in a large overlap between the drain current and drain voltage of S_6 during the turn-off transition. For selecting the external capacitance, slightly higher inductor current could be assumed during the turn-off transition, since a larger capacitance will result in a lower inductance value and higher ripple currents, as can be observed from the state plane equations of the ZVS-QSW converter in Section 4.2. In equations (4.32) to (4.37), the approximate time taken to charge the external capacitance is derived, where it is considered that the external capacitance is much larger than the equivalent charge capacitance of the module. Considering I_L to be 300 A, v_c to be 600 V, $t_{off,i}$ to be 100 ns, an external capacitance of 44 nF takes approximately 130 ns to charge from (4.37). This charging time is sufficient to significantly reduce the overlap of drain current and drain

voltage of S_6, as can be observed in Fig. 4.11, thereby reducing the turn-off losses. Therefore, for selecting the external capacitance, the charging time could be between two and three times the time it takes to charge the internal charge equivalent capacitance of the module. The external capacitance value could also be swept in LTspice simulations of the actual model of the module, so that the charging time is between two or three times the time it takes to charge the internal charge equivalent capacitance of the module, and the switching losses are minimized in simulation. The selection of this capacitance also depends on how feasible it is to practically realize the external capacitance using appropriate series and parallel combinations to meet the AC and DC voltage requirements and the RMS currents flowing through it. The series-parallel combination of this capacitance should also be minimized to reduce the loop area around the switch node and ground terminals of the module. Therefore, selecting this capacitance is an iterative process to minimize losses, meet the voltage and current requirements, and minimize the loop area around the switch node and the module's ground terminals. The total capacitance used to design the ZVS-QSW converter is then the sum of the external capacitance and the module's equivalent charge capacitance, which is 50 nF in this design.

$$i_{s6}(t) = I_L - \frac{I_L t}{t_{off,i}} \tag{4.32}$$

$$i_c(t) = I_L - i_{s6}(t) \tag{4.33}$$

$$i_c(t) = \frac{I_L t}{t_{off,i}} \tag{4.34}$$

$$C_{ext}\frac{dv_c}{dt} = \frac{I_L t}{t_{off,i}} \tag{4.35}$$

$$C_{ext}v_c = \frac{I_L t^2}{2t_{off,i}} \tag{4.36}$$

$$t = \sqrt{\frac{2C_{ext}v_c t_{off,i}}{I_L}} \tag{4.37}$$

Fig. 4.13 shows a ZVS QSW converter with external capacitances having parasitics

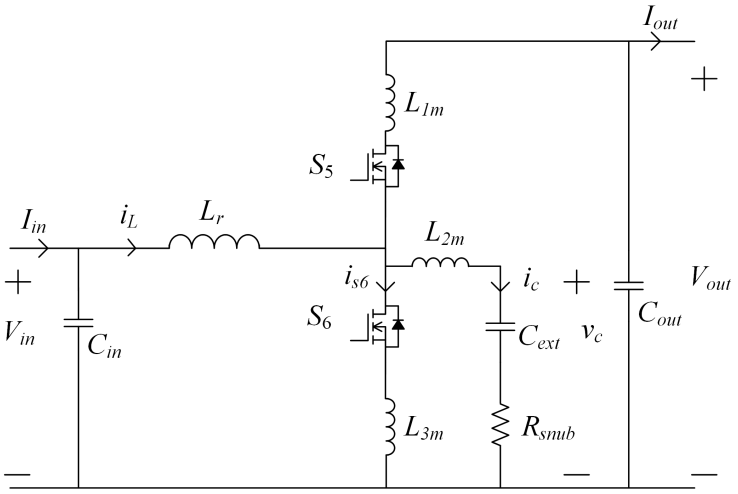


Fig. 4.13: 2-Transistor ZVS-QSW Converter with external capacitance with parasitic inductances.

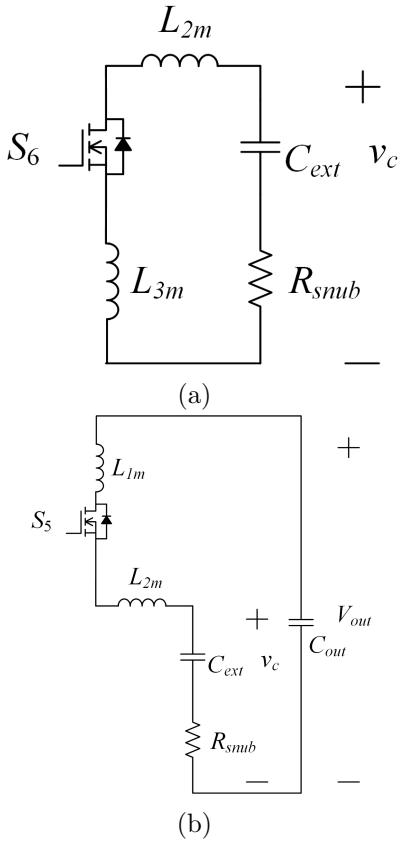


Fig. 4.14: (a) Loop for resonance for ZVS QSW with external capacitance after S_6 turns on, (b) Loop for resonance for ZVS QSW with external capacitance after S_6 turns off.

Table 4.3: Parasitic Inductances.

Parameter	**Value**
L_{1m}	5.9 nH
L_{2m}	4.9 nH
L_{3m}	860 pH

in the power module. Due to this external capacitance and parasitics of the power module, resonances occur during the turn-on and turn-off transitions of S_6. To damp these resonances, an external resistor is connected in series with the capacitance. The loop for resonance after S_6 turns on is shown in Fig. 4.14(a), and the loop for resonance after S_6 turns off is shown in Fig. 4.14(b). Both of these resonances are damped by the external resistor R_{snub}. Therefore, to calculate the losses and select the resistor R_{snub}, the resonant transitions are analyzed. Table 4.3 shows the value of parasitic inductances that are responsible for resonances after the turn-on and turn-off transitions. From Fig. 4.14(a), it can be observed that after S_6 turns on, L_{2m}, L_{3m} and C_{ext} are responsible for the resonance. The peak energy in the parasitic inductances during this transition is dissipated in R_{snub} . This resonance starts when the body diode of S_6 turns on after the voltage v_c reaches 0 due to the negative inductor current that helps in discharging the capacitance C_r. The frequency of resonance during this transition and power loss due to peak energy stored in the parasitic inductances are shown in (4.38) and (4.40). The peak current $I_{peak_{on}}$ is the peak current in L_{2m} after S_6 turns on and is close to the peak value of negative inductor current. This current can also be obtained from the simulation and is approximately 40 A. The total inductance during this transition is 5.76 nH. The $P_{loss_{on}}$ can be calculated at switching frequency f_{sw} of 70 kHz. The losses are negligible due to the very low value of $I_{peak_{on}}$. $f_{r_{on}}$ is calculated from (4.38), and is equal to 9.99 MHz.

$$f_{r_{on}} = \frac{1}{2\pi\sqrt{(L_{2m} + L_{3m})C_{ext}}} \tag{4.38}$$

$$T_{r_{on}} = 2\pi\sqrt{(L_{2m} + L_{3m})C_{ext}} \tag{4.39}$$

$$P_{loss_{on}} = \frac{1}{2}(L_{2m} + L_{3m})I^2_{peak_{on}} f_{sw} \tag{4.40}$$

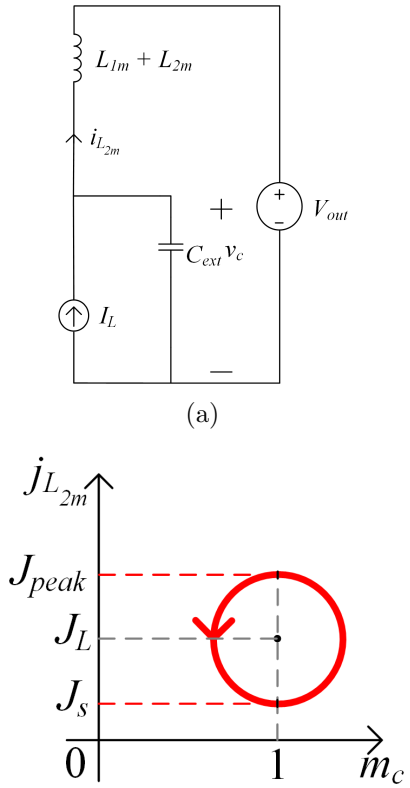


Fig. 4.15: (a) Equivalent circuit for ZVS QSW with external capacitance after S_6 turns off, (b) Normalized state plane diagram for inductor current vs capacitor voltage.

Fig. 4.15(a) shows the equivalent circuit for ZVS QSW with external capacitance after S_6 turns off. For analyzing this resonant transition, the external resistor is not considered, as it would damp the transition. Therefore, only the parasitic inductance and external capacitance are considered. Fig. 4.15(b) shows the normalized state plane diagram for the equivalent circuit for ZVS QSW with external capacitance after S_6 turns off, where $j_{L_{2m}}$ represents the normalized inductor current $i_{L_{2m}}$ and m_c represents the normalized voltage v_c. V_{out} is considered as the V_{base} for the normalized state plane diagram. I_L in Fig. 4.15(a) is the inductor current after S_6 turns off, which is approximately the positive peak value of inductor current. The frequency of resonance during this transition and

power loss due to peak energy stored in the parasitic inductances are shown in (4.41) and (4.49). To find $I_{peak_{off}}$, J_L and J_s are evaluated, where (1,J_s) represents the starting point of the state plane diagram and (1,J_L) represents the center of the normalized state plane diagram. $I_{s_{off}}$ and therefore J_s can be obtained from the simulation, where $I_{s_{off}}$ is equal to 40 A. I_L is approximately 300 A. $f_{r_{off}}$ is 7.3 MHz, $I_{peak_{off}}$ is calculated as 560 A from (4.43)-(4.48), $P_{loss_{off}}$ is calculated as 118 W from (4.49). 6 resistors of 200 mΩ given in Table 4.5 are connected in parallel for R_{snub} to handle the power loss. The total resistance becomes 33.33 mΩ. The RMS current in R_{snub} is obtained from the simulation and is equal to 31.72 A. The loss due to RMS current is 33 W in R_{snub}. The total loss in R_{snub} is approximately 151 W. The loss in R_{snub} is dominated by peak energy stored in parasitic inductance if R_{snub} is low enough for low RMS losses. Therefore, R_{snub} is kept low enough to minimize the power loss in the resistors and meet the power ratings due to losses. If R_{snub} is increased to high values, damping is improved. However, the losses then become dominated by RMS losses, leading to overall increased losses.

$$f_{r_{off}} = \frac{1}{2\pi\sqrt{(L_{1m}+L_{2m})C_{ext}}} \tag{4.41}$$

$$R_{o_{off}} = \sqrt{\frac{L_{1m}+L_{2m}}{C_{ext}}} \tag{4.42}$$

$$V_{base} = V_{out} \tag{4.43}$$

$$I_{base} = \frac{V_{base}}{R_{o_{off}}} \tag{4.44}$$

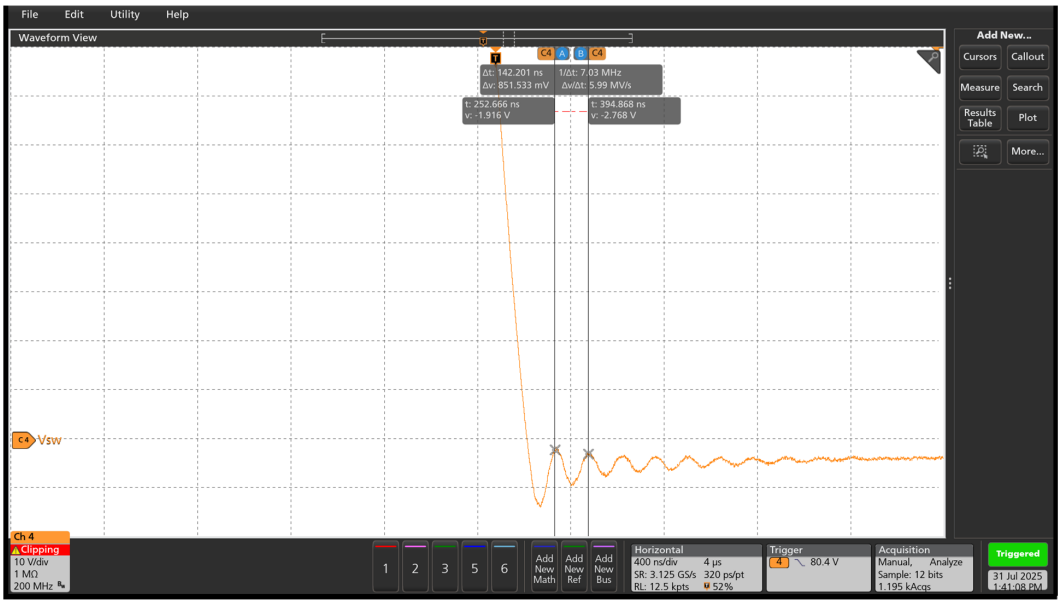
$$J_L = \frac{I_L}{V_{base}} R_{o_{off}} \tag{4.45}$$

$$J_{peak} = \frac{I_{peak_{off}}}{V_{base}} R_{o_{off}} \tag{4.46}$$

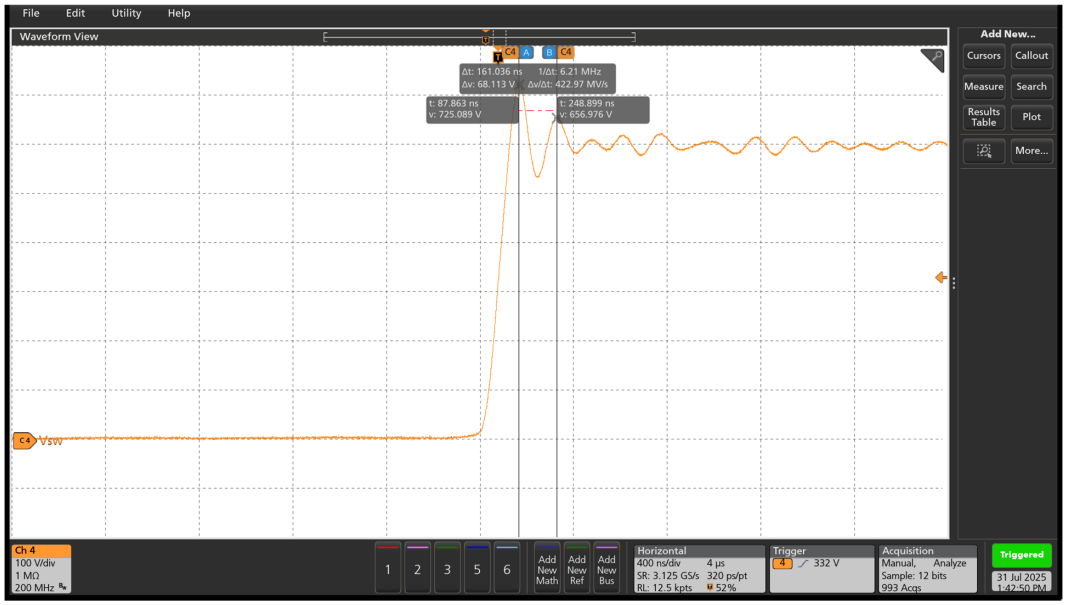
$$J_s = \frac{I_{s_{off}}}{V_{base}} R_{o_{off}} \tag{4.47}$$

$$J_{peak} = J_s + 2J_L \tag{4.48}$$

$$P_{loss_{off}} = \frac{1}{2}(L_{1m} + L_{2m})I^2_{peak_{off}} f_{sw} \tag{4.49}$$



(a)



(b)

Fig. 4.16: (a) Experimental waveform showing resonance after S_6 turns on, (b) Experimental waveform showing resonance after S_6 turns off.

Fig. 4.16(a) shows the experimental waveform for resonance after S_6 turns on. The

resonant frequency $f_{r_{on}}$ measured is 7 MHz. This difference from the calculated frequency is due to additional parasitic inductance in the PCB. Fig. 4.16(b) shows the experimental waveform for resonance after S_6 turns off. The resonant frequency $f_{r_{off}}$ measured is 6.2 MHz.

Considering the maximum R_{dson} of 3.4 mΩ from the datasheet, the total conduction losses for the top and bottom switch are around 93 W. Table 4.4 gives the estimated breakdown of losses in the module for ZVS-QSW with external capacitance at 50 kW at a conversion ratio of 0.33.

Table 4.4: Estimated breakdown of losses in the module for ZVS-QSW with External Capacitance at 50 kW.

Parameter	**Value**
P_{out}	50 kW
V_{out}	600 V
μ	0.33
Total Module Loss	282 W
Snubber Loss	151 W
Conduction Loss	93 W
Switching Loss including snubber loss	189 W

4.4 Hardware Design for ZVS-QSW Boost Converter

4.4.1 PCB Design for DC-DC Converter

The high power PCB designs for the boost converter to test two types of soft switching cases and hard switching of the boost converter are shown in Fig. 4.18. Fig. 4.18 (a) shows the top side of the power board PCB, which has 2 half-bridge modules where 1 half-bridge module has no internal capacitance and the other half-bridge module has the C_{ext} and snubber resistors connected in series with C_{ext}. There are 6 snubber resistors connected in parallel, each having a value of 200 mΩ. The power board PCB is a 6-layer PCB with

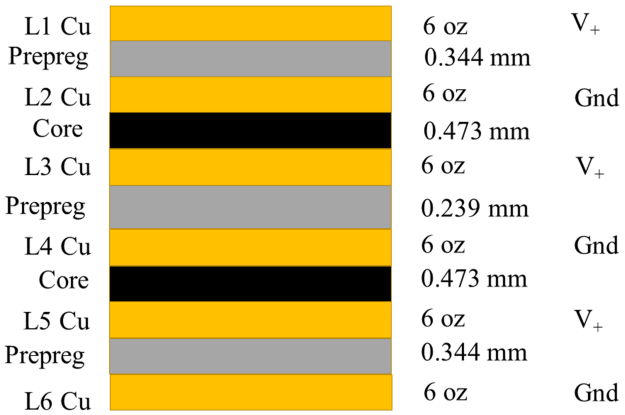
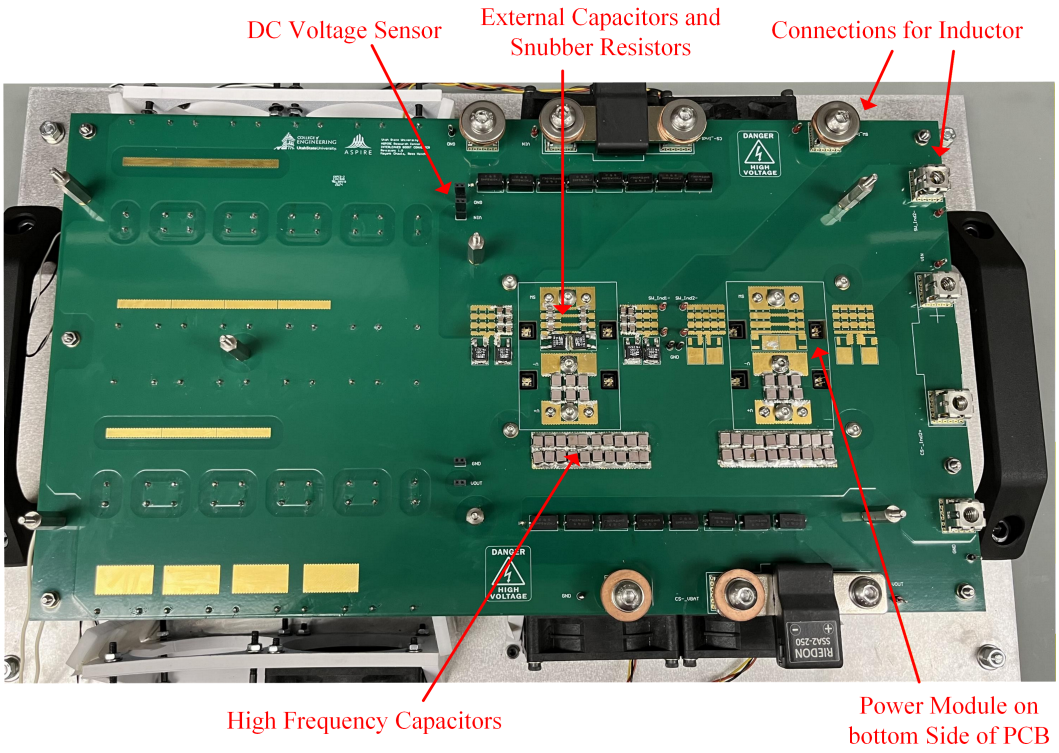


Fig. 4.17: Layer stackup for the Power Board for the DC-DC converter.

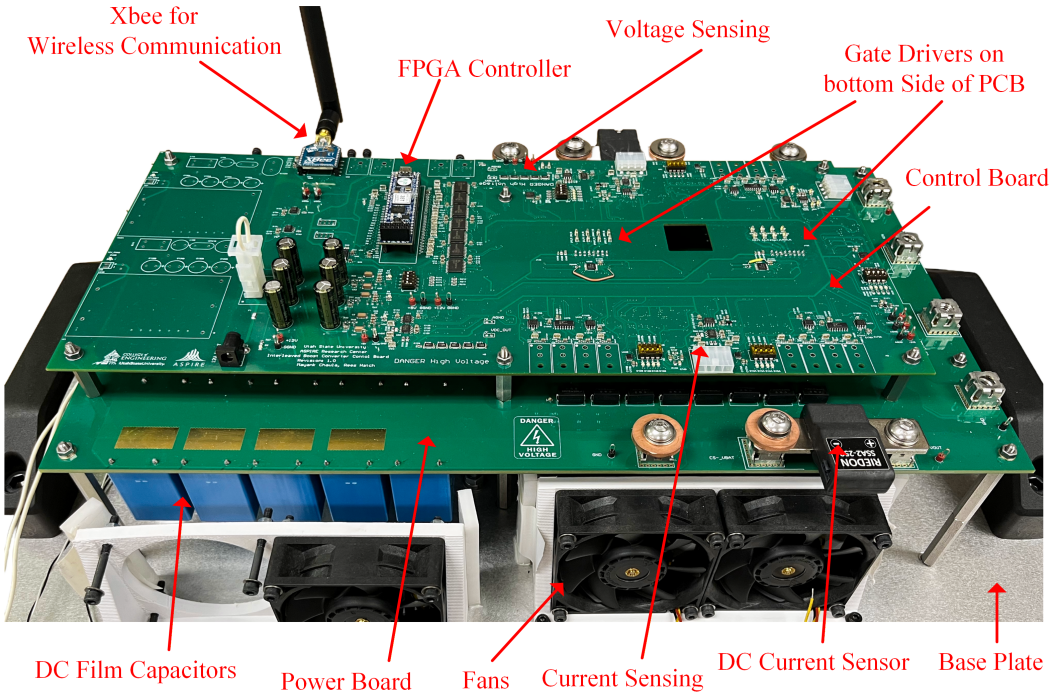
each layer having 6 oz copper to support high currents for high power. The layer stackup of the power board is shown in Fig. 4.17. The major components used in the power board are given in Table 4.5. Fig. 4.18 (b) shows the control board stacked on top of the power board. The control board PCB shown in Fig. 4.18 (b) is also designed on a 6-layer PCB with considerations for signal integrity and uses an FPGA for control signals.

Table 4.5: Major Components for the Power Board of the DC-DC Converter.

DC Film Capacitors	TDK B32778G1206K000
High Frequency Capacitors	TDK C5750C0G2J104J280KC
External Capacitors C_{ext}	Kemet C1210X223JDGACAUTO
Snubber Resistors for C_{ext}	MP725-0.20-1%



(a)



(b)

Fig. 4.18: PCB for DC-DC Converter: (a) Power board, (b) Control board, stacked with power board.

4.4.2 Inductor Design for DC-DC Converter

For the inductor design, for both the cases of soft switching with external and internal capacitances, 6 UI 93/104/30 ferrite cores with N87 material are used in parallel, due to which the total cross-sectional area of the cores becomes 6 times the effective core area. To handle the high ripple currents in the soft switching inductors, custom-designed litz wire with AWG 38 and 8000 strands is used. Fig. 4.19 shows the inductor for ZVS-QSW with external capacitance. For hard switching cases using 6 UI 93/104/30 ferrite cores with N87 material and litz wire with AWG 38 and 4570 strands, an inductance of 10.5 μH is achieved. Equations (4.54) and (4.55) are used to estimate the core losses in the inductors for three cases [82]. The values of k_i, α, and β for N87 core material from TDK are 1.25, 2.46, and 1.17 [82]. The core loss at the operating point in Table 4.1 for 1 turn for all three cases is nearly 377 W, for 2 turns for all three cases is nearly 70 W, and for 3 turns for all three cases is nearly 25 W. The window area for the cores allows a maximum of 2 turns of wire used, which also reduces the ac resistance of the wire as compared to 3 turns. A 2-turn design is finalized for all three cases for the inductor. The inductor specifications and design parameters for 50 kW operating point are given in Table 4.6 and Table 4.7.

$$L = \frac{n^2}{\mathcal{R}_g + \mathcal{R}_c} \tag{4.50}$$

$$\mathcal{R}_g = \frac{l_g}{\mu_0 A_c} \tag{4.51}$$

$$\mathcal{R}_c = \frac{l_c}{\mu_c A_c} \tag{4.52}$$

$$B_{max} = \frac{n I_{max} \mu_0}{l_g} \tag{4.53}$$

$$P_v = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} f(t)\, dt \tag{4.54}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta. \tag{4.55}$$

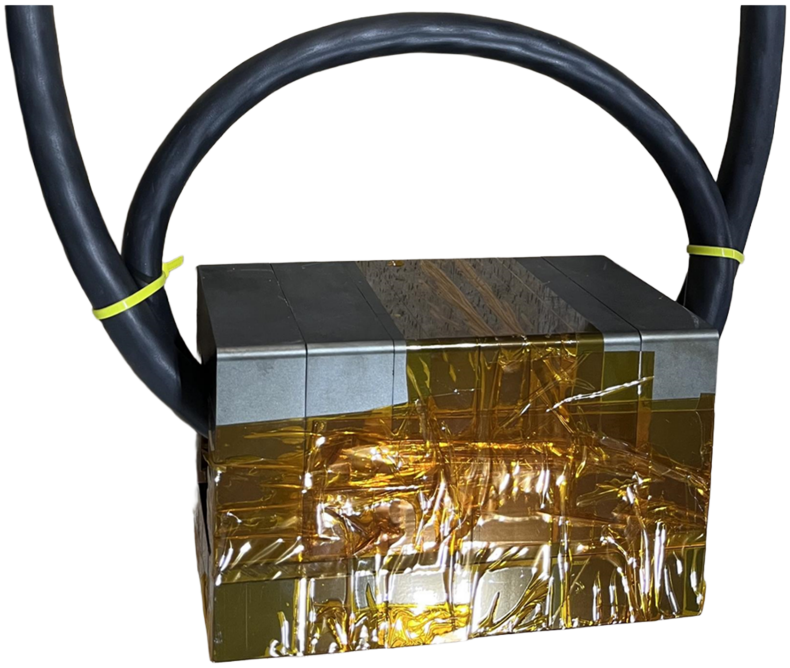
Table 4.6: Inductor Design Specifications at 50 kW.

Parameter	**ZVS-QSW External**	**ZVS-QSW Internal**	**Hard Switching**
L_r	5.1 μH	6.8 μH	10.5 μH
I_{max}	310 A	270 A	220 A
I_{rms}	165 A	150 A	136 A
Cores in parallel	6, UI 93/104/30	6, UI 93/104/30	6, UI 93/104/30
Cores Area	6 $\times$ 840 mm^2	6 $\times$ 840 mm^2	6 $\times$ 840 mm^2
Core Material	N87	N87	N87
Litz Wire	AWG 38, 8000 strands	AWG 38, 8000 strands	AWG 38, 4750 strands
Current Carrying Capability of Litz	250 A	250 A	154 A

Table 4.7: Inductor Design Parameters.

Parameter	**ZVS-QSW External**	**ZVS-QSW Internal**	**Hard Switching**
L_r	5.1 μH	6.8 μH	10.5 μH
Air gap l_g	4.8 mm	3.6 mm	2.6 mm
Number of turns	2	2	2
B_{max}	168 mT	186 mT	210 mT

The experimental measurements for inductance and the series AC resistance for all three inductors were measured using an LCR meter. The experimental measurements are shown in Fig. 4.20. The AC resistance for the inductor of 5.1 μH is 4.88 mΩ, for the inductor of 6.8 μH is 4.77 mΩ, and for the inductor of 10.5 μH is 6.91 mΩ. The approximate experimental losses in the inductor for all three cases can be calculated using the measured



(a)



(b)

Fig. 4.19: Inductors for Soft Switching and Hard Switching: (a) Soft Switching Inductor 48 cm × 30 cm × 17 cm (b) Hard Switching Inductor 48 cm × 30 cm × 17 cm.

AC resistance. The estimated breakdown of losses for ZVS-QSW with external capacitance at 50 kW, including inductor losses, is given in Table 4.8. The estimated breakdown of losses for all three cases at 50 kW, including inductor losses, is given in Table 4.9.



(a) (b) (c)

Fig. 4.20: (a) LCR measurement of the inductor for soft switching with external capacitance. (b) LCR measurement of inductor for soft switching with internal capacitance. (c) LCR measurement of inductor for hard switching.

Table 4.8: Estimated breakdown of losses for ZVS-QSW with external capacitance at 50 kW, including inductor losses.

Parameter	**Value**
P_{out}	50 kW
V_{out}	600 V
μ	0.33
Total Module Loss	282 W
Snubber Loss	151 W
Conduction Loss	93 W
Switching Loss including snubber loss	189 W
Inductor Loss	133 W
Total Loss	415 W

Table 4.9: Estimated breakdown of losses for 3 cases at 50 kW, including inductor losses.

Parameter	**ZVS-QSW External**	**ZVS-QSW Internal**	**Hard Switching**
P_{out}	50 kW	50 kW	50 kW
V_{out}	600 V	600 V	600 V
μ	0.33	0.33	0.33
Module Loss	282 W	401 W	458 W
Conduction Loss	93 W	76 W	62 W
Switching Loss	189 W	325 W	396 W
Inductor Loss	133 W	107 W	128 W
Total Loss	415 W	508 W	586 W

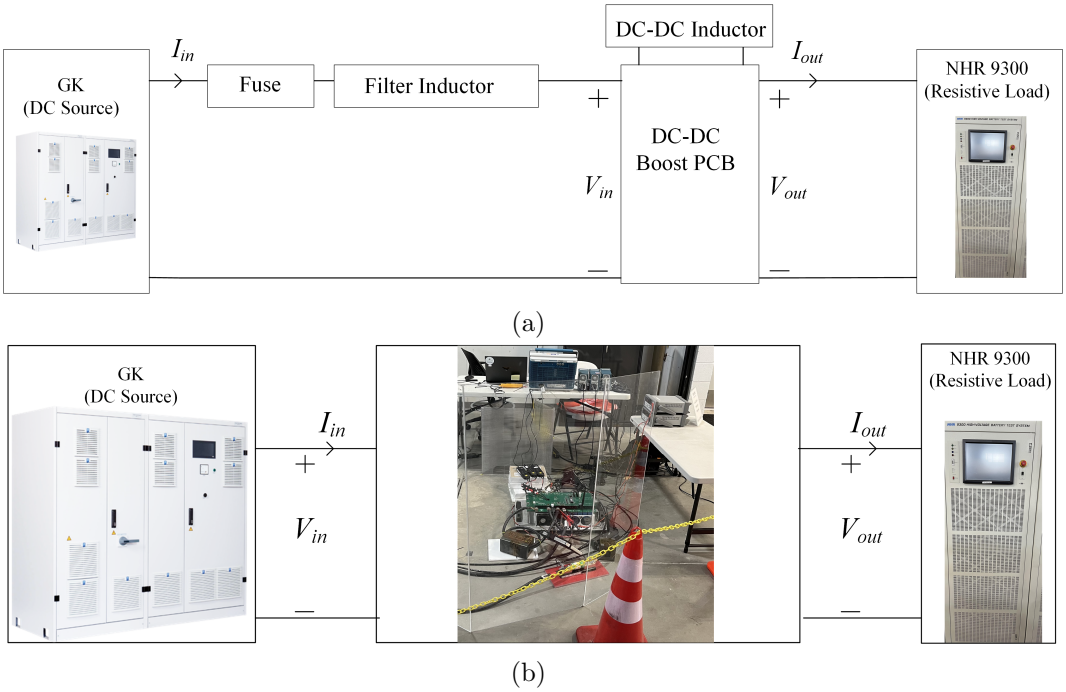
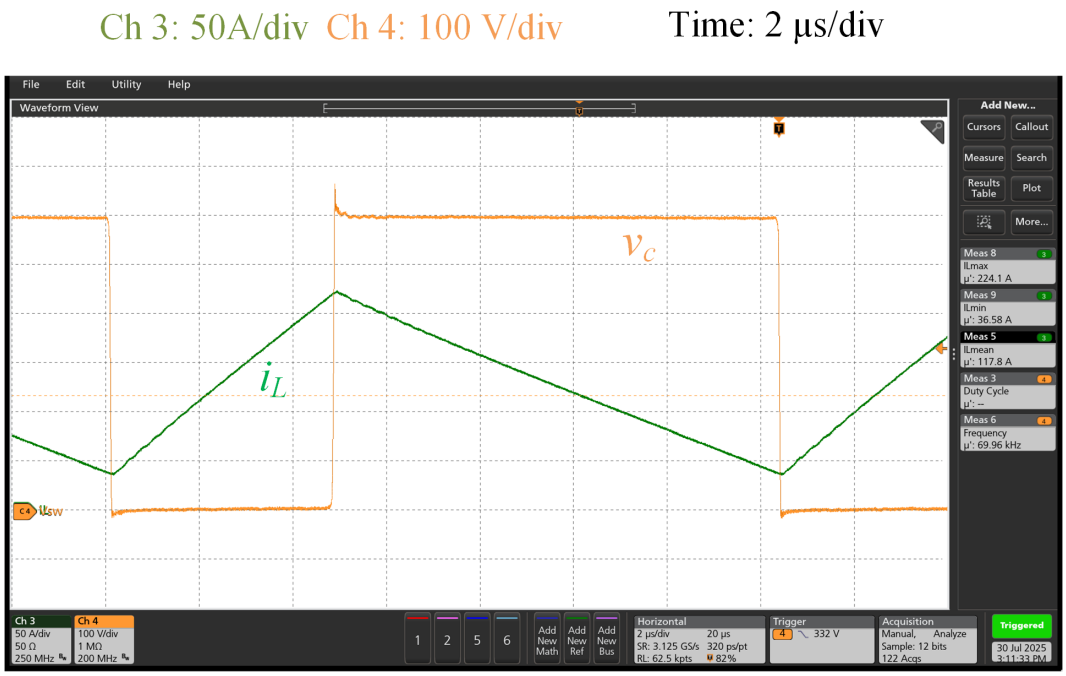


Fig. 4.21: Test Setup for DC-DC: (a) Test setup diagram (b) Actual test setup.

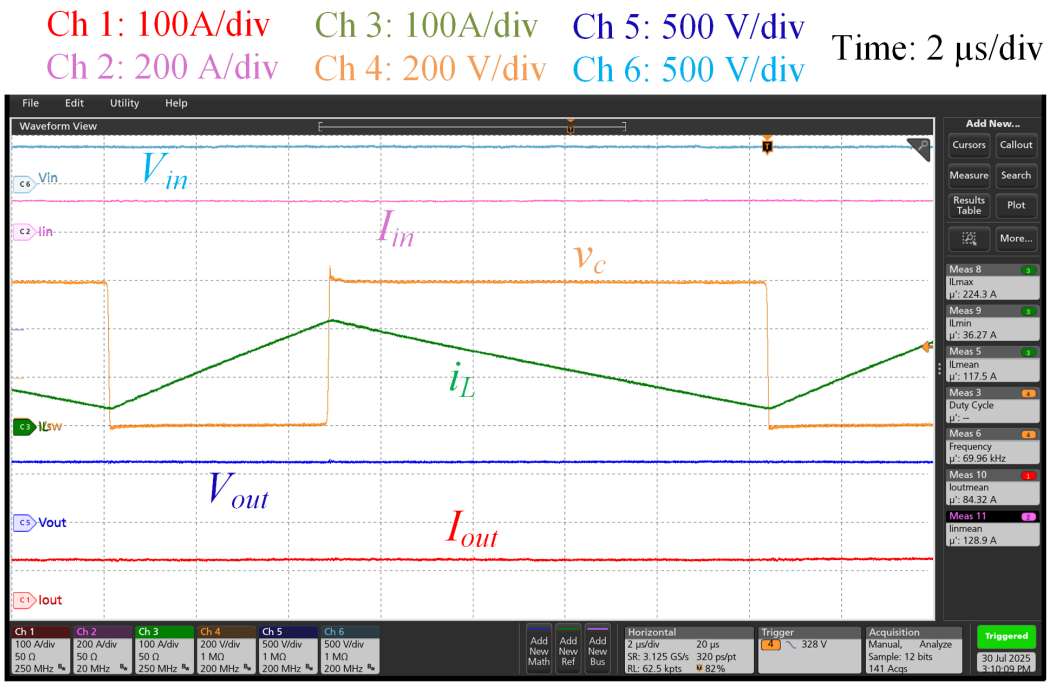
4.5 Hardware Results

For calculating the experimental losses and analyzing the DC-DC converter performance for all three cases at different power levels, Gustav Klein is used as a power supply at the input, and NHR 9300 is used as a resistive load at the output. Fig. 4.21 shows the test setup for the DC-DC converter. The current measurements are directly taken from Gustav Klein and NHR 9300, and the voltage readings are taken at the input and output terminals of the DC-DC converter using a 6-digit digital multimeter to calculate the experimental losses. Fig. 4.22, Fig. 4.23, and Fig. 4.24 show the waveforms for hard switching, soft switching with internal capacitance, and soft switching with external capacitance, respectively, of the converter at 50 KW at the operating point used for design of ZVS-QSW converter in Table 4.1.

Fig. 4.31, Fig. 4.32, Fig. 4.33, Fig. 4.34, Fig. 4.35 and Fig. 4.36 shows the loss comparison for Hard Switching converter, ZVS-QSW converter with internal capacitance and ZVS-QSW converter with external capacitance for different power levels at different coupling, input current of dc-dc converter from the WPT system and different conversion ratios

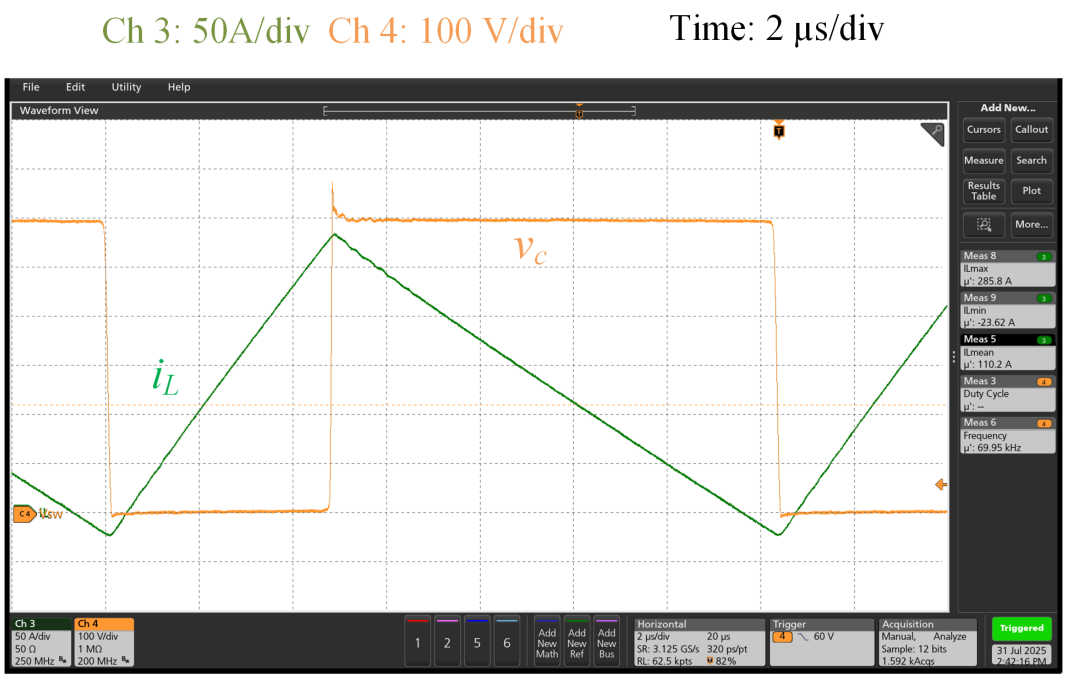


(a)

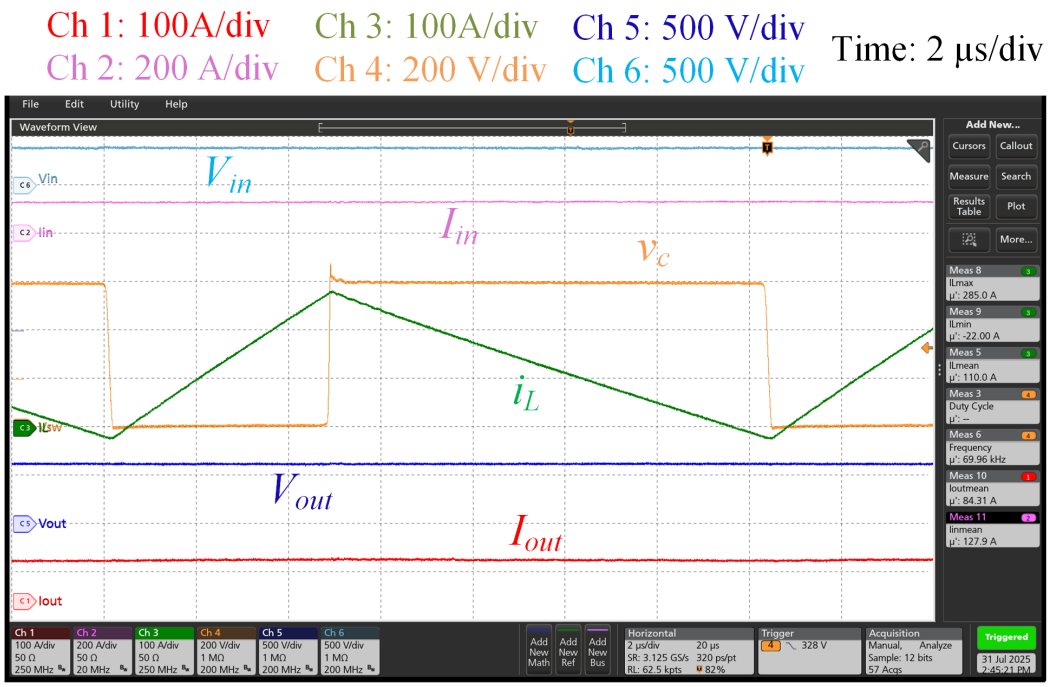


(b)

Fig. 4.22: (a) Hard Switching Waveforms for i_L and v_c. (b) Hard Switching Waveforms showing i_L, v_c, input and output voltages and currents.

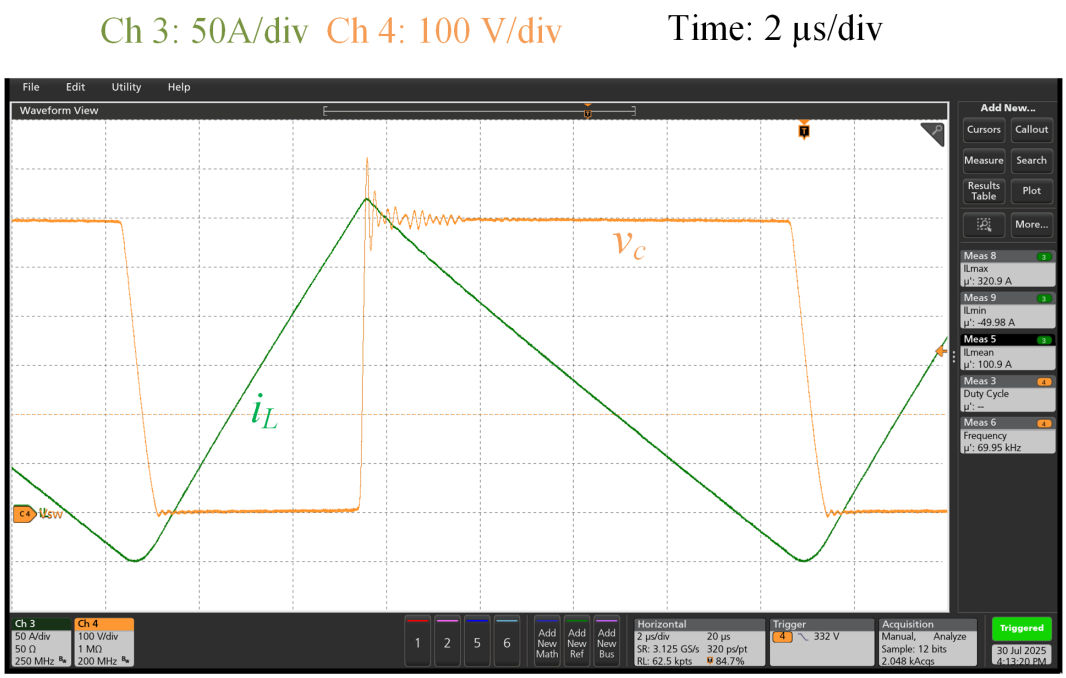


(a)

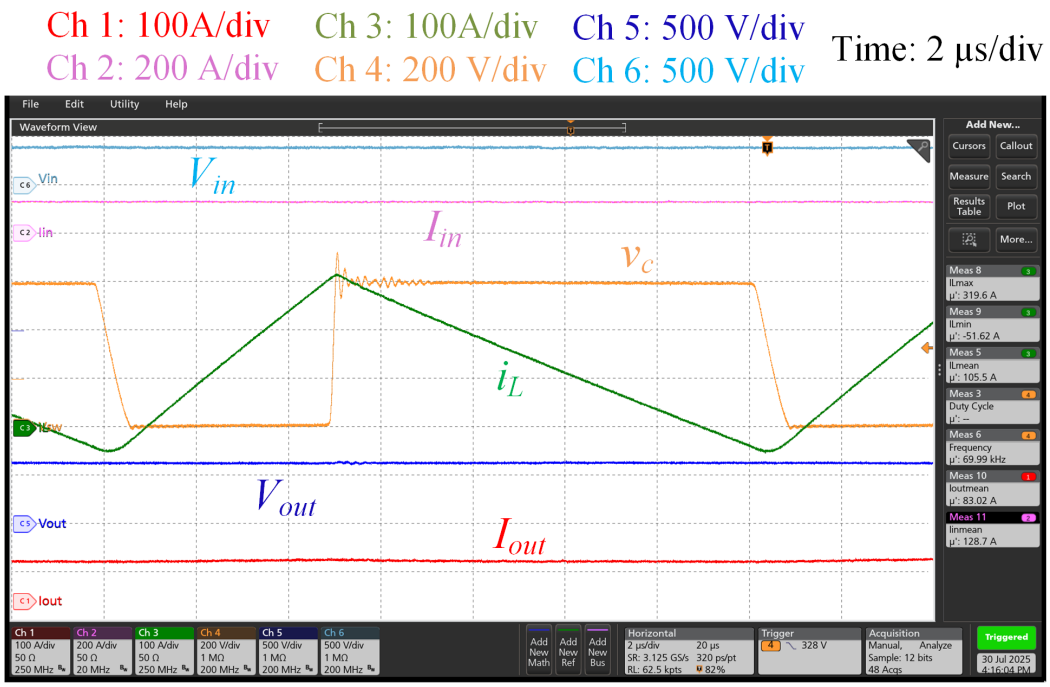


(b)

Fig. 4.23: (a) Soft Switching Waveforms with internal capacitance for i_L and v_c. (b) Soft Switching Waveforms with internal capacitance showing i_L, v_c, input and output voltages and currents.



(a)



(b)

Fig. 4.24: (a) Soft Switching Waveforms with external capacitance for i_L and v_c. (b) Soft Switching Waveforms with external capacitance showing i_L, v_c, input and output voltages and currents.

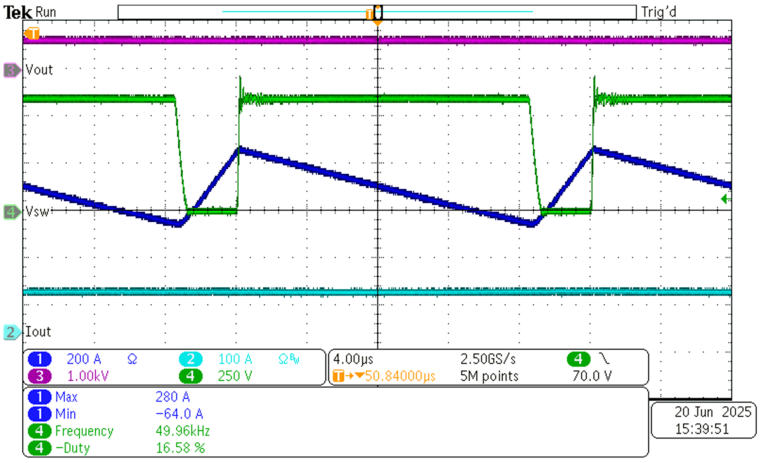


Fig. 4.25: ZVS restored at 50 kW at a conversion ratio of 0.16 at a switching frequency of 50 kHz. From top to bottom are the output voltage, switch node voltage, inductor current, and output current.

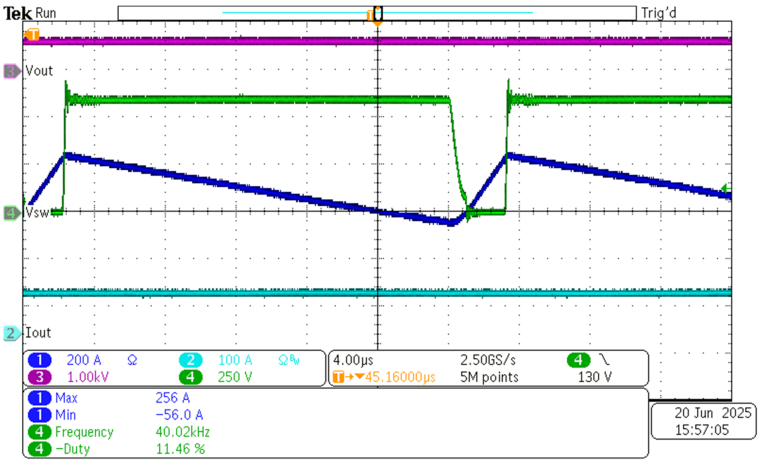


Fig. 4.26: ZVS restored at 50 kW at a conversion ratio of 0.11 at a switching frequency of 40 kHz. From top to bottom are the output voltage, switch node voltage, inductor current, and output current.

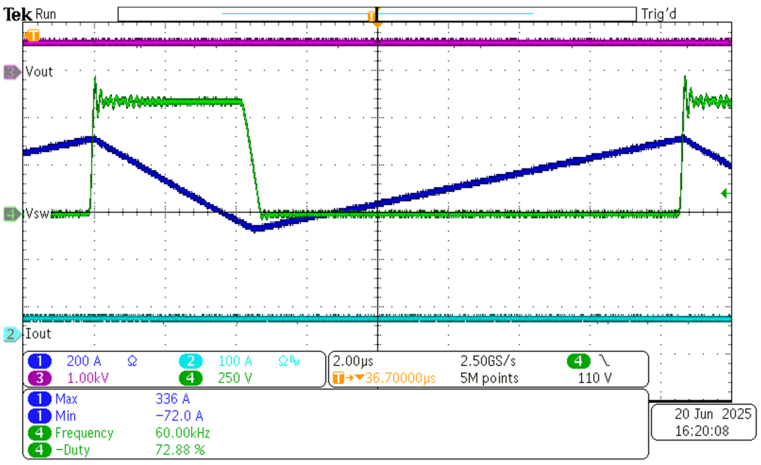


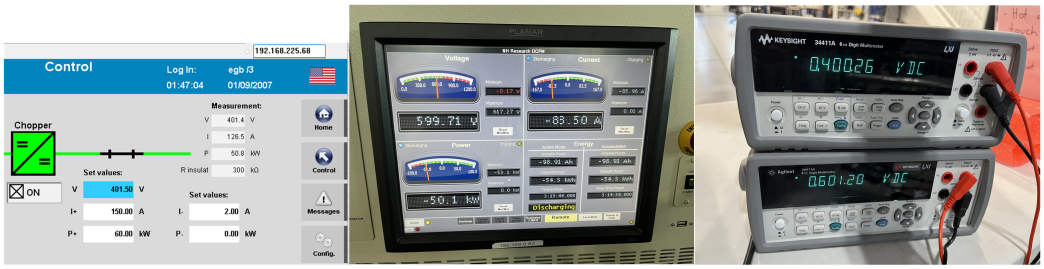
Fig. 4.27: ZVS restored at 20 kW at a conversion ratio of 0.73 at a switching frequency of 60 kHz. From top to bottom are the output voltage, switch node voltage, inductor current, and output current.

of the dc-dc converter. In Fig. 4.31, it can be seen that the losses for the ZVS-QSW converter with external capacitance have the minimum losses for almost the entire coupling coefficient range except 0.16, where it loses soft switching and goes into hard switching mode. An estimated breakdown of these losses at a conversion ratio of 0.33 or input current of 125 A and coupling of 0.2 for all three cases is shown in Table 4.9 and Table 4.8. It can be observed from these tables that the estimated total loss for soft switching with external capacitance and hard switching cases match very closely to the experimental results; there is some deviation in the estimated total loss for soft switching with internal capacitance cases as compared to the hardware results. This is due to the complexity in accurately measuring the inductor loss. However, it can be observed that the difference in module loss from estimated losses at a conversion ratio of 0.33 for soft switching with external capacitance and soft switching with internal capacitance is 119 W, and the difference in module loss from estimated losses for soft switching with external capacitance and hard switching is 176 W. This closely matches the hardware results at a conversion ratio of 0.33, where the difference in total loss for soft switching with external capacitance and soft switching with internal capacitance is 135 W, and the difference in total loss for soft switching with external capacitance and hard switching is 166 W. Fig. 4.28, Fig. 4.29, and Fig. 4.30 show

the readings from GK, NHR, and multimeters to verify the experimental losses at a conversion ratio of 0.33 at 50 kW. Table 4.10 shows the readings and calculated efficiency at a conversion ratio of 0.33 at 50 kW for three cases. A peak efficiency of 99.14% at 50 kW is observed for the ZVS-QSW converter with external capacitance. The soft switching range for the ZVS-QSW converter can be extended and restored by adjusting the switching frequency for these worst-case scenarios. Fig. 4.32 shows the restored ZVS comparisons where, at coupling of 0.16, switching frequency is adjusted to 50 kHz for all three cases, and at coupling of 0.15, the switching frequency is adjusted to 40 kHz for all three cases. Fig. 4.25 shows the waveforms for ZVS-QSW with external capacitance for restored ZVS at coupling of 0.16 or conversion ratio of 0.16 at 50 kW, and Fig. 4.26 shows the waveforms for ZVS-QSW with external capacitance for restored ZVS at coupling of 0.15 or conversion ratio of 0.11 at 50 kW. It can also be observed from Fig. 4.31 that the experimental losses at an input current of 125 A and conversion ratio of 0.33 show a similar trend for the three cases as observed from simulated losses in Table 4.2, where ZVS-QSW with external capacitance has the minimum losses. A similar trend of losses is observed in Fig. 4.33 and Fig. 4.34 for power levels of 40 kW and 30 kW, where ZVS-QSW with external capacitance has the minimum losses except at coupling of 0.15 in Fig. 4.34, where losses in hard switching are minimum due to increased rms currents for ZVS-QSW converter. Fig. 4.35 also shows a similar trend of losses except at coupling of 0.2, where the ZVS is lost for the ZVS-QSW converter with external capacitance. Fig. 4.36 shows the restored ZVS comparisons where switching frequency is adjusted for coupling of 0.2 to 60 kHz for all three cases. Fig. 4.27 shows the waveforms for ZVS-QSW with external capacitance for restored ZVS at coupling of 0.2 or conversion ratio of 0.73 at 20 kW.

Table 4.10: Exact Measurements at 50 kW for 3 cases.

Parameter	**ZVS-QSW External**	**ZVS-QSW Internal**	**Hard Switching**
V_{out}	601.2 V	600 V	600.96 V
V_{in}	400.26 V	400.77 V	401.7 V
I_{out}	83.5 A	83.35 A	83.51 A
I_{in}	126.5 A	126.2 A	126.4 A
μ	0.33	0.33	0.33
P_{out}	50.2 kW	50.01 kW	50.186 kW
Total Loss	432 W	567 W	598 W
Efficiency	99.14 %	98.87 %	98.82 %



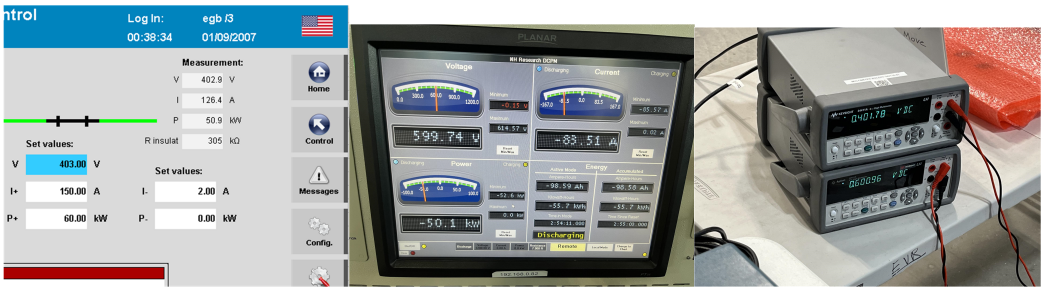
(a) (b) (c)

Fig. 4.28: Measurements at 50 kW for ZVS-QSW with external capacitance: (a) GK current measurement, (b) NHR current measurement, (c) Input and Output voltage measurements.



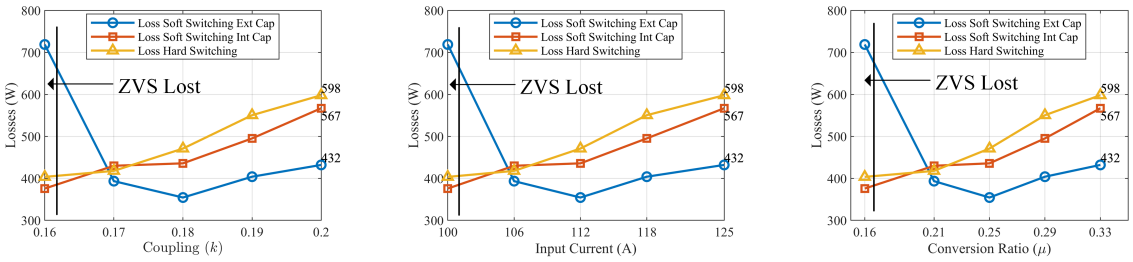
(a) (b) (c)

Fig. 4.29: Measurements at 50 kW for ZVS-QSW with internal capacitance: (a) GK current measurement, (b) NHR current measurement, (c) Input and Output voltage measurements.



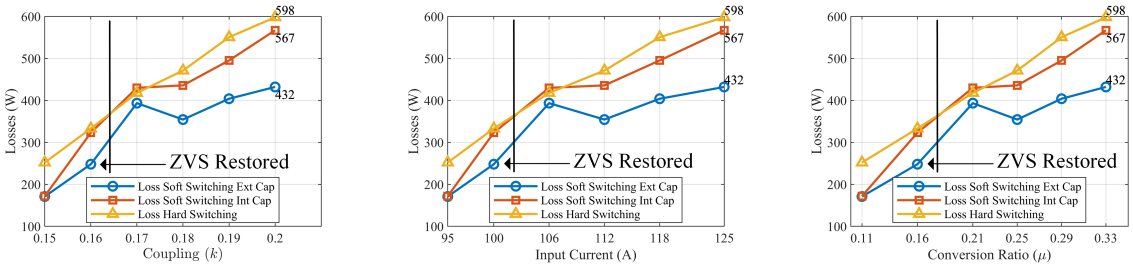
(a) (b) (c)

Fig. 4.30: Measurements at 50 kW for Hard switching converter: (a) GK current measurement, (b) NHR current measurement, (c) Input and Output voltage measurements.



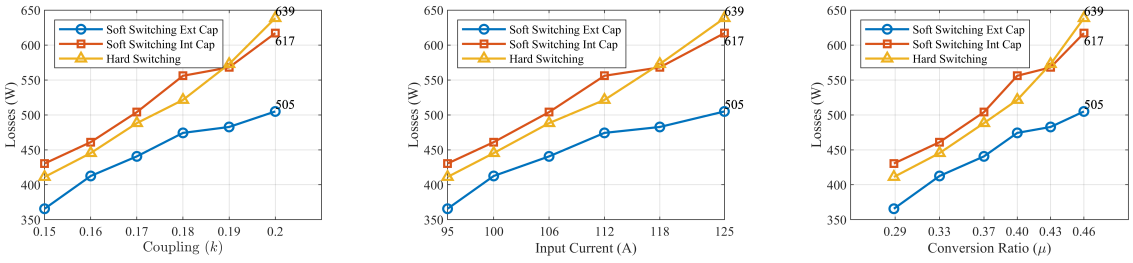
(a) (b) (c)

Fig. 4.31: Losses at 50 kW: (a) Losses vs coupling (k), (b) Losses vs Input Current (A), (c) Losses vs Conversion Ratio (μ).



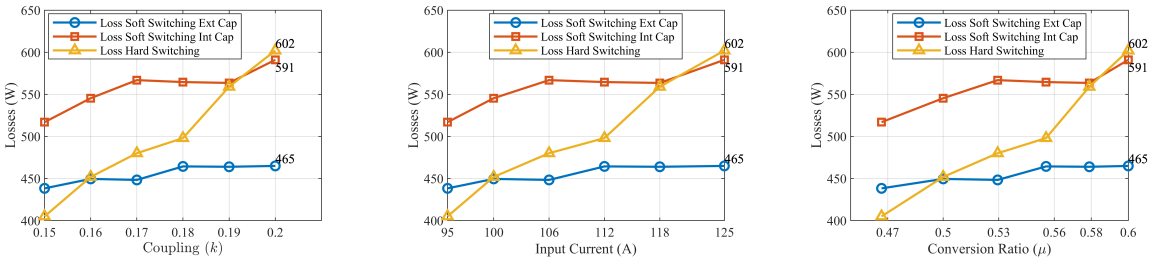
(a) (b) (c)

Fig. 4.32: Losses at 50 kW with ZVS restored: (a) Losses vs coupling (k), (b) Losses vs Input Current (A), (c) Losses vs Conversion Ratio (μ).



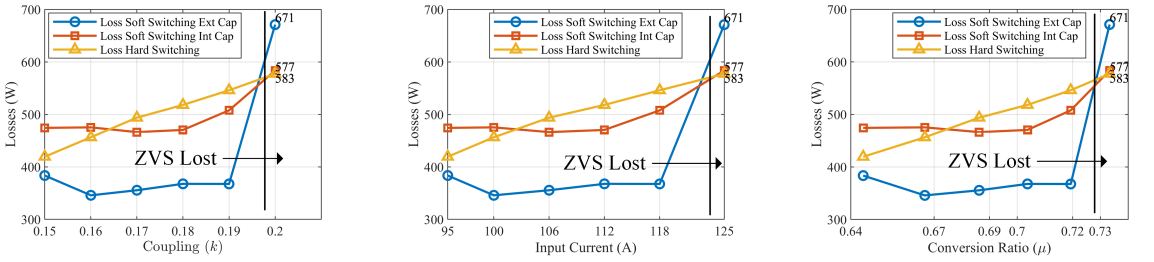
(a) (b) (c)

Fig. 4.33: Losses at 40 kW: (a) Losses vs coupling (k), (b) Losses vs Input Current (A), (c) Losses vs Conversion Ratio (μ).



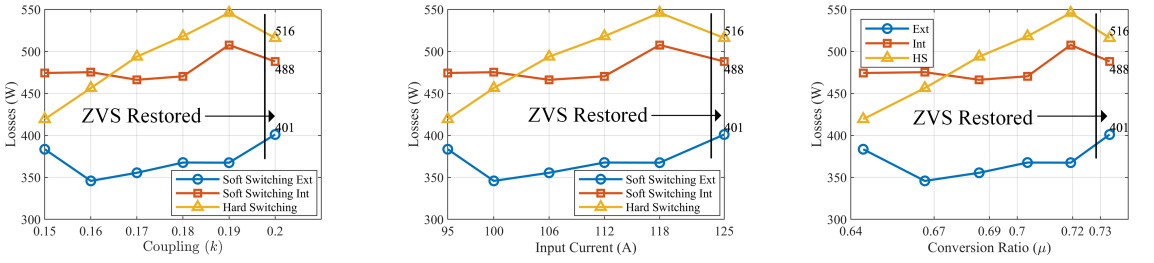
(a) (b) (c)

Fig. 4.34: Losses at 30 kW: (a) Losses vs coupling (k), (b) Losses vs Input Current (A), (c) Losses vs Conversion Ratio (μ).



(a) (b) (c)

Fig. 4.35: Losses at 20 kW: (a) Losses vs coupling (k), (b) Losses vs Input Current (A), (c) Losses vs Conversion Ratio (μ).



(a) (b) (c)

Fig. 4.36: Losses at 20 kW with ZVS restored: (a) Losses vs coupling (k), (b) Losses vs Input Current (A), (c) Losses vs Conversion Ratio (μ).

The EMI comparisons have also been done for two cases of soft-switching and hard-switching DC-DC converters. Fig. 4.37 shows the setup for measuring the EMI of all the cases of the DC-DC converter using a loop antenna. The distance of the loop antenna from the DC-DC converter setup is kept at 3 meters according to SAE J2954 standards for EMI testing. Fig. 4.38 shows the EMI comparison for three cases from 10 kHz to 30 MHz, and Fig. 4.39 shows the EMI comparison for three cases at the switching frequency of the DC-DC converter of 70 kHz. In Fig. 4.38, HS represents the EMI of a hard-switching DC-DC converter, Int represents the EMI of a soft-switching DC-DC converter with internal capacitance, Ext represents the EMI of a soft-switching DC-DC converter with external capacitance, and Amb represents the Ambient EMI with only power supplies on. It can be observed from Fig. 4.38 that for frequencies of 1 MHz - 4 MHz and 7 MHz - 30 MHz, the EMI magnitude is highest in the hard switching converter, followed by soft switching with internal capacitance, which is then followed by soft switching with external capacitance. It can also be observed that EMI magnitude for soft switching with external capacitance is highest for frequencies of 4 MHz - 7 MHz. This is due to the resonances observed in the soft-switching with external capacitance case between the external capacitance and parasitic inductances during turn-on and turn-off transitions. This can also be observed in Fig. 4.16, where the measured experimental resonance frequency lies in the 4 MHz - 7 MHz range. From Fig. 4.39, it can be observed that EMI magnitude for soft switching with external capacitance is highest at the switching frequency of the DC-DC converter, which is 70 kHz, followed by soft switching with internal capacitance, and then followed by hard switching DC-DC converter. In [83], the EMI comparison for soft switching quasi-resonant converters and hard switching converters is done, which also highlights the advantages of soft switching in the reduction of EMI at higher frequencies. To verify the trends of EMI for the three cases using the loop antenna, conducted EMI is measured using the Pearson 101 current transformer, which has a bandwidth of approximately 4 MHz. For the setup, the current sensor is used on the positive and negative polarity conductors of the input current bundled together to measure EMI. Fig. 4.40 shows the EMI comparison for three cases from

10 kHz to 4 MHz, and Fig. 4.41 shows the EMI comparison for three cases at the switching frequency of the DC-DC converter of 70 kHz. Similar trends are observed in Fig. 4.40 and Fig. 4.38 for frequencies of 1 MHz - 4 MHz, where the hard switching converter has the highest magnitude of EMI, followed by soft switching with internal capacitance, which is then followed by soft switching with external capacitance. Similar trends are also observed in Fig. 4.41 and Fig. 4.39 at a switching frequency of 70 kHz, where soft switching with external capacitance has the highest magnitude, followed by soft switching with internal capacitance, which is then followed by hard switching. Soft switching with an external capacitance case has the best EMI performance for frequencies of 1 MHz - 4 MHz and 7 MHz - 30 MHz, and worst performance at the switching frequency of the DC-DC converter, which is 70 kHz. On the contrary, the hard switching case has the best EMI performance at a switching frequency of the DC-DC converter, which is 70 kHz, and the worst EMI performance for frequencies of 1 MHz - 4 MHz and 7 MHz - 30 MHz.

Fig. 4.42 shows the thermal temperatures of a hard switching DC-DC converter, Fig. 4.43 shows the thermal temperatures of a soft switching DC-DC converter with internal capacitance, and Fig. 4.44 shows the thermal temperatures of a soft switching DC-DC converter with external capacitance. It can be observed from these figures that the soft switching DC-DC converter with external capacitance has the lowest module temperatures, which were also verified by the temperature readings from thermistors on the power modules. Higher temperatures were observed on the external capacitances and snubber resistors, which could be improved in future revisions by having more margin in the power ratings of the resistors.

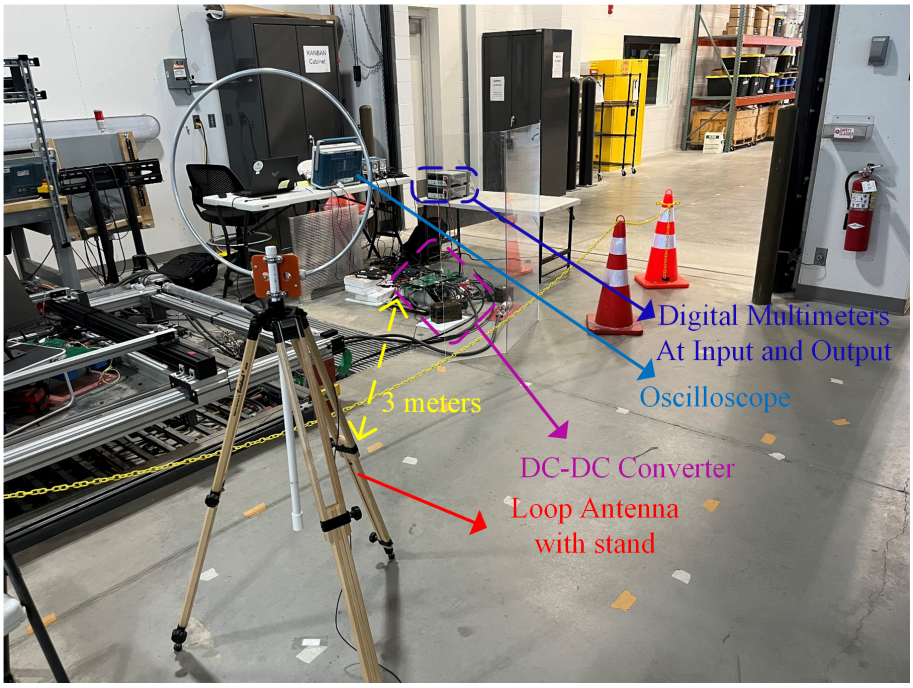


Fig. 4.37: Experimental setup for DC-DC converter for EMI Measurements.

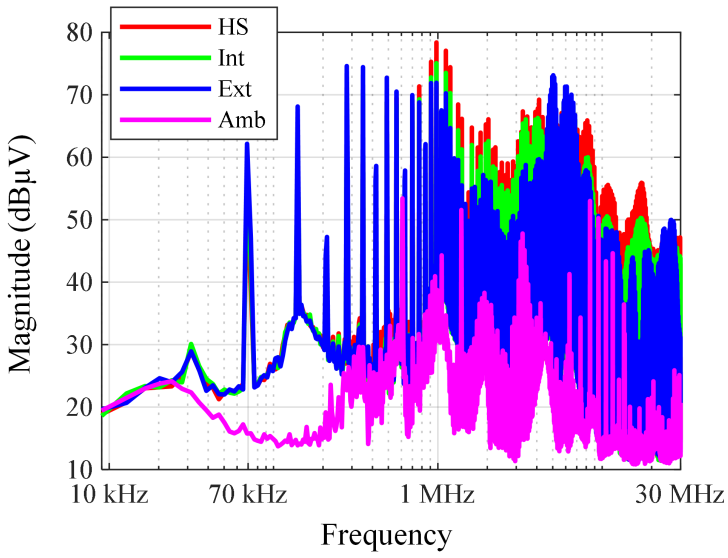


Fig. 4.38: EMI Comparisons using Loop Antenna.

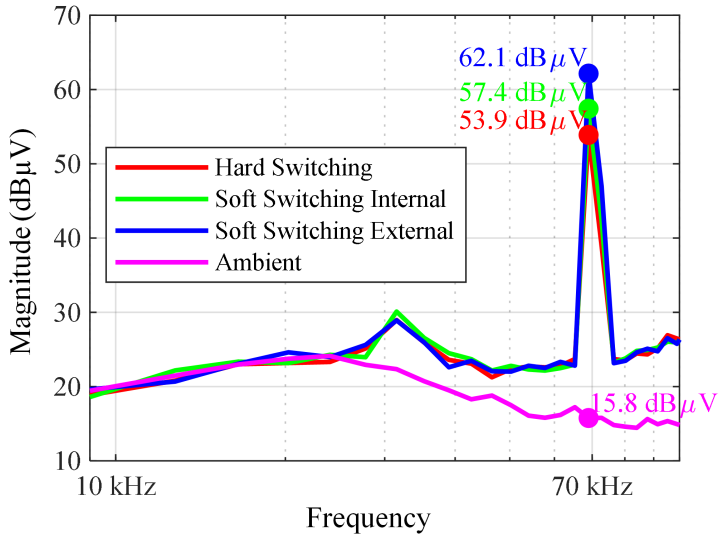


Fig. 4.39: EMI Comparison using Loop Antenna at 70 kHz.

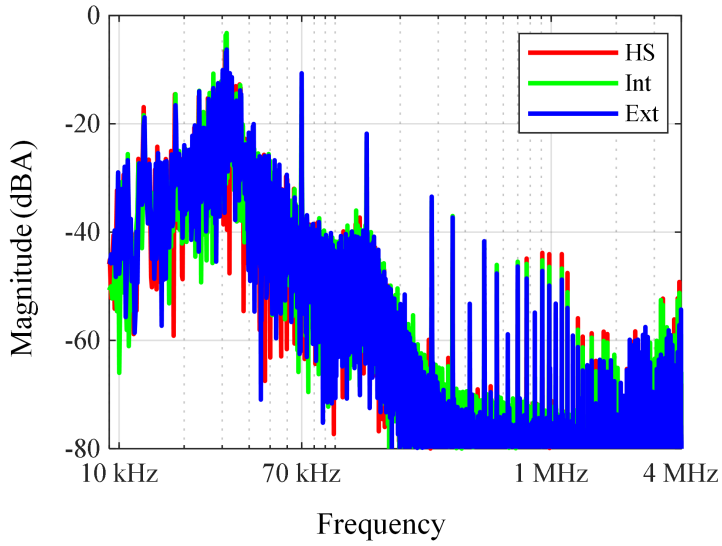


Fig. 4.40: EMI Comparisons using Pearson 101 current sensor.

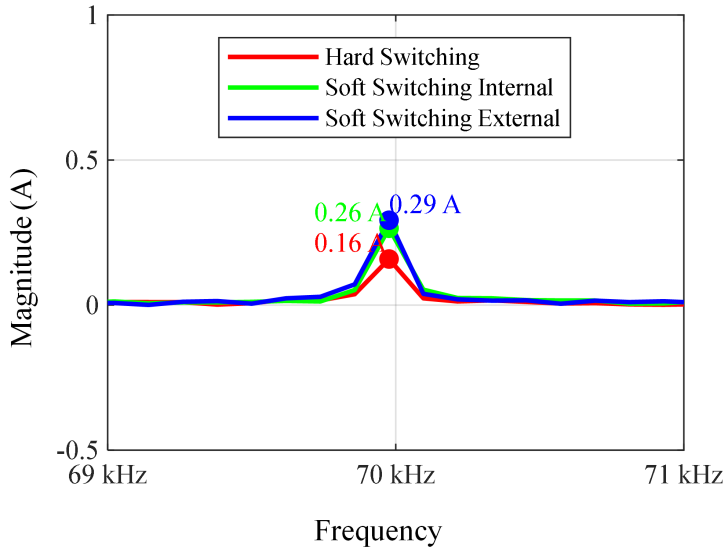


Fig. 4.41: EMI Comparison at 70 kHz using Pearson 101 current sensor.

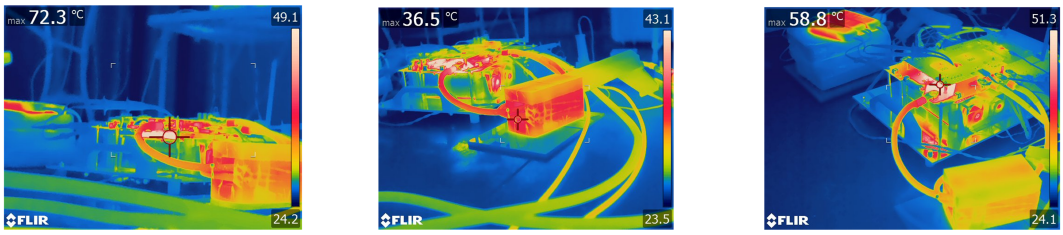


Fig. 4.42: Thermal image of Hard Switching DC-DC converter at 50 kW at input current of 125 A, showing module temperature at 72.3°C, inductor temperature at 36.5°C, and PCB temperature of switch node polygon pours at 58.8°C.

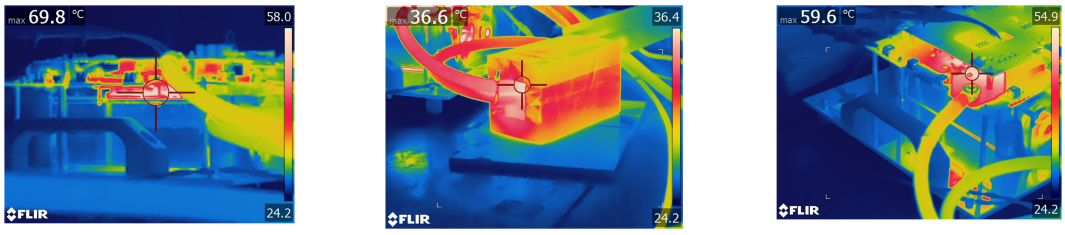


Fig. 4.43: Thermal image of DC-DC converter for soft switching with internal capacitance at 50 kW at input current of 125 A, showing module temperature at 69.8°C, inductor temperature at 36.6°C, and PCB temperature of switch node polygon pours at 59.6°C.

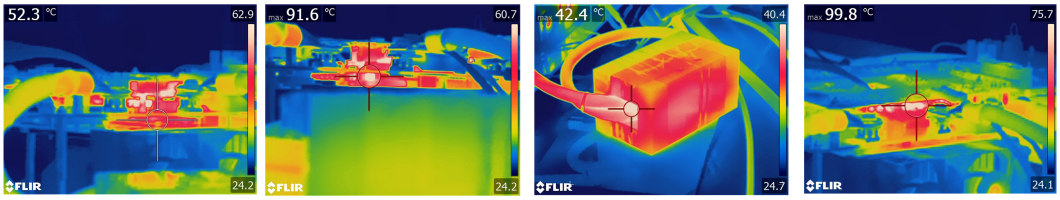


Fig. 4.44: Thermal image of DC-DC converter for soft switching with external capacitance at 50 kW at input current of 125 A, showing module temperature at 52.3°C, gate driver connector at 91.6°C, inductor temperature at 42.4°C and external capacitors and snubber resistors at 99.8°C.

4.6 Conclusion

This chapter proposes a soft switching design for DC-DC converters used in WPT systems. Design methodology for the ZVS-QSW DC-DC converter is developed for a double-sided LCC tuned WPT system. The soft switching is optimized for both turn-on and turn-off losses as compared to optimizing losses for only turn-on or only turn-off. With the proposed soft switching of the DC-DC converter, reduced losses are observed for almost the entire coupling coefficient range at 50 kW, 40 kW, 30 kW, and 20kW as compared with the conventional soft switching approach and hard switching approach for the DC-DC converter, which is verified by experimental results. The EMI comparisons are also done for all three cases, and it is observed that the proposed soft switching offers improved EMI performance at high switching frequencies. The thermal results for all three vases are also provided in this chapter.

CHAPTER 5

SYSTEM LEVEL CONTROL DESIGN FOR LCC-LCC TUNING

5.1 System Controls Description

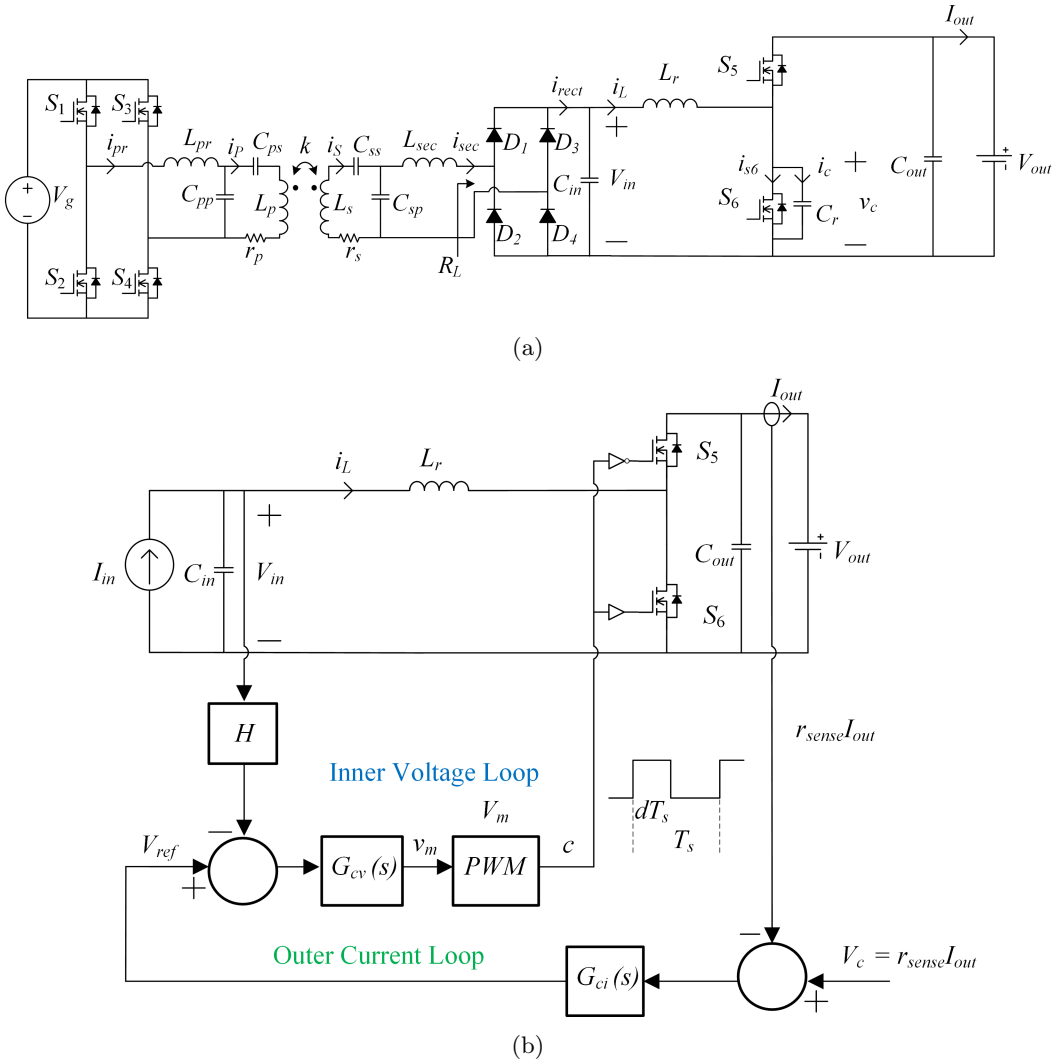


Fig. 5.1: WPT System with LCC-LCC tuning: (a) Full System with DC-DC converter, (b) Controls diagram.

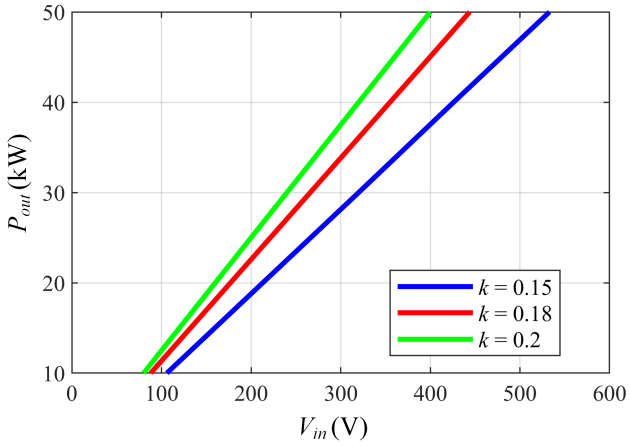


Fig. 5.2: Power Vs Voltage curves.

Fig. 5.1(a) shows the full WPT system with a ZVS-QSW DC-DC converter. Fig. 5.1(b) shows the control diagram of the DC-DC converter designed in Chapter 4. Section 4.1.1 gives a description of double-sided LCC tuning where the output power equation in terms of rectifier output voltage or V_{in} is shown in (5.1). Equations (5.2)-(5.5) represent the current source properties of double-sided LCC tuning, where $i_{sec_{rms}}$ is proportional to the open-circuit voltage V_{OC}, which is further dependent on coupling M and coupling k. The relationship between I_{rect} and $i_{sec_{rms}}$ is shown in (5.5), where I_{rect} is average value of current i_{rect}. Therefore, I_{rect} behaves as a current source that changes proportionally with a change in coupling. The rectifier output voltage V_{in} can be controlled to achieve power regulation. The P_{out} vs V_{in} curves for different couplings are shown in Fig. 5.2. From Fig. 5.2, it can be observed that for a constant power of 50 kW, if the coupling k decreases, I_{rect} decreases and therefore V_{in} can be increased proportionally to maintain constant power due to the current source properties of double-sided LCC tuning. For a constant coupling, power can also be regulated by the changing V_{in} depending on the power demanded by the battery of the vehicle, as shown in Fig. 5.2. For the inner loop control of the DC-DC converter, V_{in} is controlled using the duty cycle D of the Quasi Square Wave Boost Converter, where D is the control variable and the output is V_{in}. The reference for V_{in} or the inner loop comes from the outer loop. For the outer loop, V_{in} is the control variable and the output is the

battery current I_{out}.

$$P_{out} = \frac{V_{in}\omega M i_{P_{rms}} 2\sqrt{2}}{\omega L_{sec}\pi} \tag{5.1}$$

$$V_{OC} = \omega M i_{P_{rms}} \tag{5.2}$$

$$i_{P_{rms}} = \frac{4V_g}{\sqrt{2}\pi\omega L_{pr}} \tag{5.3}$$

$$i_{sec_{rms}} = \frac{V_{OC}}{\omega L_{sec}} \tag{5.4}$$

$$i_{sec_{rms}} = \frac{\pi I_{rect}}{2\sqrt{2}}. \tag{5.5}$$

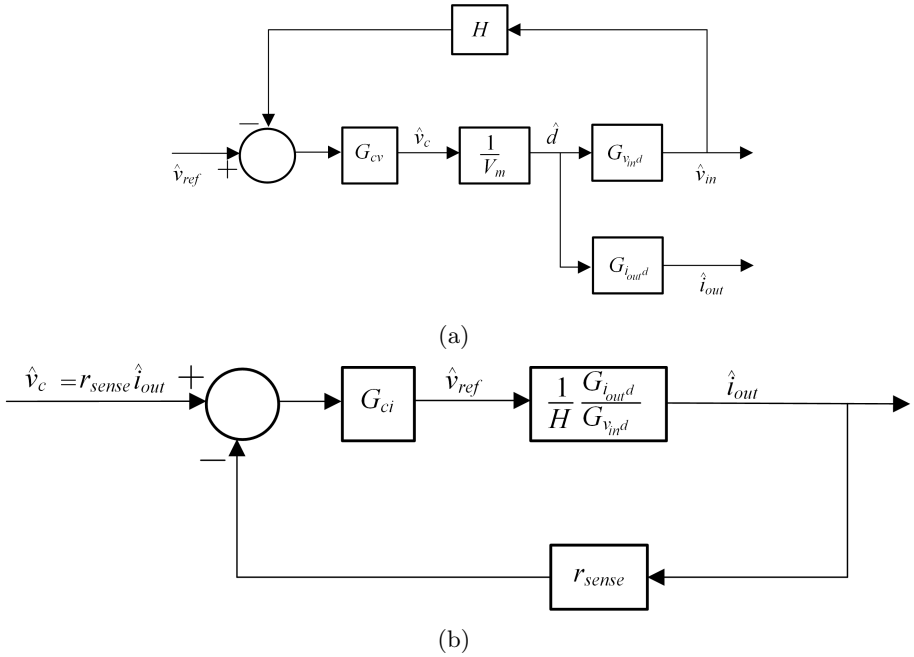


Fig. 5.3: Small Signal block diagrams for inner and outer loops: (a) Inner Loop, (b) Outer Loop.

Fig. 5.3 (a) shows the small signal diagram of inner-loop with G_{cv} as the compensator gain, $1/V_m$ as PWM gain, $G_{v_{in}d}$ is the control-to-output transfer function of the inner loop and H is the sensor gain of the voltage sensor and T_v given in (5.6), is the loop gain of the inner voltage loop. Fig. 5.3 (b) shows the small signal diagram of the outer-loop with G_{ci} as the compensator gain, r_{sense} is the sensor gain of the current sensor, and T_i is the loop gain of the outer current loop given in (5.7).

$$T_v = \frac{G_{cv} H G_{v_{in}d}}{V_m} \tag{5.6}$$

$$T_i = \frac{G_{ci} r_{sense}}{H} \frac{G_{i_{out}d}}{G_{v_{in}d}}. \tag{5.7}$$

5.2 Modeling of the Full System

5.2.1 Modeling of WPT System

To validate the current source properties of the double-sided LCC tuning, phasor modeling is used to model the impedance of the WPT system. The impedance model of the WPT system is then used to analyze the stability of the full system using Middlebrook's stability criteria using the extra element theorem [84].

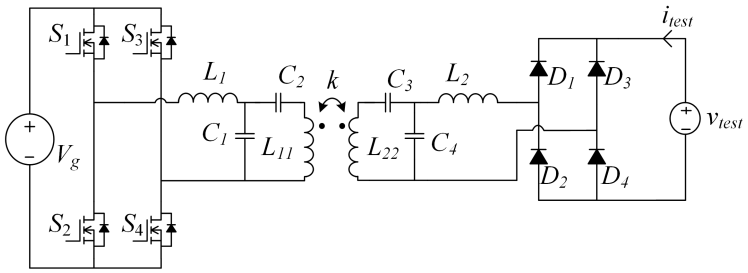


Fig. 5.4: Double-sided LCC tuning with test source at output.

Fig. 5.4 shows the WPT system with double-sided LCC tuning, where a voltage test source V_{test} is inserted at the output of the WPT system to analyze the impedance of the WPT system.

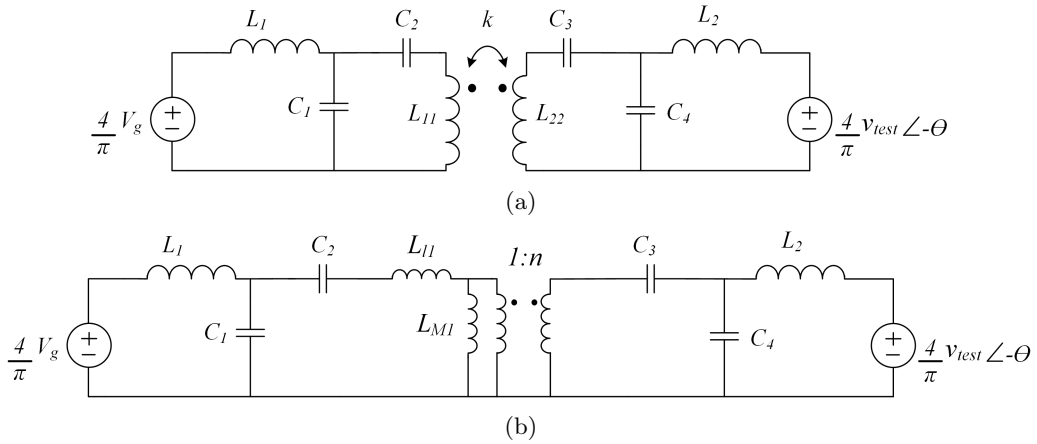


Fig. 5.5: WPT System with test source using sinusoidal approximation: (a) Equivalent Circuit, (b) Equivalent circuit with transformer model.

$$L_{l1} = (1 - k^2)L_{11} \tag{5.8}$$

$$L_{M1} = k^2 L_{11} \tag{5.9}$$

$$n = \frac{1}{k}\sqrt{\frac{L_{22}}{L_{11}}}. \tag{5.10}$$

Fig. 5.5 (a) shows the equivalent circuit of double-sided LCC tuning using sinusoidal approximation [84], which models both the inverter and the rectifier circuits. $4/\pi V_g$ and $4/\pi v_{test}$ are the peak values of the fundamental component of the output voltage of the inverter and input voltage of the rectifier, respectively. Fig. 5.5(b) shows the equivalent circuit with transformer model of the WPT system where L_{l1}, L_{M1}, and n are given in equations (5.8), (5.9), and (5.10). In Fig. 5.6, to find the impedance of the WPT system, the input is shorted, and the voltage test source is considered as the reference. i_R is the current obtained after the rectifier circuit is modeled using sinusoidal approximation, and i_R is given in (5.11), in terms of i_{test}.

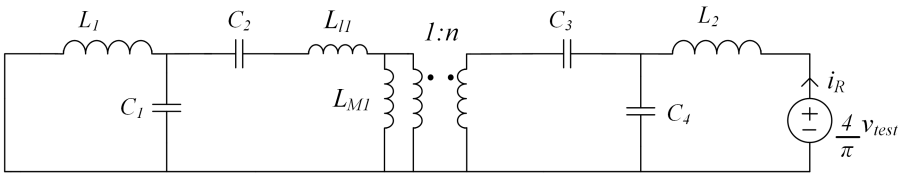


Fig. 5.6: Double-sided LCC tuning with test source and input shorted.

$$i_R = \frac{\pi}{2} i_{test} \tag{5.11}$$

The generalized phasor is given in (5.12), where $\underline{v}(t)$ is the phasor signal represented with an underbar. The small signal and DC quantity of any signal v is represented as $V + \hat{v}$, where the capital letter of the signal example V is represented as the DC quantity and the small signal quantity is denoted with a hat on the signal, such as $\hat{v}$.

$$\underline{v}(t) = Re(\underline{v}(t)e^{j\varphi(t)}) \tag{5.12}$$

For the derivation of envelope of the quantity $\underline{v}(t)$, that is $||\underline{\hat{v}}||$, the following equations from (5.13)-(5.18), are derived. In the derivations, the complex conjugate of any quantity v is denoted as v^* and the magnitude of any quantity v is denoted as $||v||$.

$$||\underline{v}|| = ||\underline{V} + \underline{\hat{v}}|| \tag{5.13}$$

$$||\underline{v}|| = \sqrt{(\underline{V} + \underline{\hat{v}})(\underline{V}^* + \underline{\hat{v}}^*)} \tag{5.14}$$

$$||\underline{v}|| = \sqrt{||\underline{V}||^2 + \underline{V}.\underline{\hat{v}}^* + \underline{V}^*.\underline{\hat{v}} + \underline{\hat{v}}.\underline{\hat{v}}^*} \tag{5.15}$$

Linearizing the above equation (5.15), we get the equation .

$$||\underline{V} + \underline{\hat{v}}|| = ||\underline{V}|| + \frac{\underline{V}.\underline{\hat{v}}^* + \underline{V}^*.\underline{\hat{v}}}{2||\underline{V}||} \tag{5.16}$$

The envolope of the quantity $\underline{v}$ that is $||\underline{\hat{v}}||$ is given in equations (5.17),(5.18) and (5.19), where the real part of any complex quantity v is denoted as $Re(v)$ and the imaginary part the real part of any complex quantity v is denoted as $Im(v)$.

$$||\underline{\hat{v}}|| = \frac{\underline{V}.\underline{\hat{v}}^* + \underline{V}^*.\underline{\hat{v}}}{2||V||} \tag{5.17}$$

$$||\underline{\hat{v}}|| = \frac{Re(\underline{\hat{v}})Re(\underline{V}) + Im(\underline{\hat{v}})Im(\underline{V})}{||\underline{V}||} \tag{5.18}$$

$$||\underline{\hat{v}}|| = \frac{Re(\underline{\hat{v}})Re(\underline{V}) + Im(\underline{\hat{v}})Im(\underline{V})}{\sqrt{Re(\underline{V})^2 + Im(\underline{V})^2}}. \tag{5.19}$$

The phasor transformed small signal model for Fig. 5.6 is shown in Fig. 5.7 which shows the phasors $\underline{\hat{v}}_{test}$ and $\underline{\hat{i}}_R$. Fig. 5.7 (b) shows the phasor transformed model referred to

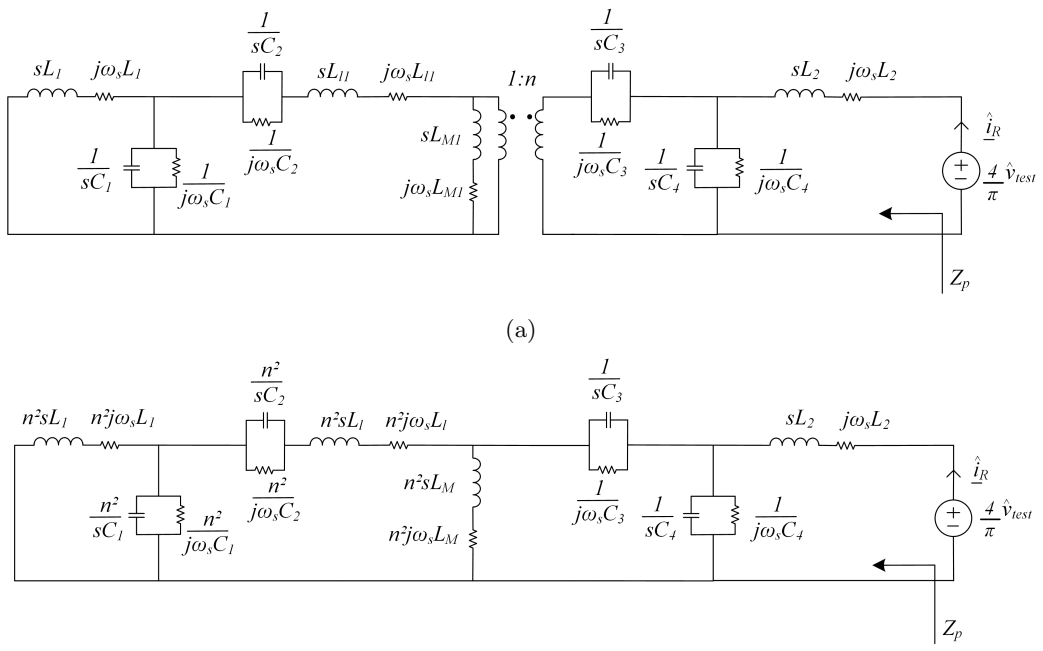


Fig. 5.7: Double-sided LCC with test source (a) phasor transformed small signal model, (b) phasor transformed small signal model referred to the secondary side of the WPT system.

the secondary for analysis of impedance. All the inductances and capacitances are modeled using the phasor transform. From the rectifier circuit model using sinusoidal approximation given in (5.11), and the envelope of any phasor given in (5.19), the envelope of phasor $\hat{\underline{i}}_R$ is given in (5.20), and (5.21).

$$||\hat{\underline{i}}_R|| = \frac{\pi}{2}\hat{i}_{test} \tag{5.20}$$

$$||\hat{\underline{i}}_R|| = \frac{Re(\hat{\underline{i}}_R)Re(\underline{I}_R) + Im(\hat{\underline{i}}_R)Im(\underline{I}_R)}{\sqrt{Re(\underline{I}_R)^2 + Im(\underline{I}_R)^2}} \tag{5.21}$$

Also,

$$\hat{\underline{i}}_R = \frac{4}{\pi}\frac{\hat{v}_{test}}{Z_p} \tag{5.22}$$

Rearranging the above three equations gives the impedance output impedance Z of the WPT system.

$$\frac{\pi}{2}\hat{i}_{test} = \frac{\left[Re(\frac{1}{Z_p})Re(\underline{I}_R) + Im(\frac{1}{Z_p})Im(\underline{I}_R)\right]\frac{4}{\pi}\hat{v}_{test}}{\sqrt{Re(\underline{I}_R)^2 + Im(\underline{I}_R)^2}} \tag{5.23}$$

$$\frac{\hat{v}_{test}}{\hat{i}_{test}} = \frac{\pi^2}{8}\frac{\sqrt{Re(\underline{I}_R)^2 + Im(\underline{I}_R)^2}}{\left[Re(\frac{1}{Z_p})Re(\underline{I}_R) + Im(\frac{1}{Z_p})Im(\underline{I}_R)\right]} \tag{5.24}$$

$$Z = \frac{\pi^2}{8}\frac{\sqrt{Re(\underline{I}_R)^2 + Im(\underline{I}_R)^2}}{\left[Re(\frac{1}{Z_p})Re(\underline{I}_R) + Im(\frac{1}{Z_p})Im(\underline{I}_R)\right]} \tag{5.25}$$

To solve the impedance Z, the impedances in Fig. 5.7 are simplified as follows,

$$Z_{1p} = n^2 sL_1 + n^2 j\omega_s L_1 \tag{5.26}$$

$$Z_{2p} = \frac{n^2}{sC_1} || \frac{n^2}{j\omega_s C_1} \tag{5.27}$$

$$Z_{3p} = \frac{n^2}{sC_2} || \frac{n^2}{j\omega_s C_2} + n^2 sL_{l1} + n^2 j\omega_s L_{l1} \tag{5.28}$$

$$Z_{4p} = n^2 sL_{M1} + n^2 j\omega_s L_{M1} \tag{5.29}$$

$$Z_{5p} = \frac{1}{sC_3} || \frac{1}{j\omega_s C_3} \tag{5.30}$$

$$Z_{6p} = \frac{1}{sC_4} || \frac{1}{j\omega_s C_4} \tag{5.31}$$

$$Z_{7p} = sL_2 + j\omega_s L_2 \tag{5.32}$$

$$Z_p = \left[\left(Z_{1p}||Z_{2p} + Z_{3p}\right)||Z_{4p} + Z_{5p}\right]||Z_{6p} + Z_{7p}. \tag{5.33}$$

The phasor transformed steady state model is shown in Fig. 5.8, which is used to find the value of $\underline{I}_R$, the steady state value of current $\underline{i}_R$. To calculate $\underline{I}_R$ in Fig. 5.8, superposition of two voltage sources $\frac{4}{\pi}nV_g$ and $\frac{4}{\pi}V_{in}\angle -\theta$ is considered. The two currents $\underline{I}_{R1}$ and $\underline{I}_{R2}$ are subtracted to calculate the value of $\underline{I}_R$.

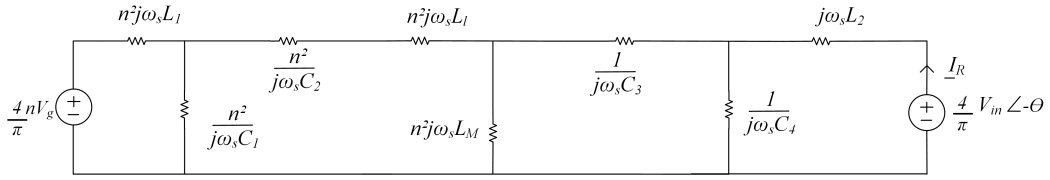


Fig. 5.8: Double-sided LCC phasor-transformed model in steady state referred to the secondary.

$$Z_{1ps} = n^2 j\omega_s L_1 \tag{5.34}$$

$$Z_{2ps} = \frac{n^2}{j\omega_s C_1} \tag{5.35}$$

$$Z_{3ps} = \frac{n^2}{j\omega_s C_2} + n^2 j\omega_s L_{l1} \tag{5.36}$$

$$Z_{4ps} = n^2 j\omega_s L_{M1} \tag{5.37}$$

$$Z_{5ps} = \frac{1}{j\omega_s C_3} \tag{5.38}$$

$$Z_{6ps} = \frac{1}{j\omega_s C_4} \tag{5.39}$$

$$Z_{7ps} = j\omega_s L_2 \tag{5.40}$$

$$Z_{ins} = \big[\big(Z_{1ps}||Z_{2ps} + Z_{3ps}\big)||Z_{4ps} + Z_{5ps}\big]||Z_{6ps} + Z_{7ps} \tag{5.41}$$

$$Z_{gs} = \big[\big(Z_{7ps}||Z_{6ps} + Z_{5ps}\big)||Z_{4ps} + Z_{3ps}\big]||Z_{2ps} + Z_{1ps} \tag{5.42}$$

$$\underline{I}_{R1} = \frac{4}{\pi}\frac{V_{in}\angle -\theta}{Z_{ins}} \tag{5.43}$$

$$\underline{I}_{R2} = \frac{4}{\pi}\frac{nV_g}{Z_{gs}} \tag{5.44}$$

$$\underline{I}_R = \underline{I}_{R1} - \underline{I}_{R2}. \tag{5.45}$$

5.2.2 Stability of the system

The stability of the system is analyzed using Middlebrook's extra element theorem [84], where the impedance of the WPT system is considered as an extra element and the effect of this impedance is used to find the corrected or new transfer functions for the dc-dc converter. The expressions of the corrected $G_{v_{in}d}$ and G_{id} are analyzed using the extra element theorem when the impedance Z of the WPT system is open or tends to ∞. Fig. 5.9 shows the averaged model of the DC-DC boost converter for analyzing the Z_N and Z_D impedances and the stability criteria for the WPT system with a DC-DC converter.

First, the expressions of the corrected $G_{v_{in}d}$ are analyzed using Middlebrook's extra element theorem. The corrected $G_{v_{in}d}$ with the impedance Z of the WPT system is given in (5.46), where $G_{v_{in}d}|Z \to \infty$ is the $Gv_{in}d$ is the old $G_{v_{in}d}$ if there is no Z or the extra element given in (5.47). The impedances Z_N and Z_D are given in equations (5.48), and (5.49) respectively. In Fig. 5.10, the circuit diagrams for analyzing Z_N and Z_D are given with the test source. It can be observed from Fig. 5.10(a), when $\hat{v}in \to 0$, the Z_N is 0. Also, from Fig. 5.10(b), Z_D is calculated when $\hat{d} = 0$. The Z_N and Z_D calculated for $Gv_{in}d$ are given in equations (5.50), and (5.51) respectively, where $||$ represents two impedances in parallel.

$$G_{v_{in}d} = \left(G_{v_{in}d}\big|_{Z\to\infty}\right)\left[\frac{1+\frac{Z_N}{Z}}{1+\frac{Z_D}{Z}}\right] \tag{5.46}$$

$$G_{v_{in}d}\big|_{Z\to\infty} = \frac{\hat{v}_{in}}{\hat{d}} \tag{5.47}$$

$$Z_N = \left.\frac{\hat{V}_{test}}{\hat{I}_{test}}\right|_{\hat{v}_{in}\to 0} \tag{5.48}$$

$$Z_D = \left.\frac{\hat{V}_{test}}{\hat{I}_{test}}\right|_{\hat{d}=0} \tag{5.49}$$

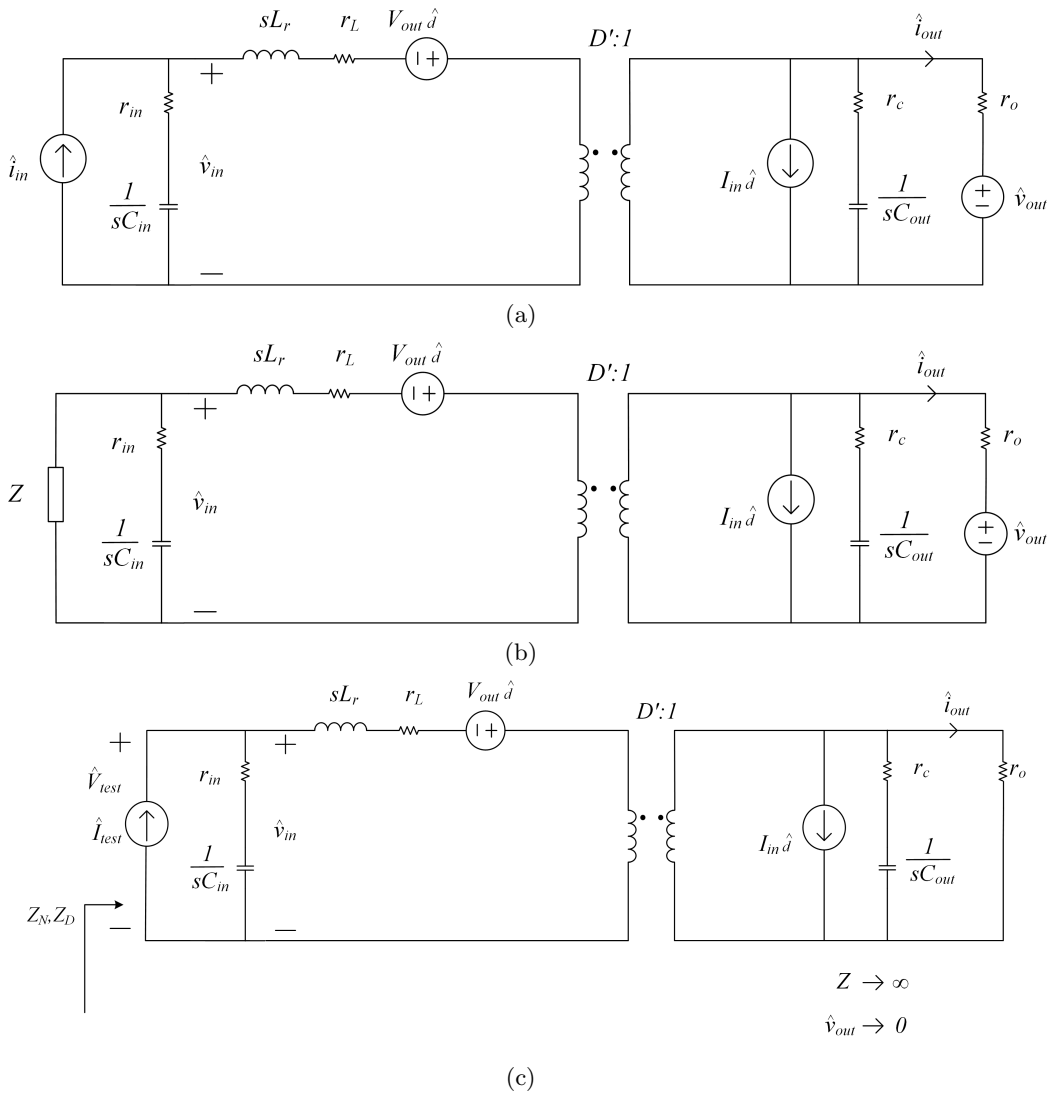


Fig. 5.9: Averaged model of DC-DC converter (a) With current source input, (b) With impedance Z of the WPT system, (c) With test source and impedances Z_N and Z_D.

$$Z_N = 0 \tag{5.50}$$

$$Z_D = \Big(r_{in} + \frac{1}{sC_{in}}\Big) || \Bigg[\Big(r_L + sL\Big) + \Big[\Big(r_o || \Big(r_c + \frac{1}{sC_{out}}\Big)\Big)(D')^2 \Big] \Bigg]. \tag{5.51}$$

Second, the expression of the corrected $G_{i_{out}d}$ is analyzed using Middlebrook's extra element theorem [84]. The corrected $G_{i_{out}d}$ with the impedance Z of the WPT system is

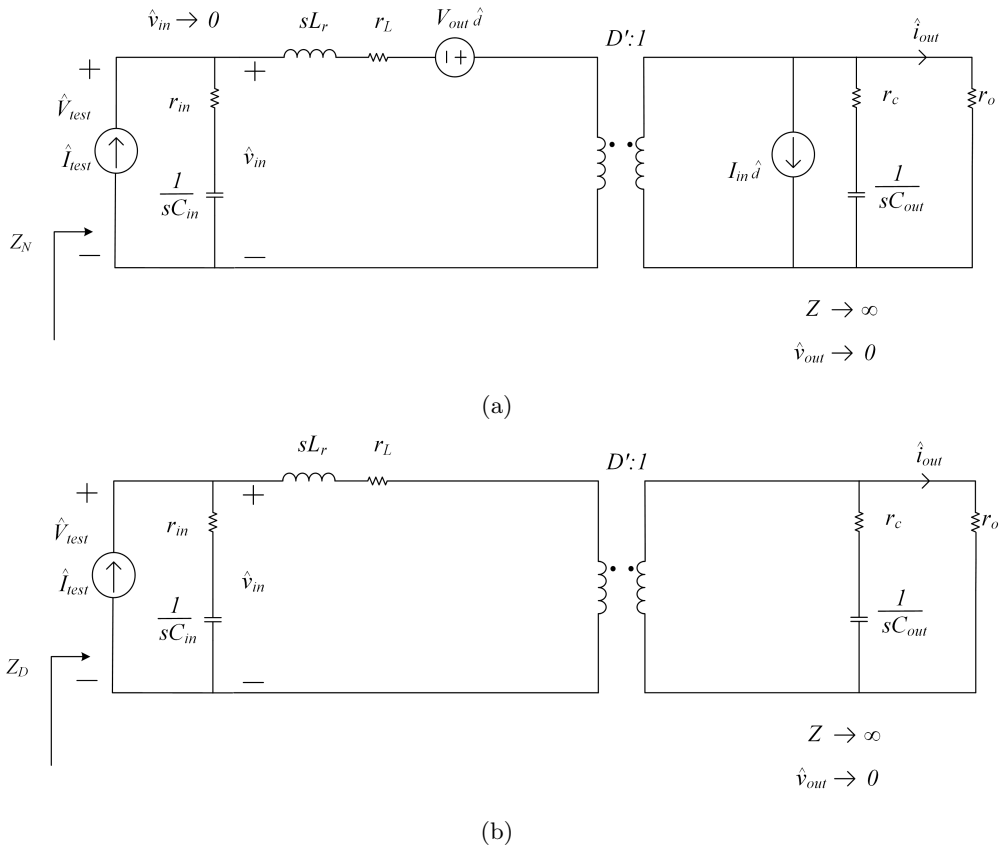


Fig. 5.10: Averaged model of DC-DC converter for impedance analysis of $G_{v_{in}d}$ (a) For Analysis of Z_N, (b) For Analysis of Z_D.

given in (5.52), where $G_{i_{out}d}|Z \to \infty$ is the $Gi_{out}d$ is the old $G_{i_{out}d}$ if there is no Z or the extra element given in (5.53). The impedances Z_N and Z_D are given in equations (5.54), and (5.55) respectively. In Fig. 5.11, the circuit diagrams for analyzing Z_N and Z_D are given with the test source. It can be observed from Fig. 5.11(a), when $\hat{i}out \to 0$, the Z_N is calculated. Also, from Fig. 5.11(b), Z_D is calculated when $\hat{d} = 0.Z_D$ calculated for $Gi_{out}d$ is given in equation (5.56), where || represents two impedances in parallel.

$$G_{i_{out}d} = \left(G_{i_{out}d}\big|_{Z\to\infty}\right)\left[\frac{1+\frac{Z_N}{Z}}{1+\frac{Z_D}{Z}}\right] \tag{5.52}$$

$$G_{i_{out}d}\big|_{Z\to\infty} = \frac{\hat{i}_{out}}{\hat{d}} \tag{5.53}$$

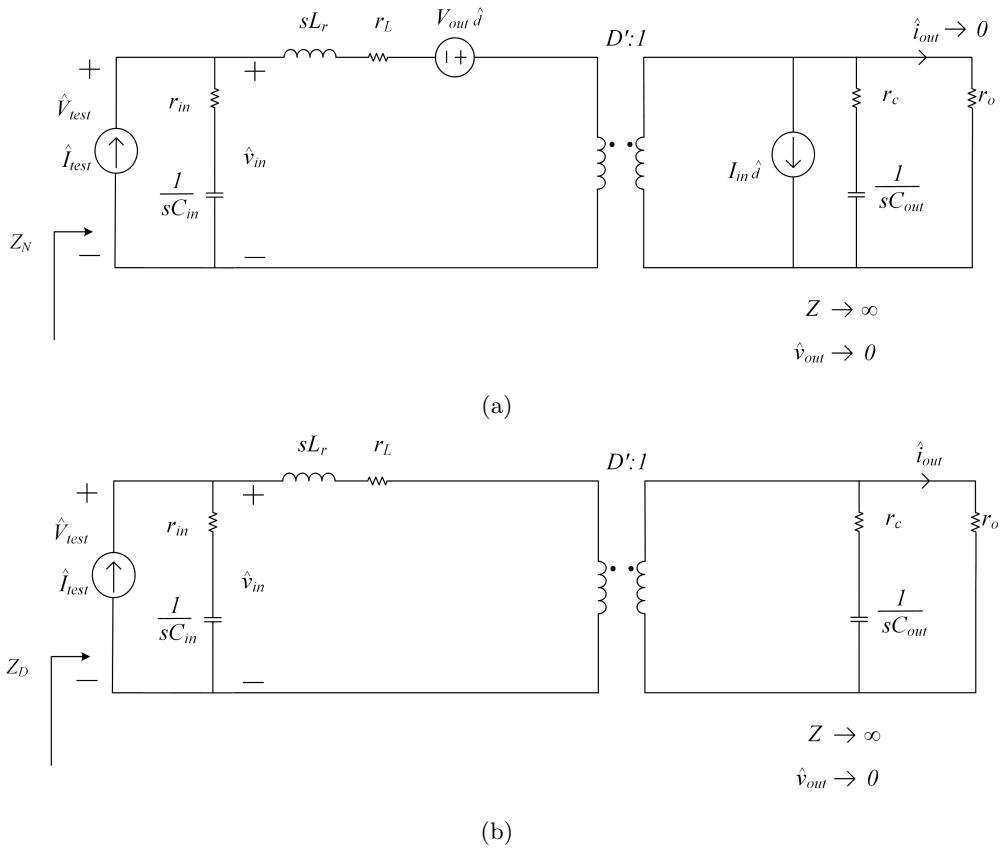


Fig. 5.11: Averaged model of DC-DC converter for impedance analysis of $G_{i_{out}d}$ (a) For analysis of Z_N (b) For analysis of Z_D.

$$Z_N = \left.\frac{\hat{V}_{test}}{\hat{I}_{test}}\right|_{\hat{i}_{out}\to 0} \tag{5.54}$$

$$Z_D = \left.\frac{\hat{V}_{test}}{\hat{I}_{test}}\right|_{\hat{d}=0} \tag{5.55}$$

$$Z_D = \left(r_{in} + \frac{1}{sC_{in}}\right) || \left[\left(r_L + sL\right) + \left[\left(r_o || \left(r_c + \frac{1}{sC_{out}}\right)\right)(D')^2\right]\right]. \tag{5.56}$$

For calculation of Z_N from Fig. 5.11(a), equations from (5.57)-(5.62), are analyzed to find the Z_N impedance. The Z_N impedance is given in (5.63).

$$\hat{V}_{test} - r_L\frac{I_{in}\hat{d}}{D'} - sL\frac{I_{in}\hat{d}}{D'} + V_{out}\hat{d} = 0 \tag{5.57}$$

$$\left(\hat{I}_{test} - \frac{I_{in}\hat{d}}{D'}\right)\left(\frac{1}{sC_{in}} + r_{in}\right) = \hat{V}_{test} \tag{5.58}$$

$$\hat{I}_{test}\left(\frac{1 + sr_{in}C_{in}}{sC_{in}}\right) = \hat{V}_{test} + \frac{I_{in}\hat{d}}{D'}\left(\frac{1 + sr_{in}C_{in}}{sC_{in}}\right) \tag{5.59}$$

$$\hat{I}_{test}\left(\frac{1 + sr_{in}C_{in}}{sC_{in}}\right) = \hat{V}_{test} + \left[\frac{I_{in}}{D'}\left(\frac{1 + sr_{in}C_{in}}{sC_{in}}\right)\left(\frac{D'}{I_{in}r_L + sLI_{in} - V_{out}D'}\right)\right]\hat{V}_{test} \tag{5.60}$$

$$\hat{I}_{test}\left(\frac{1 + sr_{in}C_{in}}{sC_{in}}\right) = \left[\frac{sC_{in}(I_{in}r_L + sLI_{in} - V_{out}D') + I_{in} + sI_{in}r_{in}C_{in}}{sC_{in}(I_{in}r_L + sLI_{in} - V_{out}D')}\right]\hat{V}_{test} \tag{5.61}$$

$$\frac{\hat{V}_{test}}{\hat{I}_{test}} = \frac{(1 + sr_{in}C_{in})(I_{in}r_L + sLI_{in} - V_{out}D')}{sC_{in}(I_{in}r_L + sLI_{in} - V_{out}D') + I_{in} + sI_{in}r_{in}C_{in}} \tag{5.62}$$

$$Z_N = \frac{(1 + sr_{in}C_{in})(I_{in}r_L + sLI_{in} - V_{out}D')}{sC_{in}(I_{in}r_L + sLI_{in} - V_{out}D') + I_{in} + sI_{in}r_{in}C_{in}}. \tag{5.63}$$

5.2.3 State Space Representation

Fig. 5.12(a) shows the state space diagram of the Quasi square wave boost converter having two positions of the switch, 1 and 0. Fig. 5.12(b) shows the state space diagram of the ZVS-QSW boost converter when the switch is in position 1. Fig. 5.12(c) shows the state space diagram of the ZVS-QSW boost converter when the switch is in position 0. The capacitor voltages and inductor currents in Fig. 5.12 are considered to be the states of the system. The inputs and outputs of the system are also defined to derive the state space model of the DC-DC converter. The states are denoted by $x(t)$, inputs by $v(t)$, and outputs of the system by $y(t)$.

$$\frac{dx(t)}{dt} = A_p x(t) + B_p v(t) \tag{5.64}$$

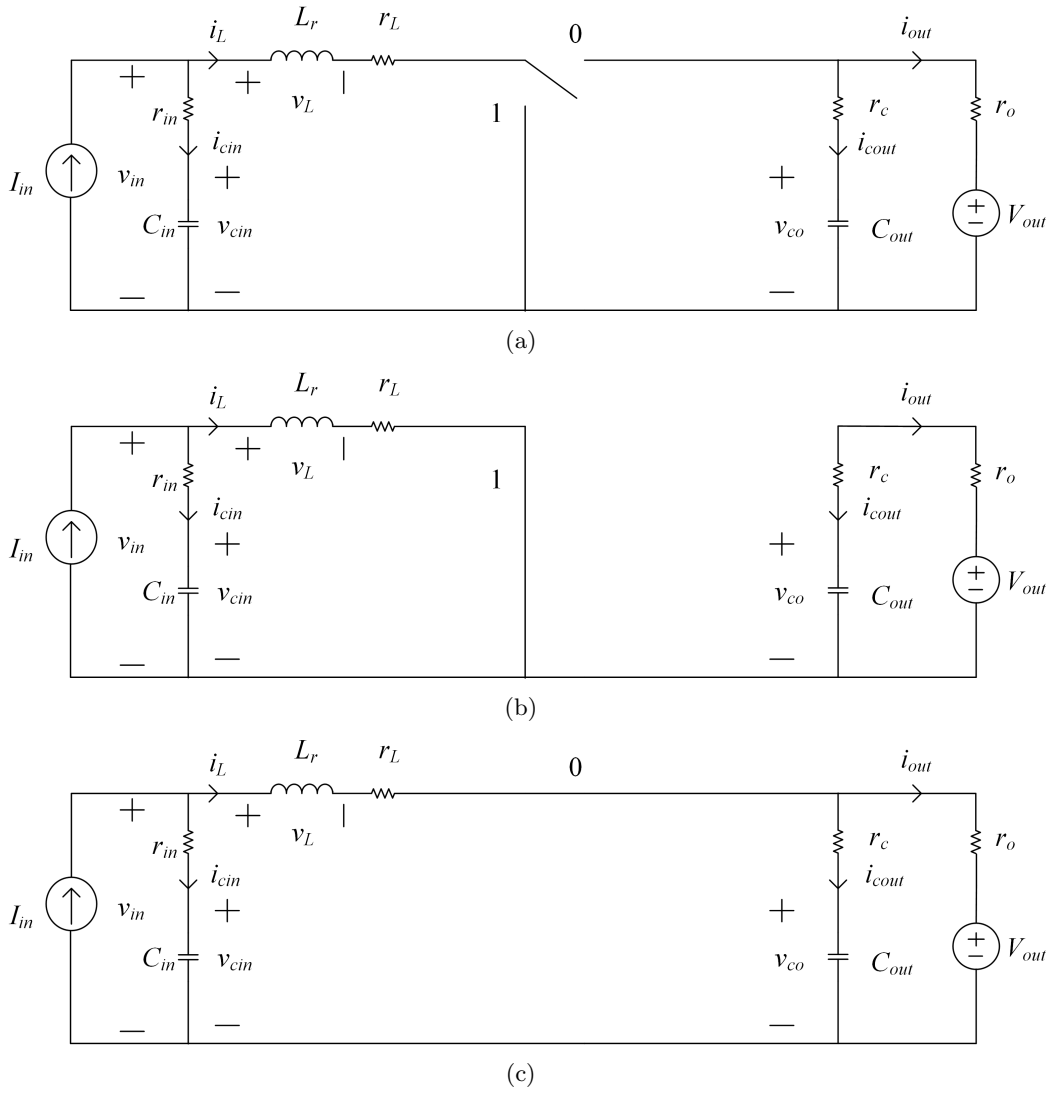


Fig. 5.12: State space model of DC-DC converter (a) With positions of switch in 1 and 0, (b) With switch in position 1, (c) With switch in position 0.

$$y(t) = C_p x(t) + E_p v(t) \tag{5.65}$$

$$x(t) = \begin{bmatrix} v_{cin} \\ i_L \\ v_{co} \end{bmatrix}, v(t) = \begin{bmatrix} I_{in} \\ V_{out} \end{bmatrix}, y(t) = \begin{bmatrix} i_{out} \\ v_{in} \\ i_L \end{bmatrix}. \tag{5.66}$$

The state space equations for the switch in state 1 are given in (5.67)-(5.76).

$$i_{cin} = I_{in} - i_L \tag{5.67}$$

$$C_{in}\frac{dv_{cin}}{dt} = I_{in} - i_L \tag{5.68}$$

$$v_{cin} + (I_{in} - i_L)r_{in} - r_L i_L - v_L = 0 \tag{5.69}$$

$$L_r\frac{di_L}{dt} = v_{cin} + I_{in}r_{in} - (r_{in} + r_L)i_L \tag{5.70}$$

$$v_{co} + r_c i_{cout} - r_o i_{out} - V_{out} = 0 \tag{5.71}$$

$$C_{out}\frac{dv_{co}}{dt} = \frac{-v_{co}}{r_c + r_o} + \frac{V_{out}}{r_c + r_o} \tag{5.72}$$

$$v_{co} - r_c i_{out} - r_o i_{out} - V_{out} = 0 \tag{5.73}$$

$$i_{out} = \frac{v_{co}}{r_c + r_o} - \frac{V_{out}}{r_c + r_o} \tag{5.74}$$

$$v_{in} = v_{cin} + r_{in}(I_{in} - i_L) \tag{5.75}$$

$$i_L = i_L. \tag{5.76}$$

The matrices A_1, B_1, C_1, E_1 during the switch in position 1 are calculated from the above equations and given in equations (5.77)-(5.80).

$$A_1 = \begin{bmatrix} 0 & -\frac{1}{C_{in}} & 0 \\ \frac{1}{L_r} & -\frac{r_{in}+r_L}{L_r} & 0 \\ 0 & 0 & -\frac{1}{C_{out}(r_o+r_c)} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{C_{in}} & 0 \\ \frac{r_{in}}{L_r} & 0 \\ 0 & \frac{1}{C_{out}(r_o+r_c)} \end{bmatrix} \tag{5.77}$$

$$C_1 = \begin{bmatrix} 0 & 0 & \frac{1}{(r_o+r_c)} \\ 1 & -r_{in} & 0 \\ 0 & 1 & 0 \end{bmatrix}, E_1 = \begin{bmatrix} 0 & -\frac{1}{(r_o+r_c)} \\ r_{in} & 0 \\ 0 & 0 \end{bmatrix} \tag{5.78}$$

$$\begin{bmatrix} \frac{dv_{cin}}{dt} \\ \frac{di_L}{dt} \\ \frac{dv_{co}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C_{in}} & 0 \\ \frac{1}{L_r} & -\frac{r_{in}+r_L}{L_r} & 0 \\ 0 & 0 & -\frac{1}{C_{out}(r_o+r_c)} \end{bmatrix} \begin{bmatrix} v_{cin} \\ i_L \\ v_{co} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{in}} & 0 \\ \frac{r_{in}}{L_r} & 0 \\ 0 & \frac{1}{C_{out}(r_o+r_c)} \end{bmatrix} \begin{bmatrix} I_{in} \\ V_{out} \end{bmatrix} \tag{5.79}$$

$$\begin{bmatrix} i_{out} \\ v_{in} \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{1}{(r_o+r_c)} \\ 1 & -r_{in} & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{cin} \\ i_L \\ v_{co} \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{(r_o+r_c)} \\ r_{in} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} I_{in} \\ V_{out} \end{bmatrix}. \tag{5.80}$$

The state space equations for the switch in position 0 are given in (5.81)-(5.92).

$$i_{cin} = I_{in} - i_L \tag{5.81}$$

$$C_{in}\frac{dv_{cin}}{dt} = I_{in} - i_L \tag{5.82}$$

$$v_{cin} + (I_{in} - i_L)r_{in} - r_L i_L - v_L - r_o i_{out} - V_{out} = 0 \tag{5.83}$$

$$v_{co} + r_c i_{cout} - r_o i_{out} - V_{out} = 0 \tag{5.84}$$

$$i_{out} = i_L - i_{cout} \tag{5.85}$$

$$i_{cout} = -\frac{v_{co}}{r_c + r_o} + \frac{V_{out}}{r_c + r_o} + \frac{r_o i_L}{r_c + r_o} \tag{5.86}$$

$$C_{out}\frac{dv_{co}}{dt} = -\frac{v_{co}}{r_c + r_o} + \frac{V_{out}}{r_c + r_o} + \frac{r_o i_L}{r_c + r_o} \tag{5.87}$$

$$C_{out}\frac{dv_{co}}{dt} = -\frac{v_{co}}{r_c + r_o} + \frac{V_{out}}{r_c + r_o} + \frac{r_o i_L}{r_c + r_o} \tag{5.88}$$

$$v_{cin} + I_{in}r_{in} - i_L(r_{in} + r_L) - r_o i_L + \frac{r_o}{r_o + r_c}V_{out} + \frac{r_o^2}{r_o + r_c}i_L - \frac{r_o}{r_o + r_c}v_{co} - V_{out} = L_r\frac{di_L}{dt} \tag{5.89}$$

$$i_o = i_L + \frac{v_{co}}{r_c + r_o} - \frac{V_{out}}{r_c + r_o} - \frac{r_o i_L}{r_c + r_o} \tag{5.90}$$

$$v_{in} = v_{cin} + r_{in}(I_{in} - i_L) \tag{5.91}$$

$$i_L = i_L. \tag{5.92}$$

The matrices A_0, B_0, C_0, E_0 during the switch in position 0 are calculated from the above equations (5.93)-(5.96).

$$A_0 = \begin{bmatrix} 0 & -\frac{1}{C_{in}} & 0 \\ \frac{1}{L_r} & \frac{-\left(r_{in}+r_L+r_o-\frac{r_o^2}{r_o+r_c}\right)}{L_r} & \frac{-r_o}{L_r(r_o+r_c)} \\ 0 & \frac{r_o}{C_{out}(r_o+r_c)} & -\frac{1}{C_{out}(r_o+r_c)} \end{bmatrix}, B_0 = \begin{bmatrix} \frac{1}{C_{in}} & 0 \\ \frac{r_{in}}{L_r} & \frac{-r_c}{L_r(r_o+r_c)} \\ 0 & \frac{1}{C_{out}(r_o+r_c)} \end{bmatrix} \tag{5.93}$$

$$C_0 = \begin{bmatrix} 0 & \frac{r_c}{r_o+r_c} & \frac{1}{(r_o+r_c)} \\ 1 & -r_{in} & 0 \\ 0 & 1 & 0 \end{bmatrix}, E_0 = \begin{bmatrix} 0 & -\frac{1}{(r_o+r_c)} \\ r_{in} & 0 \\ 0 & 0 \end{bmatrix} \tag{5.94}$$

$$\begin{bmatrix} \frac{dv_{cin}}{dt} \\ \frac{di_L}{dt} \\ \frac{dv_{co}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C_{in}} & 0 \\ \frac{1}{L_r} & \frac{-\left(r_{in}+r_L+r_o-\frac{r_o^2}{r_o+r_c}\right)}{L_r} & \frac{-r_o}{L_r(r_o+r_c)} \\ 0 & \frac{r_o}{C_{out}(r_o+r_c)} & -\frac{1}{C_{out}(r_o+r_c)} \end{bmatrix} \begin{bmatrix} v_{cin} \\ i_L \\ v_{co} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{in}} & 0 \\ \frac{r_{in}}{L_r} & \frac{-r_c}{L_r(r_o+r_c)} \\ 0 & \frac{1}{C_{out}(r_o+r_c)} \end{bmatrix} \begin{bmatrix} I_{in} \\ V_{out} \end{bmatrix} \tag{5.95}$$

$$\begin{bmatrix} i_{out} \\ v_{in} \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & \frac{r_c}{r_o+r_c} & \frac{1}{(r_o+r_c)} \\ 1 & -r_{in} & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{cin} \\ i_L \\ v_{co} \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{(r_o+r_c)} \\ r_{in} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} I_{in} \\ V_{out} \end{bmatrix}. \tag{5.96}$$

5.2.4 State Space Averaging

The DC-DC converter is represented in state space in Section 5.2.3. The state equations, including both the positions of the switch in 1 and 0 positions in terms of duty cycle d(t) of the converter, can be written as shown in equations (5.97) and (5.98).

$$\frac{dx(t)}{dt} = d(t)[A_1x(t) + B_1v(t)] + d'(t)[A_0x(t) + B_0v(t)] \tag{5.97}$$

$$y(t) = d(t)[C_1x(t) + E_1v(t)] + d'(t)[C_0x(t) + E_0v(t)]. \tag{5.98}$$

The moving Average operator is defined in equation (5.99). Taking the moving average of the states and the inputs in the equations (5.97) and (5.98) gives the averaged state space equations of the converter given in (5.99)-(5.103).

$$\langle x(t) \rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} x(\tau)\, d\tau \tag{5.99}$$

$$\frac{d\langle x(t)\rangle}{dt} = d(t)[A_1\langle x(t)\rangle + B_1\langle v(t)\rangle] + d'(t)[A_0\langle x(t)\rangle + B_0\langle v(t)\rangle] \tag{5.100}$$

$$\frac{d\langle x(t)\rangle}{dt} = [d(t)A_1 + d'(t)A_0]\langle x(t)\rangle + [d(t)B_1 + d'(t)B_0]\langle v(t)\rangle = f\big(d(t), \langle x(t)\rangle, \langle v(t)\rangle\big) \tag{5.101}$$

$$\langle y(t)\rangle = d(t)[C_1\langle x(t)\rangle + E_1\langle v(t)\rangle] + d'(t)[C_0\langle x(t)\rangle + E_0\langle v(t)\rangle] \tag{5.102}$$

$$\langle y(t)\rangle = [d(t)C_1 + d'(t)C_0]\langle x(t)\rangle + [d(t)E_1 + d'(t)E_0]\langle v(t)\rangle = g\big(d(t), \langle x(t)\rangle, \langle v(t)\rangle\big). \tag{5.103}$$

The averaged equations in (5.101) and (5.103) are perturbed at some given (dc) quiescent values. The states, inputs, and outputs are assumed to be superimposed by small ac variations at the dc quiescent values given in (5.104)-(5.107).

$$d(t) = D + \hat{d} \tag{5.104}$$

$$\langle x(t)\rangle_{T_s} = X + \hat{x} \tag{5.105}$$

$$\langle v(t)\rangle_{T_s} = V + \hat{v} \tag{5.106}$$

$$\langle y(t)\rangle_{T_s} = Y + \hat{y}. \tag{5.107}$$

The equations in (5.101) and (5.103) are then linearized around the DC values. The state space linearized small signal equations are given in (5.108), and (5.109), where A, B, G, C, E, F are the Jacobian matrices at the DC operating point given in (5.110), and (5.111).

$$\frac{d\hat{x}(t)}{dt} = A\hat{x}(t) + B\hat{v}(t) + G\hat{d}(t) \tag{5.108}$$

$$\hat{y}(t) = C\hat{x}(t) + E\hat{v}(t) + F\hat{d}(t) \tag{5.109}$$

$$A = \frac{\partial f}{\partial x}(D, X, V), B = \frac{\partial f}{\partial v}(D, X, V), G = \frac{\partial f}{\partial d}(D, X, V) \tag{5.110}$$

$$C = \frac{\partial g}{\partial x}(D, X, V), E = \frac{\partial g}{\partial v}(D, X, V), F = \frac{\partial g}{\partial d}(D, X, V). \tag{5.111}$$

Taking the laplace transform of the equations (5.108) and (5.109), the control to output transfer functions in terms of $\hat{d}(s)$ can be expressed as (5.112), the outputs $\hat{y}(s)$ are given in (5.113).

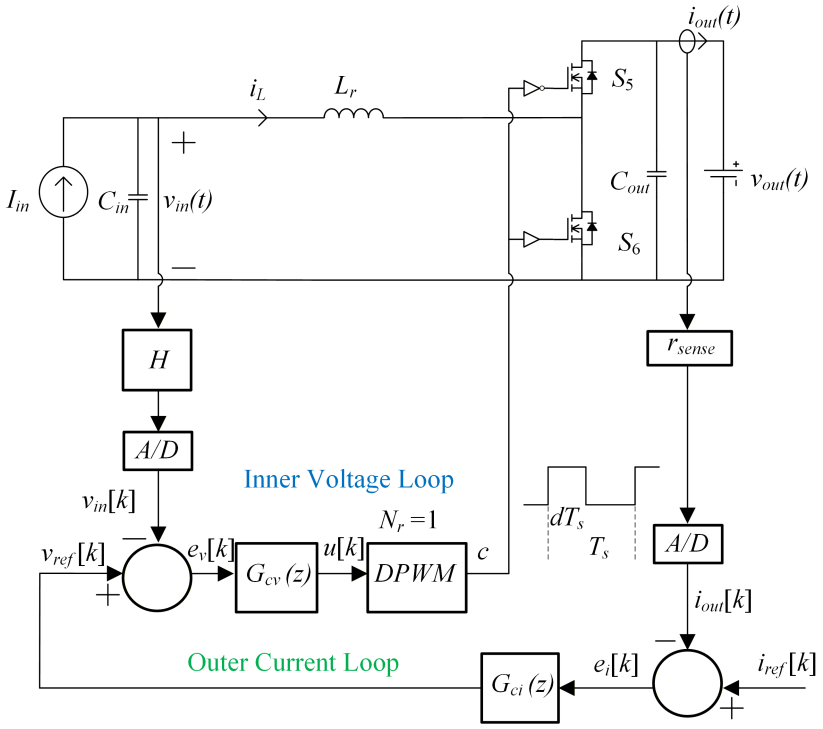
$$\hat{y}(s) = \big(C(sI - A)^{-1}G + F\big)\hat{d}(s) \tag{5.112}$$

$$\hat{y}(s) = \begin{bmatrix} \hat{i}_{out}(s) \\ \hat{v}_{in}(s) \\ \hat{i}_L(s) \end{bmatrix}. \tag{5.113}$$

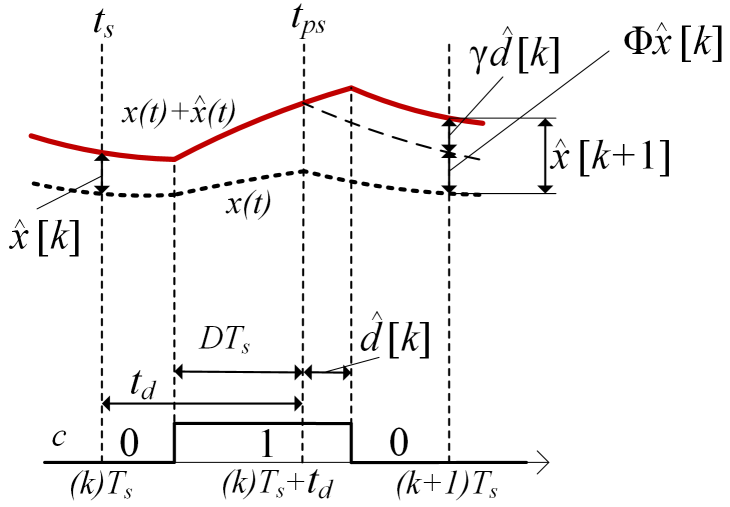
5.2.5 Discrete Time Modeling

The state space model of the DC-DC converter is derived in Section 5.2.3. The state space equations of the DC-DC converter during the positions of the switch in 0 and 1 are given in (5.114) and (5.115). The time interval during the switch in position 0 is referred to as interval 0, and the time interval during the switch in position 1 is referred to as interval 1.

$$\frac{dx(t)}{dt} = A_p x(t) + B_p v(t) \tag{5.114}$$



(a)



(b)

Fig. 5.13: (a) DC-DC converter showing digital dual loop control, (b) Discrete time model waveforms with A/D sampling in interval 0.

$$y(t) = C_p x(t) + E_p v(t). \tag{5.115}$$

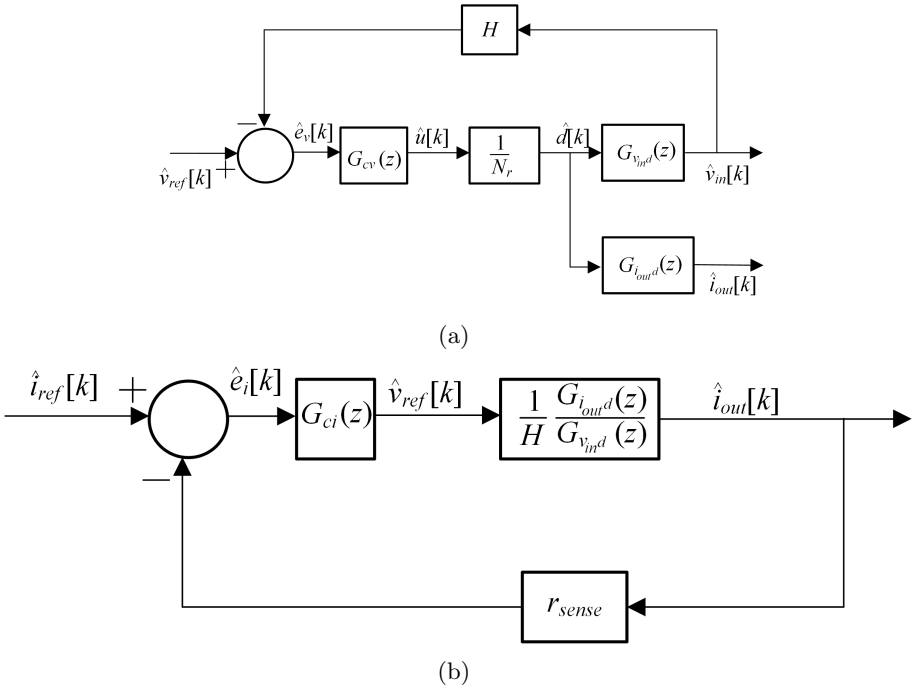


Fig. 5.14: Small Signal block diagrams for inner and outer loops for digital dual loop control: (a) Inner Loop, (b) Outer Loop.

The state equation for small signal discrete time model is given in equation (5.116), where $\hat{x}[k+1]$ is the sum of the propagation of the perturbations $\hat{x}[k]$ and $\hat{d}[k]$ in one switching period during the intervals 0 and 1. For a trailing-edge PWM with A/D sampling in the interval 0, the propagation of the perturbation $\hat{x}(k)$ throughout the switching period during the intervals 0 and 1 is denoted by ϕ and given in equation (5.117), for A/D sampling in interval 0. The propagation of the perturbation $\hat{d}$ for A/D sampling in interval 0 from the modulation edge till the end of the switching period is given in (5.118), where X_{ps} is the steady state value of the states at t_{ps}. The output equation for the small signal discrete time model is given in equation (5.119), where the C_p matrix is the matrix at the instant of A/D sampling. For sampling in interval 0, the output equation is given in (5.120). Taking the z-transform of the equations (5.116) and (5.119), the control to output transfer functions in the z-domain in terms of $\hat{d}[k]$ can be expressed as (5.121). The outputs $\hat{y}[k]$ are given in (5.123).

$$\hat{x}[k+1] = \phi\hat{x}[k] + \gamma\hat{d}[k] \tag{5.116}$$

$$\phi = e^{A_0(T_s - t_d)} e^{A_1 D T_s} e^{A_0(t_d - D T_s)} \tag{5.117}$$

$$\gamma = T_s e^{A_0(T_s - t_d)} \big[(A_1 X_{ps} + B_1 V) - (A_0 X_{ps} + B_0 V)\big] \tag{5.118}$$

$$\hat{y}[k] = C_p \hat{x}[k] \tag{5.119}$$

$$\hat{y}[k] = C_0 \hat{x}[k] \tag{5.120}$$

$$\hat{y}[z] = \big(C_p(zI - \phi)^{-1}\gamma)\hat{d}[z] \tag{5.121}$$

$$\hat{y}[z] = \begin{bmatrix} \hat{i}_{out}[z] \\ \hat{v}_{in}[z] \\ \hat{i}_L[z] \end{bmatrix} \tag{5.122}$$

$$\frac{\hat{y}[z]}{\hat{d}[z]} = \big(C_p(zI - \phi)^{-1}\gamma). \tag{5.123}$$

5.2.6 System Specifications and Matlab Plots of derived models

Table 5.1: Parameters for Double-Sided LCC Tuning.

Parameter	**Value**
f_s	85 kHz
P_{out}	50 kW
V_g	650 V
V_{in}	400 V
L_1	5.6 μH
C_1	0.63 μF
C_2	415 nF
L_{11}	13.36 μH
L_{22}	7.26 μH
k	0.2
C_3	990 nF
C_4	1040 nF
L_2	3.35 μH

From Fig. 5.15 and Fig. 5.16, it can be observed that the Z_N and Z_D impedances for both the figures are much less than the impedance Z of the WPT system, due to which the WPT system has negligible effects on the transfer functions $G_{v_{in}d}$ and $G_{i_{out}d}$ of the DC-DC converter. From Fig. 5.17, it can be observed that there is an extra phase lag at higher frequencies in the blue plot of the discrete-time model of $G_{v_{in}d}$, which is due to the effects of loop delays in digital control systems. The effects of these delays are accurately predicted by the discrete-time model, which is absent in the state space averaging approach. A similar trend is observed in Fig. 5.18 at higher frequencies for the plots of $G_{i_{out}d}$. The magnitude plots also differ at low frequencies for $G_{i_{out}d}$ shown in Fig. 5.18. Fig. 5.19 and Fig. 5.20 shows the zoomed in version of $G_{i_{out}d}$ at lower frequencies for r_o of 200 mΩ and 50 mΩ respectively. It can be seen that the magnitudes of state space averaging for both these figures remain the same, but there is a significant difference in the magnitudes of the discrete time model for both the resistances at lower frequencies. This is due to the fact

Table 5.2: Parameters for 2-Transistor ZVS-QSW boost for Matlab Plots at 50 kW.

Parameter	**Value**
f_s	70 kHz
P_{out}	50 kW
V_{out}	600 V
V_{in}	400 V
I_L	125 A
I_{out}	83 A
L_r	6.8 μH
C_r	6.66 nF
C_{in}	440 μF
C_{out}	200 μF
r_L	4.77 mΩ
r_{in}	0.45 mΩ
r_c	1 mΩ
r_o	200 mΩ
D	0.33
T_s	14.28 μs
$t_d - DT_s$	400 ns

that as r_o or battery resistance changes, there is a change in ripple current of the battery, which can be predicted by a discrete-time model but is not predicted accurately by the state space averaging model due to the sampling instant of the battery current. There are also differences in phases of the discrete-time model and state space averaging model at lower frequencies, which can be observed from Fig. 5.19 and Fig. 5.20.

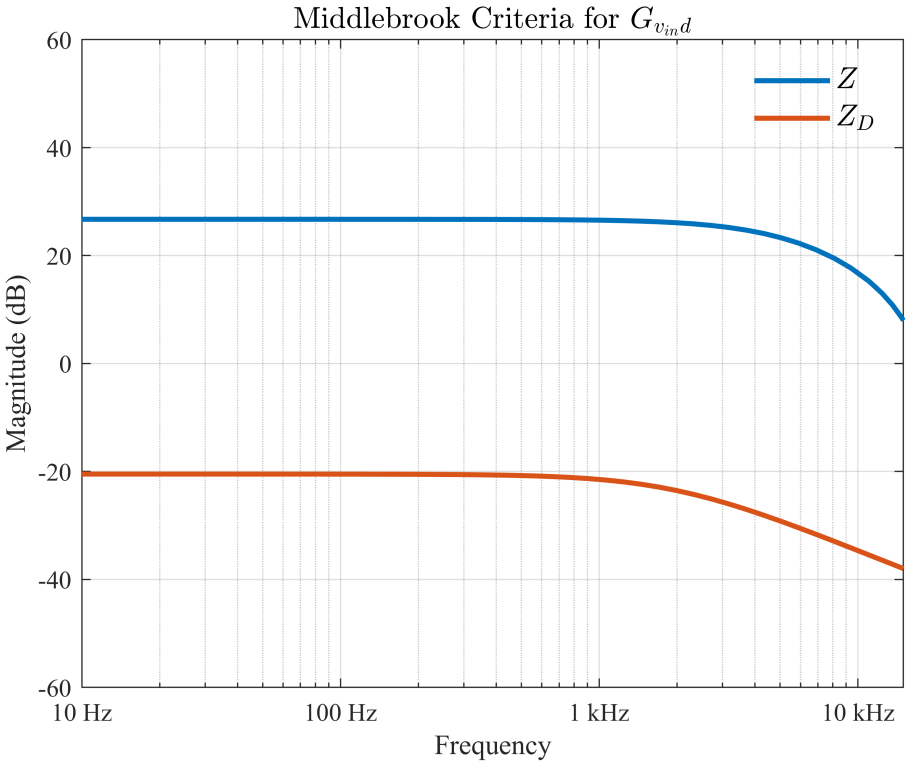


Fig. 5.15: Z and Z_D plots for Middlebrook stability criteria for $G_{v_{in}d}$.

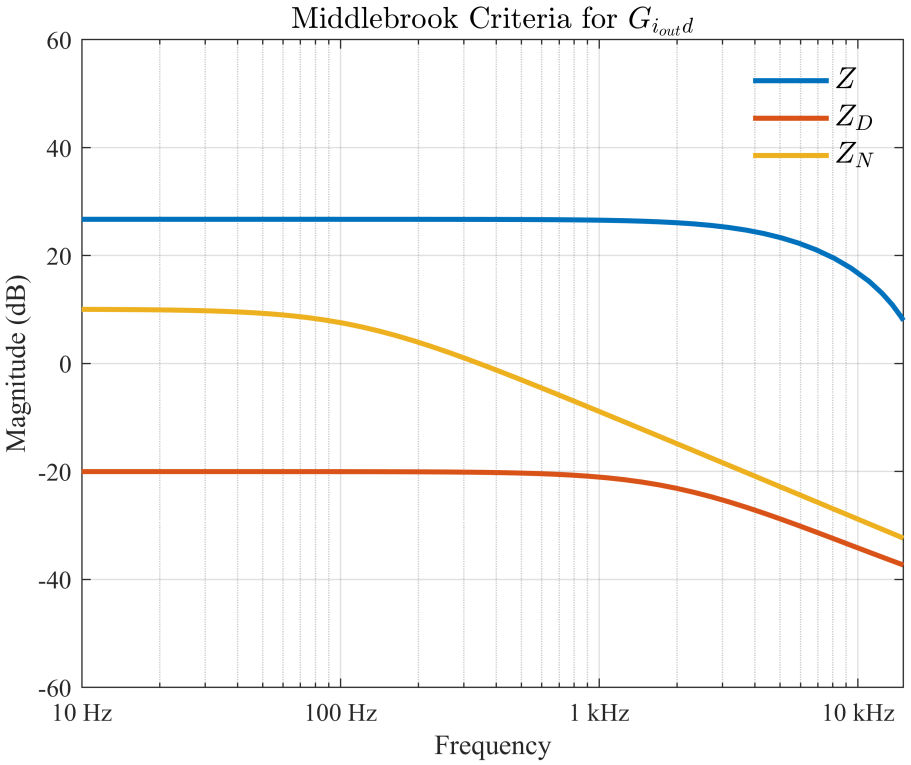


Fig. 5.16: Z , Z_D and Z_N plots for Middlebrook stability criteria for $G_{i_{out}d}$.

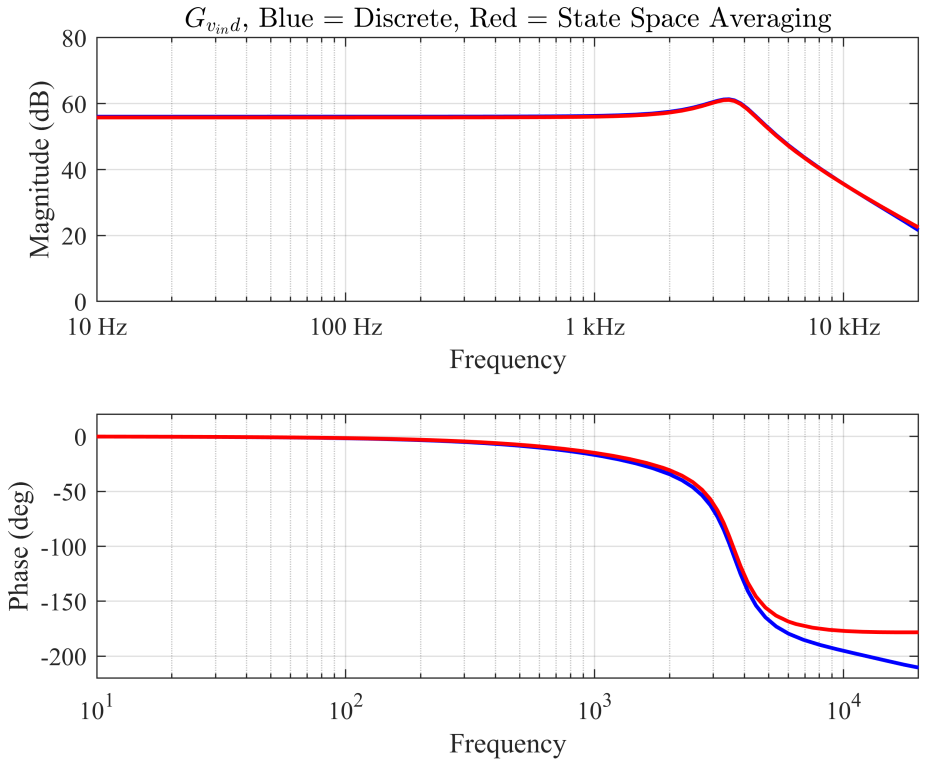


Fig. 5.17: $G_{v_{in}d}$ plot from Discrete Time modeling and State Space Averaging.

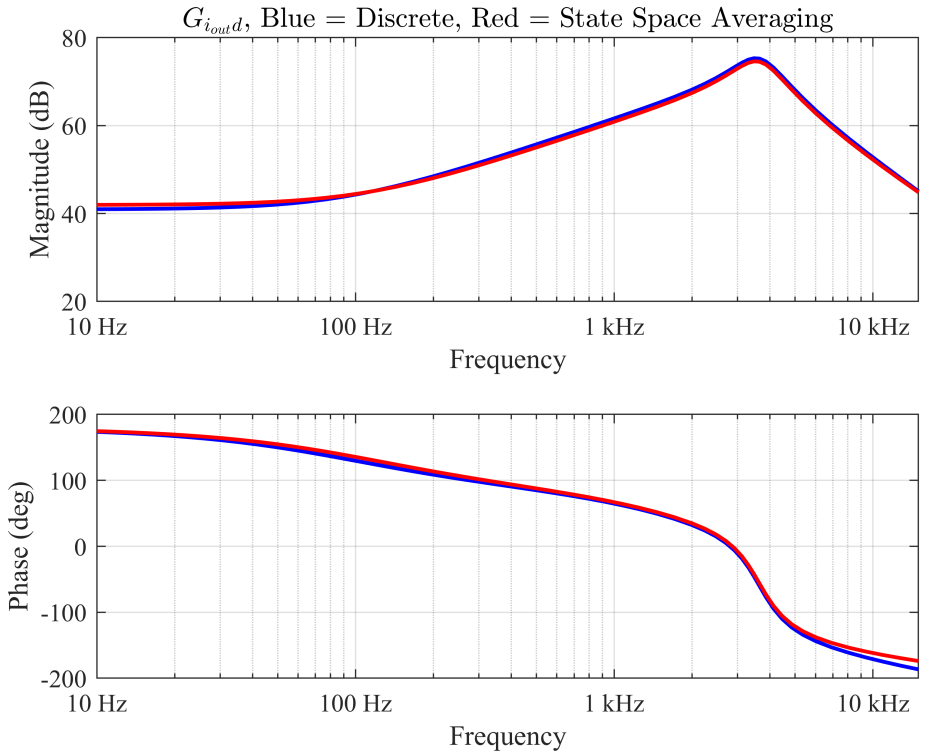


Fig. 5.18: $G_{i_{out}d}$ plot from Discrete Time modeling and State Space Averaging.

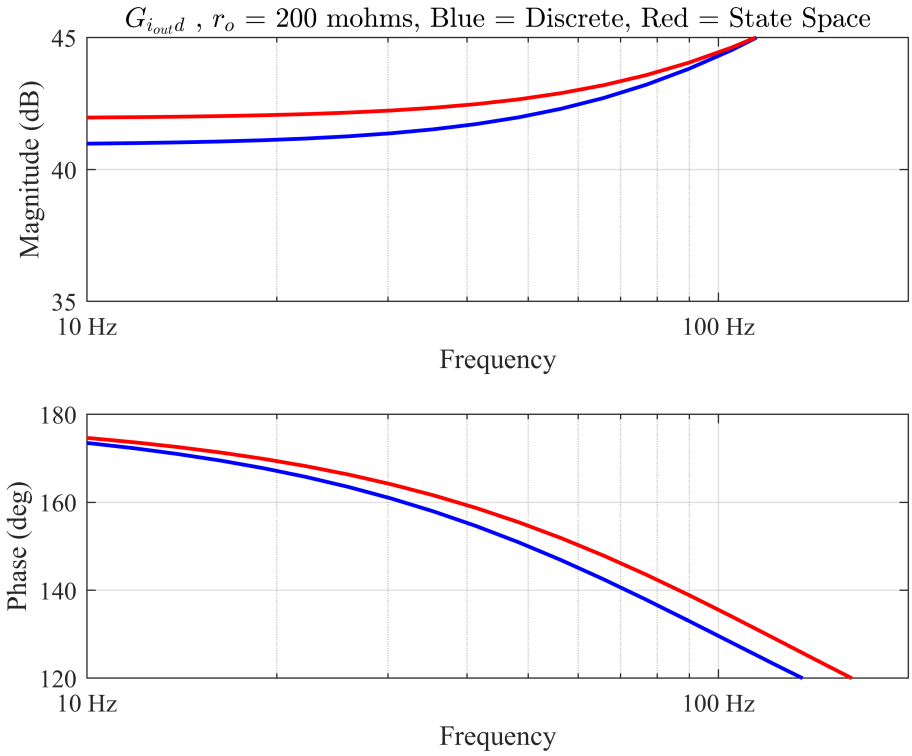


Fig. 5.19: $G_{i_{outd}}$ plot from Discrete Time and State Space Averaging with $r_o = 200$ mΩ.

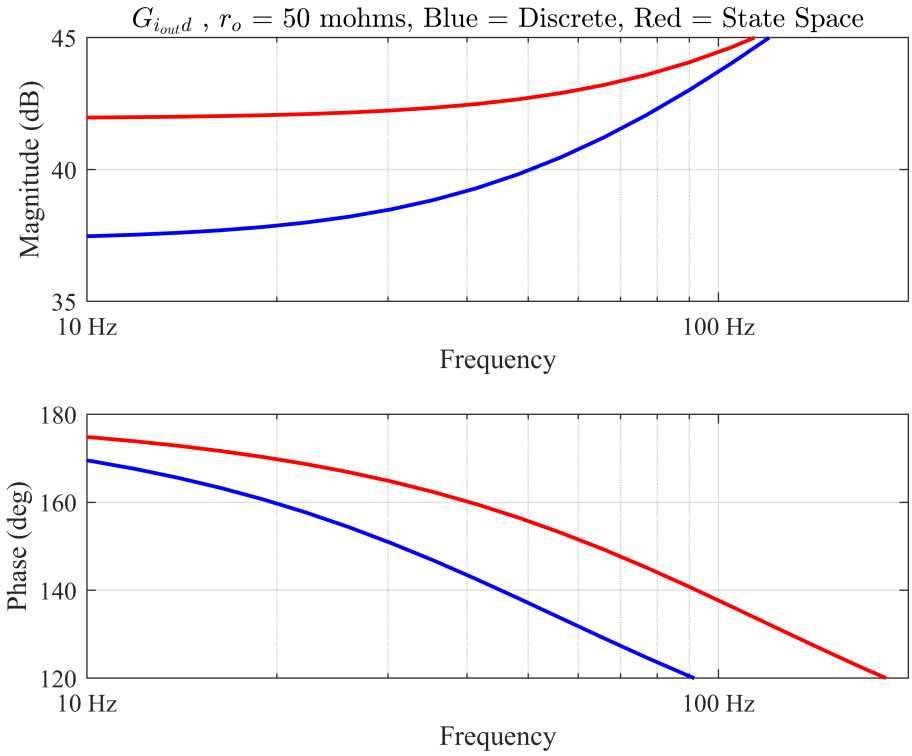


Fig. 5.20: $G_{i_{out}d}$ plot from Discrete Time and State Space Averaging with $r_o = 50$ mΩ.

5.3 Compensator Design using Discrete Time Model

The z-domain transfer functions are obtained from the equation (5.123). The direct digital compensator design is done using the methodology given in [85], where the bilinear transform method is used. For designing the compensator, the p-domain is defined, which has the characteristics of the Laplace domain. The mapping of the z-domain to the continuous-time p-domain is given in (5.124), and the inverse map is given in (5.125). If the transfer function of the compensator in z-domain is $G_c(z)$, mapping of $G_c(z)$ in p-domain is given as $G_c^{'}(p)$.

$$z(p) = \frac{1 + p\frac{T_s}{2}}{1 - p\frac{T_s}{2}} \tag{5.124}$$

$$p(z) = \frac{2}{T_s}\frac{1 - z^{-1}}{1 + z^{-1}} \tag{5.125}$$

$$G_c^{'}(p) = G_c(z). \tag{5.126}$$

The unit circle represented by $z = e^{j\omega T_s}$ in z-domain is mapped into $p = j\omega^{'}$, which represents the imaginary axis in p-domain. The p-domain frequency $\omega^{'}$ in terms of z-domain frequency ω is given in (5.127). The frequency response of $G_c^{'}(p)$ with p-domain frequency $\omega^{'}$ in terms of frequency response z-domain frequency response $G_c(z)$ is given in (5.128).

$$\omega^{'} = \frac{2}{T_s}\tan\left(\omega\frac{T_s}{2}\right) \tag{5.127}$$

$$G_c^{'}(j\omega^{'}) = G_c(e^{j\omega T_s}) \tag{5.128}$$

For designing the compensator, the design procedure in [85] is followed. First, the uncompensated loop gain $T_u(z)$ is derived using the discrete time modeling approach in Section 5.2.5. The $T_u(z)$ transfer function in z-domain is mapped to p-domain transfer function $T_u^{'}(p)$. The frequencies in z-domain are pre-warped to p-domain frequencies using the relation given in (5.127). The compensator is designed in p-domain and then mapped

into p-domain using the relation given in (5.125). The compensator used for this system is a higher-order compensator for which a cascade or parallel implementation could then be used in the z-domain. The advantages and disadvantages of the fixed-point implementation for both the parallel and cascaded realizations are explored.

5.3.1 Loop Gain and the Compensator Transfer functions for Inner Loop

The two-loop control design of the DC-DC is discussed in this section. For a counter-based DPWM (digital Pulse width Modulator), defining N_r as the number of DPWM clock cycles per switching period. First, considering N_r to be 1. The uncompensated loop gain of the inner voltage loop is given in (5.129). The uncompensated loop gain transfer $T_{uv}(z)$ function in z-domain is mapped to p-domain transfer function $T_{uv}^{'}(p)$ using the equation (5.128), where the crossover frequency of the inner voltage loop ω_{cv} in z-domain is pre-warped to p-domain, $\omega_{cv}^{'}$ using the equation (5.127).

$$T_{uv}(z) = HG_{vd}(z) \tag{5.129}$$

The compensator in p-domain, $G_{cv}^{'}(p)$ is given in (5.130). The magnitude and phase of $T_{uv}(z)$ at w_{cv} or equivalently the magnitude and phase of $T_{uv}^{'}(p)$ at $w_{cv}^{'}$ is given in equations (5.131), and (5.132). The loop gain transfer function of the inner loop in the p-domain is given in (5.133).

$$G_{cv}^{'}(p) = G_{cv0}\frac{\left(1+\frac{\omega_{Lv}^{'}}{p}\right)\left(1+\frac{p}{\omega_{z1v}^{'}}\right)\left(1+\frac{p}{\omega_{z2v}^{'}}\right)}{\left(1+\frac{p}{\omega_{p1v}^{'}}\right)\left(1+\frac{p}{\omega_{p2v}^{'}}\right)} \tag{5.130}$$

$$||T_{uv}^{'}(j\omega_{cv}^{'})|| = ||T_{uv}(e^{j\omega_{cv}T_s})|| \tag{5.131}$$

$$\angle T_{uv}^{'}(j\omega_{cv}^{'}) = \angle T_{uv}(e^{j\omega_{cv}T_s}) \tag{5.132}$$

$$T_{v}^{'}(p) = T_{uv}^{'}(p)G_{cv}^{'}(p) \tag{5.133}$$

The magnitude of loop gain $T_{v}^{'}(p)$ at crossover frequency $w_{cv}^{'}$ in p-domain is given in (5.134), and (5.135). The magnitude of $T_{uv}(z)$ at crossover frequency ω_{cv} or $||T_{uv}(e^{j\omega_{cv}T_s})||$ can

be found using equation (5.129), where $G_{vd}(z)$ is evaluated using discrete time modeling. The magnitude of loop gain $T_v^{'}(j\omega_{cv}^{'})$ is then derived in (5.136), and (5.137) in terms of $||T_{uv}(e^{j\omega_{cv}T_s})||$ and $||G_{cv}^{'}(j\omega_{cv}^{'})||$.

$$||T_v^{'}(j\omega_{cv}^{'})|| = ||T_{uv}^{'}(j\omega_{cv}^{'})|| * ||G_{cv}^{'}(j\omega_{cv}^{'})|| \tag{5.134}$$

$$||T_v^{'}(j\omega_{cv}^{'})|| = ||T_{uv}(e^{j\omega_{cv}T_s})|| * ||G_{cv}^{'}(j\omega_{cv}^{'})|| \tag{5.135}$$

$$||T_v^{'}(j\omega_{cv}^{'})|| = ||T_{uv}(e^{j\omega_{cv}T_s})|| * G_{cv0}\frac{||\left(1+\frac{\omega_{Lv}^{'}}{p}\right)\left(1+\frac{p}{\omega_{z1v}^{'}}\right)\left(1+\frac{p}{\omega_{z2v}^{'}}\right)||}{||\left(1+\frac{p}{\omega_{p1v}^{'}}\right)\left(1+\frac{p}{\omega_{p2v}^{'}}\right)||} \tag{5.136}$$

$$||T_v^{'}(j\omega_{cv}^{'})|| = ||T_{uv}(e^{j\omega_{cv}T_s})|| * G_{cv0}\frac{||\left(1+\frac{\omega_{Lv}^{'}}{j\omega_{cv}^{'}}\right)\left(1+\frac{j\omega_{cv}^{'}}{\omega_{z1v}^{'}}\right)\left(1+\frac{j\omega_{cv}^{'}}{\omega_{z2v}^{'}}\right)||}{||\left(1+\frac{j\omega_{cv}^{'}}{\omega_{p1v}^{'}}\right)\left(1+\frac{j\omega_{cv}^{'}}{\omega_{p2v}^{'}}\right)||} \tag{5.137}$$

$||T_v^{'}(j\omega_{cv}^{'})||$ at crossover frequency $\omega_{cv}^{'}$ is 1. The G_{cv0} can be found using equation (5.138). From the transfer functions of $G_{vd}(z)$, it can be observed that the phase of $G_{vd}(z)$ at ω_{cv} is close to -180 degrees. Therefore, if the phase margin of ϕ_{mv} in radians is required at crossover frequency of $\omega_{cv}^{'}$, the following equations in (5.139), (5.140), (5.141), (5.142), and (5.143) are used to find the value of $\omega_{z1v}^{'}$, $\omega_{p1v}^{'}$, $\omega_{z2v}^{'}$ and $\omega_{p2v}^{'}$, where, ϕ_{mv1} and ϕ_{mv2} are the maximum phase improvements at crossover frequency $\omega_{cv}^{'}$ due to Lead (PD) compensator [84]. The inverted zero frequency $\omega_{Lv}^{'}$ is selected to be less than $\omega_{cv}^{'}$ and sufficiently low so that the phase margin is sufficient.

$$G_{cv0} = \frac{1}{||T_{uv}(e^{j\omega_{cv}T_s})||} * \frac{\sqrt{1+\frac{\omega_{cv}^{'2}}{\omega_{p1v}^{'2}}} * \sqrt{1+\frac{\omega_{cv}^{'2}}{\omega_{p2v}^{'2}}}}{\sqrt{1+\frac{\omega_{Lv}^{'2}}{\omega_{cv}^{'2}}} * \sqrt{1+\frac{\omega_{cv}^{'2}}{\omega_{z1v}^{'2}}} * \sqrt{1+\frac{\omega_{cv}^{'2}}{\omega_{z2v}^{'2}}}} \tag{5.138}$$

$$\phi_{mv} = \phi_{mv1} + \phi_{mv2} \tag{5.139}$$

$$\omega_{z1v}^{'} = \omega_{cv}^{'} * \sqrt{\frac{1-\sin\phi_{mv1}}{1+\sin\phi_{mv1}}} \tag{5.140}$$

$$\omega_{p1v}^{'} = \omega_{cv}^{'} * \sqrt{\frac{1+\sin\phi_{mv1}}{1-\sin\phi_{mv1}}} \tag{5.141}$$

$$\omega_{z2v}^{'} = \omega_{cv}^{'} * \sqrt{\frac{1-\sin\phi_{mv2}}{1+\sin\phi_{mv2}}} \tag{5.142}$$

$$\omega_{p2v}^{'} = \omega_{cv}^{'} * \sqrt{\frac{1+\sin\phi_{mv2}}{1-\sin\phi_{mv2}}}. \tag{5.143}$$

For practical implementation, the number of DPWM clock cycles per switching period, that is N_r, is not 1 and has a value depending on the switching frequency f_s and the clock frequency f_{clk} of the digital controller, like an FPGA. The A/D converter for sensing the input voltage will also have a finite resolution, where the LSB resolution for full-scale A/D is given in (5.144). Considering both the N_r and resolution of A/D converter, $q_{v_{in}}^{(A/D)}$, the uncompensated loop gain is scaled as given in (5.145), where the λ is the scaling coefficient and given in (5.146). Scaling with λ also makes the fixed-point implementation of the compensator easier, where the resolution of the error signal $q_e^{(A/D)}$ is 1.

$$q_{v_{in}}^{(A/D)} = \frac{V_{FS}}{2^{nA/D}} \tag{5.144}$$

$$T_{uv}(z) = \frac{HG_{vd}(z)}{\lambda} \tag{5.145}$$

$$\lambda = q_{v_{in}}^{(A/D)} N_r \tag{5.146}$$

The compensator $G_{cv}^{'}(p)$ is then designed for the scaled $T_{uv}(z)$ given in (5.145). The compensator transfer function $G_{cv}(z)$ in z-domain is then obtained using bilinear transform from the equation (5.125), and is given in (5.147), and (5.148). The loop gain for the inner loop is given in equation (5.149).

$$G_{cv}(z) = G_{cvz0}\frac{(z-C_{zv1})(z-C_{zv2})(z-C_{zv3})}{(z-1)(z-C_{pv1})(z-C_{pv2})} \tag{5.147}$$

$$G_{cv}(z) = G_{cvz0}\frac{(1-C_{zv1}z^{-1})(1-C_{zv2}z^{-1})(1-C_{zv3}z^{-1})}{(1-z^{-1})(1-C_{pv1}z^{-1})(1-C_{pv2}z^{-1})} \tag{5.148}$$

$$T_v(z) = \frac{HG_{vd}(z)G_{cv}(z)}{\lambda}. \tag{5.149}$$

5.3.2 Loop Gain and the Compensator Transfer functions for Outer Loop

The uncompensated loop gain of the outer current loop is given in (5.150). If the bandwidth of the outer loop is much less than the bandwidth of the inner loop, the uncompensated loop gain of the outer current loop is given in (5.152). The uncompensated loop gain transfer $T_{ui}(z)$ function in z-domain is mapped to p-domain transfer function $T_{ui}^{'}(p)$ using the equation (5.128), where the crossover frequency of the outer current loop ω_{ci} in z-domain is pre-warped to p-domain, $\omega_{ci}^{'}$ using the equation (5.127).

$$T_{ui}(z) = \frac{r_{sense}}{H}\frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)}\frac{T_v(z)}{1+T_v(z)} \tag{5.150}$$

$$\frac{T_v(z)}{1+T_v(z)} \approx 1 \tag{5.151}$$

$$T_{ui}(z) \approx \frac{r_{sense}}{H}\frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)}. \tag{5.152}$$

The compensator in p-domain, $G_{ci}^{'}(p)$ is given in (5.153). The magnitude and phase of $T_{ui}(z)$ at w_{ci} or equivalently the magnitude and phase of $T_{ui}^{'}(p)$ at $w_{ci}^{'}$ is given in equations (5.154), and (5.155). The loop gain transfer function of the outer loop in p-domain is given in (5.156).

$$G_{ci}^{'}(p) = G_{ci0}\frac{\left(1+\frac{\omega_{Li}^{'}}{p}\right)\left(1+\frac{p}{\omega_{z1i}^{'}}\right)}{\left(1+\frac{p}{\omega_{pi}^{'}}\right)\left(1+\frac{p}{\omega_{p1i}^{'}}\right)} \tag{5.153}$$

$$||T_{ui}^{'}(j\omega_{ci}^{'})|| = ||T_{ui}(e^{j\omega_{ci}T_s})|| \tag{5.154}$$

$$\angle T_{ui}^{'}(j\omega_{ci}^{'}) = \angle T_{ui}(e^{j\omega_{ci}T_s}) \tag{5.155}$$

$$T_i^{'}(p) = T_{ui}^{'}(p)G_{ci}^{'}(p) \tag{5.156}$$

The magnitude of loop gain $T_i^{'}(p)$ at crossover frequency $w_{ci}^{'}$ in p-domain is given in (5.157),

and (5.158). The magnitude of $T_{uv}(z)$ at crossover frequency ω_{cv} or $||T_{uv}(e^{j\omega_{cv}T_s})||$ can be found using equation (5.152), where $G_{i_{out}d}(z)$ and $G_{v_{in}d}(z)$ are evaluated using discrete time modeling. The magnitude of loop gain $T_i^{'}(j\omega_{ci}^{'})$ is then derived in (5.159), and (5.160) in terms of $||T_{ui}(e^{j\omega_{ci}T_s})||$ and $||G_{ci}^{'}(j\omega_{ci}^{'})||$.

$$||T_i^{'}(j\omega_{ci}^{'})|| = ||T_{ui}^{'}(j\omega_{ci}^{'})|| * ||G_{ci}^{'}(j\omega_{ci}^{'})|| \tag{5.157}$$

$$||T_i^{'}(j\omega_{ci}^{'})|| = ||T_{ui}(e^{j\omega_{ci}T_s})|| * ||G_{ci}^{'}(j\omega_{ci}^{'})|| \tag{5.158}$$

$$||T_i^{'}(j\omega_{ci}^{'})|| = ||T_{ui}(e^{j\omega_{ci}T_s})|| * G_{ci0}\frac{||\left(1+\frac{\omega_{Li}^{'}}{p}\right)\left(1+\frac{p}{\omega_{z1i}^{'}}\right)||}{||\left(1+\frac{p}{\omega_{pi}^{'}}\right)\left(1+\frac{p}{\omega_{p1i}^{'}}\right)||} \tag{5.159}$$

$$||T_i^{'}(j\omega_{ci}^{'})|| = ||T_{ui}(e^{j\omega_{ci}T_s})|| * G_{ci0}\frac{||\left(1+\frac{\omega_{Li}^{'}}{j\omega_{ci}^{'}}\right)\left(1+\frac{j\omega_{ci}^{'}}{\omega_{z1i}^{'}}\right)||}{||\left(1+\frac{j\omega_{ci}^{'}}{\omega_{pi}^{'}}\right)\left(1+\frac{j\omega_{ci}^{'}}{\omega_{p1i}^{'}}\right)||} \tag{5.160}$$

$||T_i^{'}(j\omega_{ci}^{'})||$ at crossover frequency $\omega_{ci}^{'}$ is 1. The G_{ci0} can be found using equation (5.161). From the transfer functions of $T_{ui}(z)$, it can be observed that there is sufficient phase margin below 200 Hz. Therefore, if a phase boost of ϕ_i in radians is required at crossover frequency of $\omega_{ci}^{'}$, the following equations in (5.162), and (5.163) are used to find the value of $\omega_{z1i}^{'}$, $\omega_{p1i}^{'}$, where, ϕ_i is the maximum phase improvements at crossover frequency $\omega_{ci}^{'}$ due to Lead (PD) compensator [84]. The inverted zero frequency $\omega_{Li}^{'}$ is selected to be less than $\omega_{ci}^{'}$ and sufficiently low so that the phase margin is sufficient. An additional pole $\omega_{pi}^{'}$ at low frequency is also required in the compensator design. The PD compensator part for the outer loop can be added, as it is added here for additional phase boost, but it is not necessary for the outer loop compensator.

$$G_{ci0} = \frac{1}{||T_{ui}(e^{j\omega_{ci}T_s})||} * \frac{\sqrt{1+\frac{\omega_{ci}^{'2}}{\omega_{pi}^{'2}}} * \sqrt{1+\frac{\omega_{ci}^{'2}}{\omega_{p1i}^{'2}}}}{\sqrt{1+\frac{\omega_{Li}^{'2}}{\omega_{ci}^{'2}}} * \sqrt{1+\frac{\omega_{ci}^{'2}}{\omega_{z1i}^{'2}}}} \tag{5.161}$$

$$\omega_{z1i}^{'} = \omega_{ci}^{'} * \sqrt{\frac{1-\sin\phi_i}{1+\sin\phi_i}} \tag{5.162}$$

$$\omega_{p1i}^{'} = \omega_{ci}^{'} * \sqrt{\frac{1+\sin\phi_i}{1-\sin\phi_i}} \tag{5.163}$$

The compensator transfer function $G_{ci}(z)$ in z-domain is then obtained using bilinear transform from the equation (5.125), and is given in (5.164), and (5.167). The loop gain for the inner loop is given in equation (5.166).

$$G_{ci}(z) = G_{ciz0}\frac{(z+1)(z-C_{zi1})(z-C_{zi2})}{(z-1)(z-C_{pi1})(z-C_{pi2})} \tag{5.164}$$

$$G_{ci}(z) = G_{ciz0}\frac{(1+z^{-1})(1-C_{zi1}z^{-1})(1-C_{zi2}z^{-1})}{(1-z^{-1})(1-C_{pi1}z^{-1})(1-C_{pi2}z^{-1})} \tag{5.165}$$

$$T_i(z) = \frac{r_{sense}G_{ci}(z)}{H}\frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)}. \tag{5.166}$$

The compensator in p-domain, $G_{ci}^{'}(p)$ for parallel realization is simplified to (5.167), and $G_{ci}(z)$ is given in (5.168).

$$G_{ci}^{'}(p) = G_{ci0}\frac{(1+\frac{\omega_{Li}^{'}}{p})}{(1+\frac{p}{\omega_{pi}^{'}})} \tag{5.167}$$

$$G_{ci}(z) = G_{ciz0}\frac{(z+1)(z-C_{zi1})}{(z-1)(z-C_{pi1})} \tag{5.168}$$

5.4 Compensator Realization

5.4.1 Compensator Realization for Inner Loop

The compensator transfer function $G_{cv}(z)$ in the z-domain is obtained in Section 5.3.1, which is given in equation (5.230). Two realizations have been discussed in this section: the cascade and parallel realizations.

$$G_{cv}(z) = G_{cvz0}\frac{(1-C_{zv1}z^{-1})(1-C_{zv2}z^{-1})(1-C_{zv3}z^{-1})}{(1-z^{-1})(1-C_{pv1}z^{-1})(1-C_{pv2}z^{-1})}. \tag{5.169}$$

Due to the higher-order nature of the compensator, cascade realization is a more convenient option since the poles and zeros of the compensator can be directly implemented in cascaded structures. The cascaded realization also makes the compensator implementation less sensitive to the quantization of the coefficients, since the poles and zeros are directly quantized in this type of realization. The difference equations for the cascaded realization in the time domain are given in (5.170), (5.171), (5.172), (5.173), (5.174), (5.175), and (5.176). The cascade realization of $G_{cv}(z)$ is shown in Fig. 5.21.

$$W_{iv}(k) = e_v(k) + W_{iv}(k-1) \tag{5.170}$$

$$W_{1v}(k) = W_{iv}(k) + C_{pv1}W_{1v}(k-1) \tag{5.171}$$

$$W_{2v}(k) = W_{1v}(k) + C_{pv2}W_{2v}(k-1) \tag{5.172}$$

$$W_{3v}(k) = W_{2v}(k) - C_{zv1}W_{2v}(k-1) \tag{5.173}$$

$$W_{4v}(k) = W_{3v}(k) - C_{zv2}W_{3v}(k-1) \tag{5.174}$$

$$W_{5v}(k) = W_{4v}(k) - C_{zv3}W_{4v}(k-1) \tag{5.175}$$

$$u_{comp}(k) = G_{cvz0}W_{5v}(k). \tag{5.176}$$

For the parallel realization of $G_{cv}(z)$ in (5.230), the $G_{cv}(z)$ can be expressed as (5.177), where B_{1v}, B_{2v} and B_{3v} are calculated in (5.178), (5.179), and (5.180), respectively.

$$G_{cv}(z) = G_{cvz0} + \frac{B_{1v}}{(1-z^{-1})} + \frac{B_{2v}}{(1-C_{pv1}z^{-1})} + \frac{B_{3v}}{(1-C_{pv2}z^{-1})} \tag{5.177}$$

$$B_{1v} = \left[(1-z^{-1})G_{cv}(z)\right]_{z=1} \tag{5.178}$$

$$B_{2v} = \left[(1-C_{pv1}z^{-1})G_{cv}(z)\right]_{z=C_{pv1}} \tag{5.179}$$

$$B_{2v} = \left[(1 - C_{pv2}z^{-1})G_{cv}(z)\right]_{z=C_{pv2}}. \tag{5.180}$$

The difference equations for the parallel realization in the time domain are given in (5.181), (5.182), (5.183), (5.184), and (5.185). The parallel realization of $G_{cv}(z)$ is shown in Fig. 5.22.

$$u_i(k) = B_{1v}e_v(k) + u_i(k-1) \tag{5.181}$$

$$u_1(k) = B_{2v}e_v(k) + C_{pv1}u_1(k-1) \tag{5.182}$$

$$u_2(k) = B_{3v}e_v(k) + C_{pv2}u_2(k-1) \tag{5.183}$$

$$u_p(k) = G_{cvz0}e_v(k) \tag{5.184}$$

$$u_{comp}(k) = u_i(k) + u_1(k) + u_2(k) + u_p(k). \tag{5.185}$$

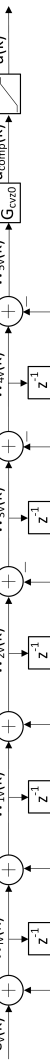


Fig. 5.21: Cascade Realization of $G_{cv}(z)$.

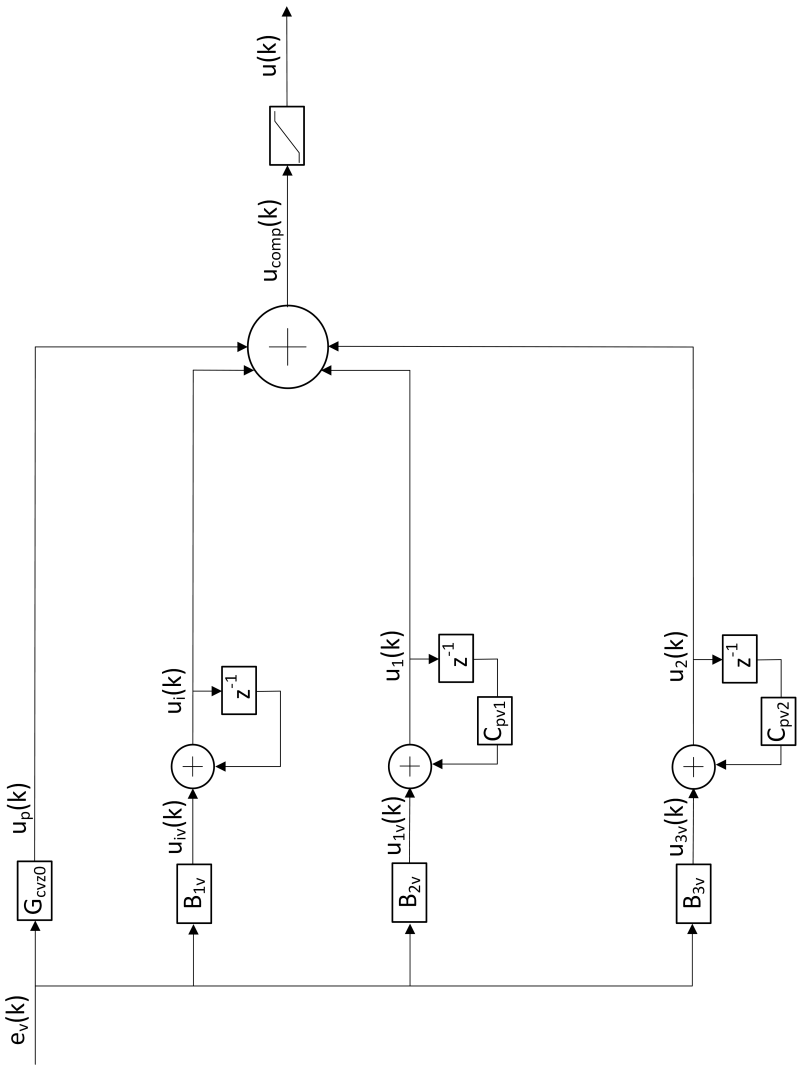


Fig. 5.22: Parallel Realization of $G_{cv}(z)$.

5.4.2 Compensator Realization for Outer Loop

The compensator transfer function $G_{ci}(z)$ in the z-domain is obtained in Section 5.3.2, which is given in equation (5.186). Two realizations, that is, the cascade and parallel realization, have been discussed for the outer loop compensator as well.

$$G_{ci}(z) = G_{ciz0}\frac{(1+z^{-1})(1-C_{zi1}z^{-1})(1-C_{zi2}z^{-1})}{(1-z^{-1})(1-C_{pi1}z^{-1})(1-C_{pi2}z^{-1})}. \tag{5.186}$$

The difference equations for the cascade realization in the time domain are given in (5.187), (5.188), (5.189), (5.190), (5.191), (5.192), and (5.193). The cascade realization of $G_{ci}(z)$ is shown in Fig. 5.23.

$$W_{ii}(k) = e_i(k) + W_{ii}(k-1) \tag{5.187}$$

$$W_{1i}(k) = W_{ii}(k) + C_{pi1}W_{1i}(k-1) \tag{5.188}$$

$$W_{2i}(k) = W_{1i}(k) + C_{pi2}W_{2i}(k-1) \tag{5.189}$$

$$W_{3i}(k) = W_{2i}(k) + W_{2i}(k-1) \tag{5.190}$$

$$W_{4i}(k) = W_{3i}(k) - C_{zi1}W_{3i}(k-1) \tag{5.191}$$

$$W_{5i}(k) = W_{4i}(k) - C_{zi2}W_{4i}(k-1) \tag{5.192}$$

$$V_{refcomp}(k) = G_{ciz0}W_{5i}(k). \tag{5.193}$$

For the parallel realization of $G_{ci}(z)$ in (5.194), the $G_{ci}(z)$ can be expressed as (5.195), where B_{1i} and B_{2i} are calculated in (5.196), and (5.197), respectively.

$$G_{ci}(z) = G_{ciz0}\frac{(z+1)(z-C_{zi1})}{(z-1)(z-C_{pi1})} \tag{5.194}$$

$$G_{ci}(z) = G_{ciz0} + \frac{B_{1i}}{(1-z^{-1})} + \frac{B_{2i}}{(1-C_{pi1}z^{-1})} \tag{5.195}$$

$$B_{1i} = \left[(1 - z^{-1})G_{ci}(z)\right]_{z=1} \tag{5.196}$$

$$B_{2i} = \left[(1 - C_{pi1}z^{-1})G_{ci}(z)\right]_{z=C_{pi1}}. \tag{5.197}$$

The difference equations for the parallel realization in the time domain are given in (5.198), (5.199), (5.200), and (5.201). The parallel realization of $G_{ci}(z)$ is shown in Fig. 5.24.

$$V_{refi}(k) = B_{1i}e_i(k) + V_{refi}(k-1) \tag{5.198}$$

$$V_{ref1}(k) = B_{2i}e_i(k) + C_{pi1}V_{ref1}(k-1) \tag{5.199}$$

$$V_{refp}(k) = G_{ciz0}e_i(k) \tag{5.200}$$

$$V_{refcomp}(k) = V_{refi}(k) + V_{ref1}(k) + V_{refp}(k). \tag{5.201}$$

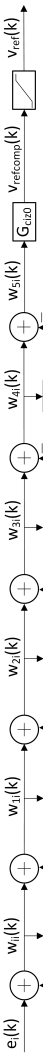


Fig. 5.23: Cascade Realization of $G_{ci}(z)$.

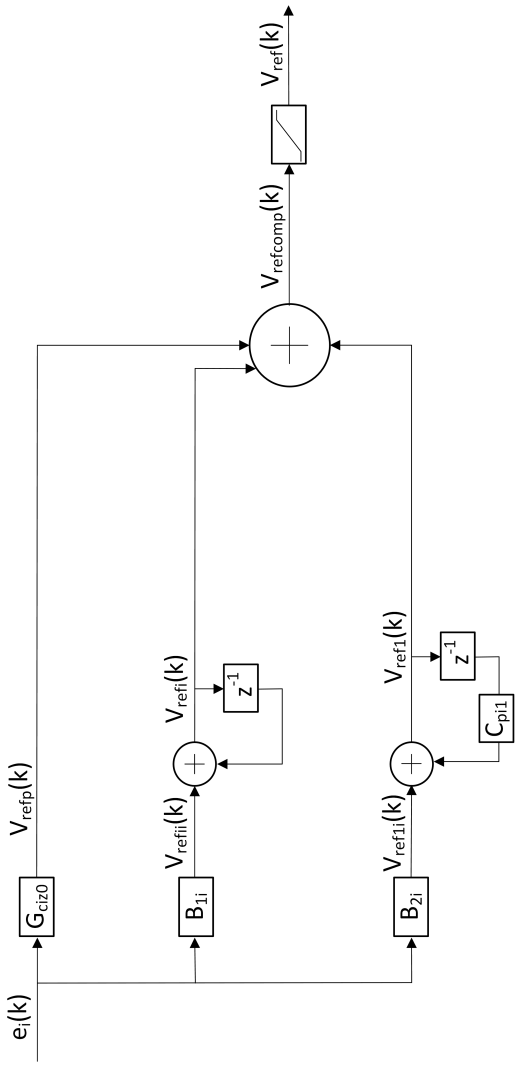


Fig. 5.24: Parallel Realization of $G_{ci}(z)$.

5.5 Matlab Plots and Fixed Point Implementation for Cascade Realization

5.5.1 Matlab plots for Inner loop and Outer Loop at 50 kW

Table 5.3: Parameters for 2-Transistor ZVS-QSW boost for Cascade Realization at 50 kW.

Parameter	**Value**
f_s	70 kHz
P_{out}	50 kW
V_{out}	600 V
V_{in}	400 V
I_L	125 A
I_{out}	83 A
L_r	6.8 μH
C_r	6.66 nF
C_{in}	440 μF
C_{out}	200 μF
r_L	4.77 mΩ
r_{in}	0.45 mΩ
r_c	1 mΩ
r_o	200 mΩ
D	0.33
H	0.005
r_{sense}	0.005
N_r	5914
nA/D	12
f_{clk}	414 MHz

The specifications for the DC-DC converter for control design for cascade realization at 50 kW are given in Table 5.3. The uncompensated loop gain for the inner loop with the scaling factor is given in (5.202), where the scaling factor λ is given in (5.203). The compensator is designed using the design process given in Section 5.3.1. The frequencies in the p-domain given in (5.204), used for designing the compensator at crossover frequency $\omega_{cv}^{'}$ for cascade realization, are given in Table 5.4.

$$T_{uv}(z) = \frac{HG_{vd}(z)}{\lambda} \tag{5.202}$$

$$\lambda = q_{v_s}^{(A/D)} N_r \tag{5.203}$$

$$G_{cv}^{'}(p) = G_{cv0} \frac{\left(1 + \frac{\omega_{Lv}^{'}}{p}\right)\left(1 + \frac{p}{\omega_{z1v}^{'}}\right)\left(1 + \frac{p}{\omega_{z2v}^{'}}\right)}{\left(1 + \frac{p}{\omega_{p1v}^{'}}\right)\left(1 + \frac{p}{\omega_{p2v}^{'}}\right)}. \tag{5.204}$$

Table 5.4: Frequencies for the compensator for the inner loop for cascade realization at 50 kW.

Parameter	**Value**
f_{cv}	7 kHz
$f_{Lv}^{'}$	2 kHz
$f_{z1v}^{'}$	2.99 kHz
$f_{p1v}^{'}$	17.47 kHz
$f_{z2v}^{'}$	2.99 kHz
$f_{p2v}^{'}$	17.47 kHz

The compensator in z-domain is given in (5.205), where the coefficients are given in Table 5.5. The loop gain is given in (5.205).

$$G_{cv}(z) = G_{cvz0} \frac{(1 - C_{zv1} z^{-1})(1 - C_{zv2} z^{-1})(1 - C_{zv3} z^{-1})}{(1 - z^{-1})(1 - C_{pv1} z^{-1})(1 - C_{pv2} z^{-1})} \tag{5.205}$$

$$T_v(z) = \frac{HG_{vd}(z) G_{cv}(z)}{\lambda}. \tag{5.206}$$

Table 5.5: Coefficients for the compensator for the inner loop for cascade realization in the z-domain at 50 kW.

Parameter	**Value**
G_{cvz0}	23.76
C_{zv1}	0.8353
C_{zv2}	0.7628
C_{zv3}	0.7628
C_{pv1}	0.1208
C_{pv2}	0.1208

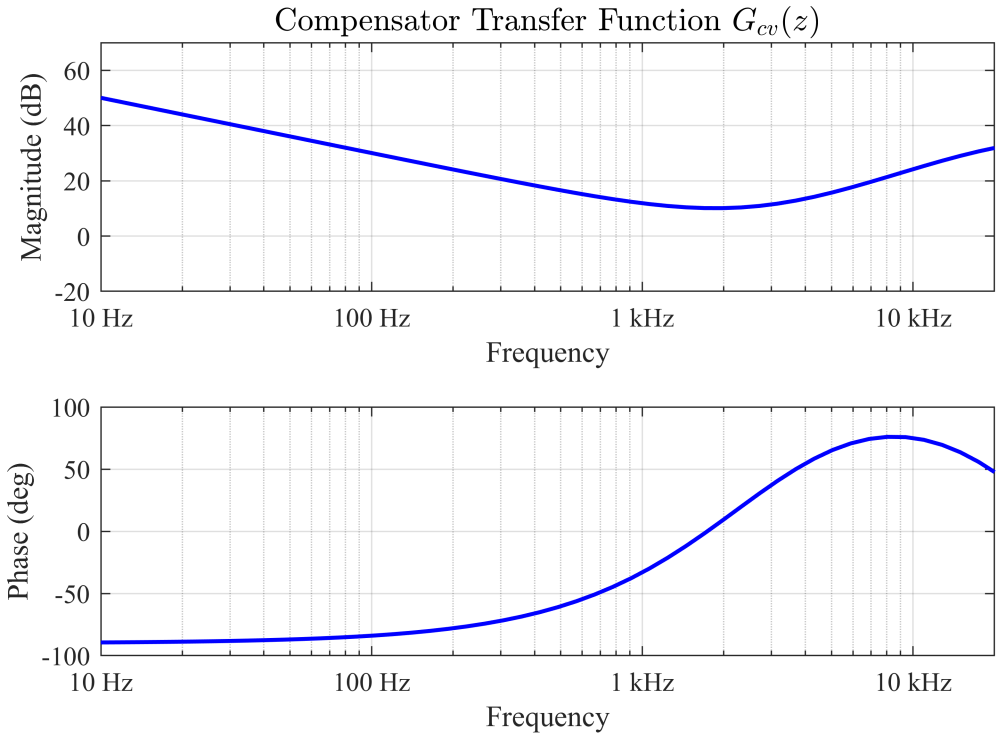
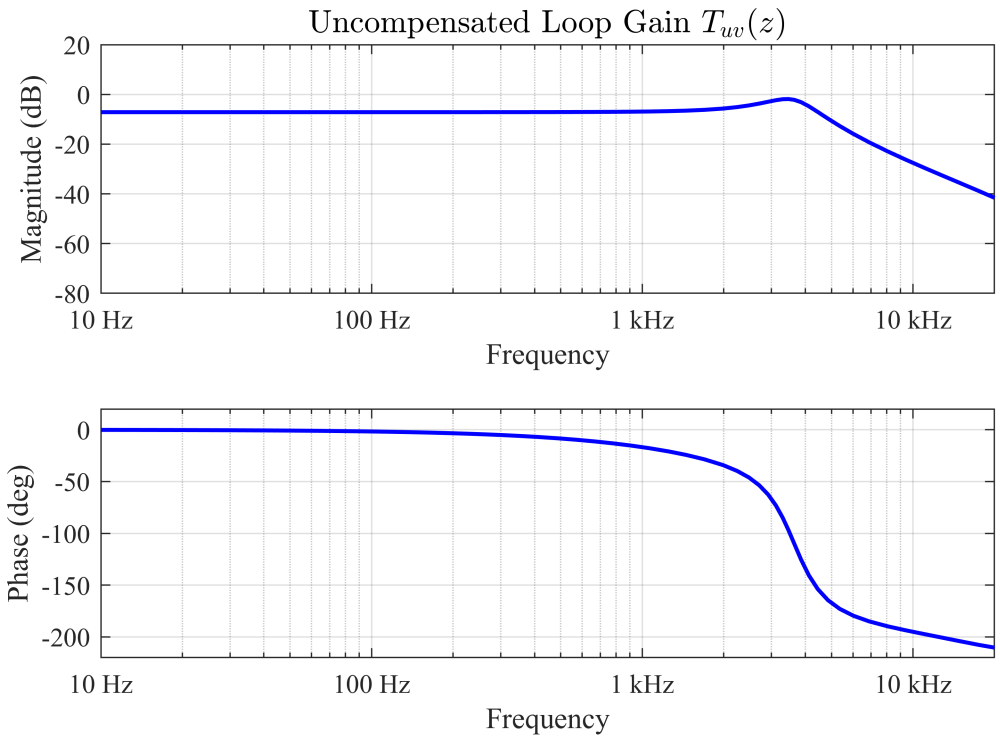
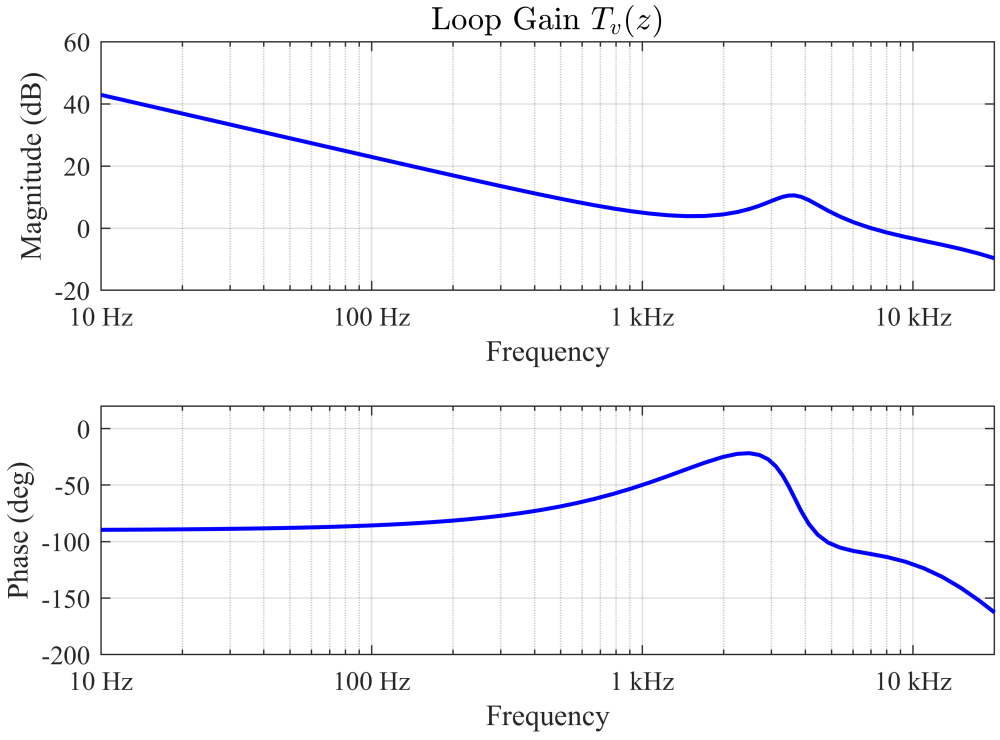


Fig. 5.25: Compensator plot for Inner Loop $G_{cv}(z)$.



(a)



(b)

Fig. 5.26: Plots for inner loop for cascade realization at 50 kW (a) Uncompensated Loop Gain $T_{uv}(z)$, (b) Loop Gain $T_v(z)$ with crossover frequency, f_{cv} of 7 kHz and phase margin of 69°.

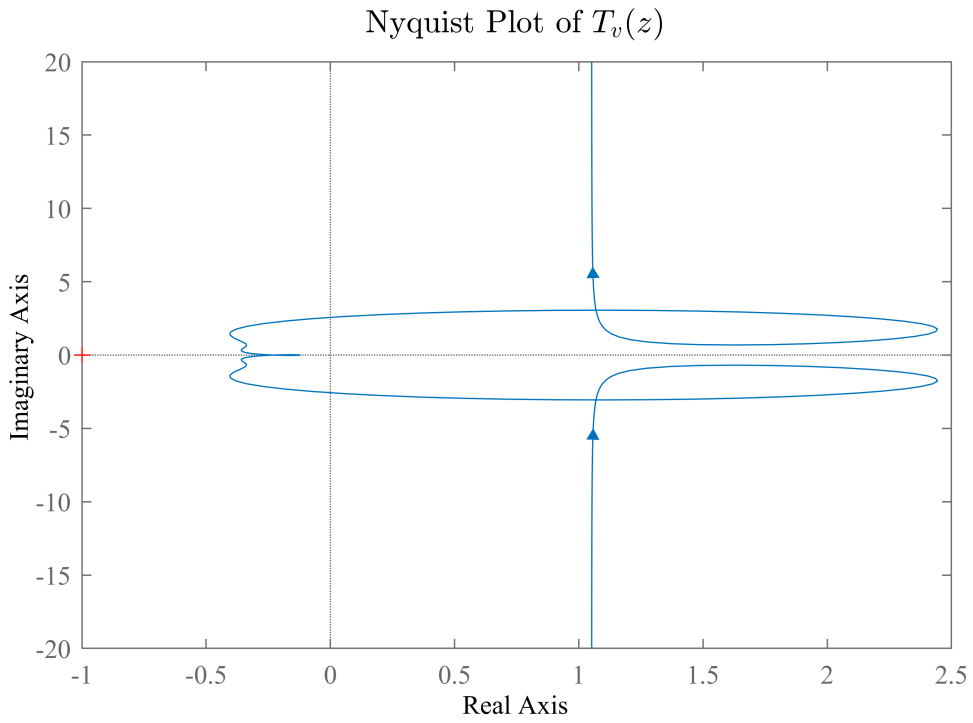


Fig. 5.27: Nyquist plot of Loop Gain $T_v(z)$.

The uncompensated loop gain for the outer loop is given in (5.207). The compensator is designed using the design process given in Section 5.3.2. The frequencies in the p-domain given in (5.208), used for designing the compensator at crossover frequency $\omega_{ci}^{'}$ for cascade realization, are given in Table 5.6.

$$T_{ui}(z) \approx \frac{r_{sense}}{H} \frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)} \tag{5.207}$$

$$G_{ci}^{'}(p) = G_{ci0} \frac{\left(1 + \frac{\omega_{Li}^{'}}{p}\right)\left(1 + \frac{p}{\omega_{z1i}^{'}}\right)}{\left(1 + \frac{p}{\omega_{pi}^{'}}\right)\left(1 + \frac{p}{\omega_{p1i}^{'}}\right)}. \tag{5.208}$$

Table 5.6: Frequencies for the compensator for the outer loop for cascade realization at 50 kW.

Parameter	**Value**
f_{ci}	40 Hz
$f_{Li}^{'}$	20 Hz
$f_{pi}^{'}$	40 Hz
$f_{z1i}^{'}$	40 Hz
$f_{p1i}^{'}$	40 Hz

The compensator in z-domain is given in (5.209), where the coefficients are given in Table 5.7. The loop gain is given in (5.210).

$$G_{ci}(z) = G_{ciz0} \frac{(1 + z^{-1})(1 - C_{zi1}z^{-1})(1 - C_{zi2}z^{-1})}{(1 - z^{-1})(1 - C_{pi1}z^{-1})(1 - C_{pi2}z^{-1})} \tag{5.209}$$

$$T_i(z) = \frac{r_{sense}G_{ci}(z)}{H} \frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)}. \tag{5.210}$$

Table 5.7: Coefficients for the compensator for cascade realization for the outer loop in the z-domain at 50 kW.

Parameter	**Value**
G_{ciz0}	0.0119
C_{zi1}	0.9982
C_{zi2}	0.9964
C_{pi1}	0.9964
C_{pi2}	0.9964

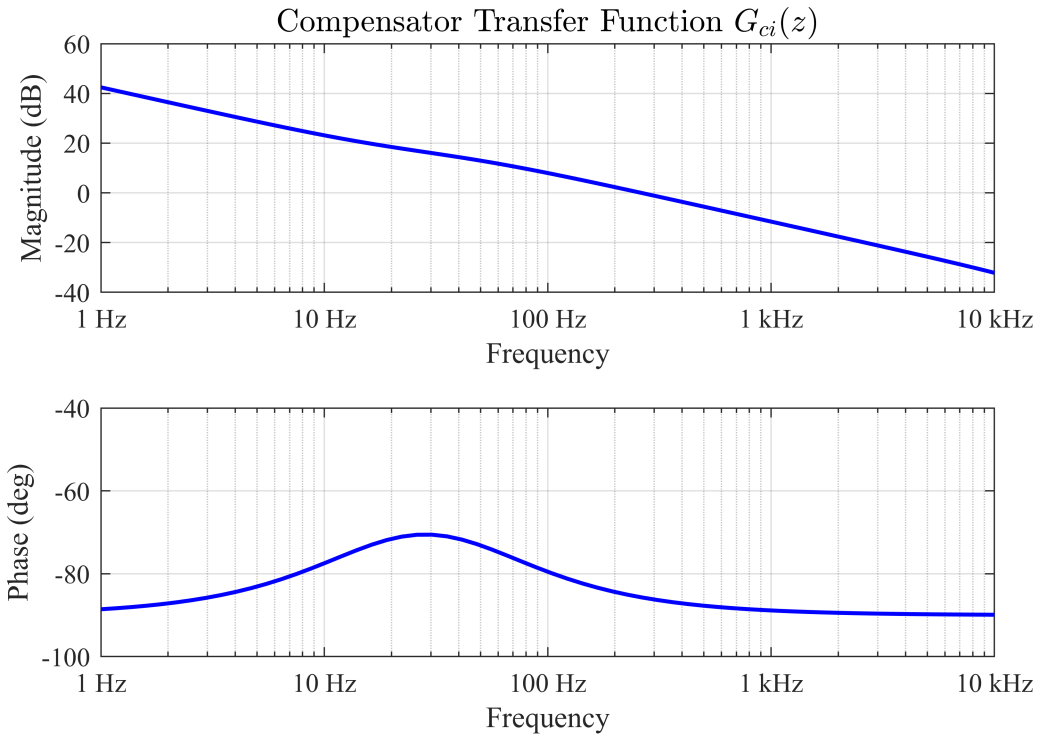
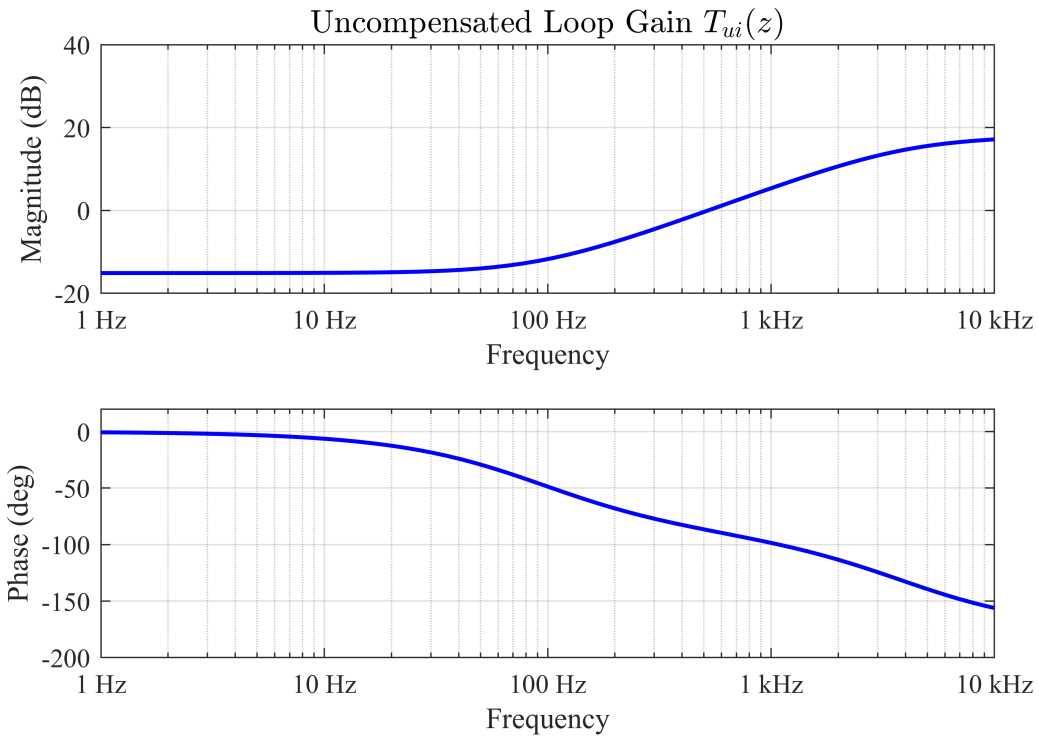
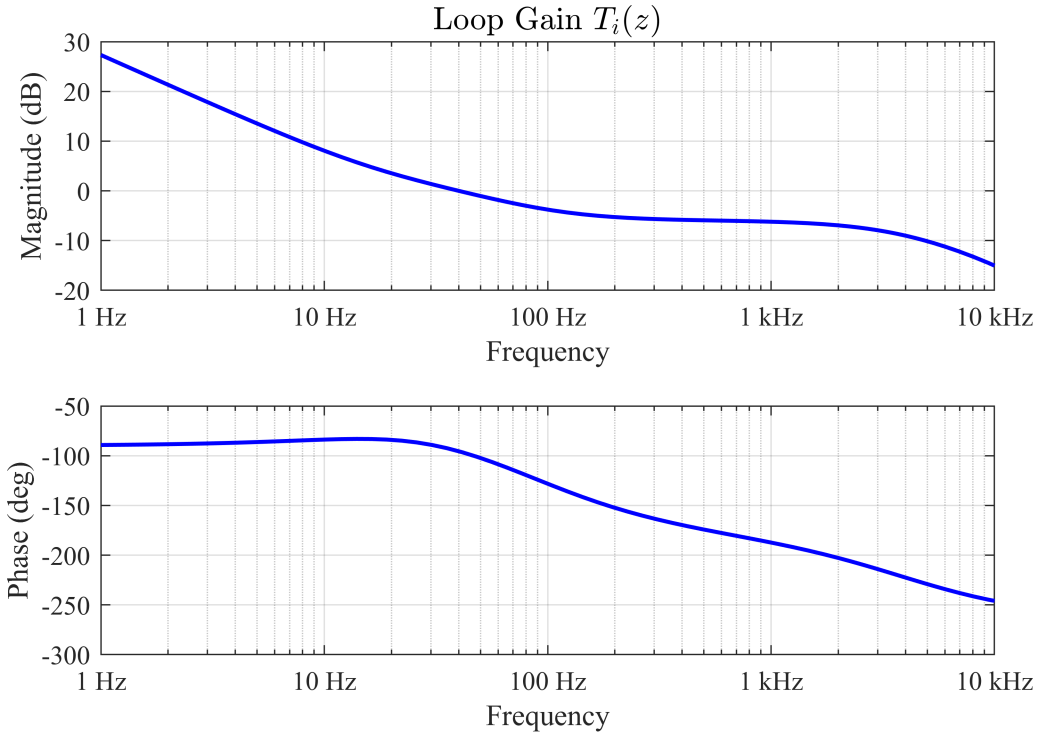


Fig. 5.28: Compensator plot for Inner Loop $G_{ci}(z)$.



(a)



(b)

Fig. 5.29: Plots for outer loop for cascade realization at 50 kW (a) Uncompensated Loop Gain $T_{ui}(z)$, (b) Loop Gain $T_i(z)$ with crossover frequency, f_{ci} of 40 Hz and phase margin of 84°.

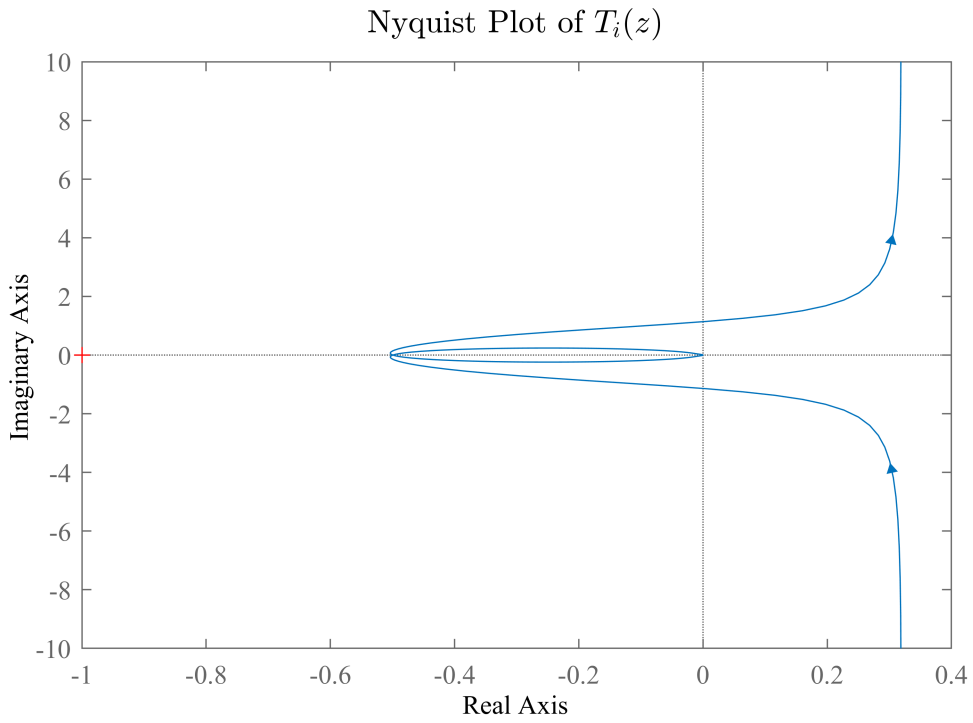


Fig. 5.30: Nyquist plot of Loop Gain $T_i(z)$.

5.5.2 Matlab plots for Inner loop and Outer Loop at 8 kW

Table 5.8: Parameters for 2-Transistor ZVS-QSW boost for Cascade Realization at 8 kW.

Parameter	**Value**
f_s	70 kHz
P_{out}	8 kW
V_{out}	250 V
V_{in}	160 V
I_L	50 A
I_{out}	32 A
L_r	6.8 μH
C_r	6.66 nF
C_{in}	440 μF
C_{out}	200 μF
r_L	4.77 mΩ
r_{in}	0.45 mΩ
r_c	1 mΩ
r_o	200 mΩ
D	0.64
H	0.005
r_{sense}	0.005
N_r	5914
nA/D	12
f_{clk}	414 MHz

The specifications for the DC-DC converter for control design for cascade realization at 8 kW are given in Table 5.8. The compensator is designed using the design process given in Section 5.3.1. The compensator in z- domain is given in (5.211), where the coefficients are given Table 5.9. The loop gain is given in (5.212).

$$G_{cv}(z) = G_{cvz0}\frac{(1 - C_{zv1}z^{-1})(1 - C_{zv2}z^{-1})(1 - C_{zv3}z^{-1})}{(1 - z^{-1})(1 - C_{pv1}z^{-1})(1 - C_{pv2}z^{-1})} \tag{5.211}$$

$$T_v(z) = \frac{HG_{vd}(z)G_{cv}(z)}{\lambda}. \tag{5.212}$$

Table 5.9: Coefficients for compensator for inner loop for cascade realization in z-domain at 8 kW.

Parameter	**Value**
G_{cvz0}	25
C_{zv1}	0.8353
C_{zv2}	0.7628
C_{zv3}	0.7628
C_{pv1}	0.1208
C_{pv2}	0.1208

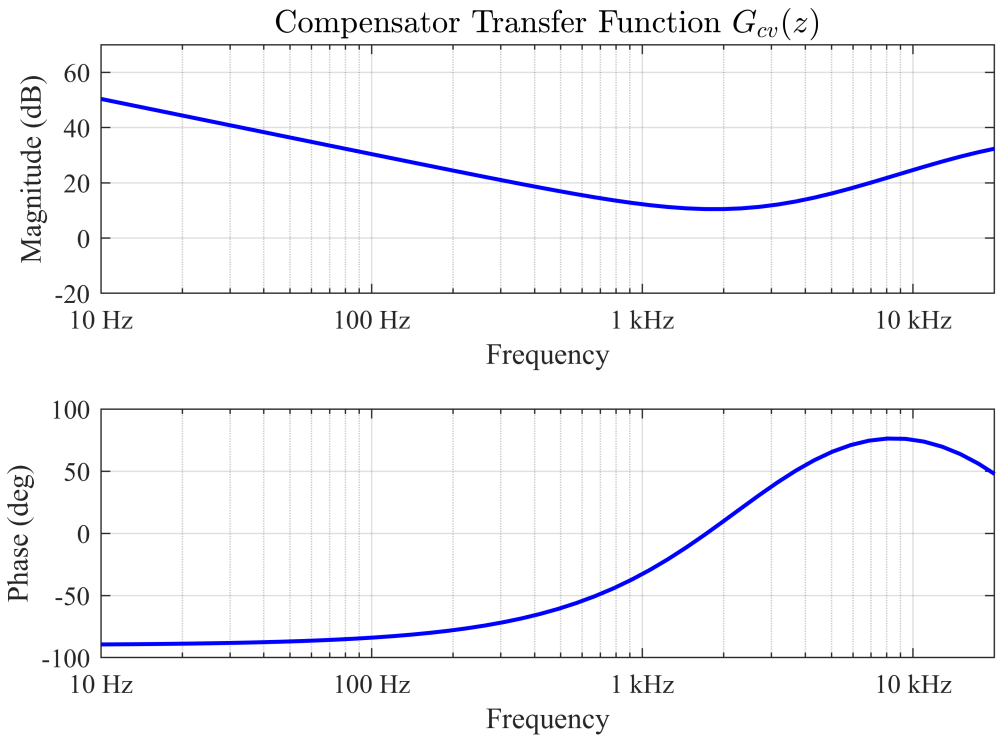
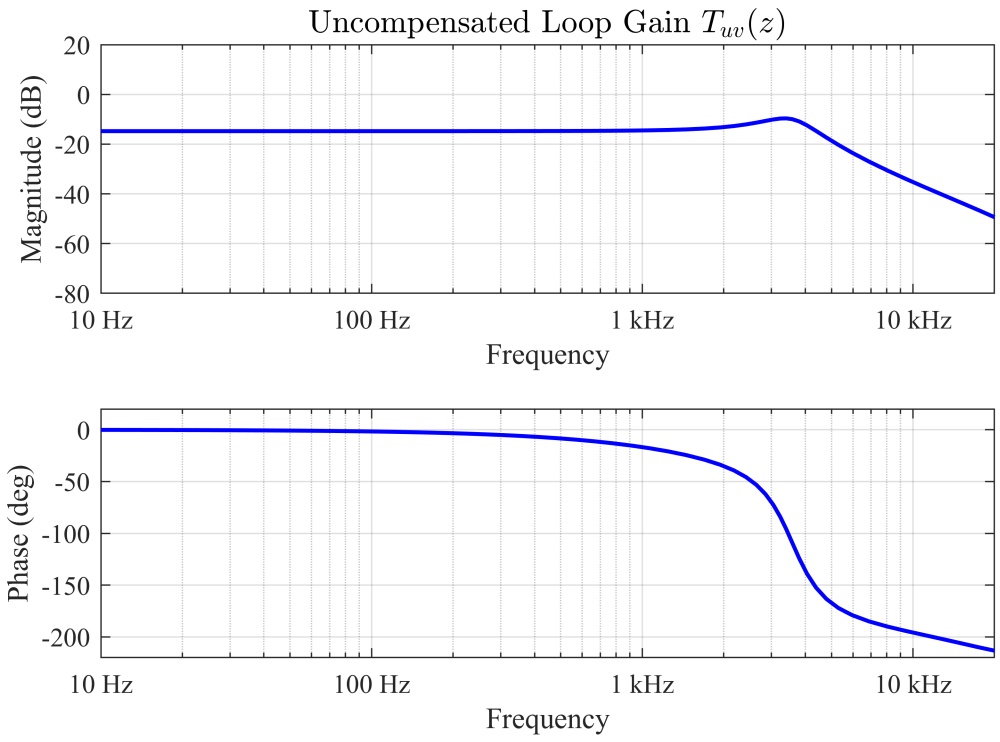
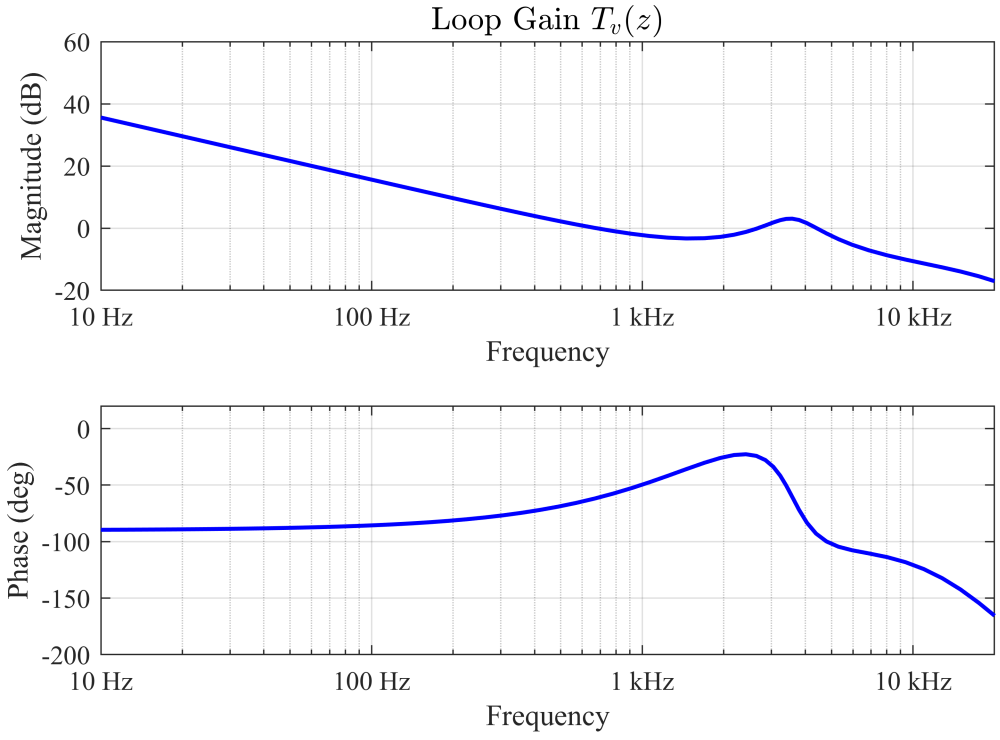


Fig. 5.31: Compensator plot for Inner Loop $G_{cv}(z)$.



(a)



(b)

Fig. 5.32: Plots for inner loop for cascade realization at 8 kW (a) Uncompensated Loop Gain $T_{uv}(z)$, (b) Loop Gain $T_v(z)$ with crossover frequency, f_{cv} of 4.4 kHz and phase margin of 86°.

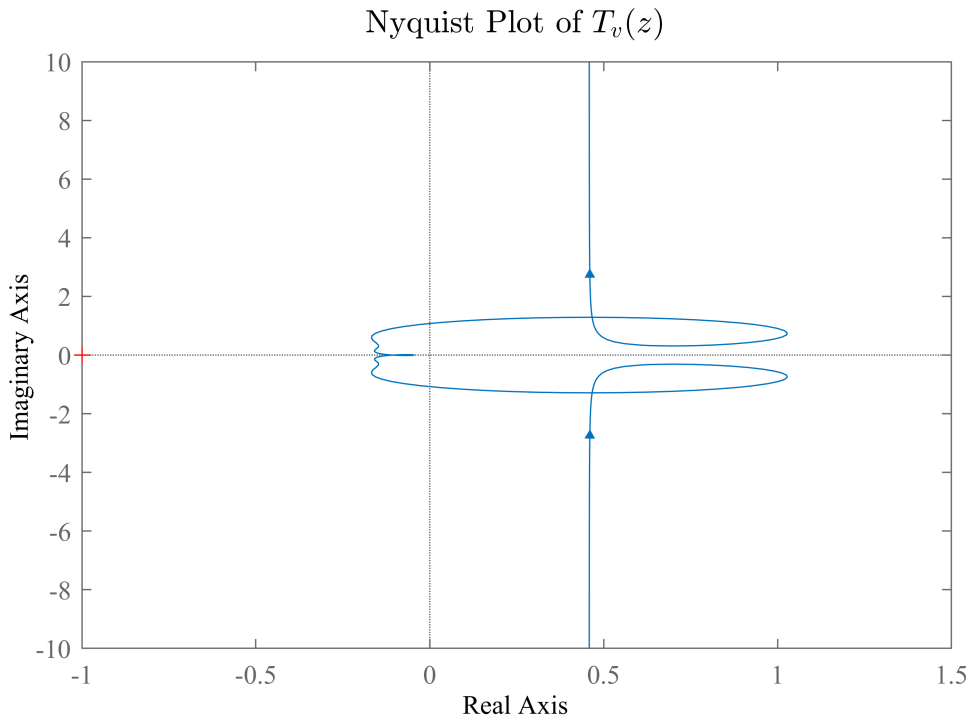


Fig. 5.33: Nyquist plot of Loop Gain $T_v(z)$.

The uncompensated loop gain for the outer loop is given in (5.213). The compensator is designed using the design process given in Section 5.3.2. The compensator in z-domain is given in (5.214), where the coefficients are given Table 5.10. The loop gain is given in (5.215).

$$T_{ui}(z) \approx \frac{r_{sense}}{H} \frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)} \tag{5.213}$$

$$G_{ci}(z) = G_{ciz0} \frac{(1+z^{-1})(1-C_{zi1}z^{-1})(1-C_{zi2}z^{-1})}{(1-z^{-1})(1-C_{pi1}z^{-1})(1-C_{pi2}z^{-1})} \tag{5.214}$$

$$T_i(z) = \frac{r_{sense}G_{ci}(z)}{H} \frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)} \tag{5.215}$$

Table 5.10: Coefficients for the compensator for cascade realization for the outer loop in z-domain at 8 kW.

Parameter	**Value**
G_{ciz0}	0.012
C_{zi1}	0.9982
C_{zi2}	0.9964
C_{pi1}	0.9964
C_{pi2}	0.9964

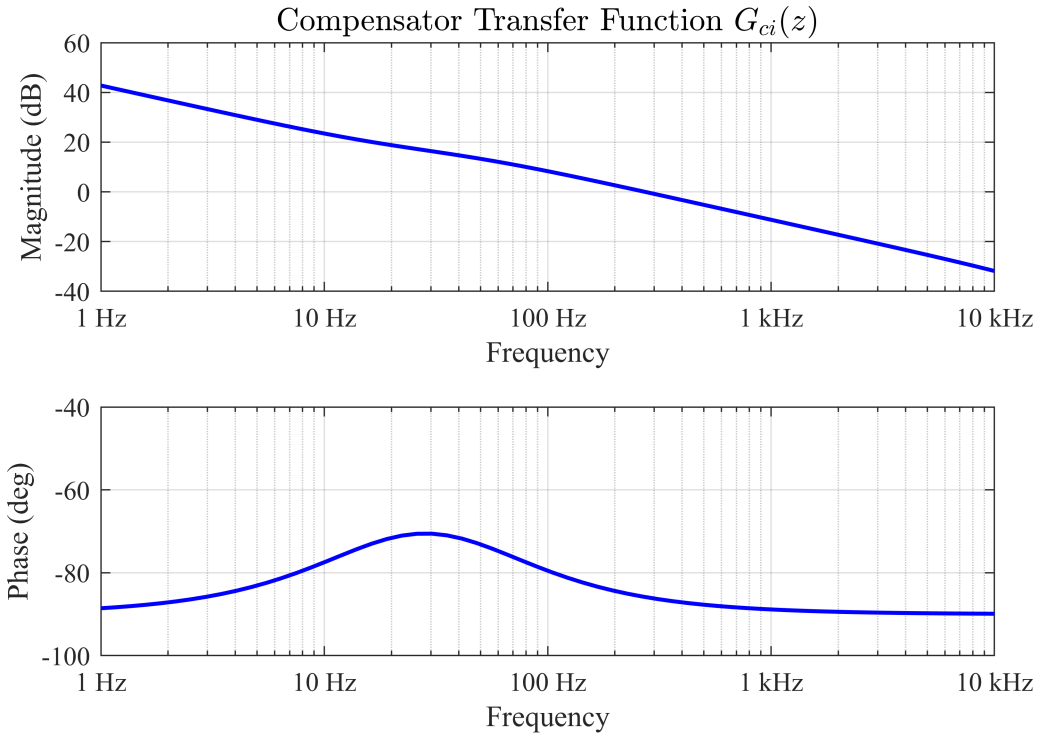
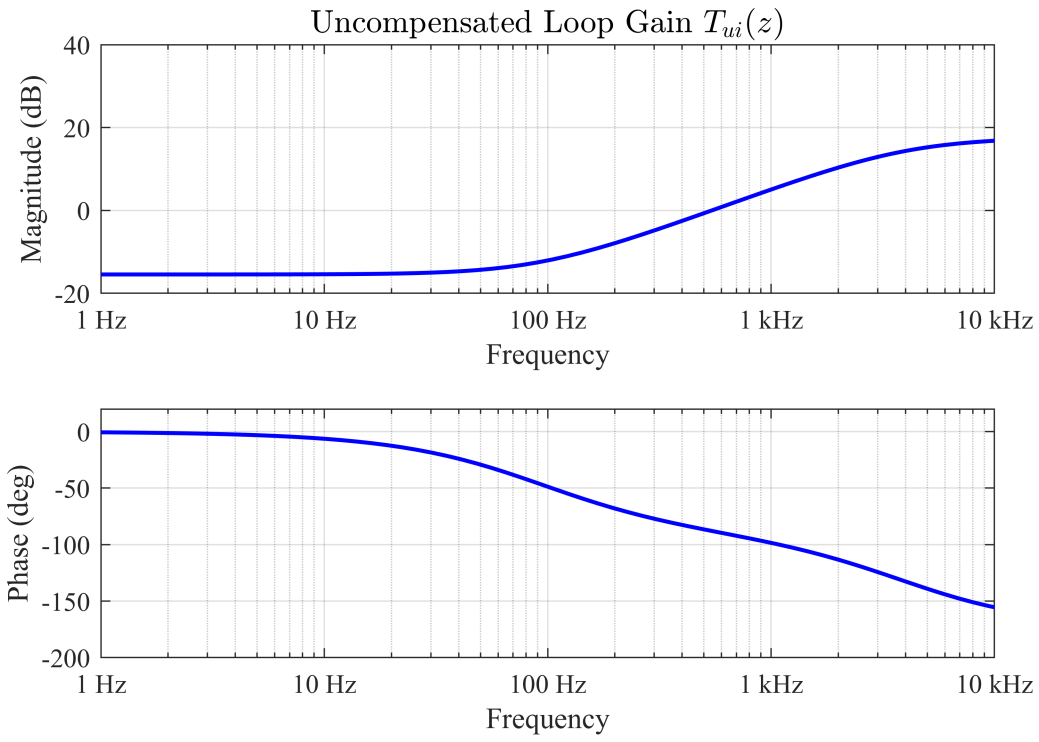
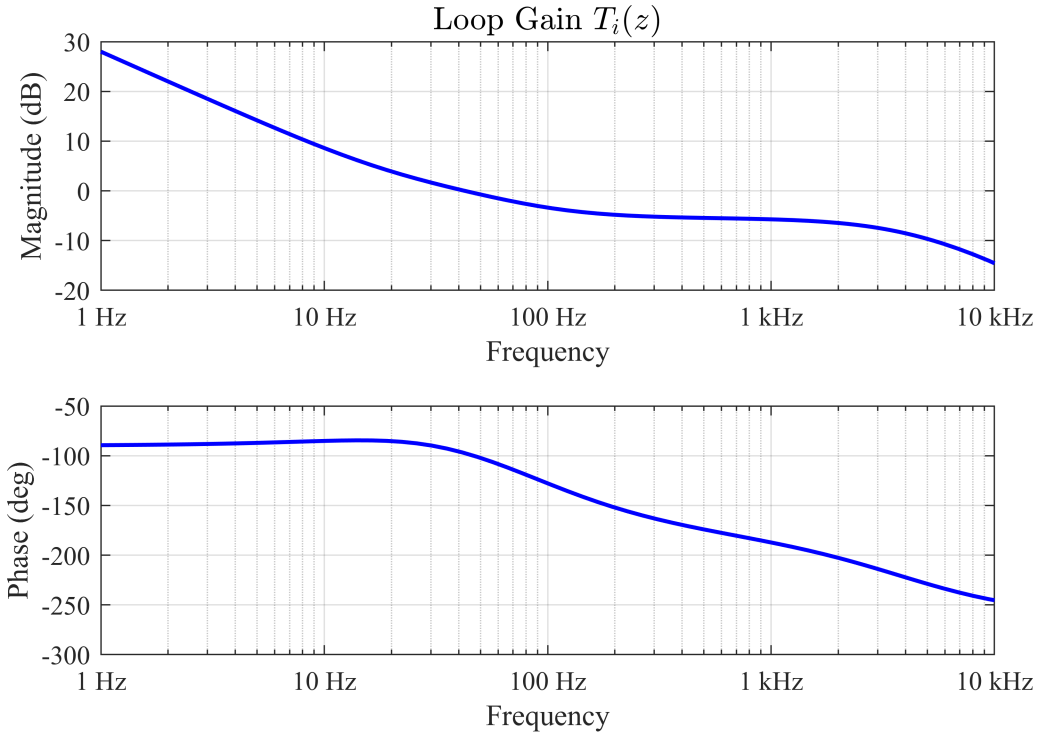


Fig. 5.34: Compensator plot for Inner Loop $G_{ci}(z)$.



(a)



(b)

Fig. 5.35: Plots for outer loop for cascade realization at 8 kW (a) Uncompensated Loop Gain $T_{ui}(z)$, (b) Loop Gain $T_i(z)$ with crossover frequency, f_{ci} of 42 Hz and phase margin of 82°.

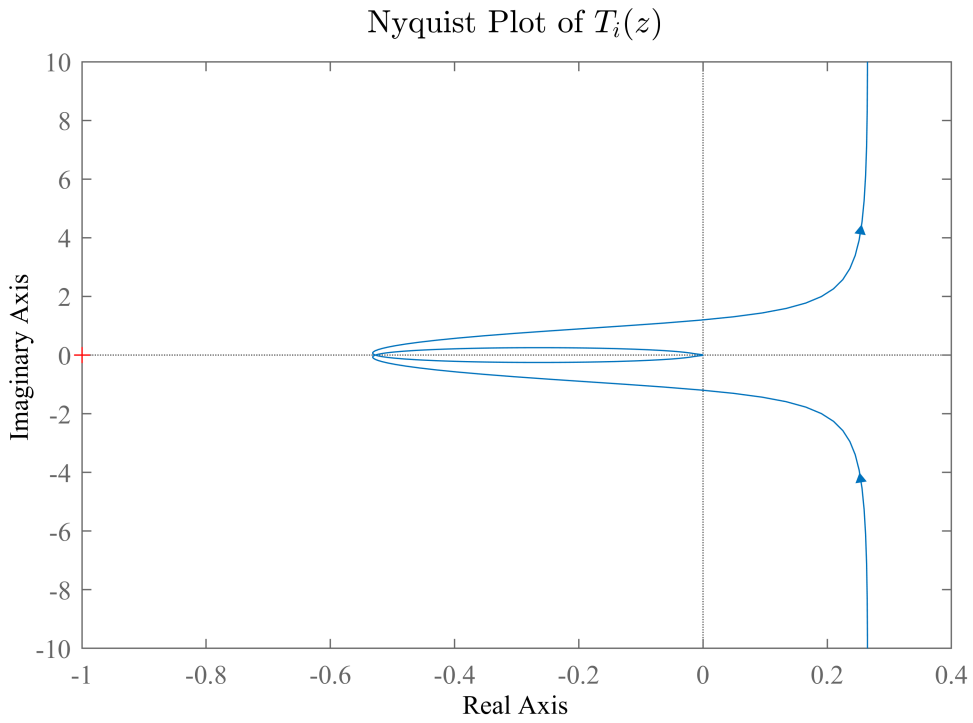


Fig. 5.36: Nyquist plot of Loop Gain $T_i(z)$.

5.5.3 Coefficient Quantization and fixed point implementation for Inner loop and Outer Loop at 50 kW

The quantization of any signal x is represented as $\tilde{x}$ and given in (5.216), where $Q_n[x]$ represents the quantization of signal x with a resolution of n bits. The quantization of the coefficients of $G_{cv}(z)$ for cascade realization is given in (5.217)-(5.222). The quantization for coefficients of $G_{ci}(z)$ for cascade realization is given in (5.223)-(5.227).

$$\tilde{x} = Q_n[x] \tag{5.216}$$

$$\tilde{G}_{cvz0} = Q_{12}[G_{cvz0}] = 001011111001_{\overline{2}} \times 2^{-5} = 23.78_{10} \tag{5.217}$$

$$\tilde{C}_{zv1} = Q_{10}[C_{zv1}] = 0110101100_{\overline{2}} \times 2^{-9} = 0.8359_{10} \tag{5.218}$$

$$\tilde{C}_{zv2} = Q_{10}[C_{zv2}] = 0110000111_{\overline{2}} \times 2^{-9} = 0.7637_{10} \tag{5.219}$$

$$\tilde{C}_{zv3} = Q_{10}[C_{zv3}] = 0110000111_{\overline{2}} \times 2^{-9} = 0.7637_{10} \tag{5.220}$$

$$\tilde{C}_{pv1} = Q_{12}[C_{pv1}] = 000011110111_{\overline{2}} \times 2^{-11} = 0.1206_{10} \tag{5.221}$$

$$\tilde{C}_{pv2} = Q_{12}[C_{pv2}] = 000011110111_{\overline{2}} \times 2^{-11} = 0.1206_{10} \tag{5.222}$$

$$\tilde{G}_{ciz0} = Q_{12}[G_{ciz0}] = 000000010111_{\overline{2}} \times 2^{-11} = 0.0112_{10} \tag{5.223}$$

$$\tilde{C}_{zi1} = Q_{12}[C_{zi1}] = 011111111100_{\overline{2}} \times 2^{-11} = 0.9980_{10} \tag{5.224}$$

$$\tilde{C}_{zi2} = Q_{12}[C_{zi2}] = 011111111001_{\overline{2}} \times 2^{-11} = 0.9966_{10} \tag{5.225}$$

$$\tilde{C}_{pi1} = Q_{12}[C_{pi1}] = 011111111001_{\overline{2}} \times 2^{-11} = 0.9966_{10} \tag{5.226}$$

$$\tilde{C}_{pi2} = Q_{12}[C_{pi2}] = 011111111001_{\overline{2}} \times 2^{-11} = 0.9966_{10}. \tag{5.227}$$

For fixed point implementation, any signal $\tilde{x}$ is represented as B2C quantity $[\tilde{x}]_q^n$ [85], where n represents the number of bits required to represent $\tilde{x}$ or the word length used to represent $\tilde{x}$ and q represents the scale factor of $\tilde{x}$ in terms of 2^q. For calculating the values of n and q, first, the largest value of $\tilde{x}$, that is $\tilde{x}_{max}$, is analyzed under the worst-case transients during control of the DC-DC converter. Then, the smallest nonzero value of $\tilde{x}$, $\tilde{x}_{min}$ is calculated. The scale factor 2^q is then determined to accurately represent the minimum value of $\tilde{x}$, that is $\tilde{x}_{min}$. The number of bits required to represent $\tilde{x}$ is then calculated using equations (5.228), and (5.229), [85], where $\mathrm{DR}_{hw}[\tilde{x}]_q^n$ represents the hardware dynamic range of $[\tilde{x}]_q^n$, and definition of ceil is followed from [85].

$$n = 1 + ceil\left(\frac{\mathrm{DR}_{hw}[\tilde{x}]_q^n}{20\log_{10} 2}\right) \tag{5.228}$$

$$\mathrm{DR}_{hw}[\tilde{x}]_q^n \triangleq 20\log_{10}\left(\frac{\tilde{x}_{max}}{2^q}\right). \tag{5.229}$$

For cascade realization of the inner loop, the hardware dynamic range is analyzed from Fig. 5.21. The steady state value of $\tilde{W}_{iv}$ is given in (5.231). The maximum value of $\tilde{W}_{iv}$ can be calculated from (5.232). The granularity of the error signal e_v is 1 due to the scaling of the inner loop by λ. Therefore, the minimum value or the resolution of $\tilde{W}_{iv}$ is also 1. The maximum and minimum value of $\tilde{W}_{1v}$ is calculated from (5.233), and (5.234). The maximum and minimum values of the signals at each stage of the cascade realization of the compensator are similarly calculated by modifying equations (5.233) and (5.234) at each

stage of the compensator. The fixed-point implementation for the inner loop for cascade realization is shown in Fig. 5.37.

$$G_{cv}(z) = G_{cvz0}\frac{(1 - C_{zv1}z^{-1})(1 - C_{zv2}z^{-1})(1 - C_{zv3}z^{-1})}{(1 - z^{-1})(1 - C_{pv1}z^{-1})(1 - C_{pv2}z^{-1})} \tag{5.230}$$

$$\tilde{W}_{iv} = \frac{\tilde{u}(1 - \tilde{C}_{pv1})(1 - \tilde{C}_{pv2})}{\tilde{G}_{cvz0}(1 - \tilde{C}_{zv1})(1 - \tilde{C}_{zv2})(1 - \tilde{C}_{zv3})} \tag{5.231}$$

$$\tilde{W}_{iv_{max}} = \frac{(N_r - 1)(1 - \tilde{C}_{pv1})(1 - \tilde{C}_{pv2})}{\tilde{G}_{cvz0}(1 - \tilde{C}_{zv1})(1 - \tilde{C}_{zv2})(1 - \tilde{C}_{zv3})} \tag{5.232}$$

$$\tilde{W}_{1v_{max}} = \frac{(N_r - 1)(1 - \tilde{C}_{pv2})}{\tilde{G}_{cvz0}(1 - \tilde{C}_{zv1})(1 - \tilde{C}_{zv2})(1 - \tilde{C}_{zv3})} \tag{5.233}$$

$$\tilde{W}_{iv_{min}} = \frac{\tilde{W}_{1v_{min}}}{(1 - \tilde{C}_{pv1})} = \frac{1}{(1 - \tilde{C}_{pv1})}. \tag{5.234}$$

For cascaded realization of the outer loop, the hardware dynamic range is analyzed from Fig. 5.23. The steady state value of $\tilde{W}_{ii}$ is given in (5.236). The maximum value of $\tilde{W}_{ii}$ can be calculated from (5.237). The granularity of the error signal e_i is 1, and the minimum value or the resolution of $\tilde{W}_{ii}$ is also 1. The maximum and minimum value of $\tilde{W}_{1i}$ is calculated from (5.238), and (5.239). The maximum and minimum values of the signals at each stage of the cascade realization of the compensator are similarly calculated by modifying equations (5.238) and (5.239) at each stage of the compensator. The fixed-point implementation for the outer loop for cascade realization is shown in Fig. 5.38.

$$G_{ci}(z) = G_{ciz0}\frac{(1 + z^{-1})(1 - C_{zi1}z^{-1})(1 - C_{zi2}z^{-1})}{(1 - z^{-1})(1 - C_{pi1}z^{-1})(1 - C_{pi2}z^{-1})} \tag{5.235}$$

$$\tilde{W}_{ii} = \frac{\tilde{V}_{ref}(1 - \tilde{C}_{pi1})(1 - \tilde{C}_{pi2})}{\tilde{G}_{ciz0}(1 + 1)(1 - \tilde{C}_{zi2})(1 - \tilde{C}_{zi2})} \tag{5.236}$$

$$\tilde{W}_{ii_{max}} = \frac{V_{ref_{max}}(1-\tilde{C}_{pi1})(1-\tilde{C}_{pi2})}{\tilde{G}_{ciz0}(1+1)(1-\tilde{C}_{zi2})(1-\tilde{C}_{zi2})} \tag{5.237}$$

$$\tilde{W}_{1i_{max}} = \frac{V_{ref_{max}}(1-\tilde{C}_{pi2})}{\tilde{G}_{ciz0}(1+1)(1-\tilde{C}_{zi2})(1-\tilde{C}_{zi2})} \tag{5.238}$$

$$\tilde{W}_{ii_{min}} = \frac{\tilde{W}_{1i_{min}}}{(1-\tilde{C}_{pi1})} = \frac{1}{(1-\tilde{C}_{pi1})}. \tag{5.239}$$

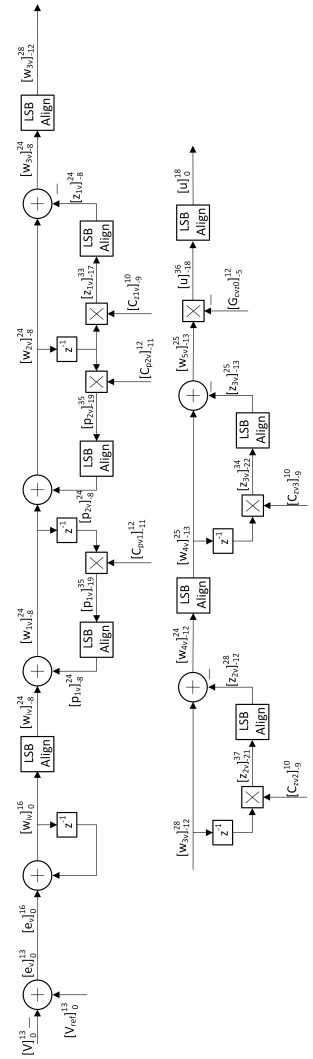


Fig. 5.37: Fixed point implementation for cascade realization of $G_{cv}(z)$.

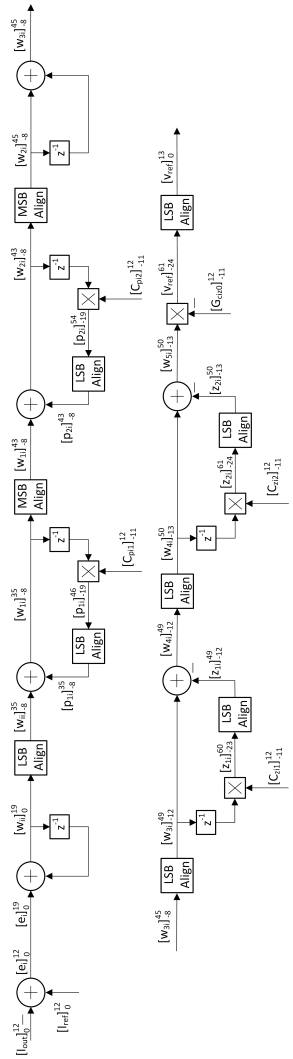


Fig. 5.38: Fixed point implementation for cascade realization of $G_{ci}(z)$.

5.6 Matlab Plots and Fixed Point Implementation for Parallel Realization

5.6.1 Matlab plots for Inner loop and Outer Loop for Parallel Realization at 50 kW

Table 5.11: Parameters for 2-Transistor ZVS-QSW boost for Parallel Realization at 50 kW.

Parameter	**Value**
f_s	70 kHz
P_{out}	50 kW
V_{out}	600 V
V_{in}	400 V
I_L	125 A
I_{out}	83 A
L_r	6.8 μH
C_r	6.66 nF
C_{in}	440 μF
C_{out}	200 μF
r_L	4.77 mΩ
r_{in}	0.45 mΩ
r_c	1 mΩ
r_o	300 mΩ
D	0.33
H	0.005
r_{sense}	0.005
N_r	3428
nA/D	12
f_{clk}	240 MHz

The specifications for the DC-DC converter for control design for parallel realization at 50 kW are given in Table 5.11. The uncompensated loop gain for parallel realization for the inner loop with the scaling factor is given in (5.240), where the scaling factor λ is given in (5.241). The compensator is designed using the design process given in Section 5.3.1. The frequencies in the p-domain given in (5.242), used for designing the compensator at

crossover frequency $\omega_{cv}^{'}$ for parallel realization, are given in Table 5.12.

$$T_{uv}(z) = \frac{HG_{vd}(z)}{\lambda} \tag{5.240}$$

$$\lambda = q_{v_s}^{(A/D)} N_r \tag{5.241}$$

$$G_{cv}^{'}(p) = G_{cv0} \frac{\left(1 + \frac{\omega_{Lv}^{'}}{p}\right)\left(1 + \frac{p}{\omega_{z1v}^{'}}\right)\left(1 + \frac{p}{\omega_{z2v}^{'}}\right)}{\left(1 + \frac{p}{\omega_{p1v}^{'}}\right)\left(1 + \frac{p}{\omega_{p2v}^{'}}\right)}. \tag{5.242}$$

Table 5.12: Frequencies for the compensator for the inner loop for parallel realization at 50 kW.

Parameter	**Value**
f_{cv}	5.1 kHz
$f_{Lv}^{'}$	1.5 kHz
$f_{z1v}^{'}$	2.1 kHz
$f_{p1v}^{'}$	12.27 kHz
$f_{z2v}^{'}$	2.6 kHz
$f_{p2v}^{'}$	9.7 kHz

The compensator in z-domain is given in (5.243),where the coefficients are given Table 5.13. The loop gain is given in (5.244).

$$G_{cv}(z) = G_{cvz0} \frac{(1 - C_{zv1}z^{-1})(1 - C_{zv2}z^{-1})(1 - C_{zv3}z^{-1})}{(1 - z^{-1})(1 - C_{pv1}z^{-1})(1 - C_{pv2}z^{-1})}. \tag{5.243}$$

$$T_v(z) = \frac{HG_{vd}(z)G_{cv}(z)}{\lambda}. \tag{5.244}$$

For the parallel realization of $G_{cv}(z)$ in (5.243), the $G_{cv}(z)$ can be expressed as (5.245), where B_{1v}, B_{2v} and B_{3v} are calculated in (5.178), (5.179), and (5.180) respectively and given in Table 5.14.

Table 5.13: Coefficients for compensator transfer function for inner loop for parallel realization in z-domain at 50 kW.

Parameter	**Value**
G_{cvz0}	4.73
C_{zv1}	0.8739
C_{zv2}	0.8272
C_{zv3}	0.7876
C_{pv1}	0.3906
C_{pv2}	0.2896

$$G_{cv}(z) = G_{cvz0} + \frac{B_{1v}}{(1 - z^{-1})} + \frac{B_{2v}}{(1 - C_{pv1}z^{-1})} + \frac{B_{3v}}{(1 - C_{pv2}z^{-1})}. \tag{5.245}$$

Table 5.14: Coefficients for the compensator for parallel realization for the inner loop in z-domain at 50 kW.

Parameter	**Value**
G_{cvz0}	4.73
B_{1v}	0.05
B_{2v}	6.45
B_{3v}	10.33
C_{pv1}	0.3906
C_{pv2}	0.2896

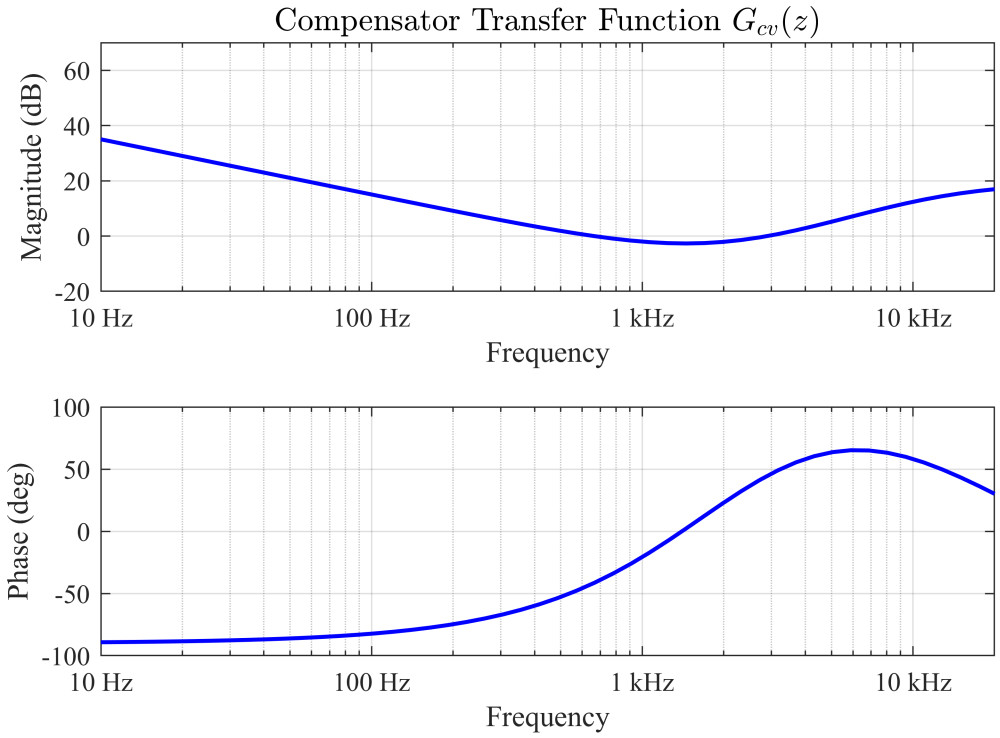
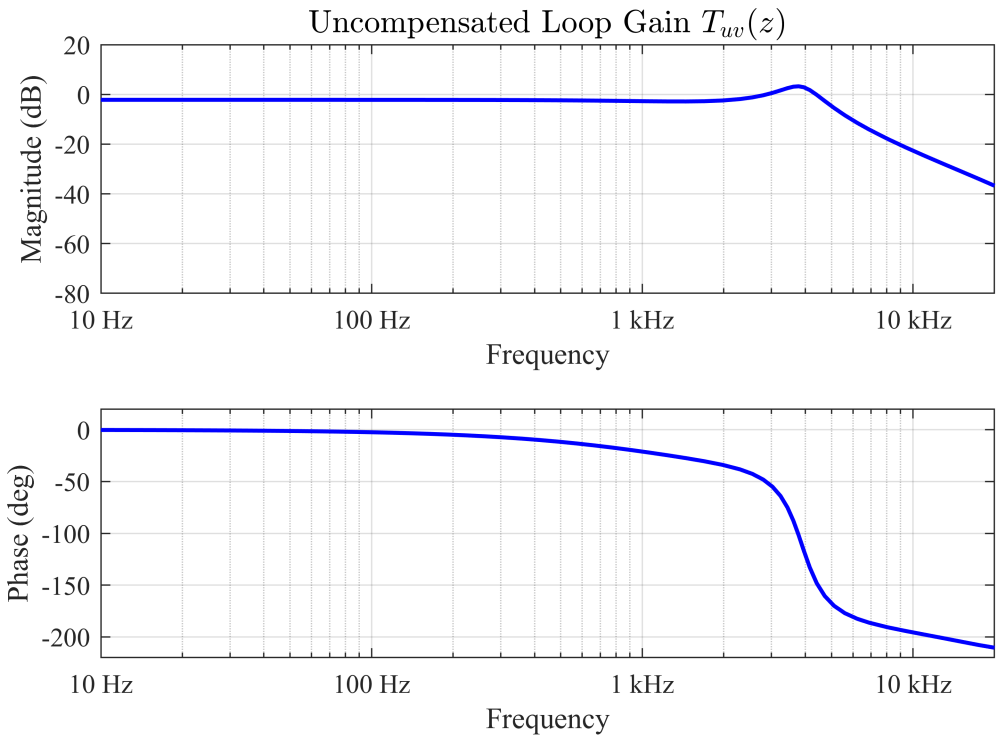
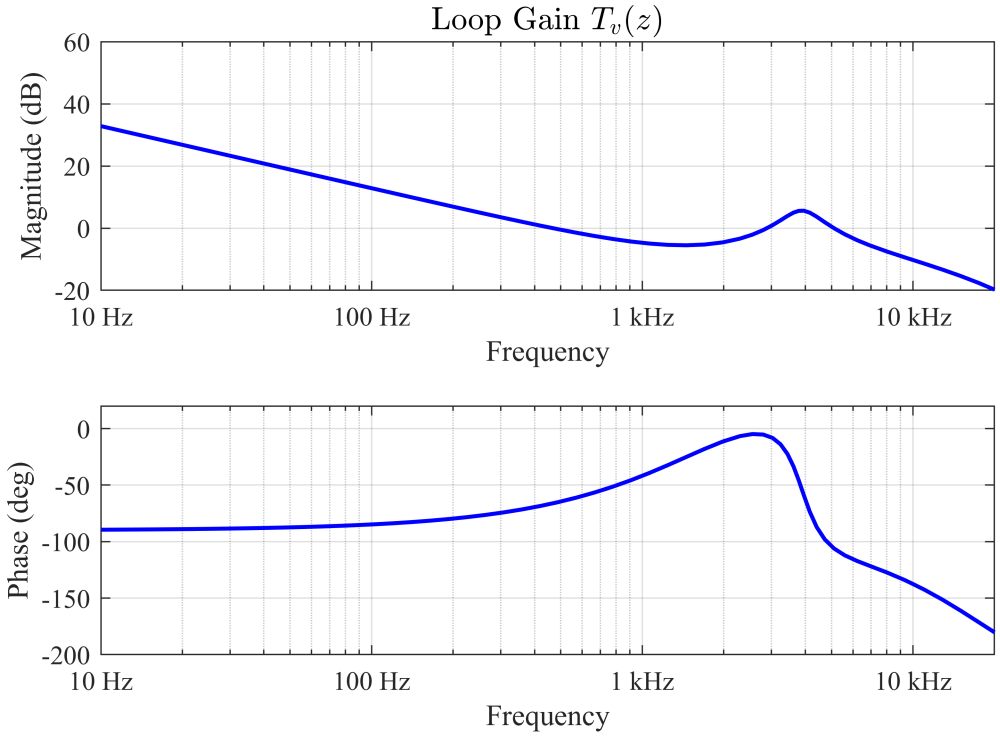


Fig. 5.39: Compensator plot for inner loop $G_{cv}(z)$ for parallel realization at 50 kW.



(a)



(b)

Fig. 5.40: Plots for inner loop for parallel realization at 50 kW (a) Uncompensated Loop Gain $T_{uv}(z)$, (b) Loop Gain $T_v(z)$ with crossover frequency, f_{cv} of 5.1 kHz and phase margin of 73°.

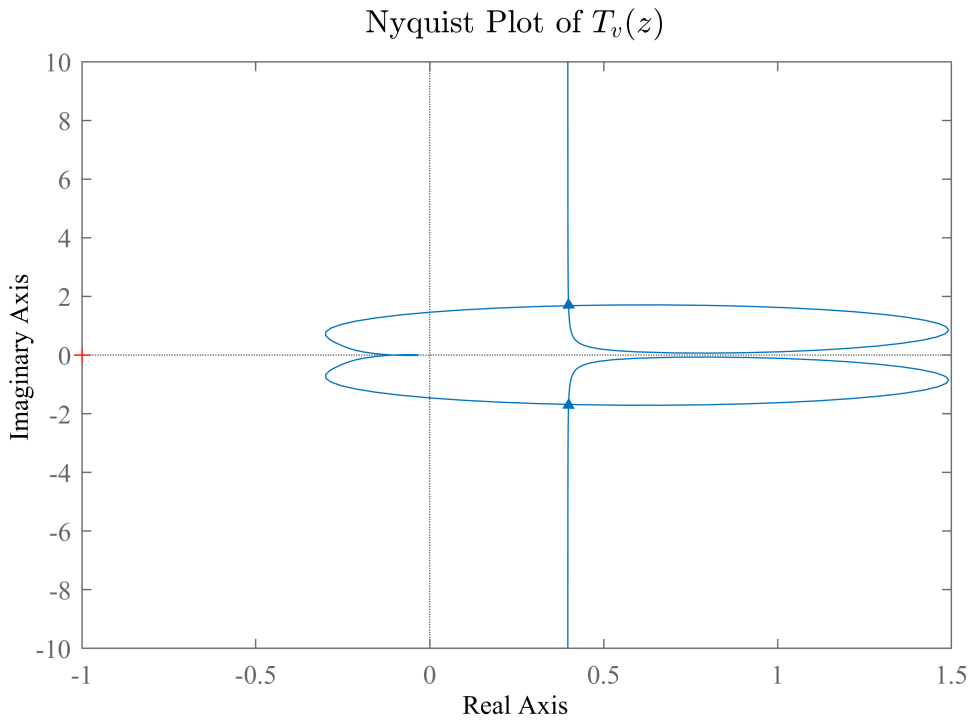


Fig. 5.41: Nyquist plot of Loop Gain $T_v(z)$ for parallel realization at 50 kW.

The uncompensated loop gain for the outer loop is given in (5.246). The compensator is designed using the design process given in Section 5.3.2. The frequencies in the p-domain given in (5.247), used for designing the compensator at crossover frequency $\omega_{ci}^{'}$ for parallel realization, are given in Table 5.15.

$$T_{ui}(z) \approx \frac{r_{sense}}{H} \frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)} \tag{5.246}$$

$$G_{ci}^{'}(p) = G_{ci0} \frac{\left(1 + \frac{\omega_{Li}^{'}}{p}\right)}{\left(1 + \frac{p}{\omega_{pi}^{'}}\right)}. \tag{5.247}$$

Table 5.15: Frequencies for the compensator for the outer loop for parallel realization at 50 kW.

Parameter	**Value**
f_{ci}	40 Hz
$f_{Li}^{'}$	20 Hz
$f_{pi}^{'}$	40 Hz

The compensator in z-domain is given in (5.248), where the coefficients are given in Table 5.16. The loop gain is given in (5.249).

$$G_{ci}(z) = G_{ciz0} \frac{(z+1)(z - C_{zi1})}{(z-1)(z - C_{pi1})} \tag{5.248}$$

$$T_i(z) = \frac{r_{sense} G_{ci}(z)}{H} \frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)}. \tag{5.249}$$

For the parallel realization of $G_{ci}(z)$ in (5.248), the $G_{ci}(z)$ can be expressed as (5.250), where B_{1i} and B_{2i} are calculated in (5.196), and (5.197) respectively, and given in Table 5.17.

$$G_{ci}(z) = G_{ciz0} + \frac{B_{1i}}{(1 - z^{-1})} + \frac{B_{2i}}{(1 - C_{pi1} z^{-1})}. \tag{5.250}$$

Table 5.16: Coefficients for compensator transfer function for parallel realization for outer loop in z-domain at 50 kW.

Parameter	**Value**
G_{ciz0}	0.0113
C_{zi1}	0.9982
C_{pi1}	0.9964

Table 5.17: Coefficients for the compensator for parallel realization for the outer loop in the z-domain at 50 kW.

Parameter	**Value**
G_{ciz0}	0.0113
B_{1i}	0.0113
B_{2i}	0.0113
C_{pi1}	0.9964

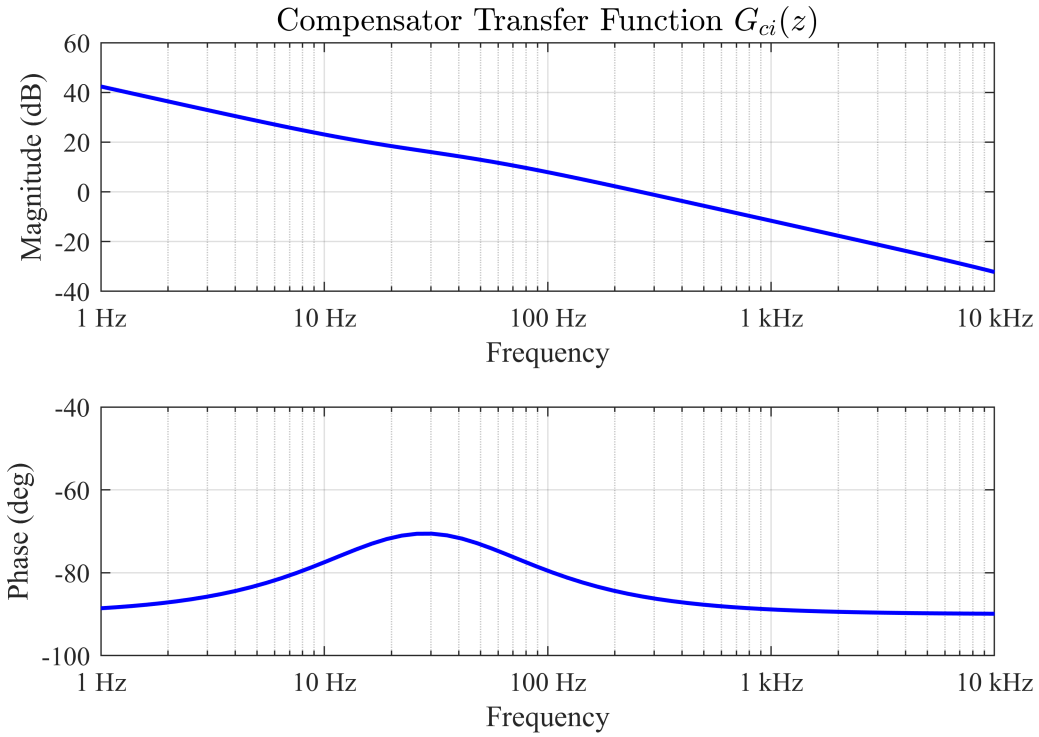
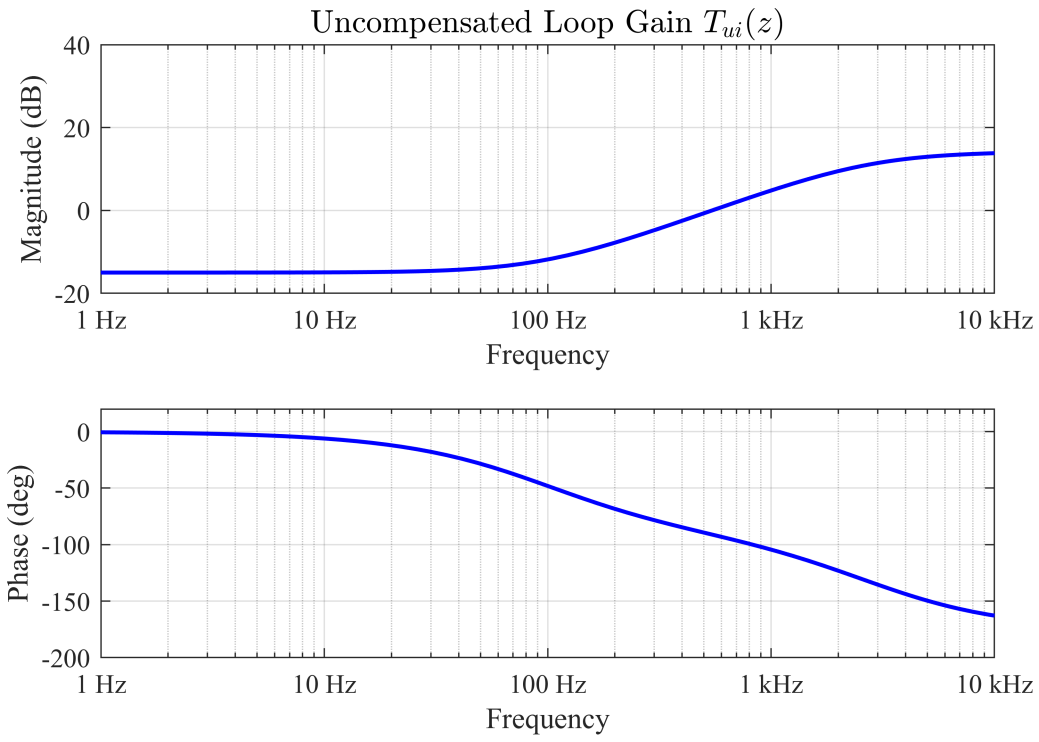
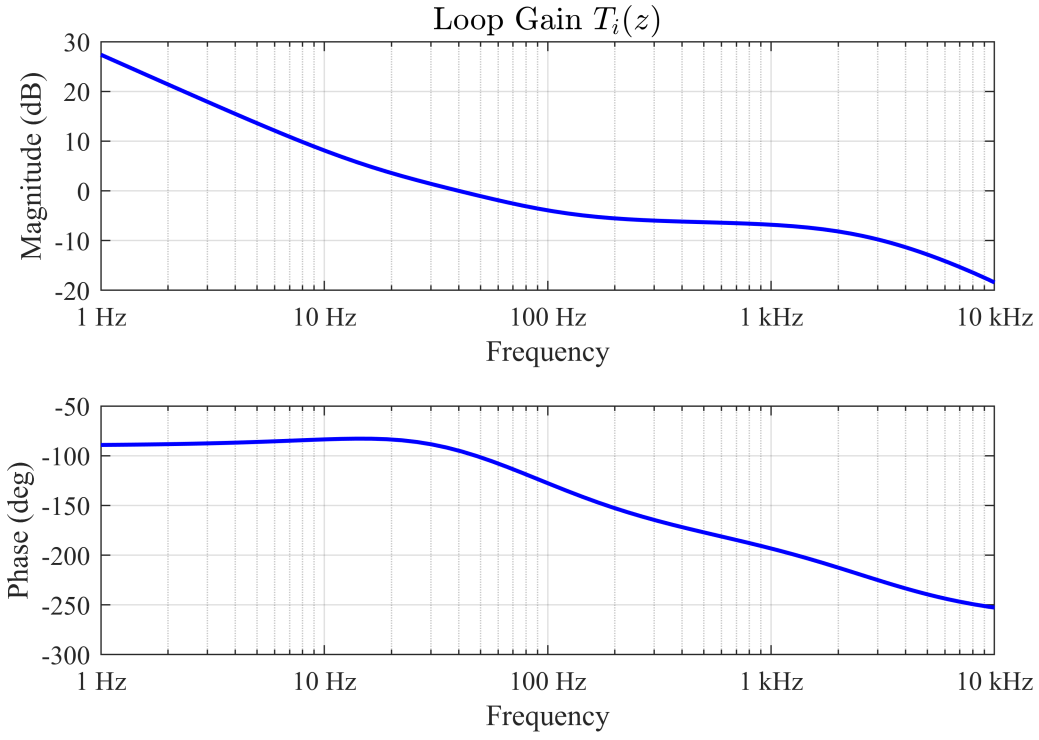


Fig. 5.42: Compensator plot for outer loop $G_{ci}(z)$ for parallel realization at 50 kW.



(a)



(b)

Fig. 5.43: Plots for outer loop for parallel realization at 50 kW (a) Uncompensated Loop Gain $T_{ui}(z)$, (b) Loop Gain $T_i(z)$ with crossover frequency, f_{ci} of 40 Hz and phase margin of 85°.

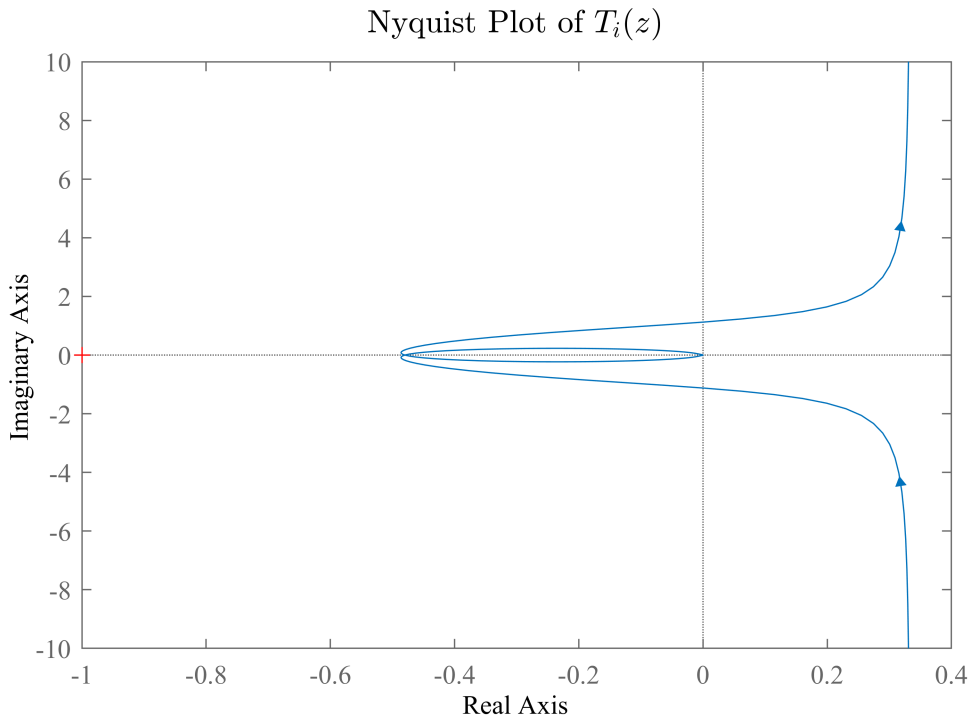


Fig. 5.44: Nyquist plot of Loop Gain $T_i(z)$ for parallel realization at 50 kW.

5.6.2 Matlab plots for Inner loop and Outer Loop for Parallel Realization at 8 kW

Table 5.18: Parameters for 2-Transistor ZVS-QSW boost for Parallel Realization at 8 kW.

Parameter	**Value**
f_s	70 kHz
P_{out}	8 kW
V_{out}	250 V
V_{in}	160 V
I_L	50 A
I_{out}	32 A
L_r	6.8 μH
C_r	6.66 nF
C_{in}	440 μF
C_{out}	200 μF
r_L	4.77 mΩ
r_{in}	0.45 mΩ
r_c	1 mΩ
r_o	300 mΩ
D	0.64
H	0.005
r_{sense}	0.005
N_r	3428
nA/D	12
f_{clk}	240 MHz

The specifications for the DC-DC converter for control design for parallel realization for 8 kW testing of the full system are given in Table 5.18. The compensator for the inner loop is designed using the design process given in Section 5.3.1. The frequencies in the p-domain given in (5.251), used for designing the compensator at crossover frequency $\omega_{cv}^{'}$ for parallel realization for 8 kW, are given in Table 5.19.

$$G_{cv}^{'}(p) = G_{cv0}\frac{\left(1+\frac{\omega_{Lv}^{'}}{p}\right)\left(1+\frac{p}{\omega_{z1v}^{'}}\right)\left(1+\frac{p}{\omega_{z2v}^{'}}\right)}{\left(1+\frac{p}{\omega_{p1v}^{'}}\right)\left(1+\frac{p}{\omega_{p2v}^{'}}\right)} \tag{5.251}$$

Table 5.19: Frequencies for the compensator for the inner loop for parallel realization at 8 kW.

Parameter	**Value**
f_{cv}	5 kHz
$f_{Lv}^{'}$	1.5 kHz
$f_{z1v}^{'}$	2.1 kHz
$f_{p1v}^{'}$	12.27 kHz
$f_{z2v}^{'}$	2.6 kHz
$f_{p2v}^{'}$	9.7 kHz

The compensator in z-domain is given in (5.252), where the coefficients are given Table 5.20. The loop gain is given in (5.253).

$$G_{cv}(z) = G_{cvz0}\frac{(1-C_{zv1}z^{-1})(1-C_{zv2}z^{-1})(1-C_{zv3}z^{-1})}{(1-z^{-1})(1-C_{pv1}z^{-1})(1-C_{pv2}z^{-1})} \tag{5.252}$$

$$T_v(z) = \frac{HG_{vd}(z)G_{cv}(z)}{\lambda}. \tag{5.253}$$

Table 5.20: Coefficients for compensator transfer function for inner loop for parallel realization in z-domain at 8 kW.

Parameter	**Value**
G_{cvz0}	11.35
C_{zv1}	0.8739
C_{zv2}	0.8272
C_{zv3}	0.7876
C_{pv1}	0.3906
C_{pv2}	0.2896

For the parallel realization of $G_{cv}(z)$ in (5.252), the $G_{cv}(z)$ can be expressed as (5.254), where B_{1v}, B_{2v} and B_{3v} are calculated in (5.178), (5.179), and (5.180) respectively and given in Table 5.21.

$$G_{cv}(z) = G_{cvz0} + \frac{B_{1v}}{(1 - z^{-1})} + \frac{B_{2v}}{(1 - C_{pv1}z^{-1})} + \frac{B_{3v}}{(1 - C_{pv2}z^{-1})}. \tag{5.254}$$

Table 5.21: Coefficients for the compensator for parallel realization for the inner loop in z-domain at 8 kW.

Parameter	**Value**
G_{cvz0}	11.35
B_{1v}	0.12
B_{2v}	15.49
B_{3v}	24.8
C_{pv1}	0.3906
C_{pv2}	0.2896

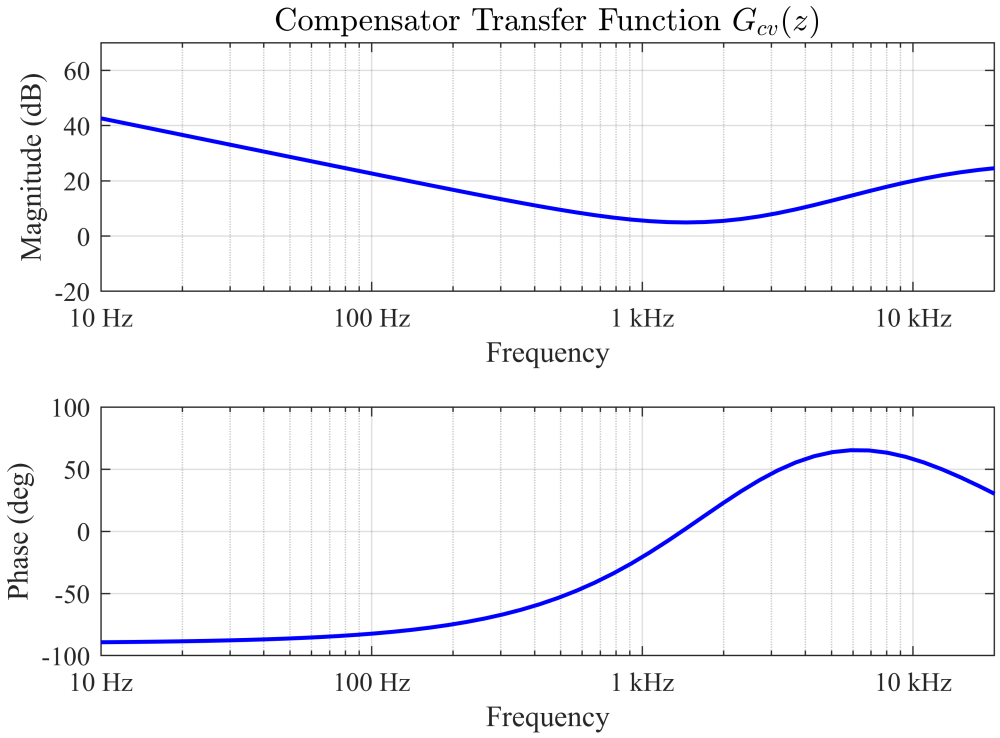
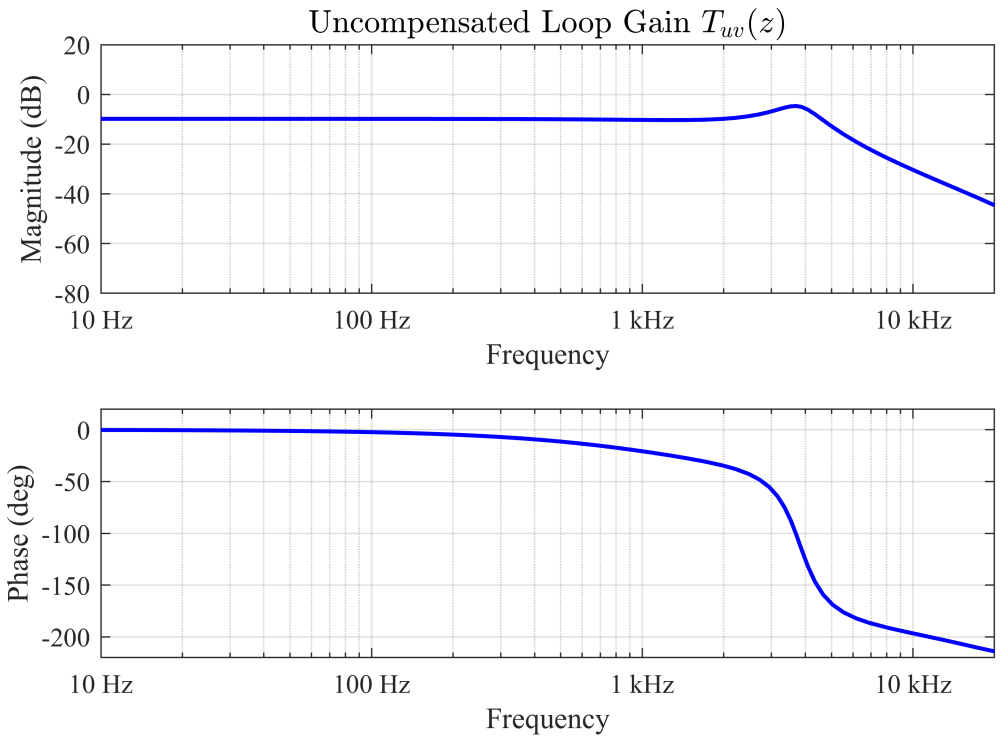
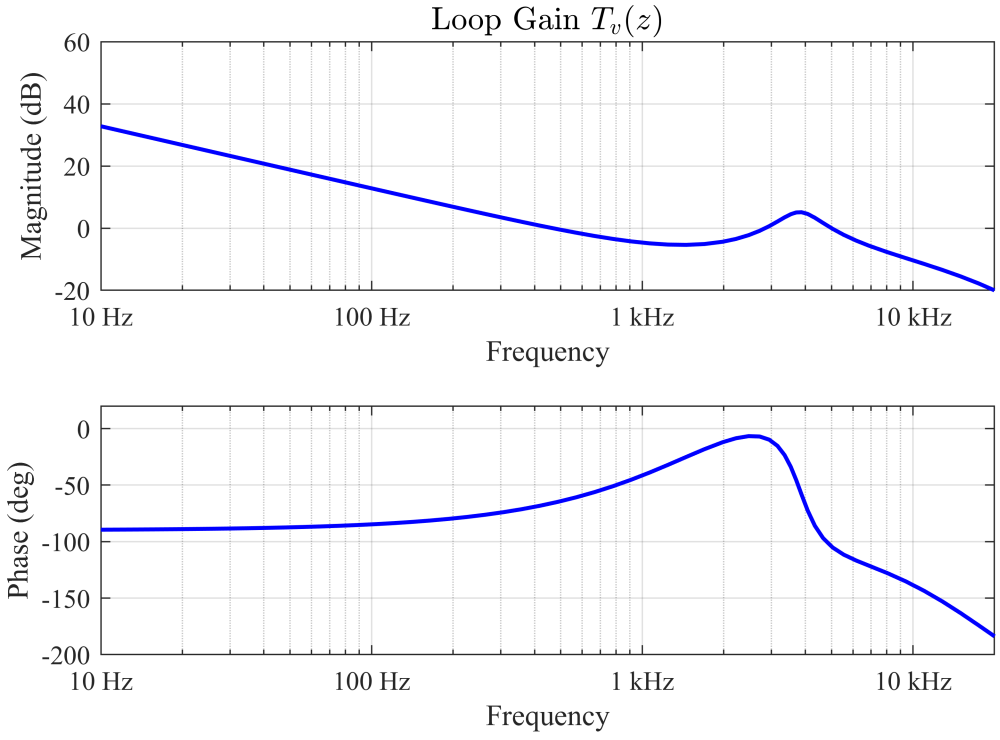


Fig. 5.45: Compensator plot for Inner Loop $G_{cv}(z)$ for parallel realization at 8 kW.



(a)



(b)

Fig. 5.46: Plots for Inner Loop for parallel realization at 8 kW(a) Uncompensated Loop Gain $T_{uv}(z)$, (b) Loop Gain $T_v(z)$ with crossover frequency, f_{cv} of 5 kHz and phase margin of 75°.

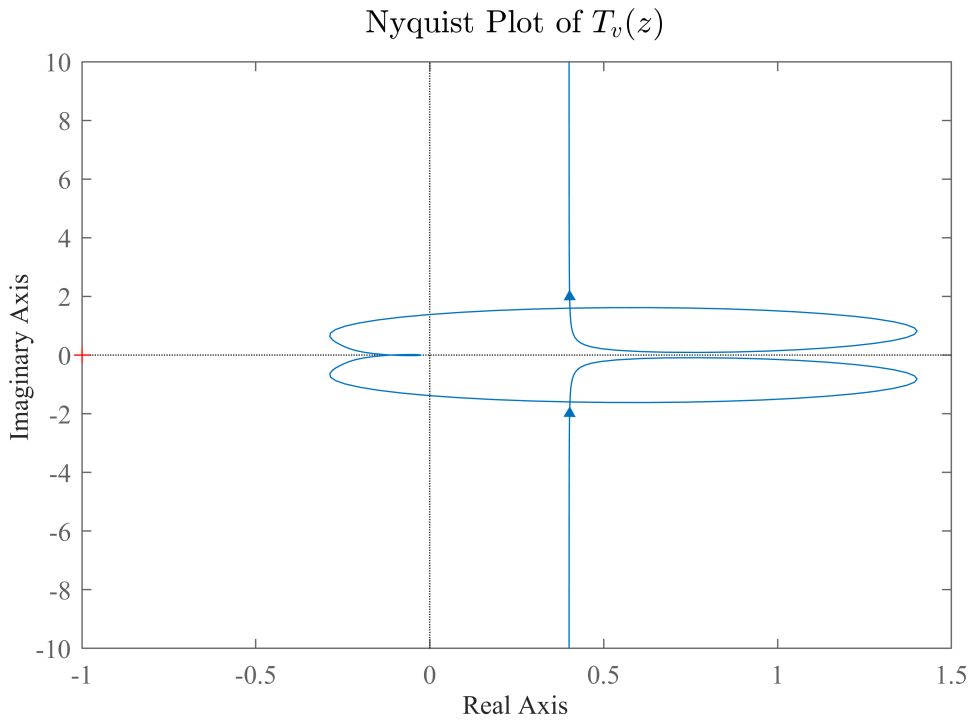


Fig. 5.47: Nyquist plot of Loop Gain $T_v(z)$ for parallel realization at 8 kW.

The compensator for the outer loop is designed similarly using the design process given in Section 5.3.2. The frequencies in the p-domain given in (5.255), used for designing the compensator at crossover frequency $\omega_{ci}^{'}$ for parallel realization, are given in Table 5.22.

$$G_{ci}^{'}(p) = G_{ci0}\frac{\left(1+\frac{\omega_{Li}^{'}}{p}\right)}{\left(1+\frac{p}{\omega_{pi}^{'}}\right)}. \tag{5.255}$$

Table 5.22: Frequencies for the compensator for the outer loop for parallel realization at 8 kW.

Parameter	**Value**
f_{ci}	40 Hz
$f_{Li}^{'}$	20 Hz
$f_{pi}^{'}$	40 Hz

The compensator in z-domain is given in (5.256), where the coefficients are given Table 5.23. The loop gain is given in (5.257).

$$G_{ci}(z) = G_{ciz0}\frac{(z+1)(z-C_{zi1})}{(z-1)(z-C_{pi1})} \tag{5.256}$$

$$T_i(z) = \frac{r_{sense}G_{ci}(z)}{H}\frac{G_{i_{out}d}(z)}{G_{v_{in}d}(z)}. \tag{5.257}$$

For the parallel realization of $G_{ci}(z)$ in (5.256), the $G_{ci}(z)$ can be expressed as (5.258), where

Table 5.23: Coefficients for compensator transfer function for parallel realization for outer loop in z-domain at 8 kW.

Parameter	**Value**
G_{ciz0}	0.0113
C_{zi1}	0.9982
C_{pi1}	0.9964

B_{1i} and B_{2i} are calculated in (5.196), and (5.197) respectively, and given in Table 5.24.

$$G_{ci}(z) = G_{ciz0} + \frac{B_{1i}}{(1 - z^{-1})} + \frac{B_{2i}}{(1 - C_{pi1}z^{-1})} \tag{5.258}$$

Table 5.24: Coefficients for the compensator for parallel realization for the outer loop in z-domain at 8 kW.

Parameter	**Value**
G_{ciz0}	0.0113
B_{1i}	0.0113
B_{2i}	0.0113
C_{pi1}	0.9964

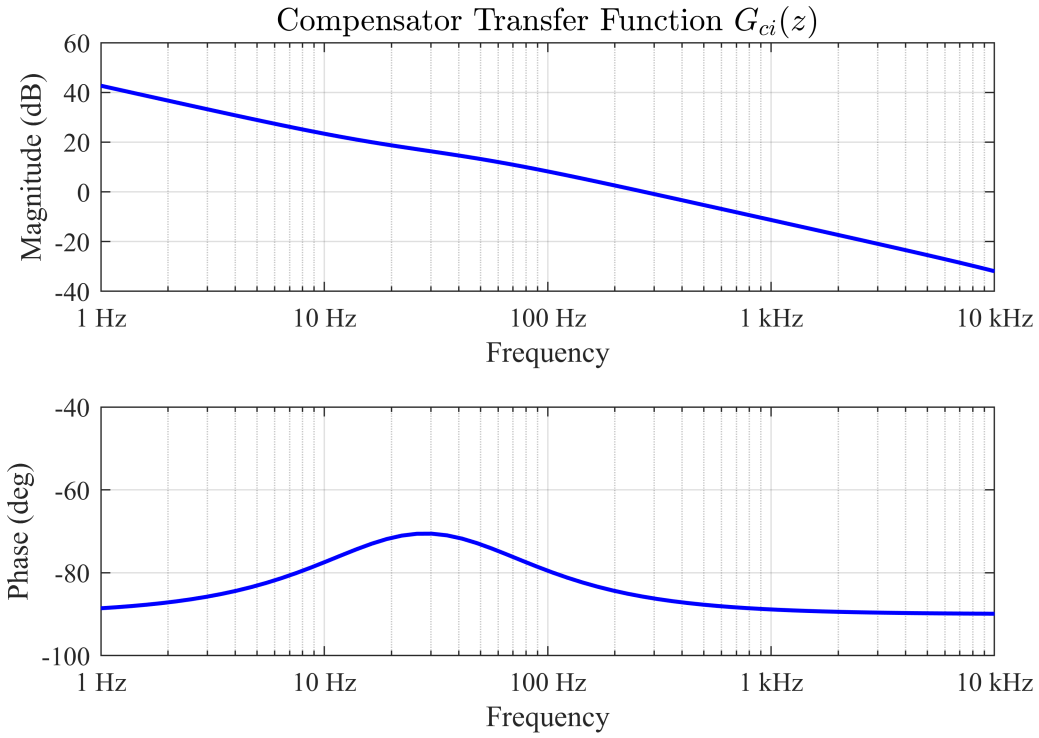
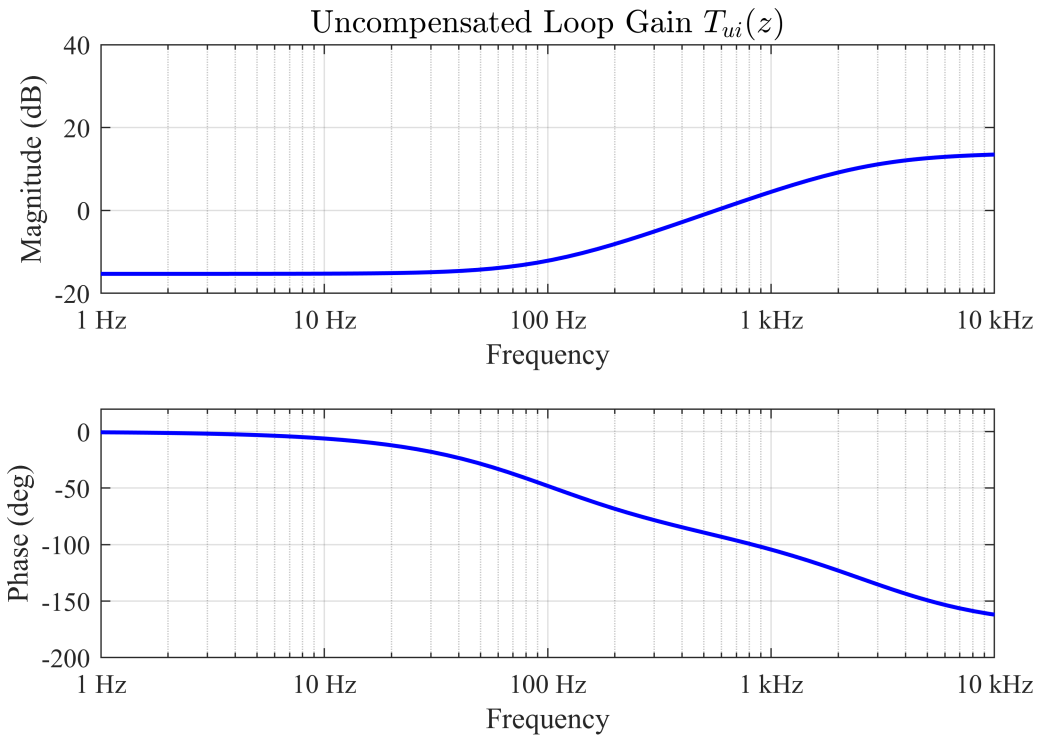
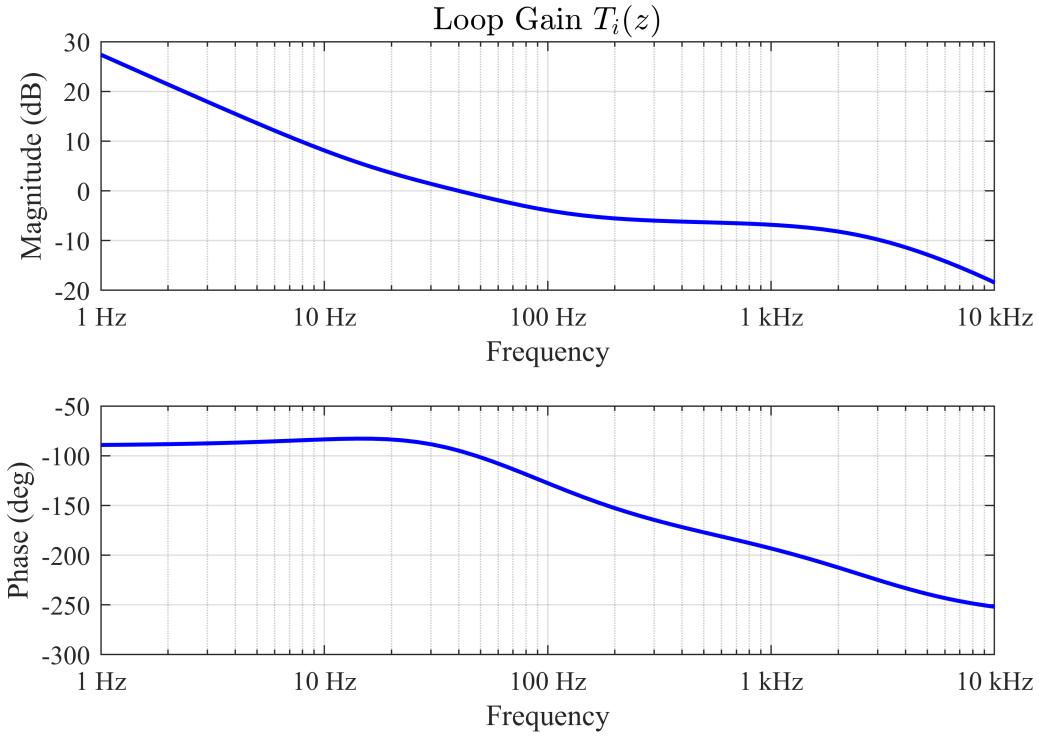


Fig. 5.48: Compensator plot for outer loop $G_{ci}(z)$ for parallel realization at 8 kW.



(a)



(b)

Fig. 5.49: Plots for outer loop for parallel realization at 8 kW (a) Uncompensated Loop Gain $T_{ui}(z)$, (b) Loop Gain $T_i(z)$ with crossover frequency, f_{ci} of 40 Hz and phase margin of 85°.

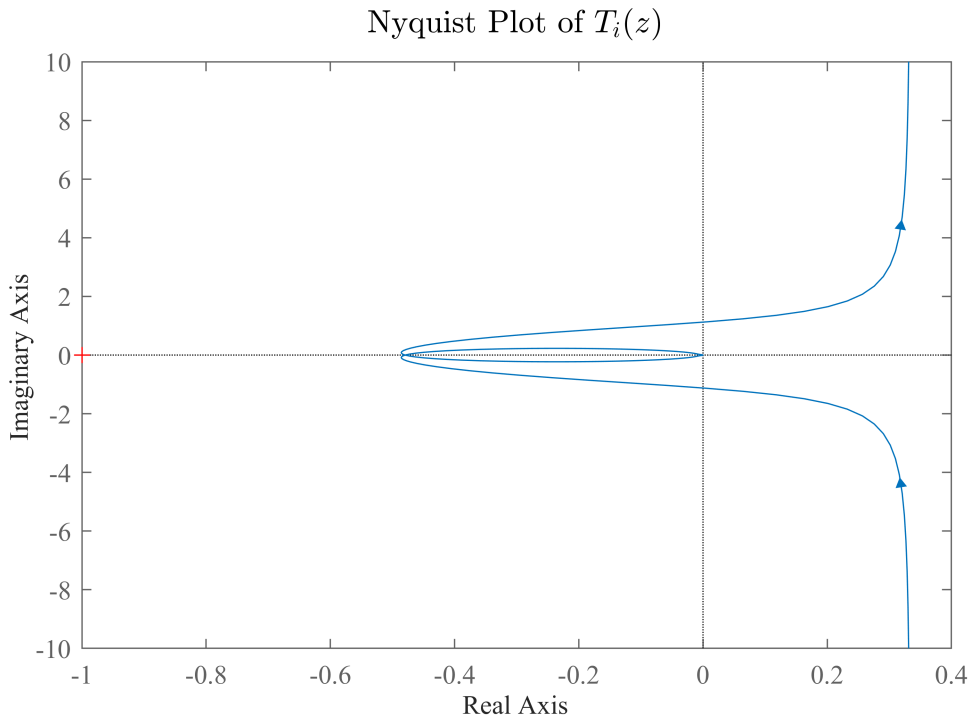


Fig. 5.50: Nyquist plot of Loop Gain $T_i(z)$ for parallel realization at 8 kW.

5.6.3 Coefficient Quantization and fixed point implementation for Inner loop and Outer Loop at 50 kW for Parallel Realization

The quantization of any signal x is represented as $\tilde{x}$ and given in (5.259), where $Q_n[x]$ represents the quantization of signal x with a resolution of n bits. The quantization of the coefficients of $G_{cv}(z)$ for parallel realization is given in (5.260)-(5.265). The quantization for coefficients of $G_{ci}(z)$ for parallel realization is given in (5.266)-(5.269).

$$\tilde{x} = Q_n[x] \tag{5.259}$$

$$\tilde{G}_{cvz0} = Q_{12}[G_{cvz0}] = 001001011101_{\overline{2}} \times 2^{-7} = 4.7266_{10} \tag{5.260}$$

$$\tilde{B}_{1v} = Q_{12}[B_{1v}] = 000001100110_{\overline{2}} \times 2^{-11} = 0.0498_{10} \tag{5.261}$$

$$\tilde{B}_{2v} = Q_{10}[B_{2v}] = 001100111010_{\overline{2}} \times 2^{-7} = 6.4531_{10} \tag{5.262}$$

$$\tilde{B}_{3v} = Q_{10}[B_{3v}] = 001010010101_{\overline{2}} \times 2^{-6} = 10.33_{10} \tag{5.263}$$

$$\tilde{C}_{pv1} = Q_{12}[C_{pv1}] = 001100100000_{\overline{2}} \times 2^{-11} = 0.3906_{10} \tag{5.264}$$

$$\tilde{C}_{pv2} = Q_{12}[C_{pv2}] = 001001010001_{\overline{2}} \times 2^{-11} = 0.2896_{10} \tag{5.265}$$

$$\tilde{G}_{ciz0} = Q_{12}[G_{ciz0}] = 000000010111_{\overline{2}} \times 2^{-11} = 0.0112_{10} \tag{5.266}$$

$$\tilde{B}_{1i} = Q_{12}[B_{1i}] = 000000010111_{\overline{2}} \times 2^{-11} = 0.0112_{10} \tag{5.267}$$

$$\tilde{B}_{2i} = Q_{12}[B_{2i}] = 000000010111_{\overline{2}} \times 2^{-11} = 0.0112_{10} \tag{5.268}$$

$$\tilde{C}_{pi1} = Q_{12}[C_{pi1}] = 011111111001_{\overline{2}} \times 2^{-11} = 0.9966_{10}. \tag{5.269}$$

For fixed point implementation, any signal $\tilde{x}$ is represented as B2C quantity $[\tilde{x}]_q^n$ [85], where n represents the number of bits required to represent $\tilde{x}$ or the word length used to represent $\tilde{x}$ and q represents the scale factor of $\tilde{x}$ in terms of 2^q. For calculating the values of n and q, first, the largest value of $\tilde{x}$, that is $\tilde{x}_{max}$, is analyzed under the worst-case transients during control of the DC-DC converter. Then, the smallest nonzero value of $\tilde{x}$, $\tilde{x}_{min}$ is calculated. The scale factor 2^q is then determined to accurately represent the minimum value of $\tilde{x}$, that is $\tilde{x}_{min}$. The number of bits required to represent $\tilde{x}$ is then calculated using equations (5.270), and (5.271), [85], where $\mathrm{DR}_{hw}[\tilde{x}]_q^n$ represents the hardware dynamic range of $[\tilde{x}]_q^n$, and definition of ceil is followed from [85].

$$n = 1 + ceil\left(\frac{\mathrm{DR}_{hw}[\tilde{x}]_q^n}{20\log_{10} 2}\right) \tag{5.270}$$

$$\mathrm{DR}_{hw}[\tilde{x}]_q^n \triangleq 20\log_{10}\left(\frac{\tilde{x}_{max}}{2^q}\right). \tag{5.271}$$

For parallel realization of the inner loop, the hardware dynamic range is analyzed from Fig. 5.22. The granularity of the error signal e_v is 1 due to the scaling of the inner loop by λ. The maximum and minimum value of $\tilde{u}_i$ is calculated from (5.272), and (5.273), respectively. The maximum and minimum value of $\tilde{u}_1$ is calculated from (5.274), and (5.275), respectively. The maximum and minimum values of $\tilde{u}_2$ and $\tilde{u}_p$ is calculated similarly as (5.274), and (5.275). The fixed-point implementation for the inner loop for parallel realization is shown in Fig. 5.51.

$$\tilde{u}_{i_{max}} = N_r - 1 \tag{5.272}$$

$$\tilde{u}_{i_{min}} = \tilde{B}_{1v} \tag{5.273}$$

$$\tilde{u}_{1_{min}} = \frac{\tilde{B}_{2v}}{(1 - \tilde{C}_{pv1})} \tag{5.274}$$

$$\tilde{u}_{1_{max}} = \frac{\tilde{B}_{2v}\tilde{e}_v}{(1 - \tilde{C}_{pv1})}. \tag{5.275}$$

For parallel realization of the outer loop, the hardware dynamic range is analyzed from Fig. 5.24. The granularity of the error signal e_i is 1. The maximum value of $\tilde{V}_{refi}$ is calculated corresponding to the number of bits nA/D of the A/D converter. The minimum value of $\tilde{V}_{refi}$ is calculated from (5.276). The maximum and minimum value of $\tilde{V}_{ref1}$ is calculated from (5.277), and (5.278), respectively. The maximum and minimum values of $\tilde{V}_{refp}$ is calculated similarly as (5.277), and (5.278). The fixed-point implementation for the outer loop for parallel realization is shown in Fig. 5.52.

$$\tilde{V}_{refi_{min}} = \tilde{B}_{1i} \tag{5.276}$$

$$\tilde{V}_{ref1_{min}} = \frac{\tilde{B}_{2i}}{(1 - \tilde{C}_{pi1})} \tag{5.277}$$

$$\tilde{V}_{ref1_{max}} = \frac{\tilde{B}_{2i}\tilde{e}_i}{(1 - \tilde{C}_{pi1})}. \tag{5.278}$$

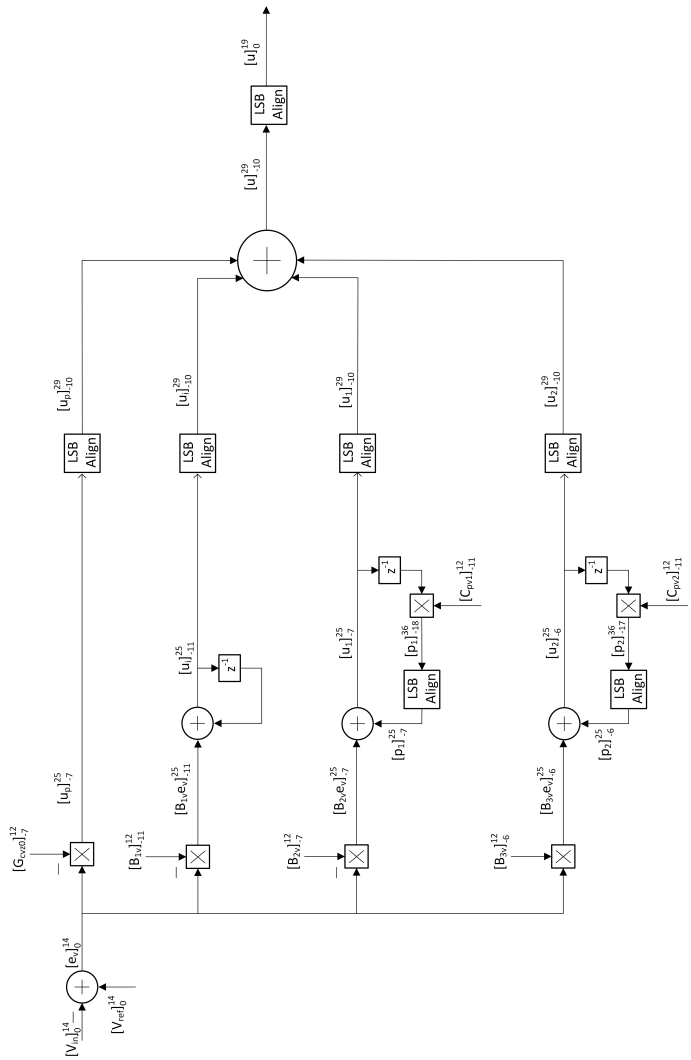


Fig. 5.51: Fixed Point Implementation for Parallel Realization of $G_{cv}(z)$.

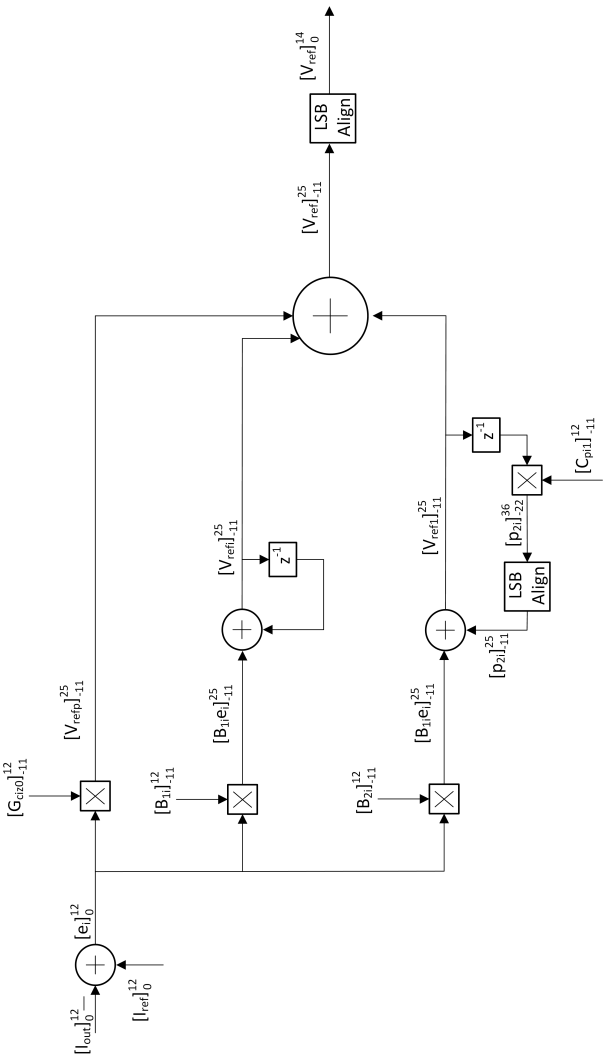


Fig. 5.52: Fixed Point Implementation for Parallel Realization of $G_{ci}(z)$.

5.7 Experimental Results of full system at 50 kW and 8 kW

5.7.1 System Description for Experiments

For the experimental verification of control systems for a full WPT system at 50 kW and 8 kW, Gustav Klein is used as a power supply at the input of the WPT system, and NHR 9300 is used as a battery at the output of the DC-DC converter. Fig. 5.54 and Fig. 5.55 show the test setup for the full WPT system shown in Fig. 5.53. Experimental setups with the oscilloscope at two different positions are used to test the full system. The setup with scope on the rectifier shown in Fig. 5.54 supports dynamic testing, and the setup with scope on the table shown in Fig. 5.58 provides accurate waveforms for stationary testing. The values of the tuning inductors and the capacitors for the full system are given in Table 5.25. Fig. 5.56 and Fig. 5.57 show close-up views of the secondary and primary sides, respectively.

The high-power PCB designs for the power board of the inverter and rectifier are shown in Fig. 5.59. Fig. 5.59(a) shows the top side of the power board PCB, which has the high-frequency capacitors and bleeder resistors. Fig. 5.59(b) shows the bottom side of the power board PCB, which has the DC film capacitors, high frequency capacitors, and power modules [86]. The power board PCB is a 6-layer PCB, with each layer featuring 6 oz copper to support high currents. The layer stackup of the power board is shown in Fig. 5.60 (b). Fig. 5.60(a) shows the control board stacked on top of the power board. The control board PCB shown in Fig. 5.60(a) is designed on a 4-layer PCB with considerations for signal integrity and uses an FPGA for control signals. The control board PCB also includes the sensing for DC voltages, DC currents, and AC currents. There is an additional connector on the control board for a daughter board PCB, which includes the fiber connectors for synchronizing multiple primaries and also primary to secondary to replicate a passive rectifier. The length of the primary pad is 2 m $\times$ 1 m, and the length of the secondary pad is 1 m $\times$ 1 m. The coupling coefficient k versus position (m) of the secondary pad with respect to the primary pad is shown in Fig. 5.61. The estimated time that the secondary pad is over the primary pad at a highway speed of 60 miles/hr is about 75 ms. Therefore, the control system should be fast enough to maintain constant power with misalignment.

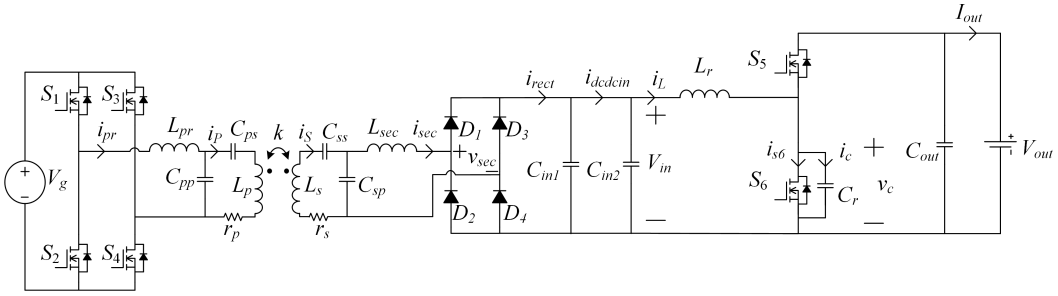


Fig. 5.53: Full WPT System diagram showing Primary and Secondary Side for experimental setup.

Table 5.25: Parameters for the full WPT system for Testing.

Parameter	**Value**
f_s for LCC-LCC tuning	85 kHz
f_s for DC-DC Converter	70 kHz
L_{pr}	5.6 μH
C_{pp}	0.63 μF
C_{ps}	415 nF
L_p	13.36 μH
L_s	7.26 μH
k	0.2
C_{ss}	990 nF
C_{sp}	1040 nF
L_{sec}	3.35 μH
L_r	6.8 μH
C_r	6.66 nF
C_{in1}	240 μF
C_{in2}	200 μF
C_{out}	200 μF

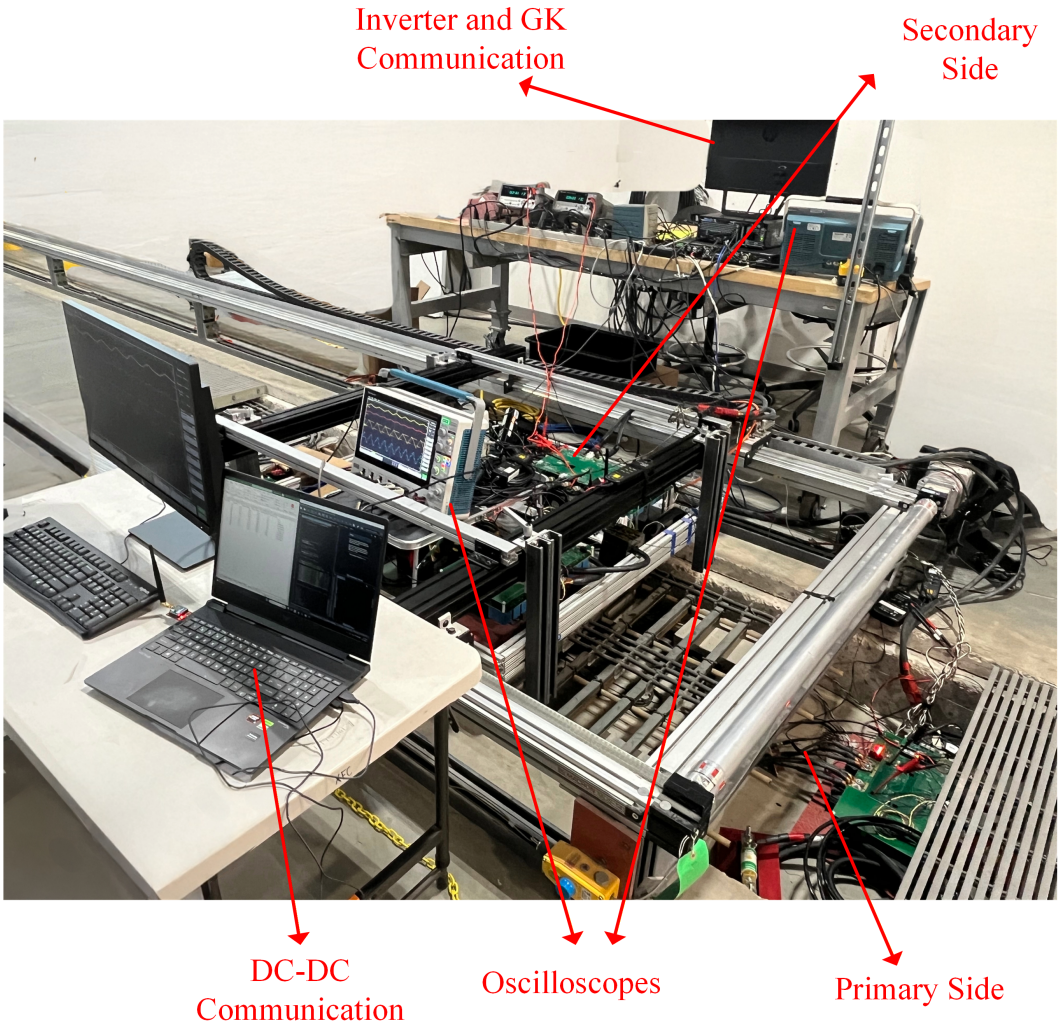


Fig. 5.54: Full WPT System showing Primary and Secondary Side with scope on rectifier.

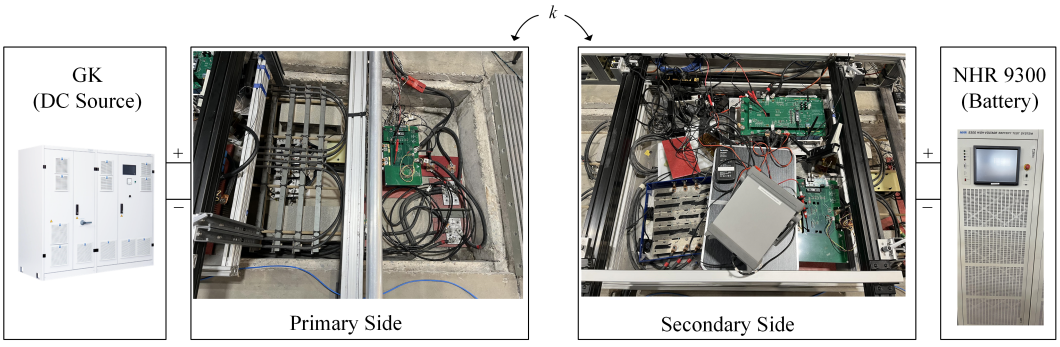


Fig. 5.55: Full WPT System showing Primary and Secondary Side for experimental setup with DC Source and Battery.

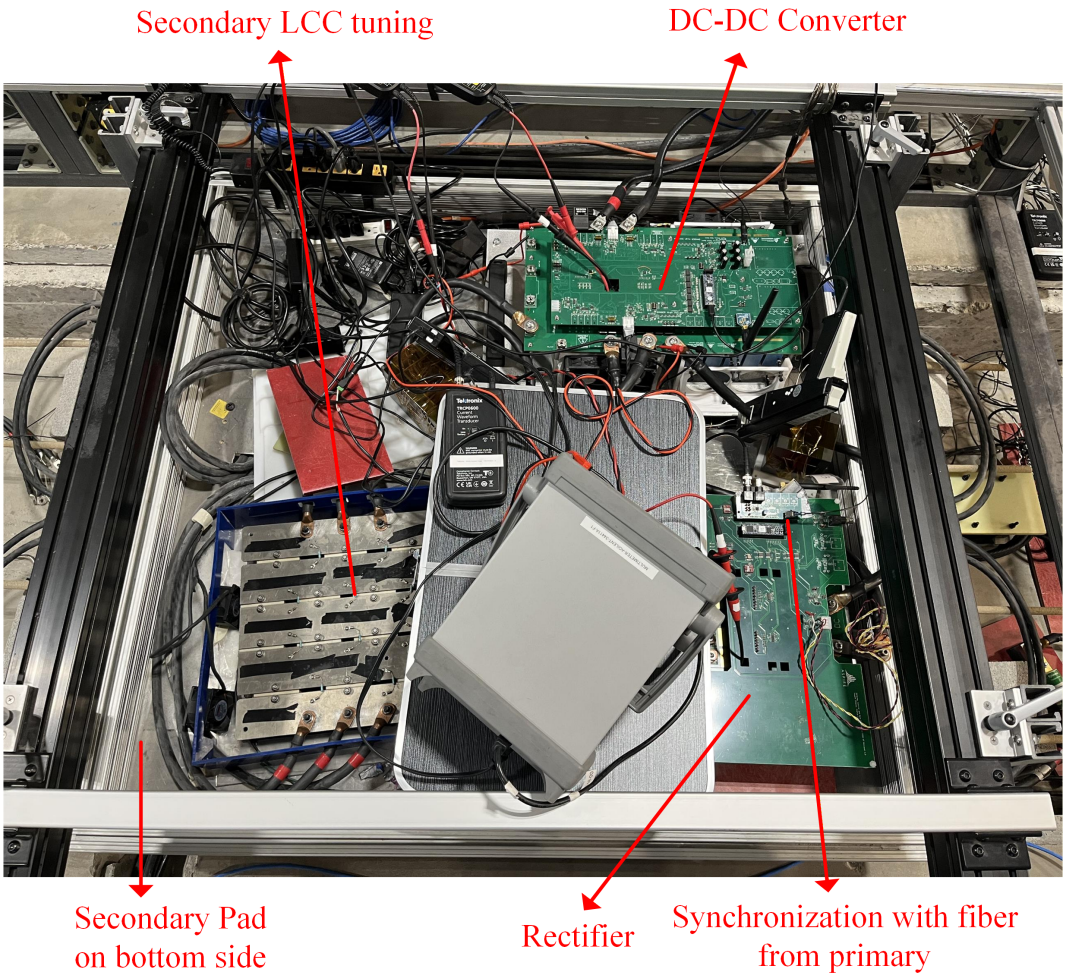


Fig. 5.56: Full WPT system showing secondary side with length of secondary pad 1 m × 1 m.

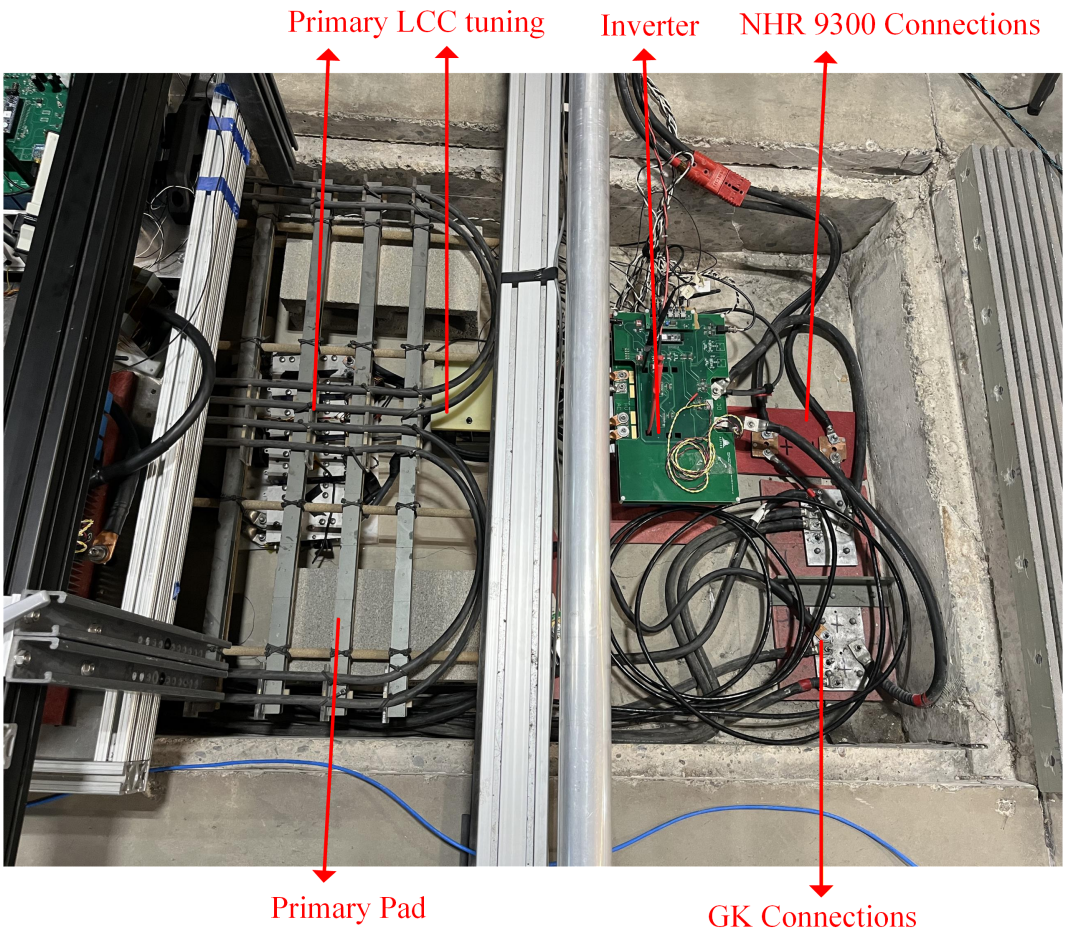


Fig. 5.57: Full WPT system showing primary side with length of primary pad 2 m × 1 m.

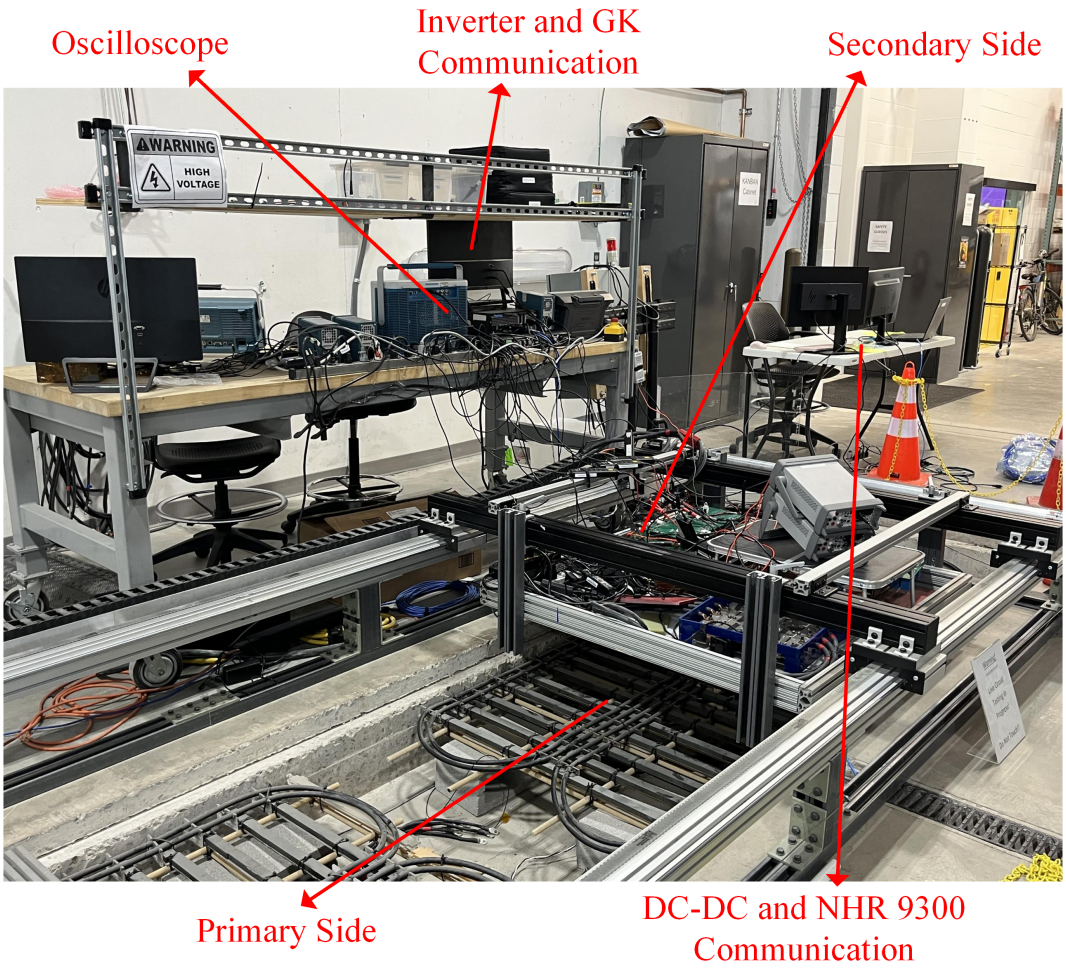
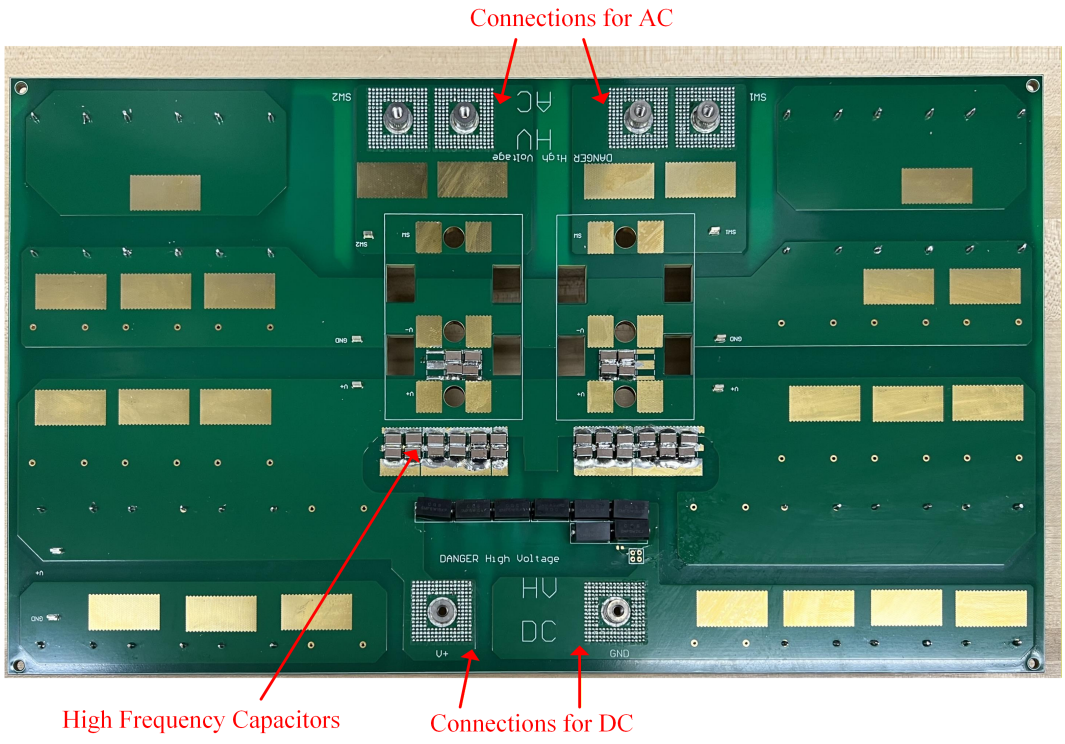
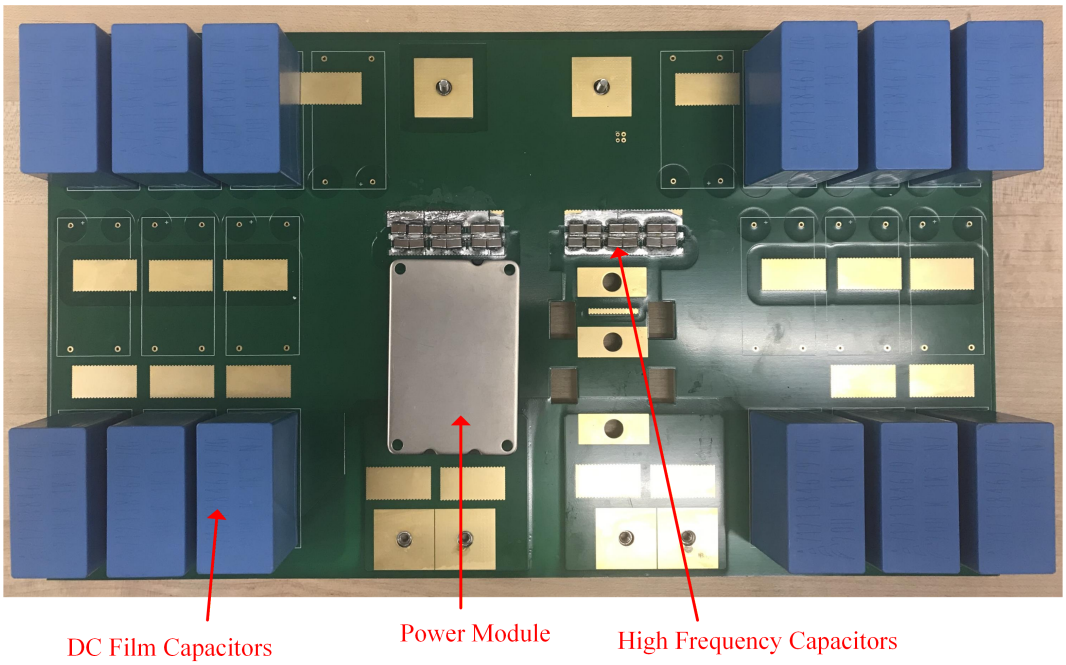


Fig. 5.58: Full WPT System showing Primary and Secondary Side with scope on the Table.

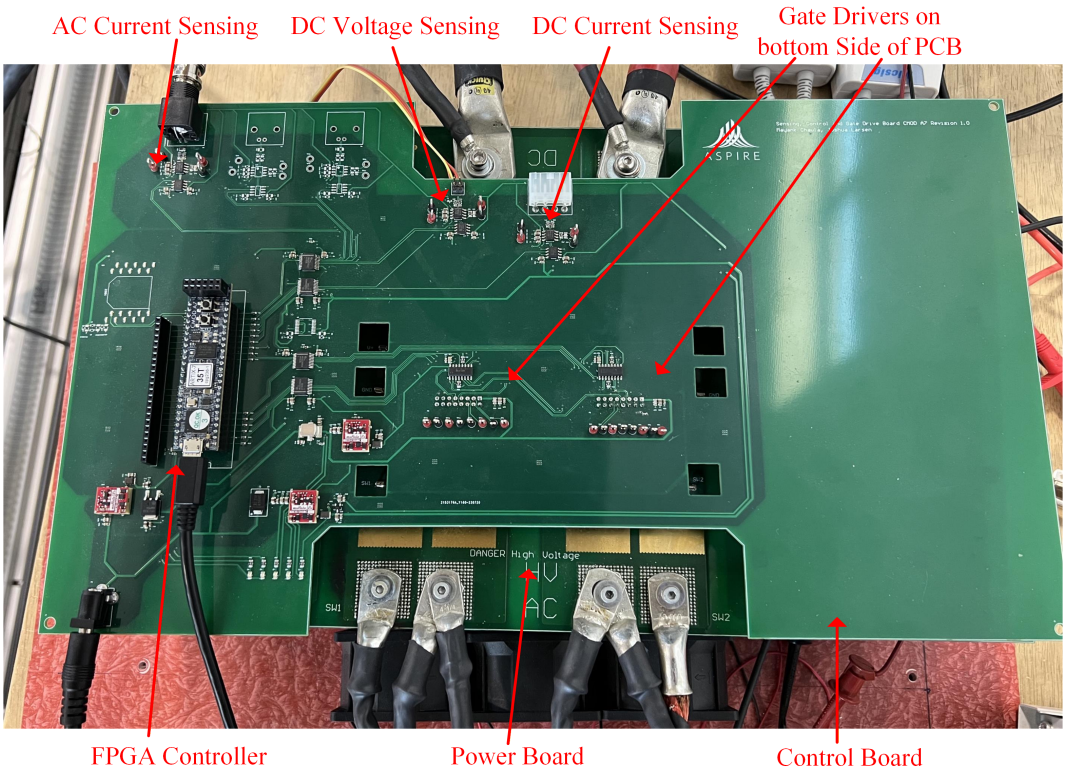


(a)

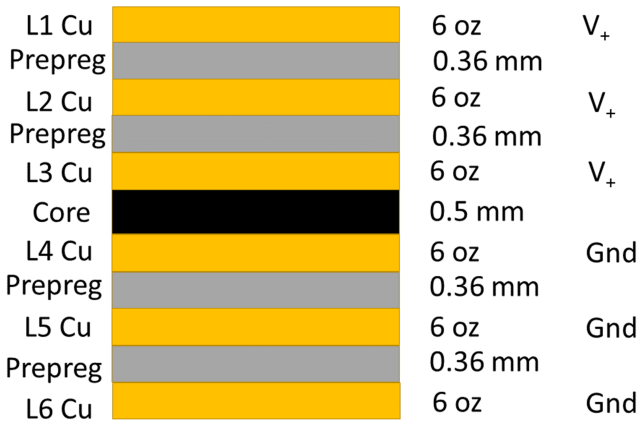


(b)

Fig. 5.59: PCB for the power board of the Inverter/Rectifier: (a) top view, (b) bottom view showing the power module.



(a)



(b)

Fig. 5.60: (a) 4-layer Control board stacked with Power board for Inverter/Rectifier, (b) Layer Stackup for 6-layer Power board for Inverter/Rectifier.

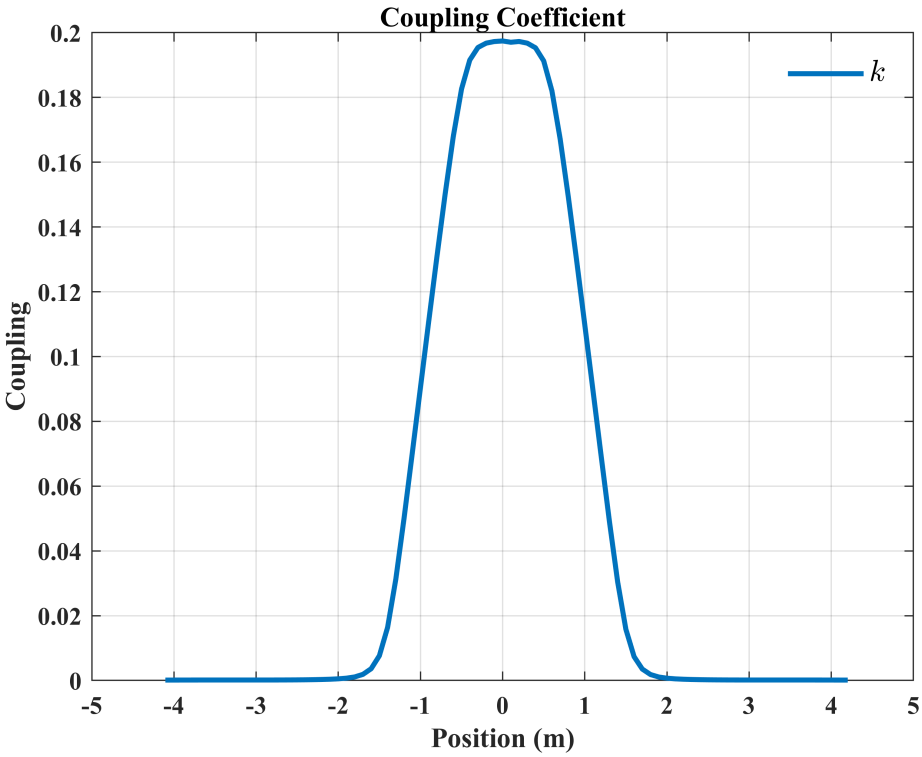


Fig. 5.61: Coupling Coefficient k vs position (m) of secondary with respect to primary or misalignment for WPT system.

5.7.2 Experimental Results

First, the full WPT system is tested in open loop with the scope on the rectifier. Fig. 5.62 shows the waveforms of the full system at coupling of 0.2 at 50 kW with rectifier Voltage of 402 V, average rectifier current i_{dcdcin} of 125 A, battery voltage of 600 V, and battery current of 83 A. The waveforms show that the rectifier current and battery current exhibit significant ripple. This is because the scope is on the rectifier, and the current waveforms are affected by EMI from the WPT system. Fig. 5.63 and Fig. 5.64 show waveforms at a similar operating point as Fig. 5.62 with the scope on the table. From the waveforms, the ripple in the battery current and the rectifier current i_{dcdcin} is very small.

For testing the control loops, the cascade structures were first designed at a PWM clock of 414 MHz. Fig. 5.65 shows the waveforms at 50 kW, with the inner loop to regulate the DC-DC input voltage V_{in} at a rectifier current of 118 A and a battery voltage of 600 V. To test the transient response, a step in rectifier voltage was given from 420 V to 430 V. The system settled in around 200 μs. Fig. 5.67 shows the waveforms when both the inner voltage loop and outer current loop are working and both the output battery current and the rectifier voltage are being regulated at 8.8 kW. To test the transient response, a step in battery current was given from 33 A to 35.5 A at 8.8 kW as shown in Fig. 5.68, where the rectifier voltage changes from 160 V to 180 V. While the dual loop works fine with cascade structures at the operating point, there were significant challenges during the startup of both loops, as shown in Fig. 5.69. In Fig. 5.69, for the startup of the inner loop, the system reached the operating point in open loop, and then the system switched to closed loop from open loop by an external command given from the communication system to the controller. There were large transients during startup, as shown in the waveforms of Fig. 5.69. When it was made to reach the desired operating point directly in closed loop, the system triggered faults due to large transients, so an open-loop-to-closed-loop approach was used for cascade structures. These large transients can be explained by the long cascade structure of the higher-order compensator, where the error amplifies at each stage, resulting in large transients when the error is large. This can also be seen in Fig. 5.66, where a large

step in rectifier voltage from 480 V to 508 V is given at 45 kW. The large error gets amplified at each stage of the cascaded structure. For the fixed-point implementation of this cascaded structure, it becomes difficult to calculate the peak value at each stage. Saturation limits can be put at the final output, since the integrator and other stages are cascaded in this structure, the intermediate values get amplified, resulting in large transients with this type of structure for higher-order compensators. The antiwindup is more complex and difficult to achieve with a cascade structure. With parallel structures, the integrator stage is separated from other stages, and therefore saturation limits for the intermediate integrator stage are easy to calculate. The antiwindup is easy to achieve with a parallel structure for higher-order compensators. Therefore, parallel structures were then used for controls. The PWM clock was also decreased from 414 MHz to 240 MHz due to complex fixed-point implementation and to resolve timing constraints in the FPGA used.

The control loops were then tested with the parallel structures, which were designed at a PWM clock of 240 MHz. Fig. 5.70 shows the waveforms when both the inner voltage loop and outer current loop are working and both the output battery current and the rectifier voltage are being regulated at 9 kW, the rectifier current is 46 A, and the battery voltage is 250 V. To test the transient response, a step in battery current was given from 33 A to 36 A at 9 kW as shown in Fig. 5.71, where the rectifier voltage changes from 178 V to 195 V. The system settles in 2 ms. Fig. 5.72, Fig. 5.73, and Fig. 5.74 show the startup at 10 kW for the parallel realization, with cursors at the rectifier voltage, battery current, and peak battery current, respectively. For the startup of parallel realization, the system is always ramped up in a closed loop. The PWM output of the DC-DC converter is saturated at a minimum duty cycle close to the pass-through mode of the boost converter and transitions from saturation mode to regulation mode as the system reaches the operating point at which it can be regulated. For capturing the startup waveforms. The battery voltage is fixed at 250 V, or the desired battery voltage, and the input voltage of the WPT system or power supply is ramped to replicate the change in coupling factor during dynamic motion. From these figures, it can be observed that the startup from saturation mode to regulation mode occurs

in about 3 ms, which is fast enough for the highway speed of 60 miles/hr, during which the secondary pad is over the primary pad for 75 ms. The startup using parallel structures is stable and much better than the cascade structures for a higher-order compensator in this system. The peak battery current during startup is 57 A. Therefore, parallel structures are also used to test the dual loop control at 50 kW.

The control loops were then tested at 50 kW with parallel realization. Fig. 5.75 shows the waveforms at 50 kW with the inner loop regulating the DC-DC input voltage V_{in} at a rectifier current of 125 A and a battery voltage of 600 V. To test the transient response, a step in rectifier voltage was given from 402 V to 422 V. The system settled in less than 1 ms. Fig. 5.76 and Fig. 5.77 show the waveforms when both the inner voltage loop and outer current loop are working, and both the output battery current and the rectifier voltage are being regulated at 50 kW, the rectifier current is 123 A, and the battery voltage is 600 V. Fig. 5.78 shows the waveforms for the primary side when both the inner voltage loop and outer current loop are working, and both the output battery current and the rectifier voltage are being regulated at 50 kW, the rectifier current is 118 A, and the battery voltage is 600 V. Fig. 5.79 shows the transient response, where a step in battery current was applied from 84.6 A to 81.95 A at 50 kW, and the rectifier voltage changed from 446 V to 435 V, representing the controls at a coupling of 0.19. The rectifier voltage settles in 2 ms. Fig. 5.80 shows the transient response, where a step in battery current was applied from 81.95 A to 84.74 A at 50 kW, and the rectifier voltage changed from 435 V to 451 V, representing the controls at a coupling of 0.19. The rectifier voltage settles in 2 ms.

To test the startup at high power, battery voltage is adjusted to 580 V instead of 600 V, because when the NHR 9300 was operated at 600 V, it was required to set the NHR in the 1200 V operating range option, due to which fluctuations in voltage of NHR were observed in open loop or the saturation mode due to a large difference in voltage from the set operating range. Therefore, to ensure safe operation, the NHR was set to the 600 V operating range, and the battery voltage or output voltage was set to 580 V. Fig. 5.81 and Fig. 5.82 show the waveforms when both the inner voltage loop and outer

current loop are working, and both the output battery current and the rectifier voltage are being regulated at 48.7 kW, the rectifier current is 94 A, and the battery voltage is 580 V to represent the coupling factor of 0.15. Fig. 5.83, Fig. 5.84, and Fig. 5.85 show the startup at 48.7 kW for the parallel realization, with cursors at the rectifier voltage, battery current, and peak battery current, respectively. For the startup of parallel realization, the system is always ramped up in a closed loop. The PWM output of the DC-DC converter is similarly saturated to a minimum duty cycle close to the pass-through mode of the boost converter and transitions from saturation mode to regulation mode as the system reaches the operating point at which it can be regulated at a coupling factor of 0.15. For capturing the startup waveforms. The battery voltage is fixed at 580 V, or the desired battery voltage and the input voltage of the WPT system or power supply is ramped up to replicate the change in coupling factor in dynamic motion. From these figures, it can be observed that the startup from saturation mode to regulation mode occurs in about 5 ms, which is fast enough for the highway speed of 60 miles/hr, during which the secondary pad is over the primary pad for 75 ms. The peak battery current during startup is 104 A. The startup at this operating point is also verified in PLECS simulation as shown in Fig. 5.87. The startup from saturation mode to regulation mode occurs similarly in 5 ms. The peak value of battery current observed in the simulation is around 102 A. These values are very close to the experimental results shown in Fig. 5.85. Fig. 5.86 shows the transient response, where a step in battery current was given from 83.57 A to 81.44 A at 48.7 kW and the rectifier voltage changes from 545 V to 535 V, representing the controls at coupling of 0.15. The rectifier voltage settles in less than 2 ms. From Fig. 5.61, the change in coupling by a difference of 0.1 occurs due to a change in the position of the secondary pad with respect to the primary pad by 0.05 m. The rectifier current changes with coupling; the inner and outer loops should be able to regulate the input voltage and battery current, respectively, within approximately 2 ms to maintain constant power despite misalignment at a highway speed of 60 miles/hr. From the above experimental results, it can be observed that the closed-loop control settles within 2 ms. Fig. 5.90, Fig. 5.91, Fig. 5.93, and Fig. 5.92 show

the stable thermal operation of the full WPT system at 50 kW.

Fig. 5.88 and Fig. 5.89 show the waveforms obtained from PLECS simulation at 50 kW for parallel realization to replicate a dynamic system. In Fig. 5.88, the simulation starts with a coupling coefficient of 0.13. After 10 ms, the rectifier current reaches 80 A after the battery voltage reaches 600 V. After every 10 ms, the coupling coefficient is increased by 0.1 until it reaches 0.2 at the aligned position of the primary and secondary. This is done in the simulation to observe the response time after each change in the coupling coefficient. The duty cycle of the DC-DC converter is saturated at its minimum value till it reaches the point where the DC-DC converter can regulate the output power. After 30 ms, the coupling coefficient reaches 0.15, where the rectifier current is 94 A. The controller turns on between 30 ms and 40 ms and starts regulating the battery current at approximately 83 A and output power of approximately 50 kW. The rectifier voltage reaches approximately 555 V during this time interval. In Fig. 5.89, the coupling coefficient changes from 0.15 to 0.16 at 40 ms, due to which the rectifier current changes from 94 A to 100 A. The controller starts regulating the battery current and output power, causing the rectifier voltage to change from 555 V to 516 V. The system settles between 2 ms and 3 ms. The controller continues to regulate the battery current and output power until the coupling coefficient reaches 0.2 and the rectifier current reaches approximately 125 A at 80 ms.

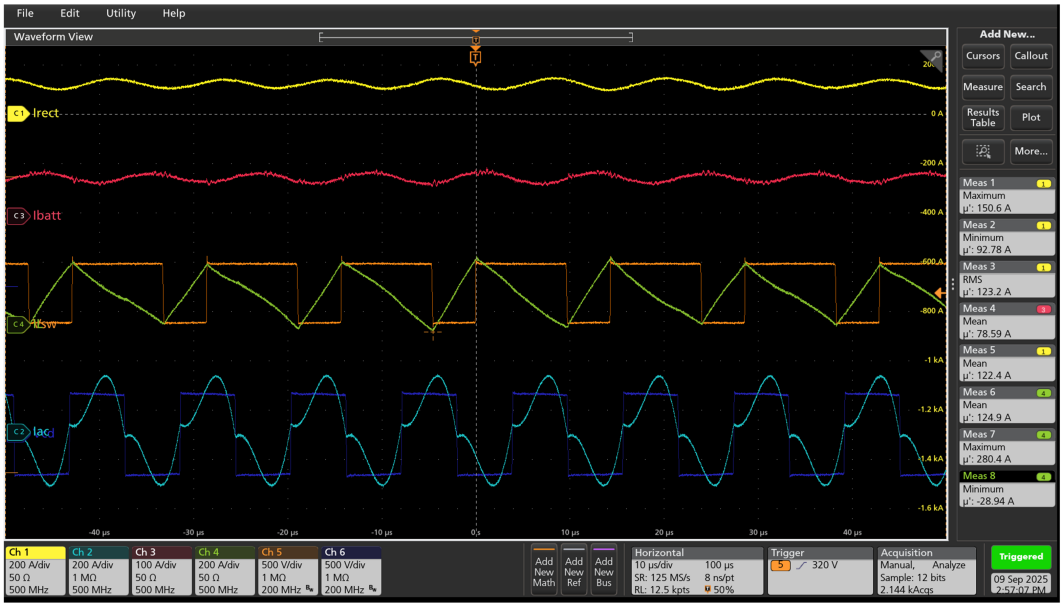


Fig. 5.62: Open Loop waveforms at 50 kW at rectifier Voltage of 402 V and average rectifier Current i_{dcdcin} of 125 A at 0.2 coupling with scope on rectifier side showing large ripple in currents due to EMI interference from WPT system. From top to bottom are rectifier current, battery current, switch node voltage, and Inductor Current of the DC-DC, switch node voltage, and tank current of the rectifier.

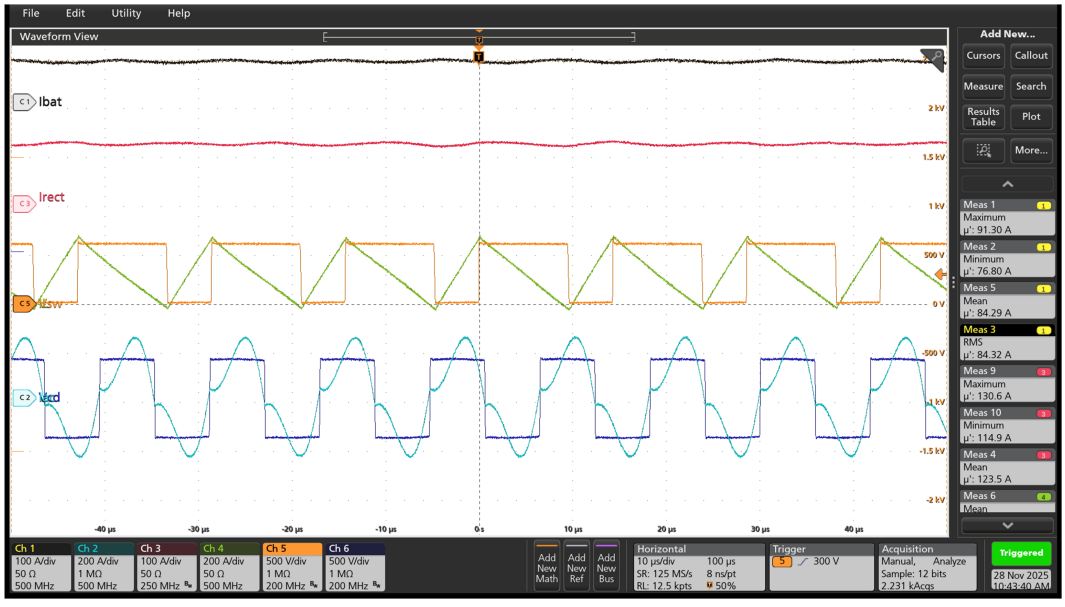


Fig. 5.63: Open Loop waveforms at 50 kW at rectifier Voltage of 402 V and average rectifier Current i_{dcdcin} of 125 A at 0.2 coupling with scope on table showing accurate waveforms. From top to bottom are battery current, rectifier current, switch node voltage, and Inductor Current of the DC-DC, switch node voltage, and tank current of the rectifier.

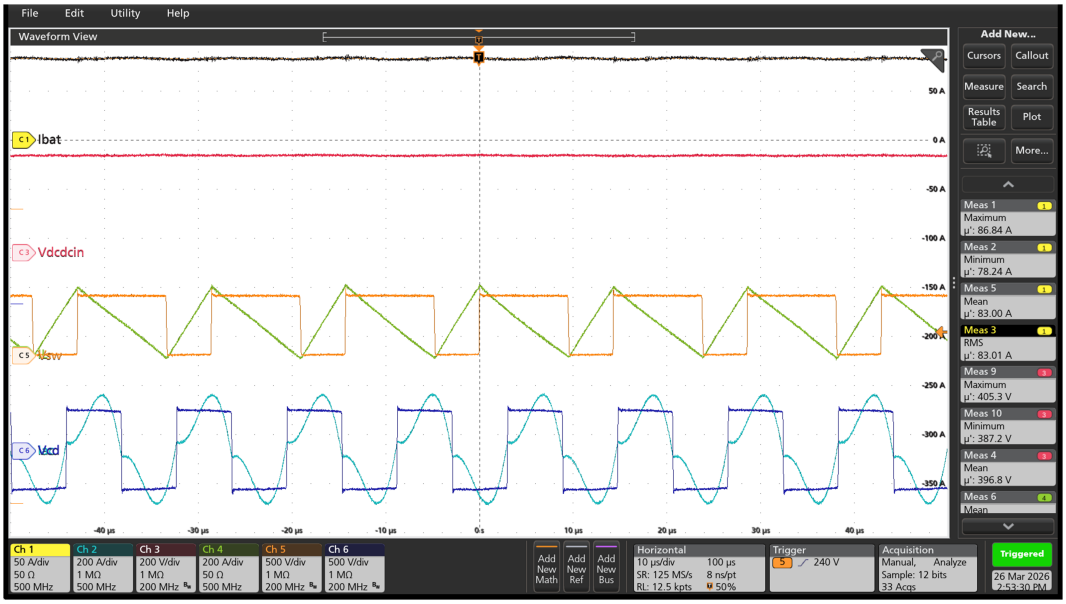


Fig. 5.64: Open Loop waveforms at 50 kW at rectifier Voltage of 402 V and average rectifier Current i_{dcdcin} of 125 A at 0.2 coupling with Scope on Table. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and Inductor Current of DC-DC, switch node voltage, and tank current of the rectifier.

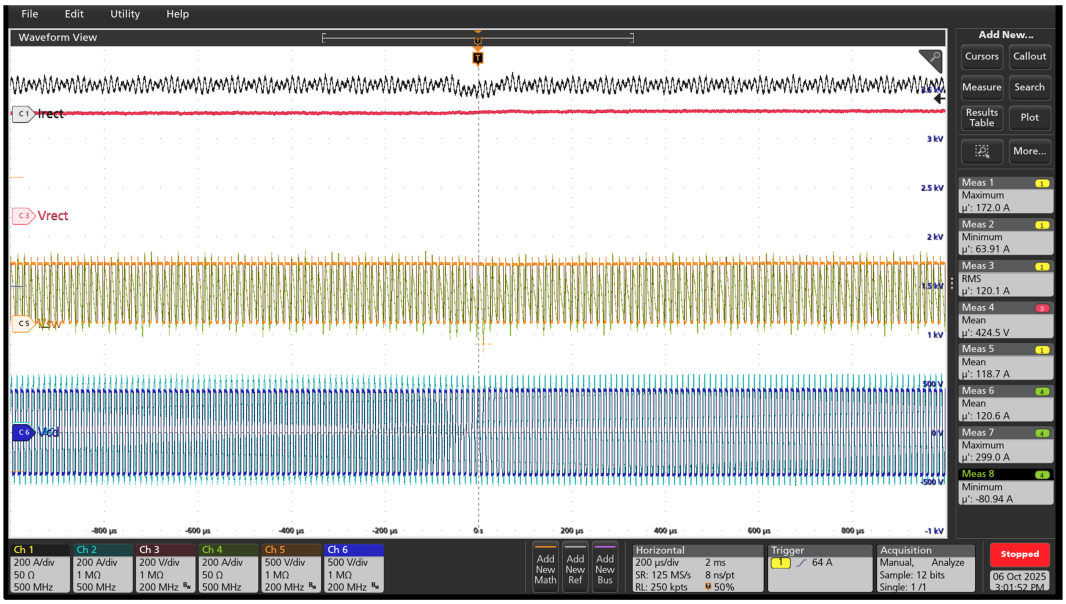


Fig. 5.65: Closed Loop Waveforms at 50 kW with inner loop working and Step in rectifier voltage V_{in} from 420 V to 430 V at 50 kW with Cascade Realization at rectifier current of 118 A and coupling of 0.19. From top to bottom are rectifier current, rectifier voltage V_{in}, switch node voltage, and Inductor Current of DC-DC, switch node voltage, and tank current of the rectifier.

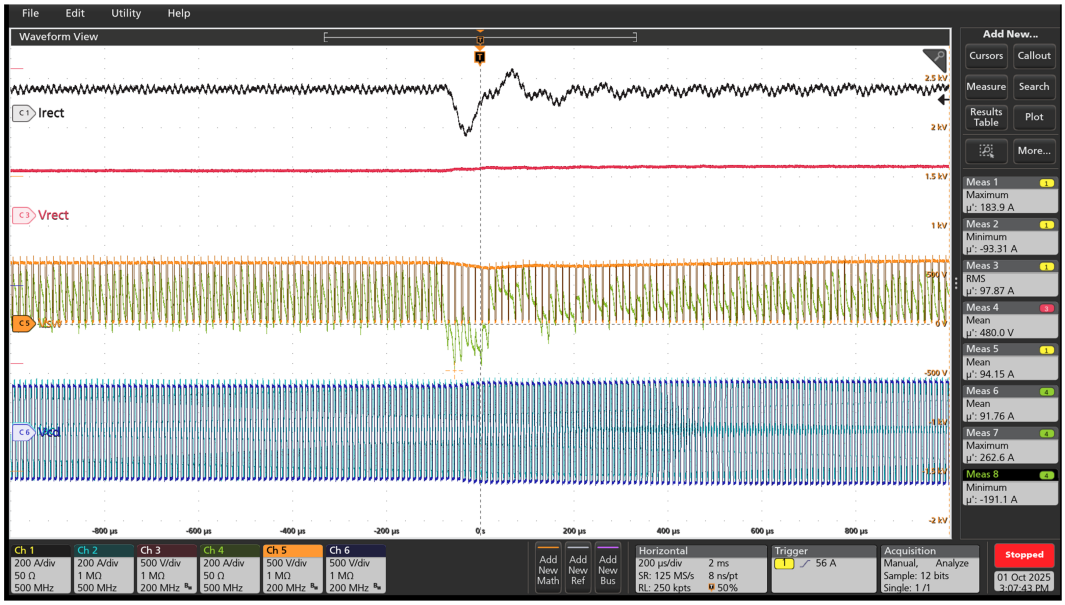


Fig. 5.66: Closed Loop Waveforms with inner loop working and Step in rectifier voltage V_{in} from 480 V to 508 V at 45 kW with Cascade Realization at rectifier current of 94 A. From top to bottom are rectifier current, rectifier voltage V_{in}, switch node voltage, and Inductor Current of DC-DC, switch node voltage, and tank current of the rectifier.

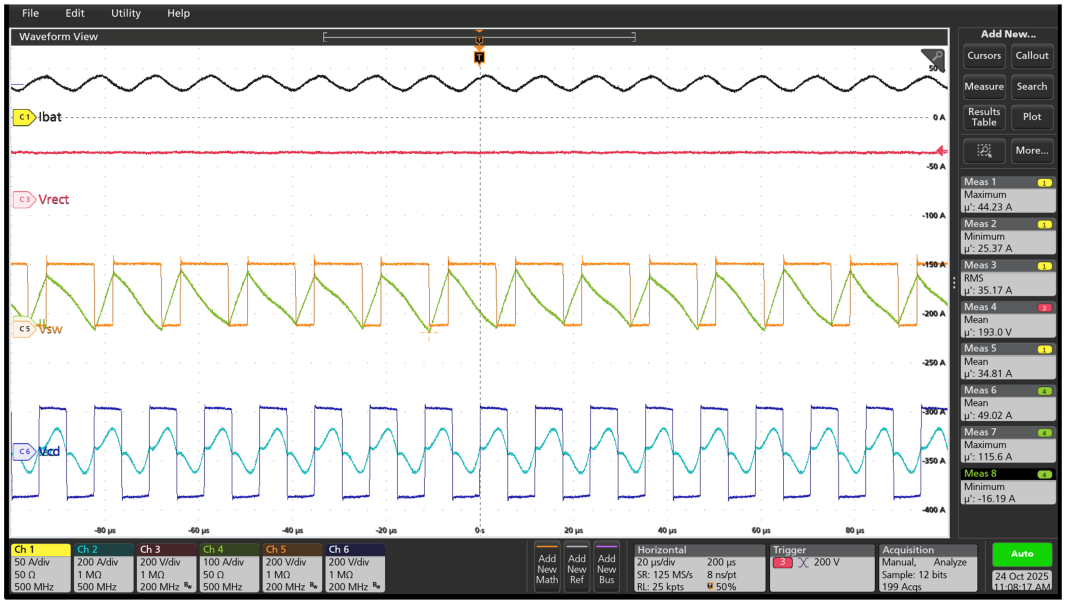


Fig. 5.67: Closed Loop Waveforms at 8.8 kW with inner and outer loop working at Rectifier Voltage of 180 V, rectifier current of 49 A, and Battery Current of 35.5 A with Cascade realization. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and Inductor Current of DC-DC, switch node voltage, and tank current of the rectifier.

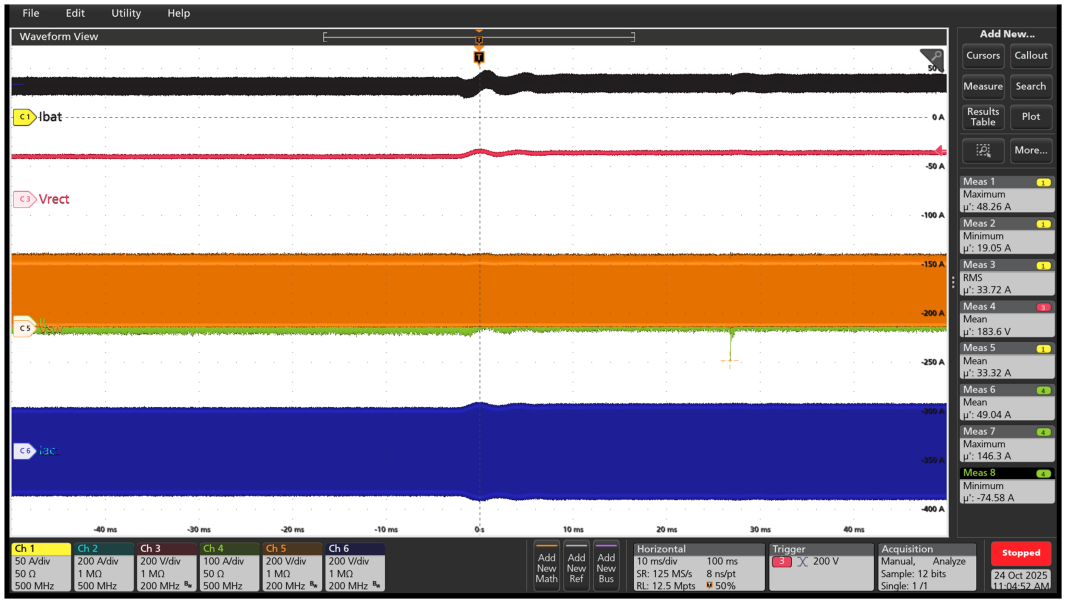


Fig. 5.68: Closed Loop Waveforms at 8.8 kW with inner and outer loop working and Step in Battery Current from 33 A to 35.5 A at 8.8 kW with Cascade Realization, where the rectifier voltage changes from 160 V to 180 V. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

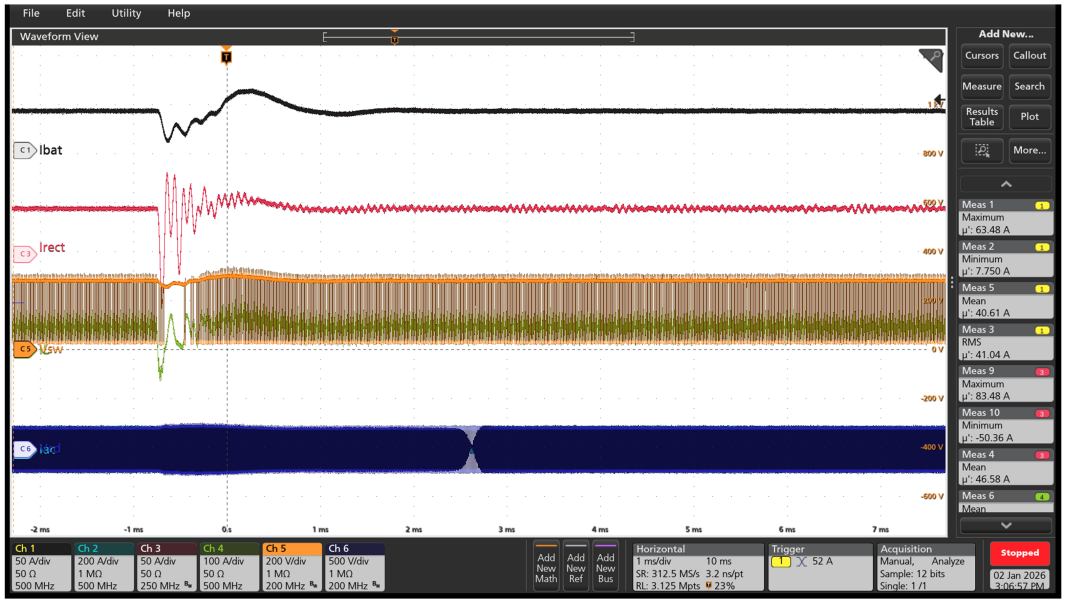


Fig. 5.69: Startup waveform at 10 kW for the inner loop with cascade realization, showing large transients from open loop to closed loop. From top to bottom are battery current, rectifier current, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

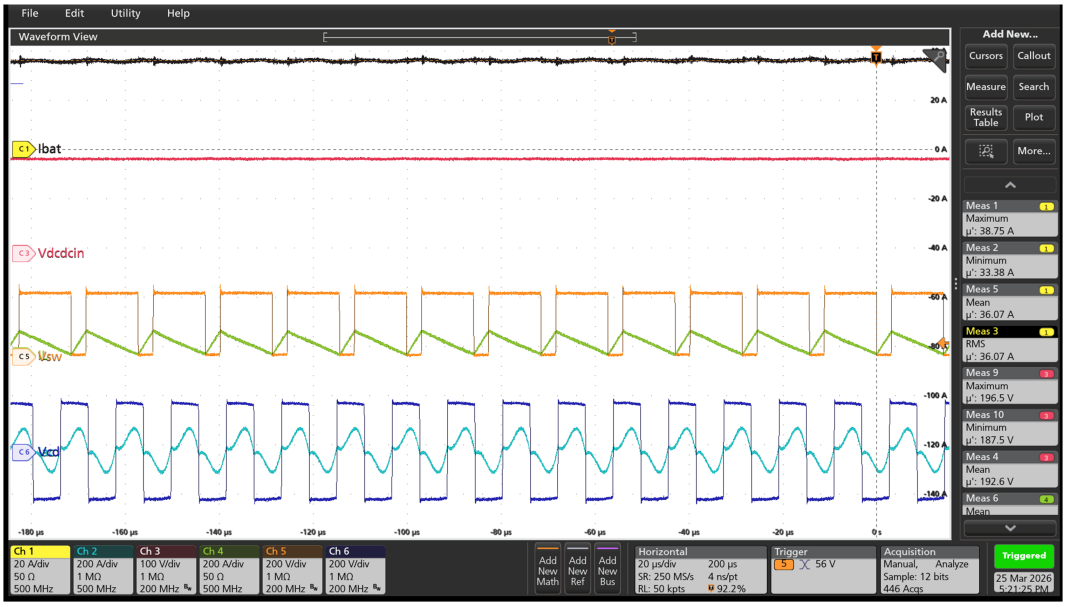


Fig. 5.70: Closed loop waveforms at 9 kW with inner and outer loop working at rectifier voltage of 195 V, rectifier current of 46 A, and battery current of 36 A with parallel realization. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

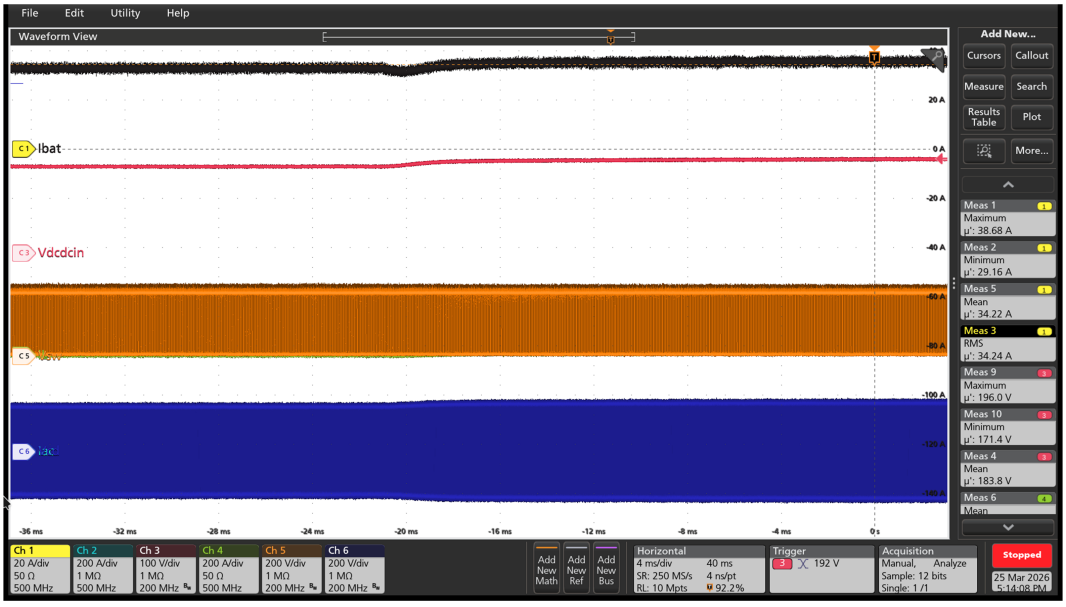


Fig. 5.71: Closed loop waveforms at 9 kW with inner and outer loop working and step in battery current from 33 A to 36 A at 9 kW with parallel realization, where the rectifier voltage changes from 178 V to 195 V. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier. The rectifier voltage settles in 2 ms.

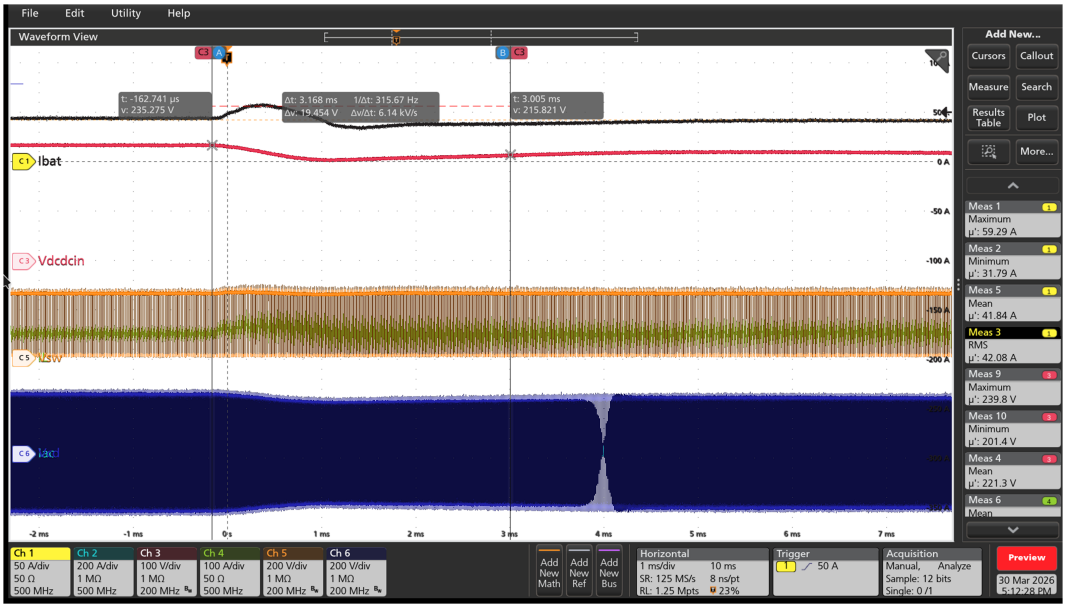


Fig. 5.72: Startup waveform at 10 kW with inner and outer loop working, showing the cursor at input voltage during startup for parallel realization. The system always operates in closed loop and goes from saturation mode to closed loop mode during the startup when the input current is ramped up from the power supply to replicate the lowest coupling factor point that can be regulated by closed loop. The complete startup from saturation mode to closed loop mode happens in 3 ms.

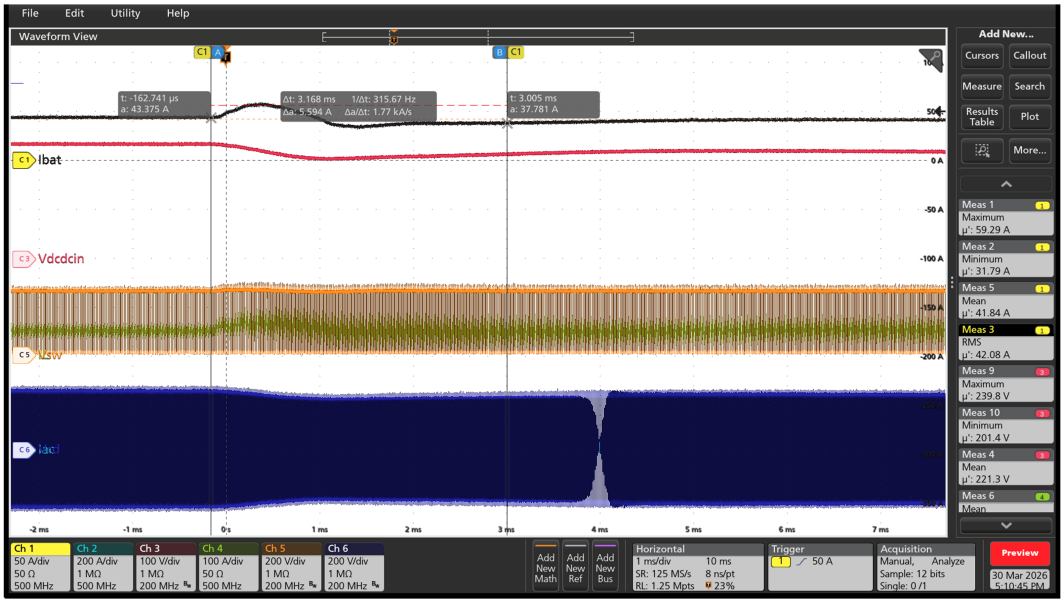


Fig. 5.73: Startup waveform at 10 kW with inner and outer loop working for parallel realization, showing cursor at battery current during startup. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

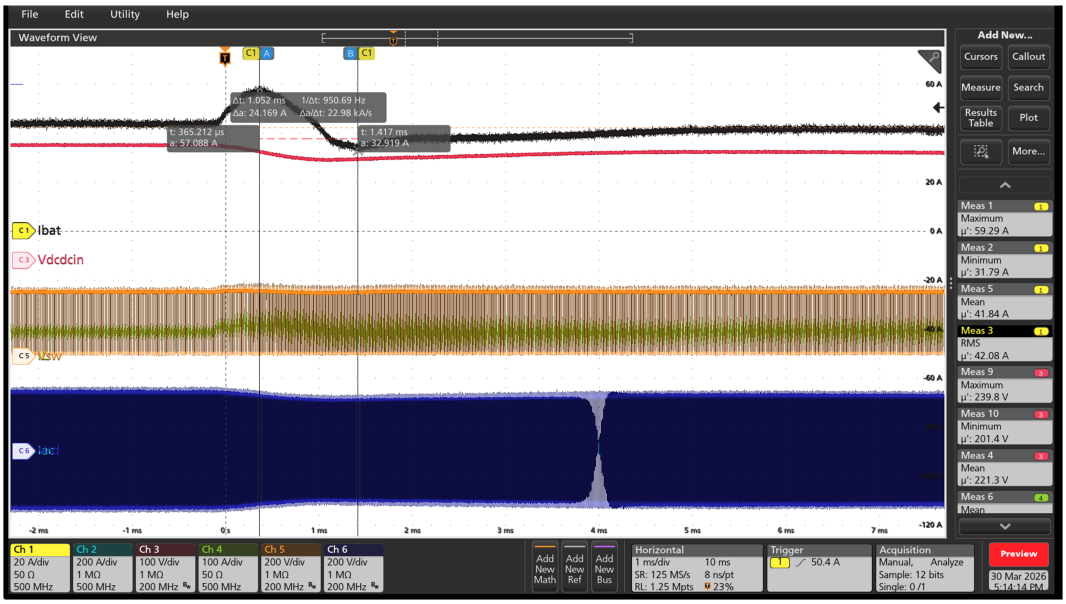


Fig. 5.74: Startup waveform at 10 kW with inner and outer loop working for parallel realization, showing peak battery current of 57 A during startup. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

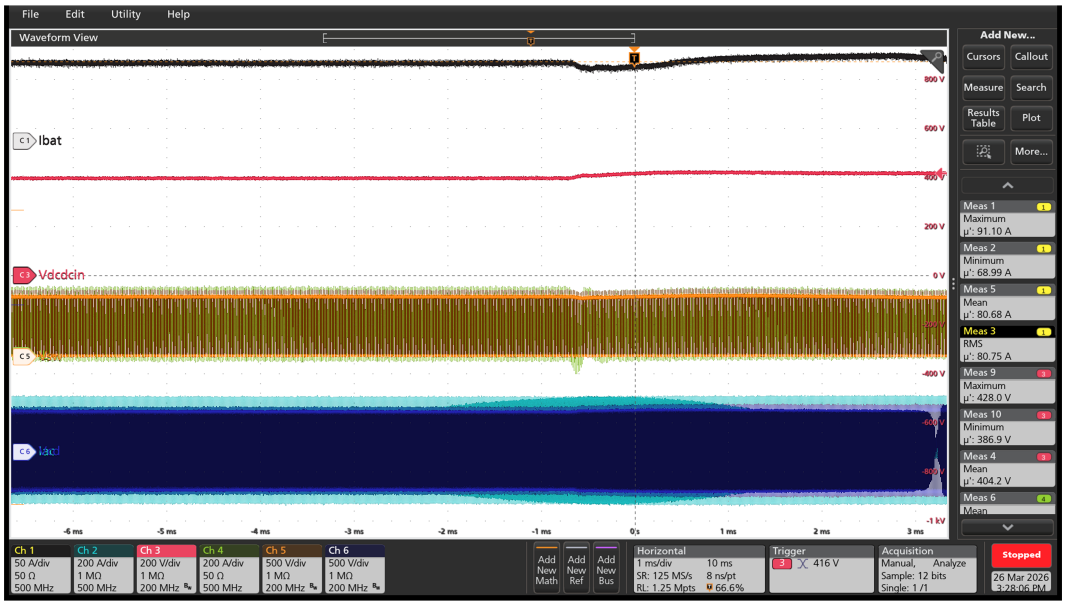


Fig. 5.75: Closed loop waveforms at 50 kW with inner loop working with parallel realization and step in rectifier Voltage from 402 V to 422 V at 50 kW with rectifier current of 125 A and battery voltage of 600 V. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier. The rectifier voltage settles in less than 1 ms.

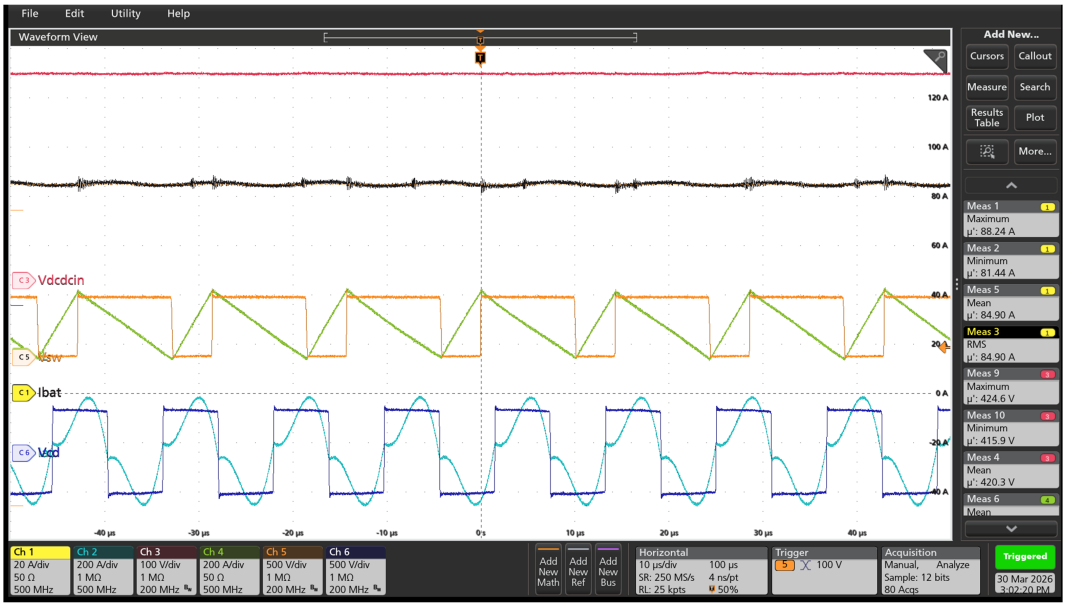


Fig. 5.76: Closed Loop waveforms at 50 kW with inner and outer loop working for parallel realization at rectifier Voltage of 422 V, battery voltage of 600 V, battery Current of 84 A, rectifier current of 123 A. From top to bottom are rectifier voltage V_{in}, battery current, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

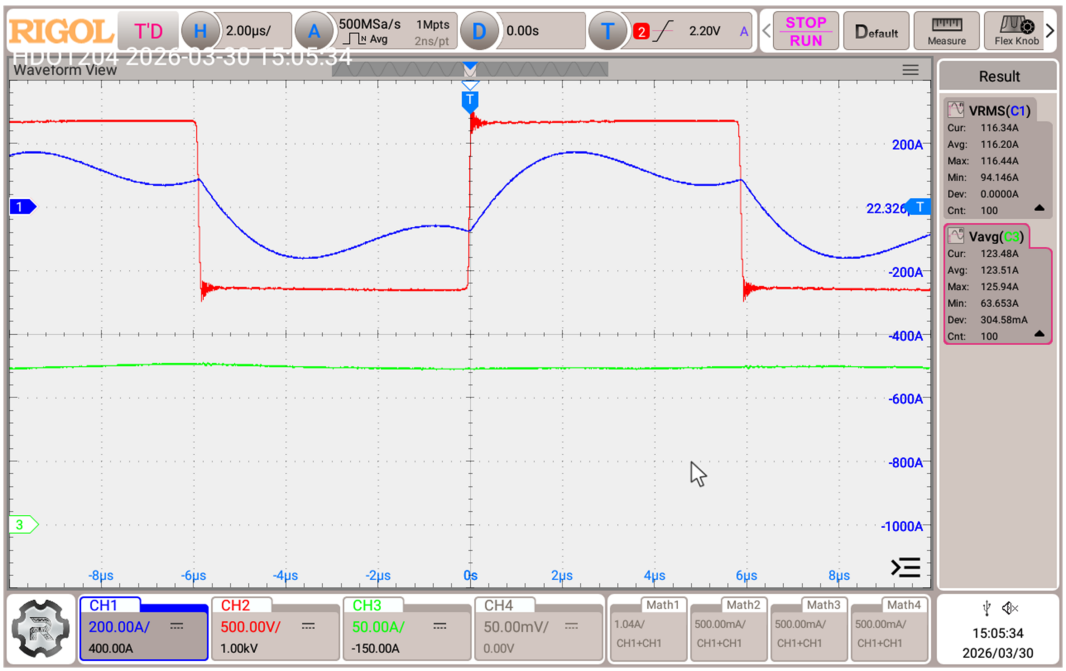


Fig. 5.77: Closed loop waveforms at 50 kW with inner and outer loop working for parallel realization at rectifier Voltage of 422 V and rectifier current of 123 A. From top to bottom are the primary switch node voltage, bridge current, and secondary rectifier current.

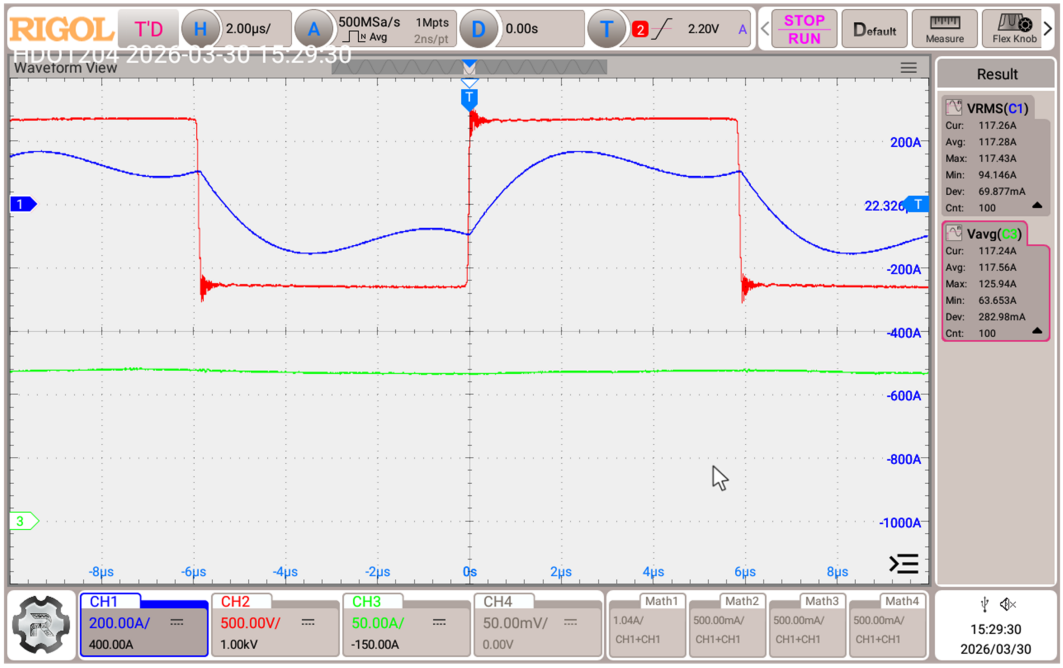


Fig. 5.78: Closed loop waveforms at 50 kW with inner and outer loop working for parallel realization at rectifier Voltage of 446 V, rectifier current of 118 A, battery current of 84 A, and battery voltage of 600 V. From top to bottom are the primary switch node voltage, bridge current, and secondary rectifier current.

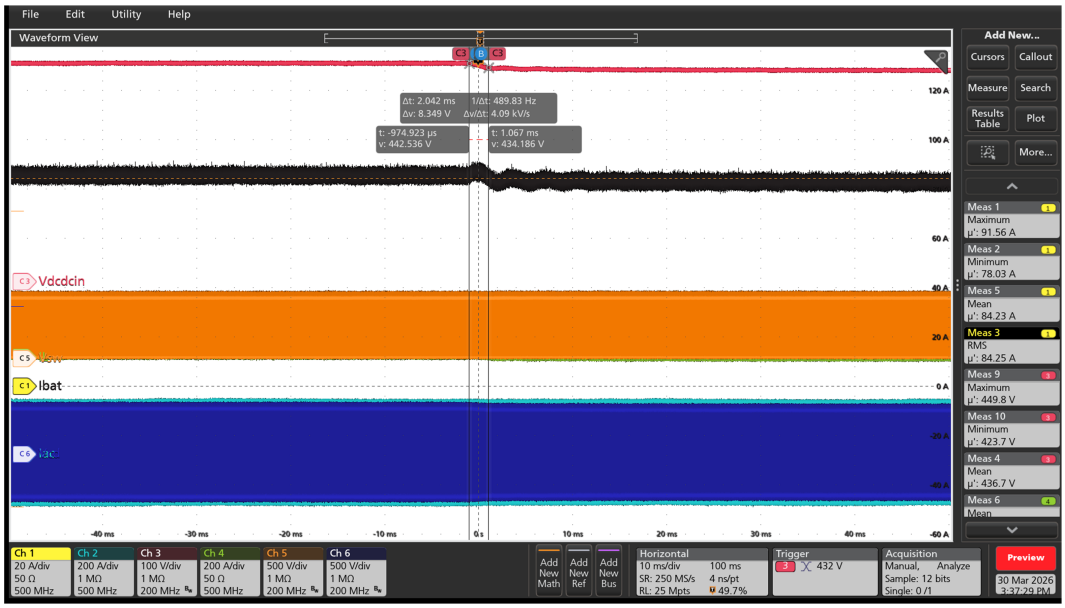


Fig. 5.79: Closed loop waveforms at 50 kW with inner and outer loop working for parallel realization and step in battery Current from 84.6 A to 81.95 A at 50 kW, where the rectifier voltage changes from 446 V to 435 V, representing coupling at 0.19. From top to bottom are rectifier voltage V_{in}, battery current, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier. The rectifier voltage settles in 2 ms.

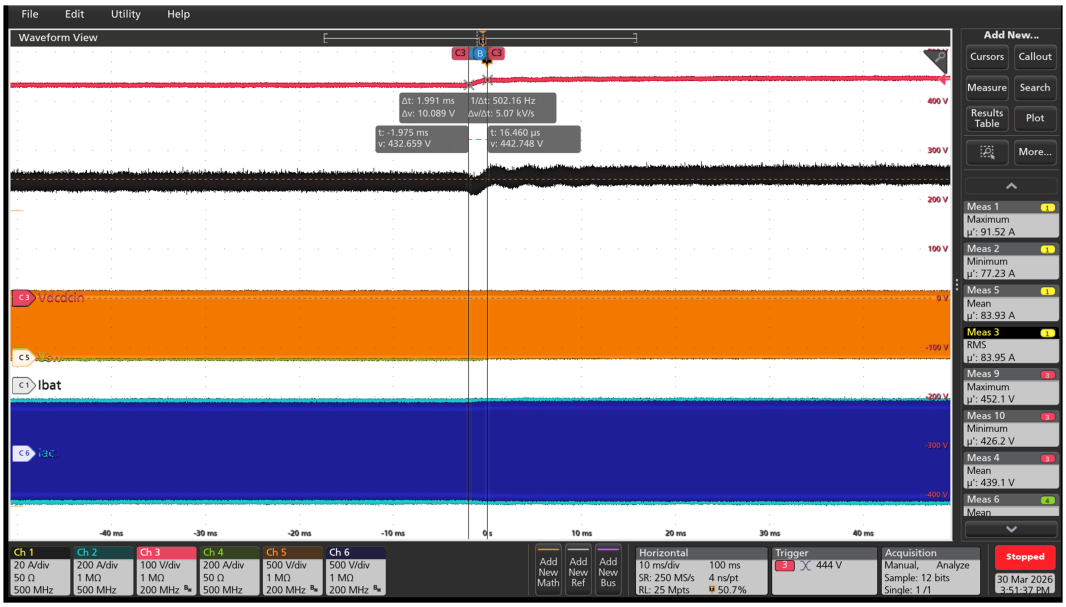


Fig. 5.80: Closed Loop Waveforms at 50 kW with inner and outer loop working for parallel realization and step in Battery Current from 81.95 A to 84.74 A at 50 kW, where the rectifier voltage changes from 435 V to 451 V, representing coupling at 0.19. From top to bottom are rectifier voltage V_{in}, battery current, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier. The rectifier voltage settles in 2 ms.

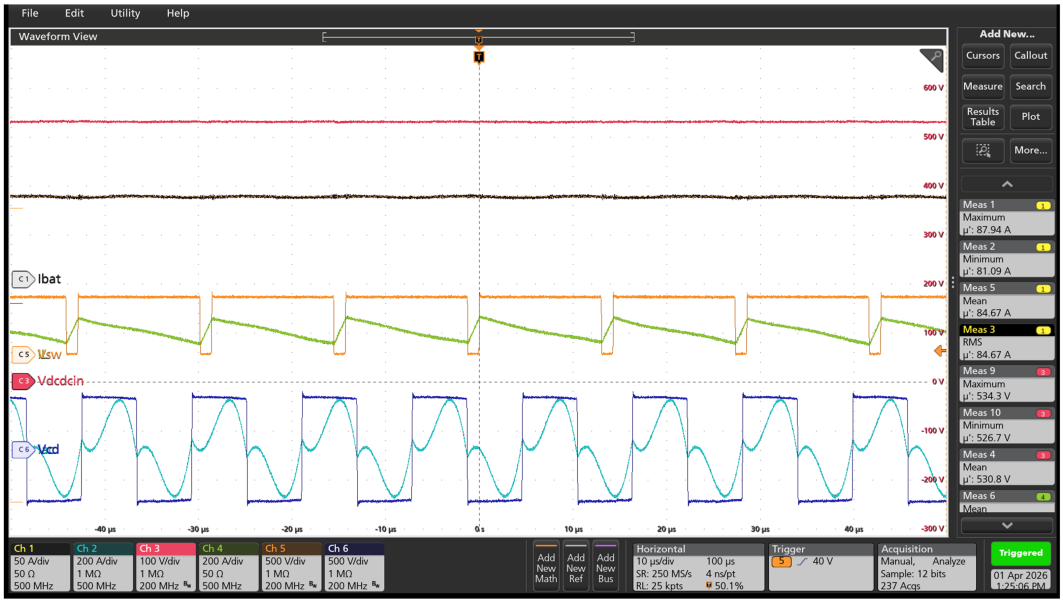


Fig. 5.81: Closed Loop Waveforms at 48.7 kW with inner and outer loop working for parallel realization at rectifier Voltage of 532 V, battery voltage of 580 V, battery Current of 83.9 A, rectifier current of 94 A, representing coupling of 0.15. From top to bottom are rectifier voltage V_{in}, battery current, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.



Fig. 5.82: Closed loop waveforms at 48.7 kW with inner and outer loop working for parallel realization at rectifier Voltage of 532 V and rectifier current of 94 A. From top to bottom are the primary switch node voltage, bridge current, and secondary rectifier current.

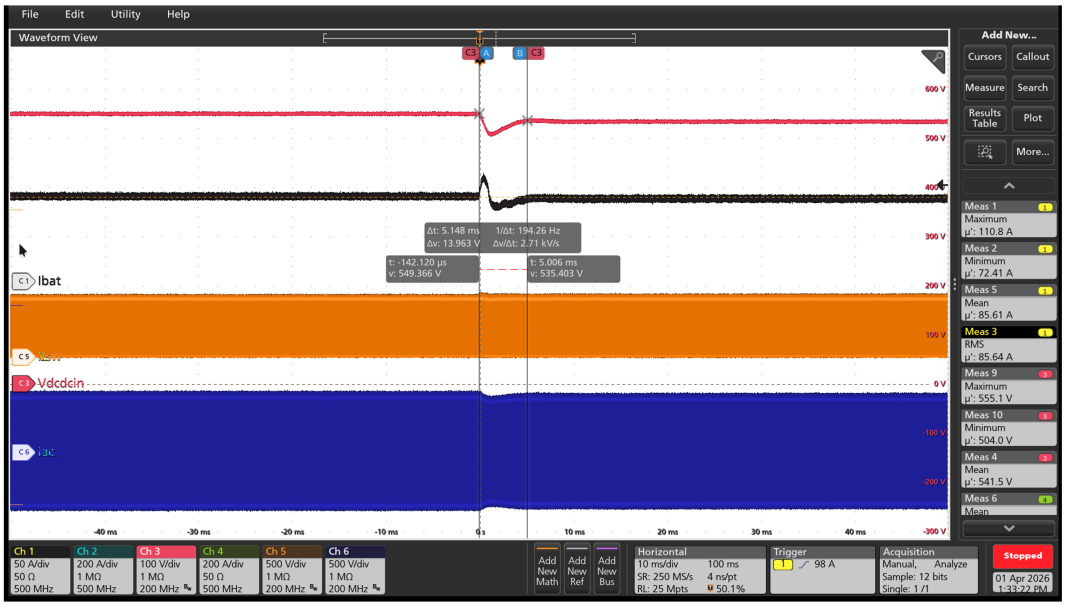


Fig. 5.83: Startup waveform at 48.7 kW with inner and outer loop working, showing cursor at input voltage during startup for parallel realization. The system always operates in closed loop and goes from saturation mode to closed loop mode during the startup when input current is ramped up from the power supply to replicate the lowest coupling factor 0.15, which can be regulated by closed loop. The complete startup from saturation mode to closed loop mode happens in 5 ms.

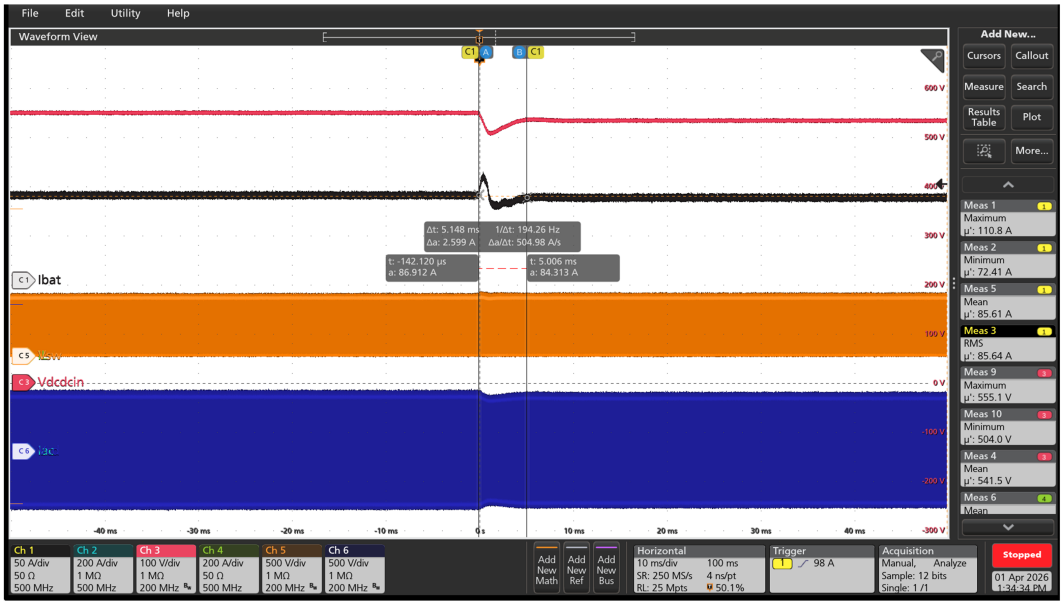


Fig. 5.84: Startup waveform at 48.7 kW with inner and outer loop working for parallel realization, showing the cursor at battery current during startup. From top to bottom are rectifier voltage V_{in}, battery current, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

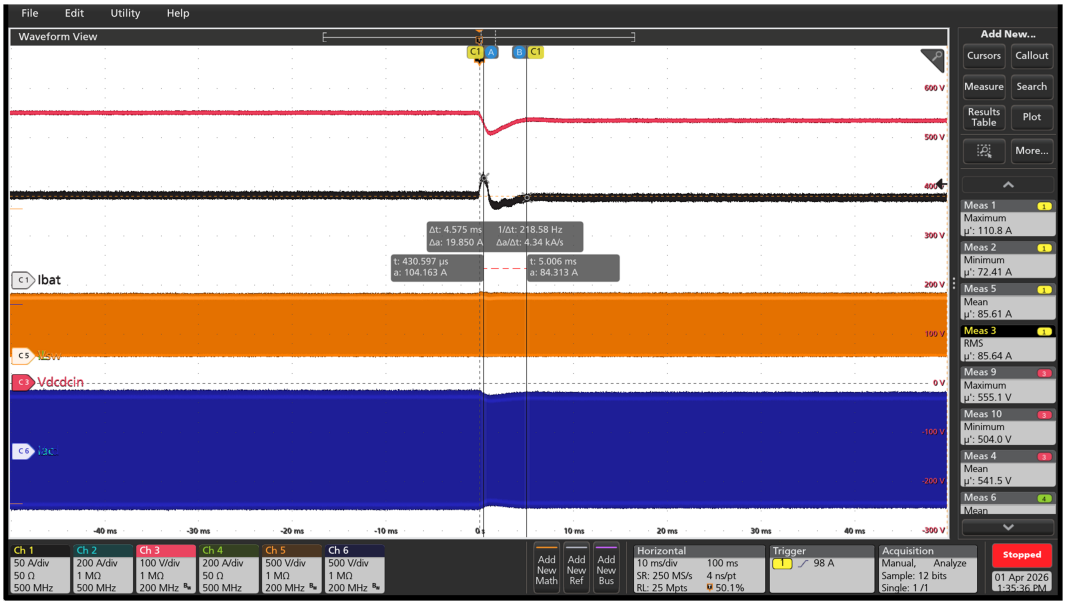


Fig. 5.85: Startup waveform at 48.7 kW with inner and outer loop working for parallel realization, showing peak current of 104 A during startup. From top to bottom are rectifier voltage V_{in}, battery current, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

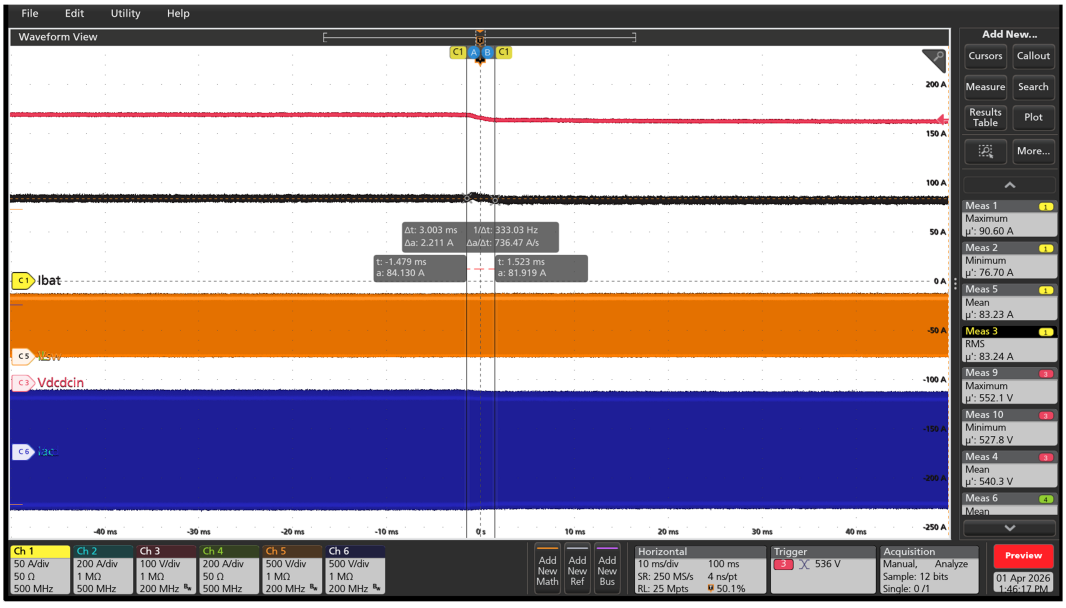


Fig. 5.86: Closed loop waveforms at 48.7 kW with inner and outer loop working for parallel realization and step in battery Current from 83.57 A to 81.44 A at 48.7 kW, where the rectifier voltage changes from 545 V to 535 V, representing coupling at 0.15. From top to bottom are rectifier voltage V_{in}, battery current, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier. The rectifier voltage settles in less than 3 ms.

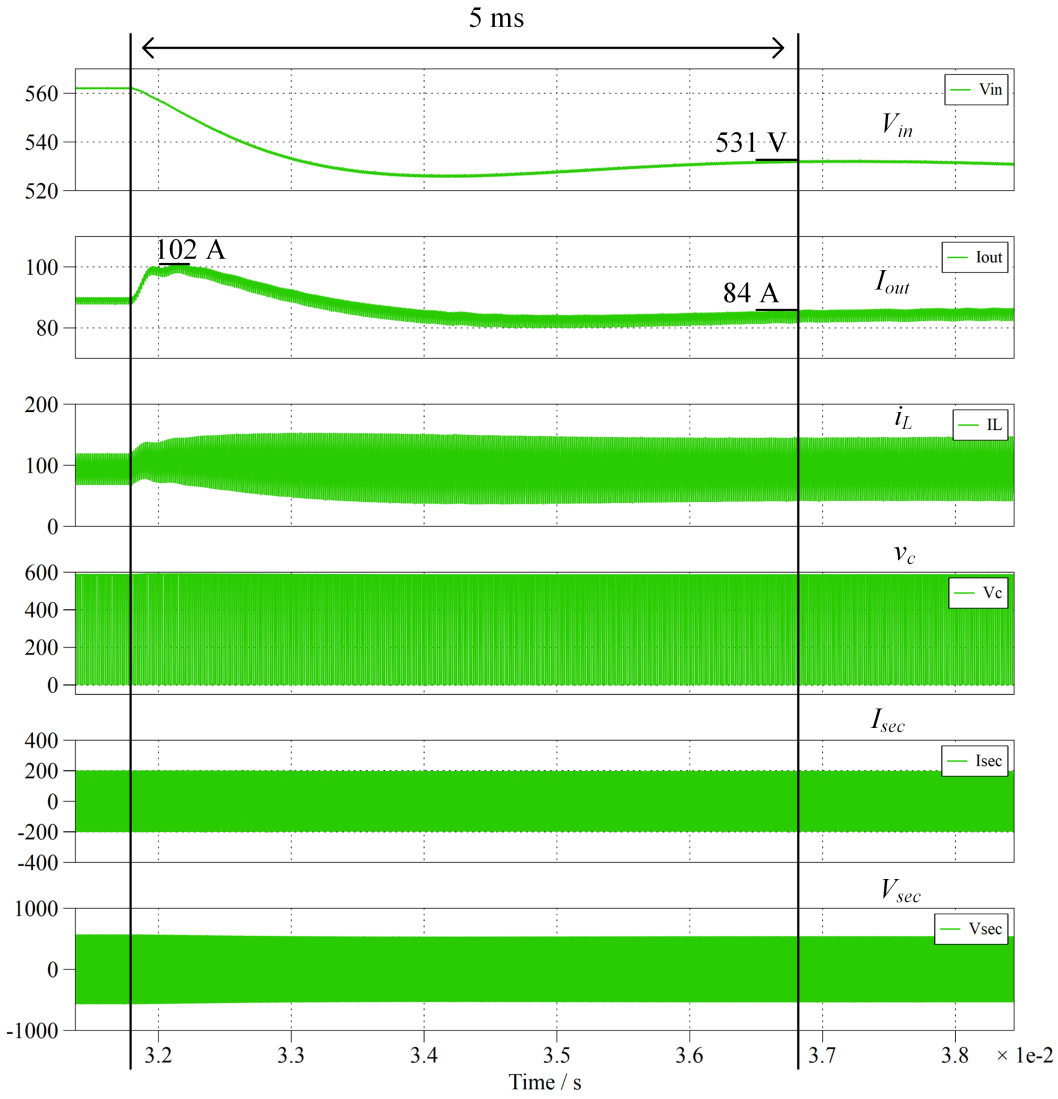


Fig. 5.87: Startup waveform at 48.7 kW from PLECS simulation with inner and outer loop working for parallel realization. The system always operates in closed loop and goes from saturation mode to closed loop mode during startup. The complete startup from saturation mode to closed loop mode happens in 5 ms.

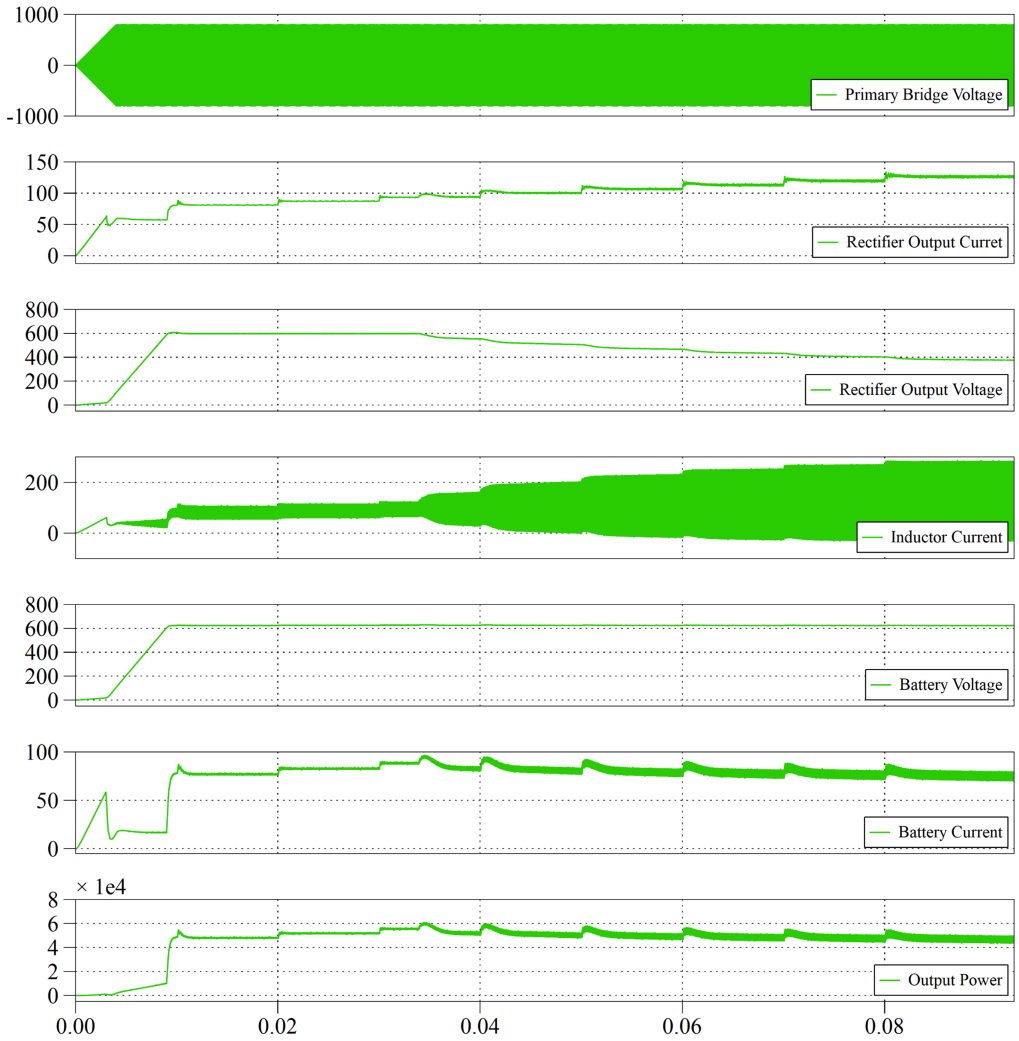


Fig. 5.88: Dynamic waveforms at 50 kW from PLECS simulation with inner and outer loops working for parallel realization.

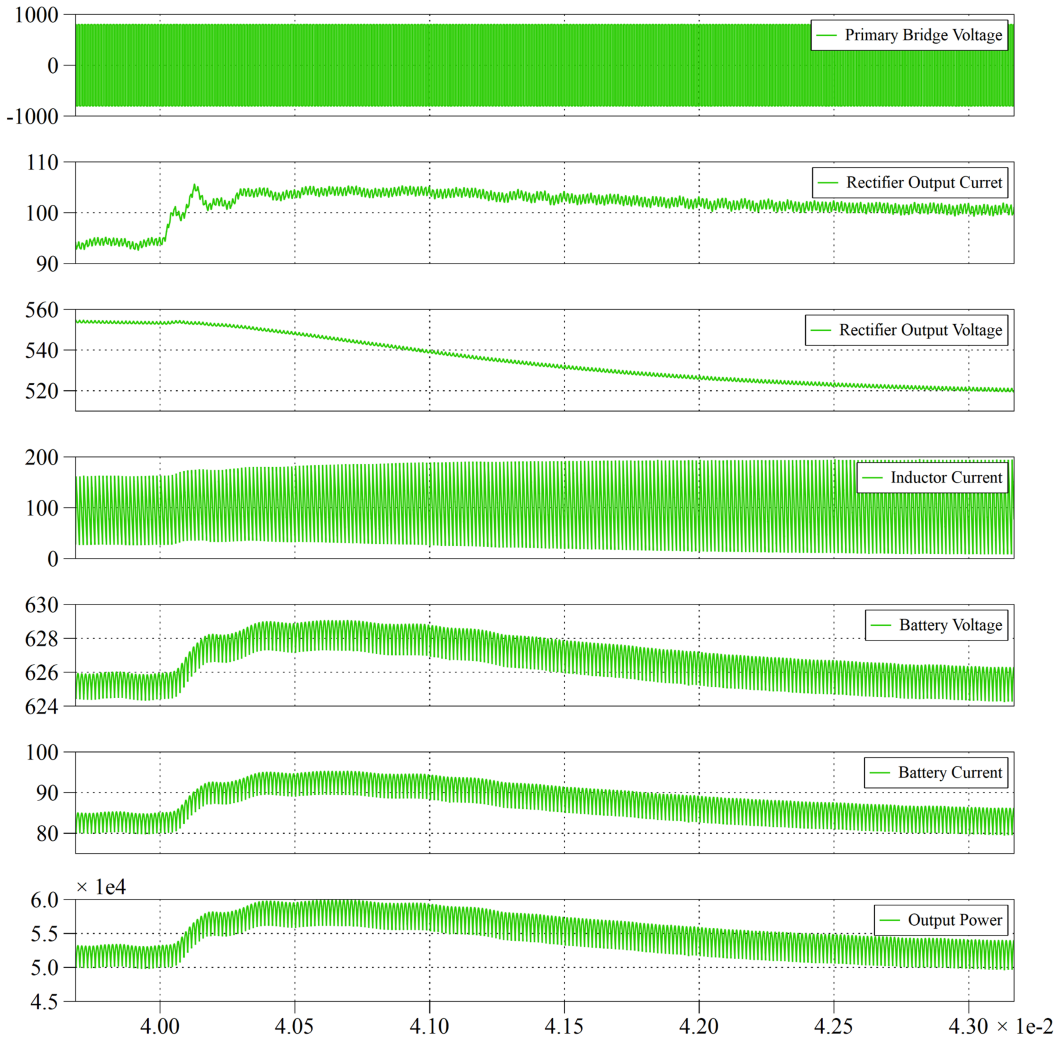


Fig. 5.89: Dynamic waveforms at 50 kW from PLECS simulation with inner and outer loops working for parallel realization at 40 ms.

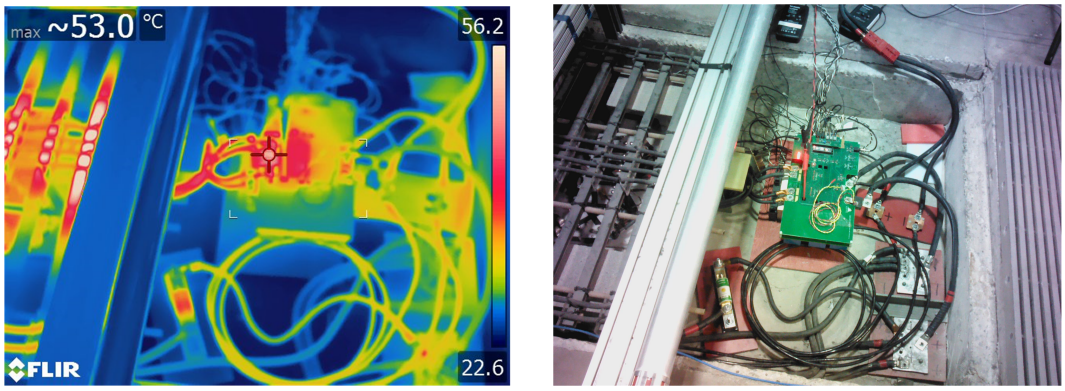


Fig. 5.90: Thermal image of the primary inverter at 50 kW at rectifier current of 125 A.

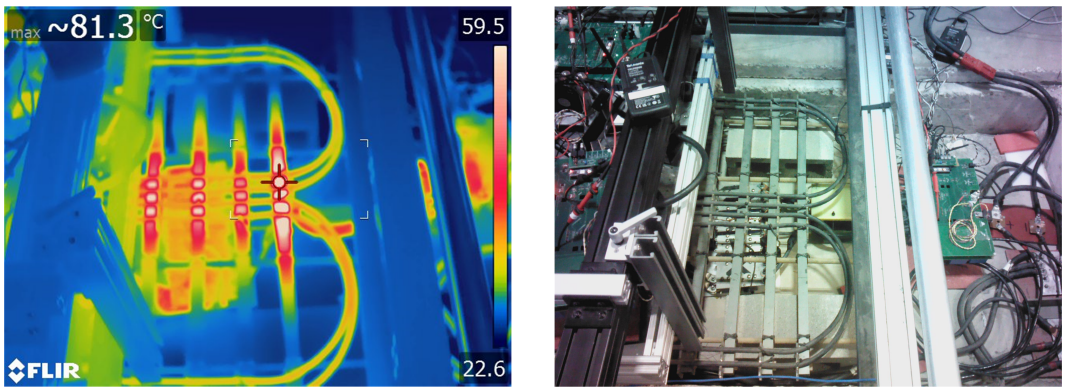


Fig. 5.91: Thermal image of the primary pad at 50 kW at rectifier current of 125 A.

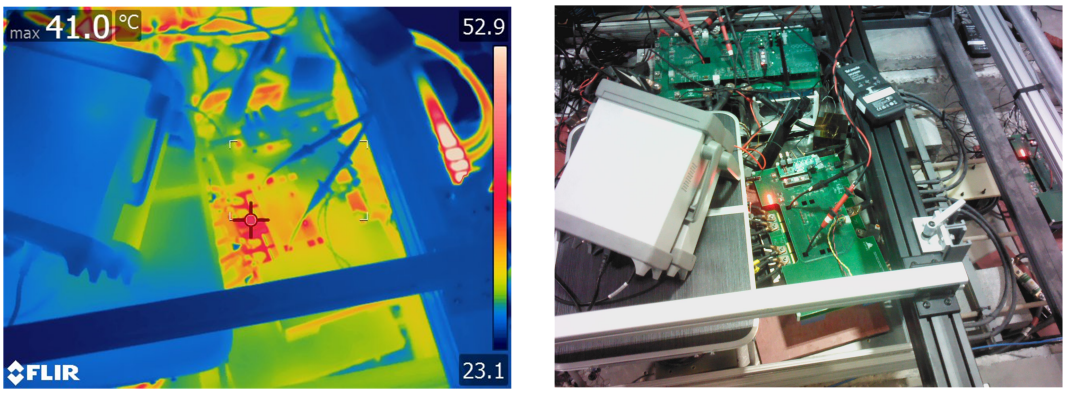


Fig. 5.92: Thermal image of secondary rectifier at 50 kW at rectifier current of 125 A.

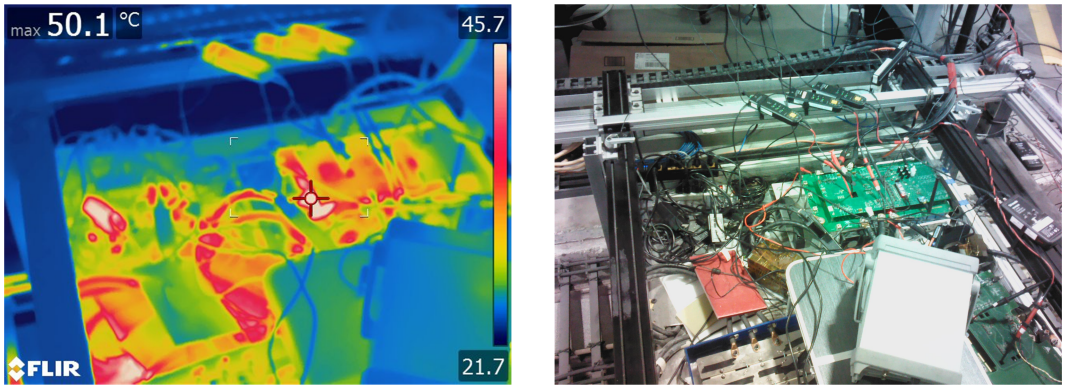


Fig. 5.93: Thermal image of DC-DC converter at 50 kW at rectifier current of 125 A.

5.7.3 Experimental Results for Dynamic Testing at 8 kW

For the Dynamic testing of a full WPT system at 8 kW, Gustav Klein is used as the power supply at the input of the WPT system, and NHR 9300 is used as the battery at the output of the DC-DC converter. Fig. 5.94 shows the experimental setup of the full rail system, in which the secondary side could be moved over the primary side. Fig. 5.95 shows the location of primary and secondary pads when they are in an aligned position. Fig. 5.95 shows the probe and oscilloscope setup on the secondary side. The power supply voltage is kept constant at 290 V. The load or NHR 9300 voltage is set to 250 V. The start position of the secondary side is shown in Fig. 5.94. To collect the experimental results, the secondary side is moved at approximately 1 mph. Due to space constraints and the location shown in the aligned position, to replicate the secondary passing over the primary, the secondary side is reversed after it reaches the aligned position. After the secondary reaches the aligned position, it is reversed and brought back to the start position. The battery current is regulated to approximately 33.5 A at a power of approximately 8.37 kW by DC-DC controls. Fig. 5.97 and Fig. 5.98 show the waveforms on the secondary side for this experimental setup. Fig. 5.99 shows the waveforms on the primary side for this experimental setup. In Fig. 5.97 and Fig. 5.98, the movement of secondary over primary is labeled into time intervals a, b, c, d, e, f, g, and h. During time interval a, the secondary is approaching the primary, and the rectifier or inductor current is 0. The NHR 9300 voltage fluctuates during this interval because of the nature of the NHR 9300 load when operating in constant-

voltage mode. As the secondary side approaches the primary side during time interval b, the NHR 9300 remains at 250 V, and the rectifier current, or the inductor current in green, begins to rise. The duty cycle of the DC-DC converter is saturated at its minimum value during this time interval, and the rectifier current is constant at approximately 240 V. When the average inductor current exceeds the battery current of 33.5 A over the time interval c, the battery current can be regulated via DC-DC control, and the controller begins regulating it. It can be noted that the large ripple in battery current is not actually present, but is due to the oscilloscope being placed on the rectifier and interference from the WPT system's magnetic field. The rectifier voltage changes from 240 V at the start of this interval to approximately 140 V at the end, with an average inductor current of approximately 60 A at the end of the interval, or at the aligned position of the secondary and primary. During the time interval d or the aligned position of the secondary and primary, the rectifier voltage is constant at approximately 140 V. During the time interval e, when the secondary is in reverse position and leaves the primary pad, the average inductor current starts decreasing, and the rectifier voltage changes from 140 V to 240 V to keep the average battery current constant at 33.5 A, thereby maintaining constant power with misalignment. The time interval h represents the sum of the time intervals c, d, and e, during which the controller maintains a constant battery current of 33 A and a constant output power of 8.37 kW. The average inductor current is 60 A at rectifier voltage of 140 V at an approximate coupling coefficient of 0.2, and the average inductor current is approximately 35 A at rectifier voltage of 240 V at an approximate coupling coefficient of 0.12. The DC-DC converter controller maintains constant power over the coupling coefficient range of 0.12-0.2 in this experimental setup. The time interval f replicates the time interval b, during which the average inductor current starts decreasing and drops to 0 at the end of this interval. The time interval g replicates that of f, during which the secondary completely leaves the primary. From the waveforms of the primary side in Fig. 5.99, it can be observed that, over the entire time interval h, the average input current in green remains constant at 35A.

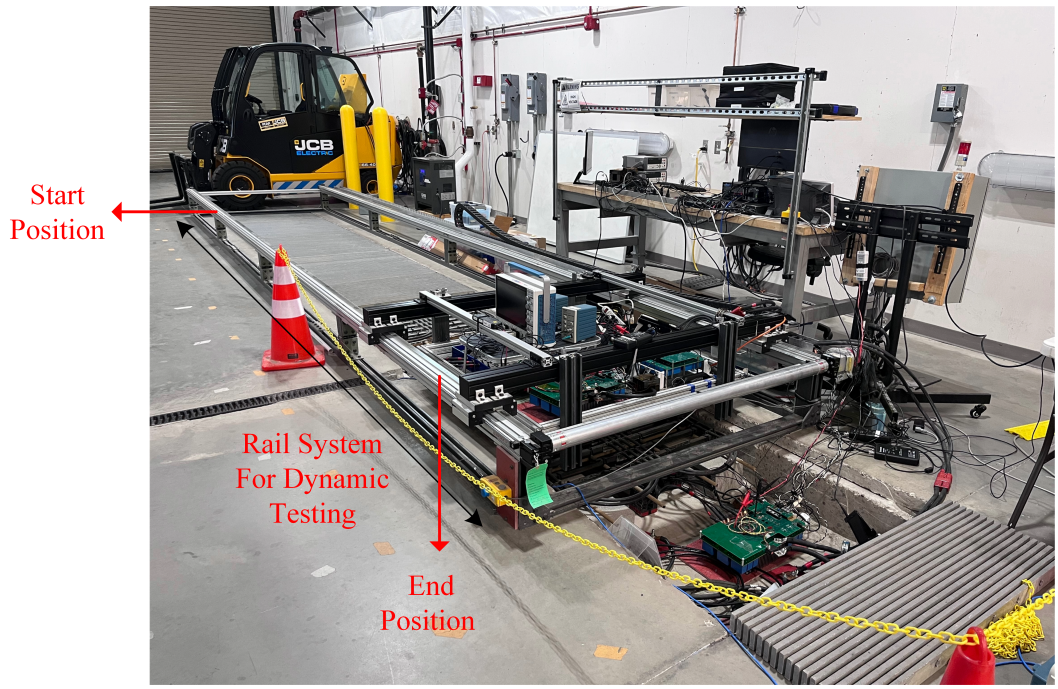


Fig. 5.94: Experimental setup of WPT System for Dynamic Testing, showing the full Rail System.

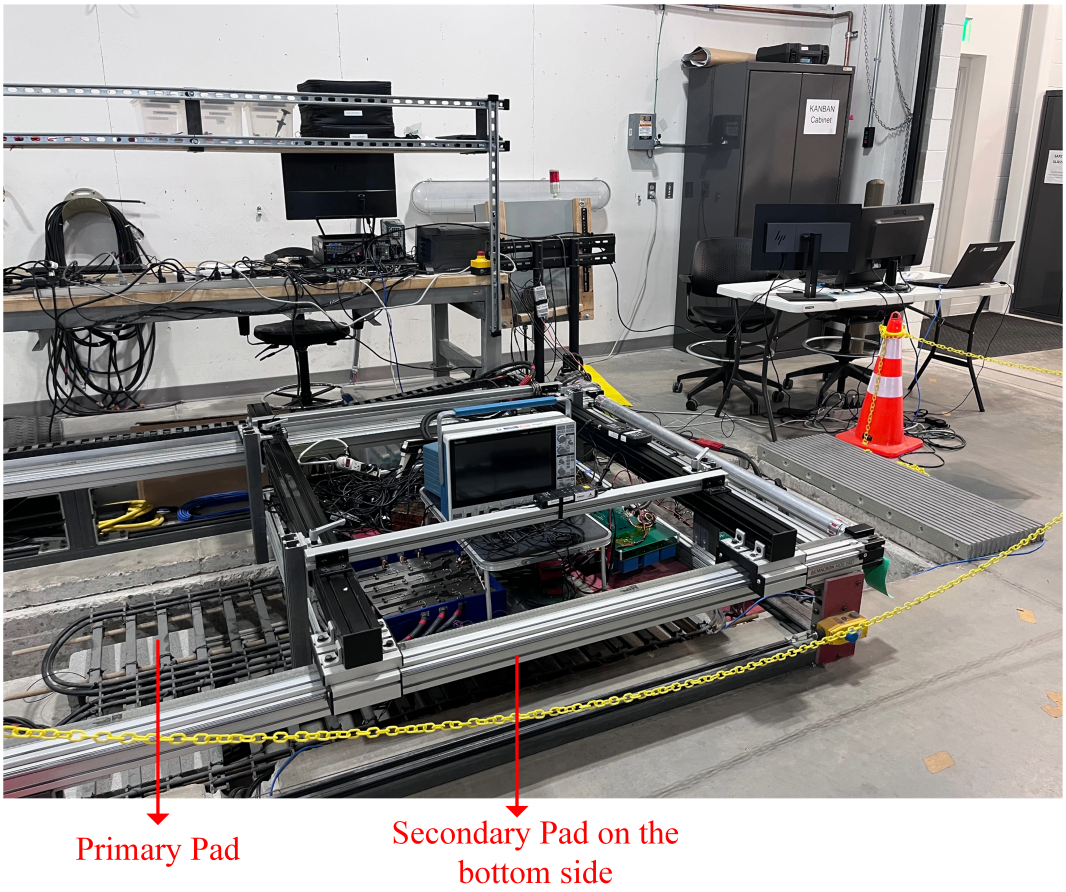


Fig. 5.95: Experimental setup for Dynamic Testing, showing the location of the primary and secondary pad when aligned.

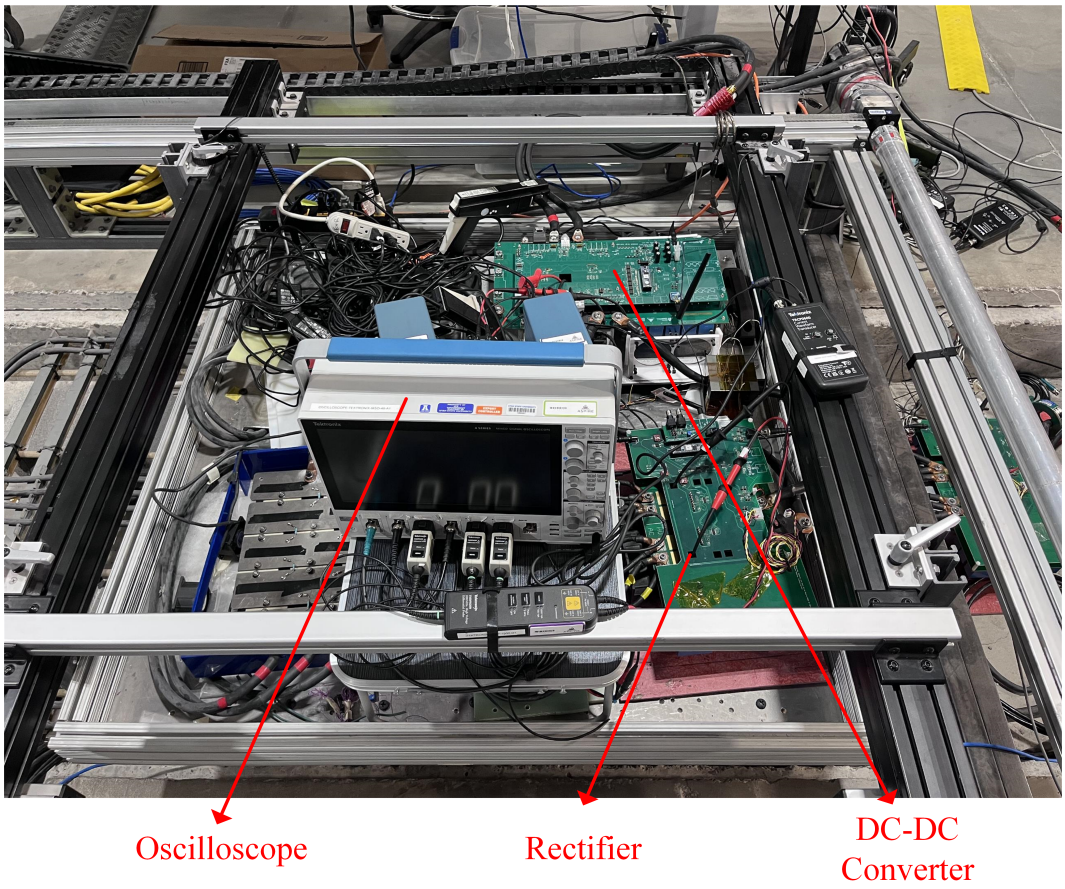


Fig. 5.96: Experimental setup for Dynamic Testing, showing the probe and oscilloscope setup.

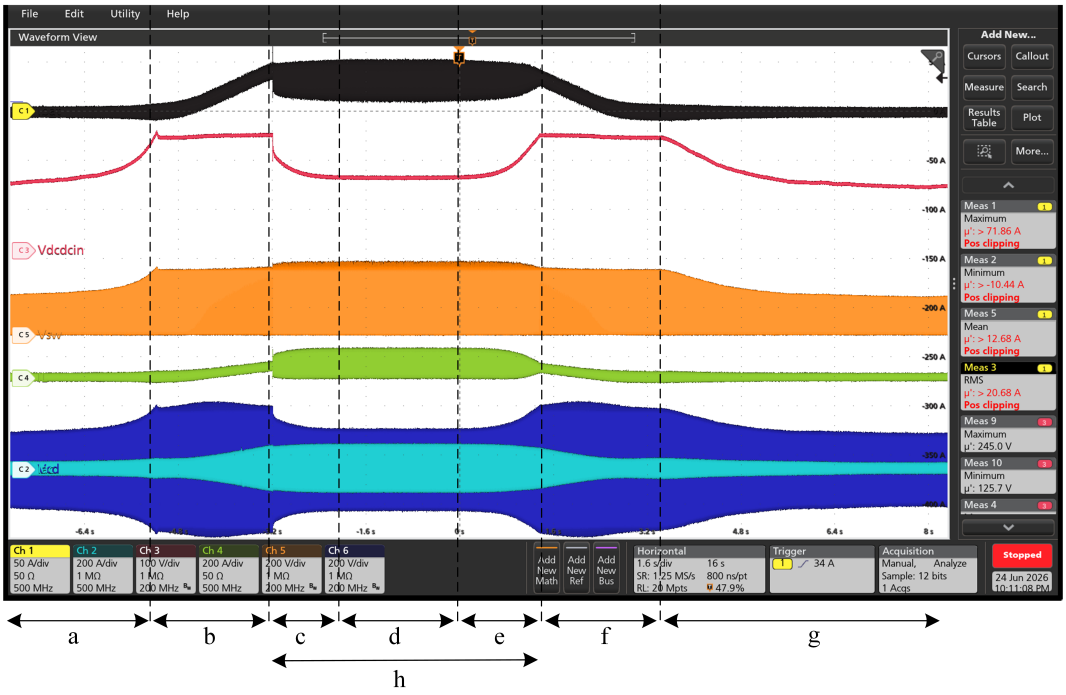


Fig. 5.97: Dynamic Waveforms for the secondary side at a speed of 1 mph. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

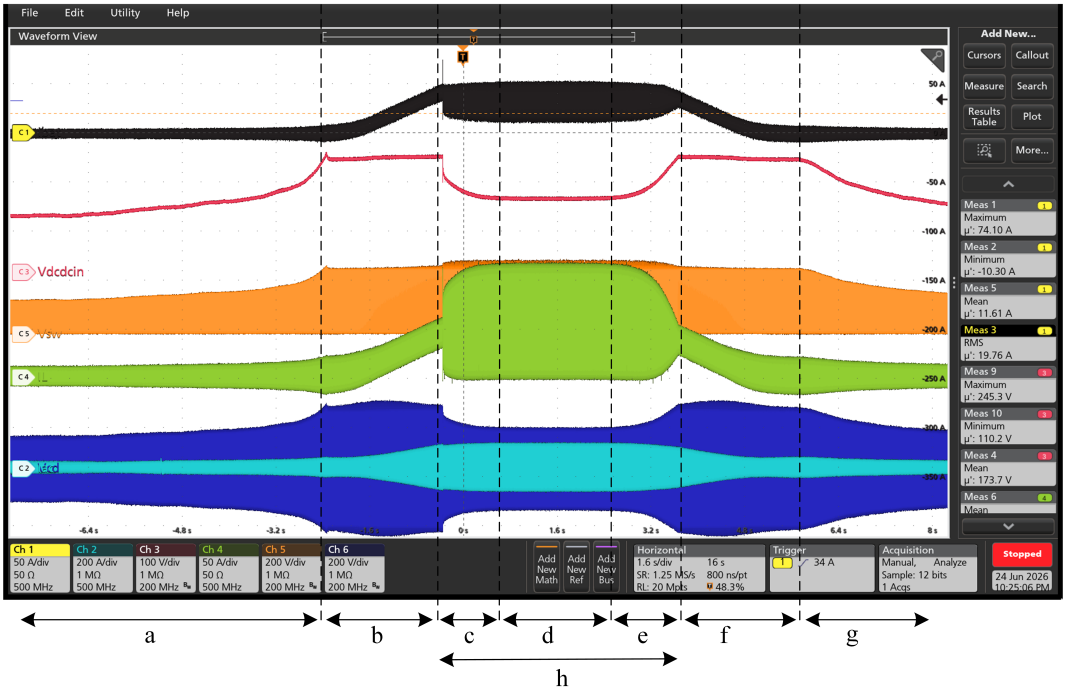


Fig. 5.98: Dynamic Waveforms for the secondary side at a speed of 1 mph, with slightly less time over the primary, and a zoomed-in scale of inductor current of DC-DC. From top to bottom are battery current, rectifier voltage V_{in}, switch node voltage, and inductor current of DC-DC, switch node voltage, and tank current of the rectifier.

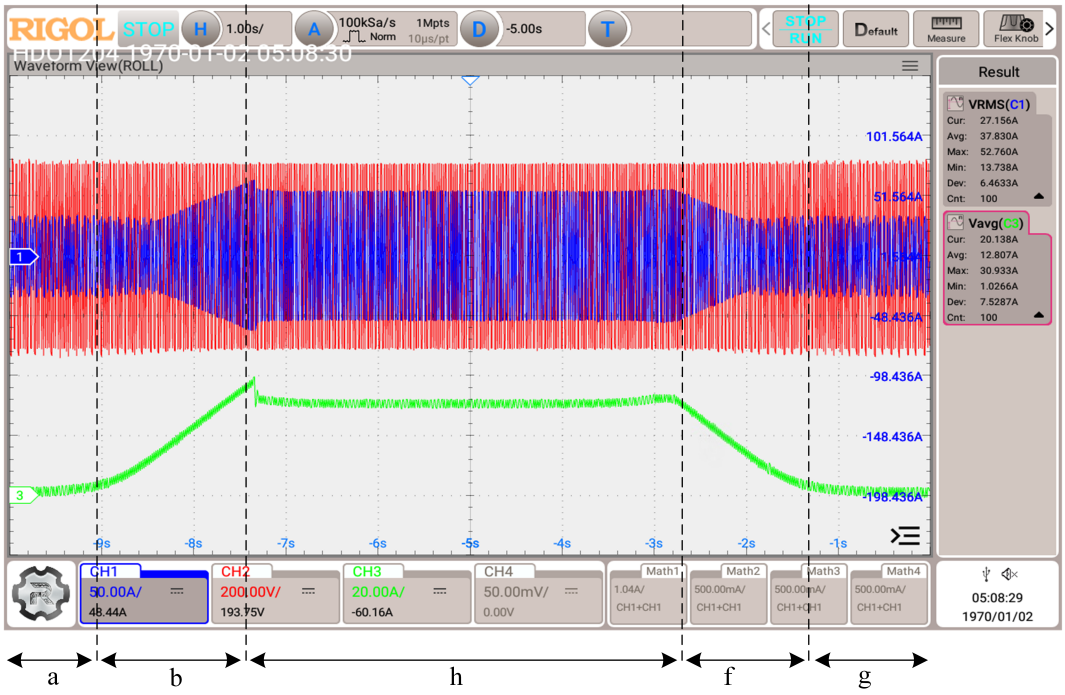


Fig. 5.99: Dynamic Waveforms for the primary side at a speed of 1 mph. From top to bottom are the primary switch-node voltage, primary bridge current, and input current of the WPT system.

5.8 Conclusion

In this chapter, the stability analysis of the full WPT system with double-sided LCC tuning and ZVS-QSW boost converter is provided. The impedance modeling of the WPT system is done using phasor modeling. The ZVS-QSW boost converter is modeled using discrete time modeling to achieve an accurate model at high frequencies, and also includes accurate modeling with battery resistance as compared with average modeling of DC-DC converters for the WPT system. Higher-order compensators are used to achieve high bandwidth and improved stability of the control loops. A comparison is also made between cascade and parallel realizations for the implementation of higher-order compensators. The experimental results for dual loop controls at 50 kW are provided to meet the fast response requirement for DWPT systems. The dynamic results of the full WPT system are presented at 8 kW, where constant power is maintained for a coupling coefficient range of 0.12-0.2.

CHAPTER 6

PARALLEL RESONANT SERIES-SERIES TUNING

In this chapter, a parallel resonant series-series (PRSS) tuning method is proposed for IPT systems to deliver nearly constant power from primary to secondary for a range of coupling coefficient k without any external controls required. The design of the tuning method is based on k between the primary and secondary coils and can be used for any type of coil. Moreover, the range of coupling coefficient over which nearly constant power is desired can be selected by the designer. This helps in designing the PRSS tuning method for both static and dynamic IPT systems. Section 6.1 mentions the PRSS tuning and the concept by which it can achieve nearly constant power. Section 6.2 provides the design procedure for the PRSS tuning method for IPT systems. Section 6.3 gives a design example for tuning a DWPT system, and analysis and simulation results for the design example have been provided. This section also gives a comparison of PRSS tuning with series-series and double-sided LCC tuning in terms of Output Power.

6.1 Parallel Resonant Series-Series (PRSS) Tuning

6.1.1 Background of series-series compensation

This tuning method for IPT systems is a further extension of a series-series compensation [87]. In Fig. 6.1, V_g is the input DC voltage, L_p and L_s are the self-inductances of primary and secondary coils respectively, r_p and r_s are the equivalent series resistances of the primary and secondary coils respectively, k is the coupling coefficient between primary and secondary coil, M is defined as the mutual inductance between the two coils and given in (6.1), and C_{ps} and C_{ss} are the compensation capacitors for L_p and L_s respectively, V_{out} and I_{out} are the output voltage and current. Fig. 6.2 represents an equivalent circuit of series-series compensation where the inverter and rectifier of Fig. 6.1 are modeled using

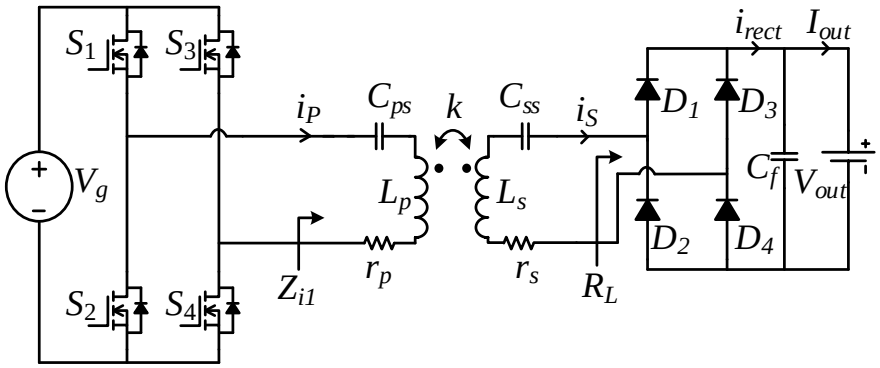


Fig. 6.1: IPT system with series-series compensation.

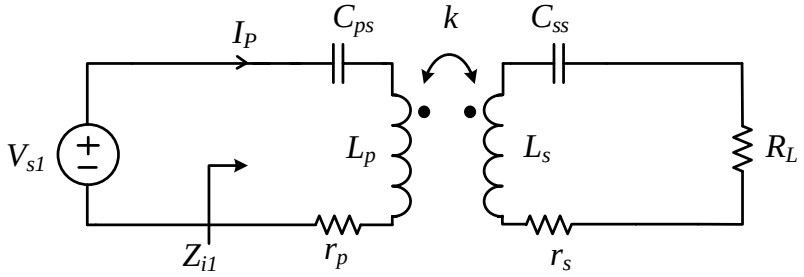


Fig. 6.2: Equivalent circuit of series-series compensation.

sinusoidal approximation [84]. V_{s1} is the peak value of the fundamental component of the output voltage of the H-bridge inverter by sinusoidal approximation as shown in Fig. 6.2 and given in (6.2), R_L in Fig. 6.2 is the equivalent load resistance seen from the rectifier circuit as shown in Fig. 6.1 and is given in (6.3). Z_{i1} is the input impedance seen from the point shown in Fig. 6.2. If L_s and L_p are compensated by C_{ss} and C_{ps} respectively using series-series compensation operating at the switching frequency w_s equal to the resonant frequency w_r, Z_{i1} is purely resistive which can be analyzed using a T-model of coupled inductors for a series-series compensation [87], and Z_{i1} at w_r denoted as $Z_{i1}(w_r)$ is given in (6.4).

$$M = k\sqrt{L_p L_s} \tag{6.1}$$

$$V_{s1} = \frac{4}{\pi} V_g \tag{6.2}$$

$$R_L = \frac{8V_{out}^2}{\pi^2 P_{out}} \tag{6.3}$$

$$Z_{i1}(w_r) = r_p + \frac{w_r^2 M^2}{R_L + r_s}. \tag{6.4}$$

The power transferred to the secondary circuit for series-series compensation in Fig. 6.2 is given in (6.5), [87], where $I_{P_{rms}}$ is the root-mean-square (RMS) value of i_P in Fig. 6.1. P_{out} is defined as output power given in (6.6), and is nearly equal to the power transferred to the secondary P_s given in (6.5).

$$P_s = \frac{w_r^2 M^2}{R_L + r_s} I_{P_{rms}}^2 \tag{6.5}$$

$$P_{out} = V_{out} I_{out}. \tag{6.6}$$

From the series-series compensation, it can be observed from the power transfer equation (6.5) that if w_r, R_L, and r_s are kept constant, the power transfer to the secondary can be changed by either changing $I_{P_{rms}}$ or M. With misalignment in the IPT system, the value of coupling coefficient k will decrease, due to which M will decrease from (6.1), and from (6.5), it is possible to maintain a nearly constant power for a range of k by increasing $I_{P_{rms}}$ slightly as k decreases.

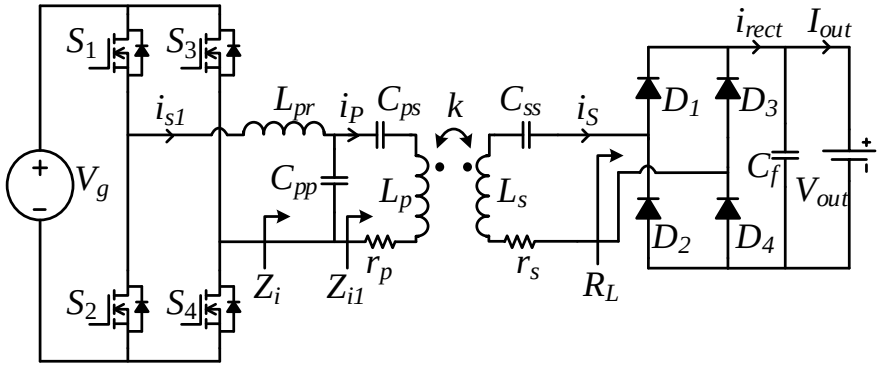


Fig. 6.3: Parallel resonant series-series (PRSS) tuning.

6.1.2 Introduction to PRSS tuning

Fig. 6.3 represents the PRSS tuning, where a parallel resonant tank is added before

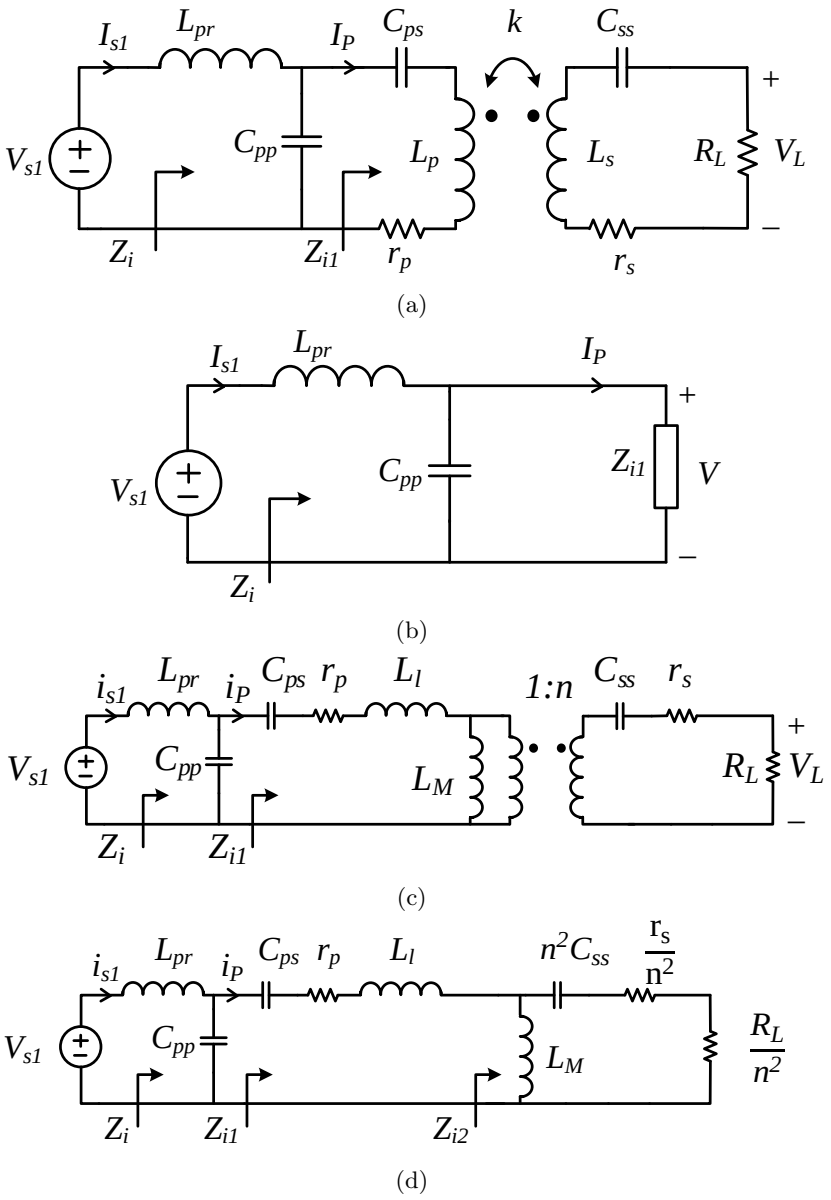


Fig. 6.4: Equivalent circuit models of PRSS tuning: (a) Equivalent circuit, (b) Equivalent circuit with Z_{i1}, (c) Transformer model for equivalent circuit, and (d) Transformer model referred to primary for equivalent circuit.

a series-series compensation. L_{pr} and C_{pp} in Fig. 6.3 are the inductance and capacitance of the tank respectively. Fig. 6.4(a) represents an equivalent circuit for PRSS tuning in Fig. 6.3. V_{s1} is the peak value of the fundamental component of the output voltage of the H-bridge inverter by sinusoidal approximation and given in (6.2), Z_i and Z_{i1} are the input impedance from the point shown in Fig. 6.4(a). If the system is operated at the switching frequency (w_s) equal to the resonant frequency (w_r) of L_p and C_{ps}, and L_s and C_{ss}, then Z_{i1} is purely resistive and is equal to $Z_{i1}(w_r)$ as mentioned in Section 6.1.1.

The equivalent model of Fig. 6.4(a) can be represented in Fig. 6.4(b), where a parallel resonant tank has a resistive load of Z_{i1} at resonant frequency w_r. The expression for peak value I_P and peak value I_{s1} in Fig. 6.4(a) are given in (6.7), and (6.8), where s is equal to jw.

$$I_P = \left| \frac{\frac{1}{sC_{pp}}}{Z_{i1} + \frac{1}{sC_{pp}}} \right| I_{s1} \tag{6.7}$$

$$I_{s1} = \frac{V_{s1}}{|Z_i|} \tag{6.8}$$

$$I_{P_{rms}} = \frac{I_P}{\sqrt{2}}. \tag{6.9}$$

It should be noted that $I_{P_{rms}}$ given in (6.9) is the current that is responsible for transferring power in the proposed tuning, as mentioned in series-series compensation given in (6.5). It can also be observed from (6.4), as the value of k decreases, the value of $|Z_{i1}(w_r)|$ also decreases. In Fig. 6.4(b), $|Z_{i1}|$ is the resistive load to the parallel tank at w_r. Fig. 6.5 represents the behavior of input impedance $|Z_i|$ with resistive load $|Z_{i1}|$ where $|Z_{i0}|$ is the resistance when $|Z_{i1}|$ is shorted given in (6.10), and $|Z_{i\infty}|$ is the resistance when $|Z_{i1}|$ is open circuited given in (6.11). If the switching frequency of operation (f_s) is less than f_m, which is the intersection frequency of $|Z_{i0}|$ and $|Z_{i\infty}|$, $|Z_i|$ decreases with decrease in resistive load $|Z_{i1}|$ from Theorem 22.1 in [84]. With decrease in $|Z_{i1}|$, $|Z_i|$ should decrease below f_m, due to which I_{s1} and I_P should increase. Thus, a nearly constant power can be maintained over

a range of k by increasing I_P and, consequently, $I_{P_{rms}}$ slightly as k decreases.

$$Z_{i0} = sL_{pr} \tag{6.10}$$

$$Z_{i\infty} = sL_{pr} + \frac{1}{sC_{pp}}. \tag{6.11}$$

For analyzing Z_i, transformer model of coupled inductors given in Fig. 6.4(c) is used, where L_l, L_M and turns ratio n are given in (6.12), (6.13), and (6.14) respectively. Z_i and Z_{i1} in Fig. 6.4(c) are analyzed in terms of impedances defined by means of phasors rotating at frequency w, where $s = jw$ is used for analysis. All the impedances in Fig. 6.4(c) are referred to the primary side as shown in Fig. 6.4(d), where impedance Z_{i2} shown in Fig. 6.4(d) is given in (6.15). Fig. 6.4(d) is then used to derive Z_{i1} given in (6.16), and Z_i given in (6.17), in terms of Z_{i2}.

$$L_l = (1 - k^2)L_p \tag{6.12}$$

$$L_M = k^2 L_p \tag{6.13}$$

$$n = \frac{1}{k}\sqrt{\frac{L_s}{L_p}} \tag{6.14}$$

$$Z_{i2} = \frac{(\frac{r_s}{n^2} + \frac{R_L}{n^2} + \frac{1}{sn^2C_{ss}})(sL_M)}{(\frac{r_s}{n^2} + \frac{R_L}{n^2} + \frac{1}{sn^2C_{ss}}) + (sL_M)} \tag{6.15}$$

$$Z_{i1} = \frac{1}{sC_{ps}} + r_p + sL_l + Z_{i2} \tag{6.16}$$

$$Z_i = sL_{pr} + \frac{(Z_{i1})(\frac{1}{sC_{pp}})}{(Z_{i1}) + (\frac{1}{sC_{pp}})}. \tag{6.17}$$

6.2 Design Procedure for PRSS Tuning

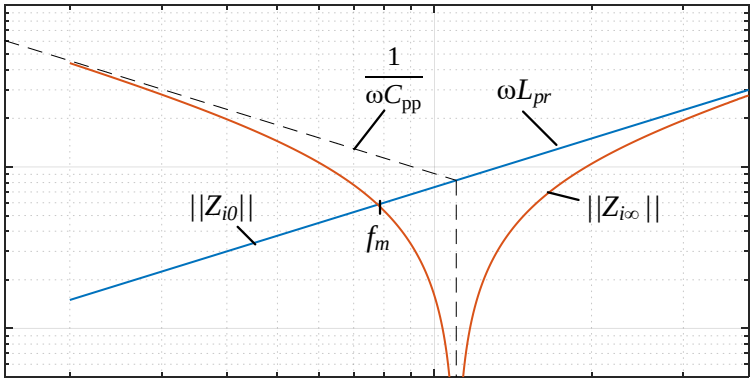


Fig. 6.5: $|Z_i|$ plots for parallel LC tank for limiting cases $|Z_{i1}| \to 0$ and $|Z_{i1}| \to \infty$.

6.2.1 Detailed design procedure

This section describes the complete design procedure and steps to be followed for designing the PRSS tuning for IPT systems. The parameters in Fig. 6.3 are the same as the parameters mentioned in Section 6.1.1.

(i) The primary coil and secondary coil are designed considering the following self-inductances and losses in the coil represented by L_p, r_p, L_s, and r_s, and then also determining the quality factors Q_1 and Q_2 of primary and secondary coil, respectively, from (6.18).

$$Q_1 = \frac{w_s L_p}{R_p} \text{ and } Q_2 = \frac{w_s L_s}{R_s}. \tag{6.18}$$

(ii) C_{ss} and C_{ps} are selected using series-series compensation, where switching frequency w_s is kept equal to the resonant frequency w_r of L_s and C_{ss}, and L_p and C_{ps} [87].

(iii) Then, determining the value of load resistance R_L at which the maximum efficiency occurs for a series-series tuned system using the equation given as (6.19), in [88]. V_{out} in Fig. 6.3 is also evaluated from (6.20), where P_{out} is output power, which is a known value and is nearly equal to P_s, the power transferred to the secondary circuit. It should be noted here that R_L at the maximum efficiency point is chosen for a better system performance. In a practical system, R_L would depend on the battery voltage of the system.

$$R_L = k r_s \sqrt{Q_2 Q_1} \tag{6.19}$$

$$V_{out} = \sqrt{\frac{R_L \pi^2 P_{out}}{8}}. \tag{6.20}$$

(iv) The magnitude of Z_{i1}, $|Z_{i1}|$ mentioned in Fig. 6.4(b) is calculated at switching frequency of operation w_s ($w_s = w_r = 2\pi f_s$) at lowest coupling coefficient (k) value for the range of constant power to be achieved from (6.4), and is equal to $|Z_{i1}(w_r)|$. $|Z_{i1}|$ calculated can be denoted as $|Z_{i1}|_{nom}$. Using this value of $|Zi1|_{nom}$, calculate $I_{P_{rms}}$ in Fig. 6.4(b) at w_s from the power transfer equation given in (6.5), for a value of k that is somewhere in lower to middle range of k for constant power transfer.

(v) After the values $|Z_{i1}|_{nom}$ and $I_{P_{rms}}$ from (iv) are evaluated, determine the peak value $I_P (I_P = \sqrt{2} I_{P_{rms}})$ and peak value $V (V = I_P |Z_{i1}|_{nom})$ denoted in Fig. 6.4(b) across $|Zi1|$ at this operating point.

(vi) Follow a detailed design procedure for a parallel resonant tank such that f_s is less than f_m as shown in Fig. 6.5 and also verify the zero voltage switching (ZVS) condition [84].

6.2.2 Parallel resonant tank design for PRSS tuning

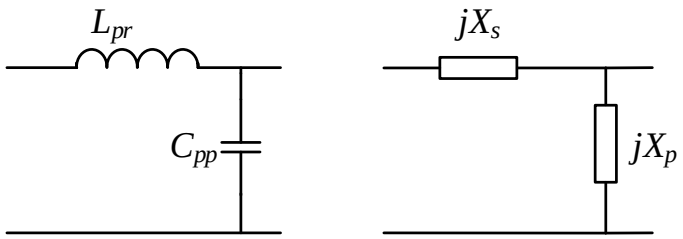


Fig. 6.6: Parallel LC tank network.

For the parallel resonant tank design of Fig. 6.4(b) and Fig. 6.6, solve the output v-i characteristics of the resonant inverter using the values obtained in Section 6.2.1 step (vi) using (6.21), [84]. V_{oc} is the peak open circuit voltage across Z_{i1} in Fig. 6.4 (b) when $Z_{i1} \to \infty$ or Z_{i1} is open circuited. $I_{P_{sc}}$ is the peak short circuit current in Z_{i1} in Fig. 6.4(b) when $Z_{i1} \to 0$ or Z_{i1} is shorted.

$$\frac{V^2}{V_{oc}^2} + \frac{I_P^2}{I_{P_{sc}}^2} = 1. \tag{6.21}$$

Then finding $|Z_{o0}|$ (magnitude of output impedance with input V_{s1} shorted) and $|H_\infty|$ (open circuit gain in terms of tank elements) in Fig. 6.4(b) at frequency of operation w_s ($w_s = w_r$) from (6.22), and (6.23).

$$|Z_{o0}| = \frac{V_{oc}}{I_{Psc}} \tag{6.22}$$

$$|H_\infty| = \frac{V_{oc}}{V_{s1}}. \tag{6.23}$$

Resonant tank elements in Fig. 6.6 are then selected to meet the specifications at the frequency of operation w_s ($w_s = w_r$).

$$X_s = w_s L_{pr} \tag{6.24}$$

$$X_p = -\frac{1}{w_s C_{pp}}. \tag{6.25}$$

$Z_{o0}(jw_s)$ and $H_\infty(jw_s)$ can also be founded from Fig. 6.6 as given in (6.26), and (6.27), respectively. Solving for X_s and X_p from (6.29), and (6.28), respectively, and then finally L_{pr} and C_{pp} using (6.24), and (6.25), respectively.

$$Z_{o0}(jw_s) = \frac{jX_pX_s}{X_p + X_s} \tag{6.26}$$

$$H_\infty(jw_s) = \frac{jX_p}{jX_p + jX_s} \tag{6.27}$$

$$jX_p = \frac{Z_{o0}(jw_s)}{1 - H_\infty(jw_s)} \tag{6.28}$$

$$X_s = X_p \frac{1 - H_\infty(jw_s)}{H_\infty(jw_s)}. \tag{6.29}$$

After solving for L_{pr} and C_{pp}, it is to be verified that the switching frequency of operation (f_s) is less than f_m, where f_m is given in (6.30). The ZVS conditions for the inverter transistors can be verified from (6.31) and (6.32), [84], where Z_{i0} and $Z_{i\infty}$ are

given in (6.33) and (6.34), respectively.

$$f_m = \frac{1}{2\pi\sqrt{2L_{pr}C_{pp}}} \tag{6.30}$$

$$|Z_{i1}(w_r)| < R_{crit} \tag{6.31}$$

$$R_{crit} = |Zo0|\sqrt{\frac{-Z_{i\infty}}{Z_{i0}}} \tag{6.32}$$

$$Z_{i0} = jX_s \tag{6.33}$$

$$Z_{i\infty} = j(X_s + X_p). \tag{6.34}$$

6.3 Design Example of PRSS Tuning

This section provides a design example of a 10 kW DWPT system for PRSS tuning, which uses standard values of the range of coupling coefficient (k) seen in DWPT systems, for which a nearly constant power system is designed. The design example has then been verified with simulations.

6.3.1 Design analysis

(i) Selecting the values of Q_1 and Q_2 to be 333 and 336 respectively. The values of r_p and r_s calculated from (6.18), are 0.08 Ω and 0.1 Ω respectively.

(ii) Then compensating L_p and L_s from Table 6.1 with C_{ps} and C_{ss} respectively using series-series compensation at resonant frequency w_r equal to switching frequency of operation w_s ($w_s = 2\pi f_s$). The calculated values of C_{ps} and C_{ss} are 70 nF and 56 nF, respectively.

(iii) Calculating the value of R_L from (6.19), to be 3 Ω and value of V_{out} to be 190 V from (6.20). The value of V_{out} is slightly adjusted to 180 V for better performance.

(iv) $|Z_{i1}|$ equal to $|Z_{i1}(w_r)|$ mentioned in Fig. 6.4(b) is calculated from (6.4), at f_s. The value of $|Z_{i1}|nom$ at f_s and $k = 0.09$ is calculated to be 2 Ω. IP_{rms} at $k = 0.12$ at f_s to transfer output power of 10 kW is calculated to be 50 A.

Table 6.1: Parameters used for DWPT design of PRSS tuning.

Parameter	**Value**
f_s	85 kHz
V_g	300 V
L_p	50 μH
L_s	63 μH
k	$0.09 - 0.2$

(v) V and I_P in Fig. 6.4(b) are calculated to be 142 V and 70.7 A respectively.

(vi) Then selecting V_{oc} to be 550 V and calculating L_{pr} and C_{pp} using the detailed design procedure in Section 6.2.2 to be 7.5 μH and 110 nF respectively.

f_m can be obtained from (6.30), and is equal to 123 kHz. R_{crit} at f_s can be evaluated from (6.32), for ZVS conditions and is equal to 13.4 Ω. $|Z_{i1}(w_r)|$ at $k = 0.09$ is 2 Ω and at $k = 0.2$ is 11.5 Ω. Thus, the ZVS condition given in (6.31) is satisfied for the entire range of k from 0.09 to 0.2. The plot of Z_{i0} and $Z_{i\infty}$ vs frequency is given in Fig. 6.7, from which we can observe that the switching frequency of operation (f_s) is less than f_m as mentioned in Section 6.2.2. Fig. 6.8 shows the curve of Z_i vs frequency, where we can observe that, at f_s = 85 kHz, $|Z_i|$ decreases slightly as the value of k decreases from 0.2 to 0.09, due to which $I_{P_{rms}}$ increases slightly to maintain the constant power transfer mentioned in Section 6.2.2. Fig. 6.9 shows the plot of $|H|$ where $|H|$ is given in (6.35), where V_L is the maximum voltage across R_L as shown in Fig. 6.4(a). It can be observed that, since $|H|$ is nearly constant at f_s = 85 kHz for k = 0.09 - 0.2, V_L and $V_{L_{rms}}$ (RMS voltage across R_L) are constant and since R_L which is equal to 3 Ω for this design is constant, thus power across R_L (P_L) given in (6.36), or approximate value of output power is nearly constant.

$$|H| = \frac{V_L}{V_g} \tag{6.35}$$

$$P_L = \frac{V_{L_{rms}}^2}{R_L}. \tag{6.36}$$

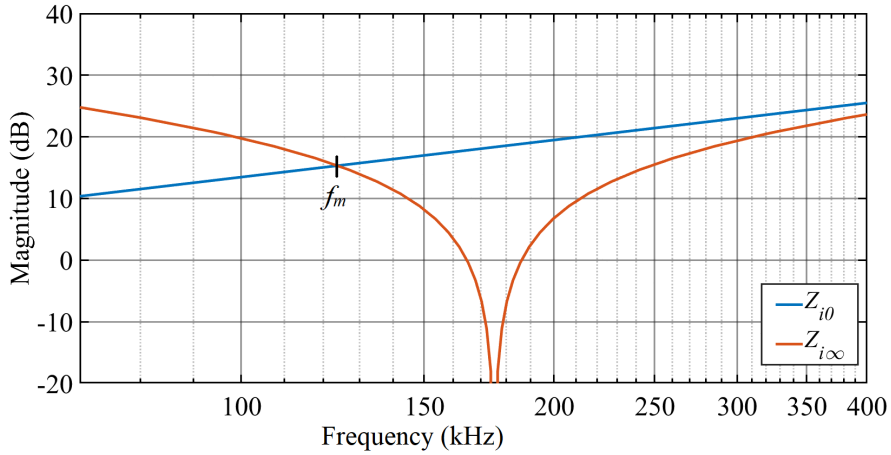


Fig. 6.7: Z_{i0} and $Z_{i\infty}$ plots of LC tank design for PRSS tuning.

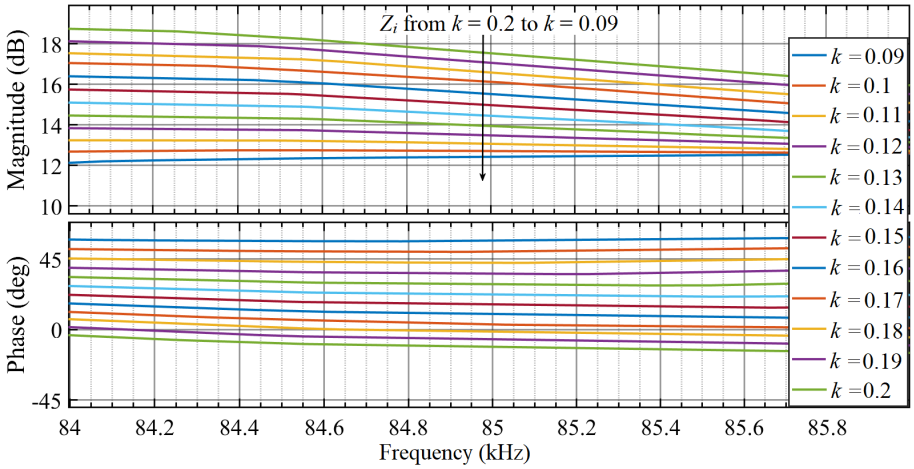


Fig. 6.8: Z_i vs frequency plots for PRSS tuning.

6.3.2 Simulation results and comparison of PRSS tuning with S-S and LCC-LCC tuning

The DWPT design for PRSS tuning, for which the analysis is shown in Section 6.3.1, is simulated in LTspice, for which the results are shown in Fig. 6.10, where output power is given as a function of coupling coefficient k. PRSS curve in Fig. 6.10 represents the Output Power (kW) for PRSS tuning. It can be observed from the PRSS curve that the Output Power remains close to 10 kW for the entire range of k from 0.09 to 0.2, where the maximum deviation in Output Power from 10 kW is seen at 12.5 kW.

Table 6.2 gives the RMS voltage (V), RMS current (I) and apparent power (S) for L_{pr},

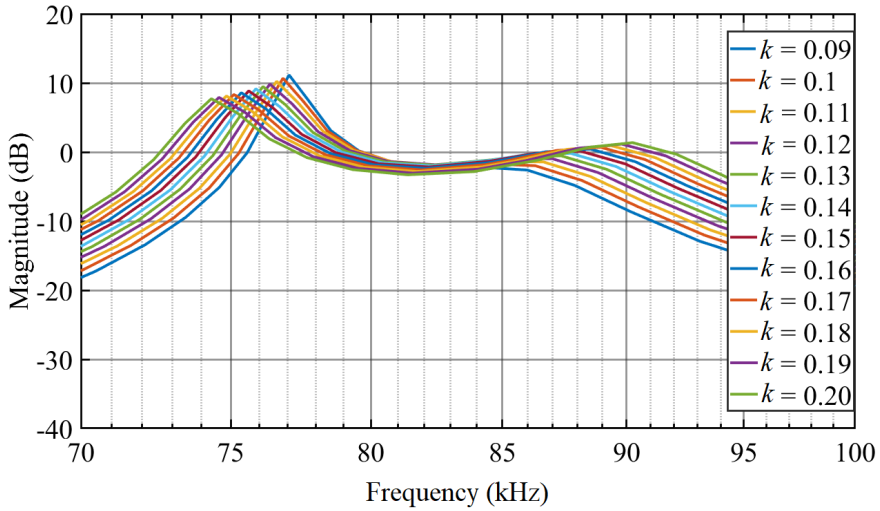


Fig. 6.9: $|H|$ vs frequency plots for PRSS tuning.

C_{pp}, C_{ps} and L_p shown in Fig. 6.3, which are obtained from the simulation results of 10 kW DWPT system for PRSS tuning. The quality factor (Q) for L_{pr} and L_p is taken to be 300, and for C_{pp} and C_{ps} is taken to be 1000, based on which the total loss in 4 components is calculated and given in Table 6.2. The values of V, I, S, and total loss for $k = 0.09$, 0.15, and 0.2 are within the bounds of any 10 kW IPT system.

This section also shows a comparison of output power vs coupling coefficient k curves for PRSS, series-series, and LCC-LCC tuning in Fig. 6.10. For comparison between different types of tuning, the output power at $k = 0.15$ is kept the same at 11 kW, and the power variation for the three types of tuning is analyzed. For series-series (S-S) tuning, the Output Power vs k curves are obtained for parameters of a 10 kW DWPT design in Section 6.3.1 before adding the parallel LC resonant tank and are represented by the S-S curve in Fig. 6.10. It can be observed from Fig. 6.10 that the output power increases as the value of k decreases from 0.2 to 0.09. The maximum output power deviation for S-S from 10 kW is seen at approximately 18 kW. Output power vs k curves are also obtained for a 10 kW double-sided LCC tuning (LCC-LCC) [89] and are represented by the LCC-LCC curve in Fig. 6.10. It can be observed from Fig. 6.10 that the output power for LCC-LCC tuning decreases as the value of k decreases from 0.2 to 0.09. The maximum output power deviation for

Table 6.2: V, I and S for components of PRSS tuning.

Parameter	$k = 0.09$	$k = 0.15$	$k = 0.2$
$V_{L_{pr}}$	334 V	274 V	254 V
$I_{L_{pr}}$	66 A	46 A	39 A
$S_{L_{pr}}$	22 kVA	12.6 kVA	9.9 kVA
$V_{C_{pp}}$	195 V	327 V	347 V
$I_{C_{pp}}$	19 A	25 A	25 A
$S_{C_{pp}}$	3.7 kVA	8.1 kVA	8.6 kVA
$V_{C_{ps}}$	1676 V	1011 V	751 V
$I_{C_{ps}}$	62 A	37 A	28 A
$S_{C_{ps}}$	103.9 kVA	37.4 kVA	21 kVA
V_{L_p}	1670 V	1032 V	801 V
I_{L_p}	62 A	37 A	28 A
S_{L_p}	103.5 kVA	38.1 kVA	22.4 kVA
Total Loss	526 W	214 W	137 W

LCC-LCC from 10 kW is seen at approximately 15 kW. From the PRSS curve in Fig. 6.10, the output power does not vary much as the value of k decreases from 0.2 to 0.09. Output power at $k = 0.2$ is 9 kW and at $k = 0.09$ is 10 kW. The maximum output power deviation for LCC-LCC from 10 kW is seen at 12.5 kW.

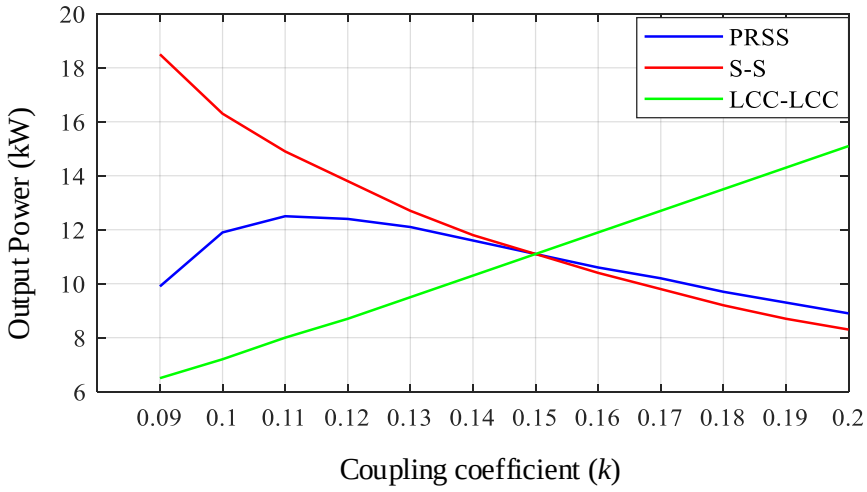


Fig. 6.10: Output Power (kW) vs k curves for PRSS, S-S and LCC-LCC tuning.

6.4 Conclusion

A parallel resonant series-series (PRSS) tuning method for IPT systems to maintain nearly constant power over a range of coupling coefficient k has been proposed in this chapter. A detailed design procedure for PRSS tuning has been presented in the paper for achieving a nearly constant power for the range of k selected according to the application of the IPT system. The ZVS analysis for the proposed tuning to achieve ZVS for the inverter transistors has also been presented in this chapter. A design example of the proposed tuning method for a DWPT system has been shown in this chapter. The DWPT design example has been verified with simulations showing a nearly constant power curve for the range of k selected. Finally, a brief comparison of the PRSS tuning with series-series and double-sided LCC tuning, showing the output power curves, has been done in this chapter. The PRSS tuning achieved a nearly constant power for the DWPT design example with minimum deviation of output power for k ranging from 0.09 to 0.2, compared to series-series tuning, where output power increased with decrease in value of k from 0.2 to 0.09, and double-sided LCC tuning, where Output Power decreased with decrease in value of k from 0.2 to 0.09.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

The increasing demand for electric vehicles in this decade and the need to reduce global CO2 emissions in the future have created a need to develop large-scale charging infrastructure. While there has been significant research on fast charging for electric vehicles, there are still limitations related to range anxiety, the large batteries used in EVs, and long wait times at charging stations. Dynamic wireless charging offers significant advantages over fast charging and stationary wireless charging to tackle these limitations. However, there is less research on large-scale high-power dynamic wireless charging systems. This dissertation focuses on loss analysis of large-scale distribution architectures, achieving highly efficient DC-DC converters for misalignment and power controls, designing system-level stability for wireless charging systems, designing more accurate and high-bandwidth controls for conventional tuning architectures, and also single-stage architectures to eliminate the need for additional DC-DC converters and complicated controls for designing misalignment-tolerant DWPT systems. The contributions of this dissertation and guidelines for future work are provided in this chapter.

The third chapter of the dissertation proposes loss models and a case study for power distribution architectures for large-scale dynamic wireless charging systems. The loss models include the resistances at different sections of the distribution architectures, which provide insights into how these losses could affect the distribution architectures used, depending on the traffic conditions on highways where multiple primaries are activated at a single time instant. A case study for a 1-mile, 1 MW wireless charging system is also provided, including a new DC current distribution architecture and a DC voltage distribution architecture. The efficiency and loss results are provided, which researchers can use to decide on the architecture to use for different scenarios.

The fourth chapter of the dissertation proposes techniques for designing highly efficient

high-power DC-DC converters for DWPT systems. This chapter examines how the turn-off losses of the power module become significant at high power levels. While there is enough literature on optimizing turn-on losses for high-power DC-DC converters, this work optimizes both the turn-on and turn-off losses for high-power DC-DC converters. The design procedure for ZVS-QSW DC-DC converters is developed for a double-sided LCC tuned WPT system. The proposed soft-switching with external capacitance is compared with conventional soft-switching with internal capacitance for ZVS-QSW DC-DC converters and hard switching at 50 kW. The approach has been verified with actual module models in LTspice simulations. The results have been verified with experiments at 50 kW, 40 kW, 30 kW, and 20 kW across different coupling factors. The EMI comparisons at 50 kW have also been provided for all three cases. With the proposed soft-switching optimization, peak efficiencies of 99% can be achieved in a DC-DC converter at 50 kW.

The fifth chapter of the dissertation provides a detailed analysis of the design of control systems for a double-sided LCC tuned system with a ZVS-QSW DC-DC converter. The stability analysis of the full system is provided using Middlebrook's criteria. The WPT system is modeled using a phasor modeling approach. The ZVS-QSW is modeled using state-space averaging and discrete-time modeling techniques, and both are compared. The discrete-time modeling approach yields more accurate models at high frequencies and when battery resistance is included. This technique is then used to design higher-bandwidth, stable digital controls using higher-order z-domain compensators. Two types of compensator realizations, the cascade and parallel, are compared for the implementation of higher-order compensators. The control scheme is then tested at 8 kW and 50kW to test the performance of the compensators. The fast response of the controls at startup and during misalignment verifies that the controls can be implemented at a highway speed of 60 miles/hr. The dynamic experiments for the full WPT system are conducted at 8 kW and 1 mph, with constant power maintained over a coupling coefficient range of 0.12-0.2.

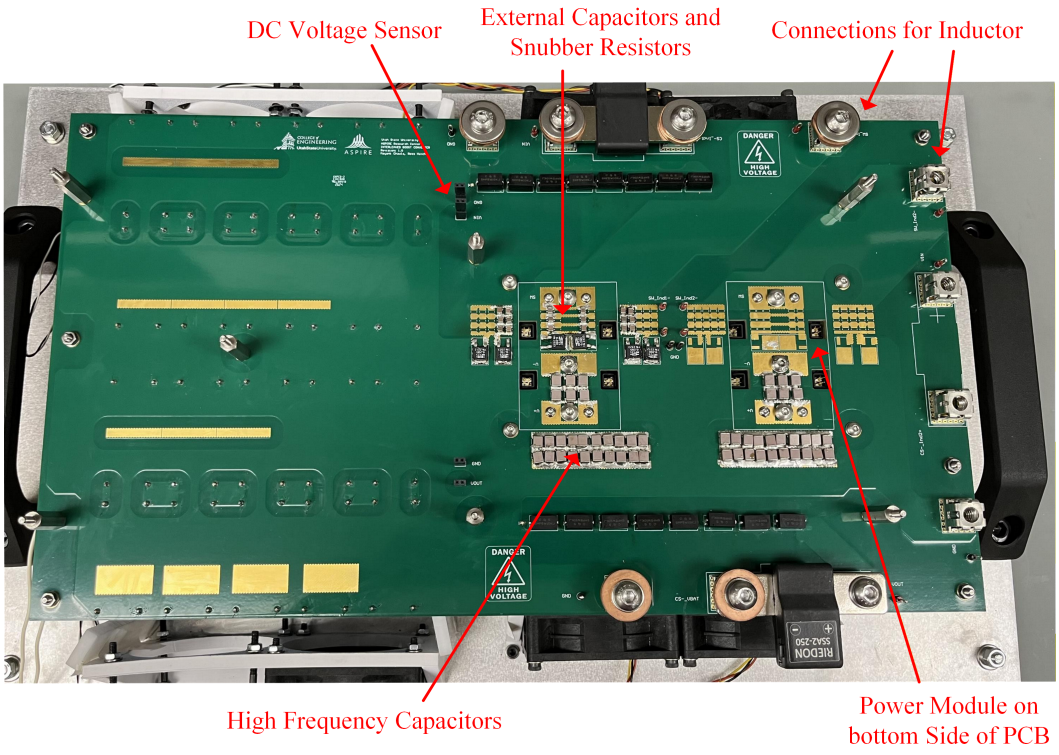
The sixth chapter of the dissertation proposes a novel tuning method, Parallel Resonant Series-Series tuning for designing IPT systems. With this proposed tuning, a nearly constant

power can be achieved across a range of coupling coefficients without any external controls or a DC-DC converter. The system can maintain high efficiency by achieving ZVS in the primary switches, and a ZVS analysis is provided in the chapter. The proposed tuning is compared with conventional series-series and double-sided LCC tuning, and simulation results for a 10 kW system are provided for all three methods.

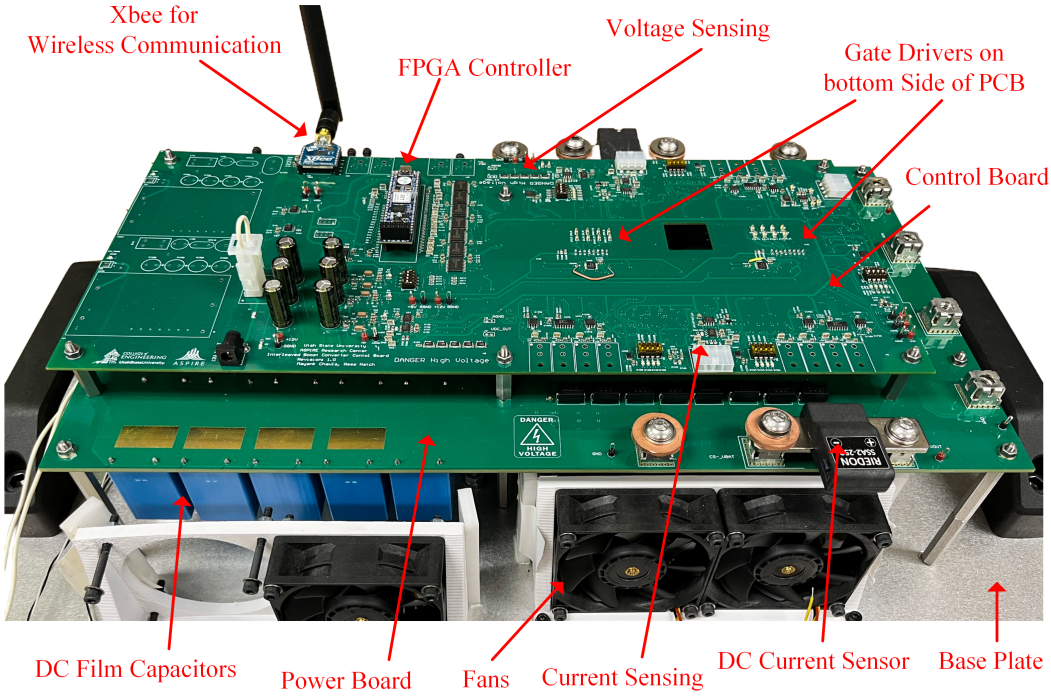
For future work in Chapter 3, the hardware for DC current distribution and the topology of the grid-tied converter could be analyzed for the case study developed in this dissertation, since DC current distribution offers higher efficiency under heavy traffic.

For future work on DC-DC converters and controls, a two-phase ZVS-QSW converter could be tested for higher powers to increase the power levels up to 100 kW as shown in Fig. 7.1 and Fig. 7.2. Two DC-DC converters could then be connected in parallel to increase power to 200 kW and be synchronized using the fiber connectors on the DC-DC control board PCB. This could be tested for dynamic wireless charging of electric trucks. The design of ZVS-QSW could also be extended to high-power non-inverting buck-boost converters to increase the range of voltage levels on the rectifier circuit. The control technique could be tested with multiple primaries on the indoor rail setup at EVR at low speeds, as shown in Fig. 7.3, and then finally on the test track at EVR at high speeds.

For future testing on PRSS tuning, the same primary and secondary pad of Fig. 7.3, including the inverter and rectifier, could be used, and the capacitor combinations for tuning have been developed in Fig. 7.4 and Fig. 7.5.



(a)



(b)

Fig. 7.1: PCB for two-phase DC-DC Converter: (a) Power board, (b) Control board, stacked with power board.

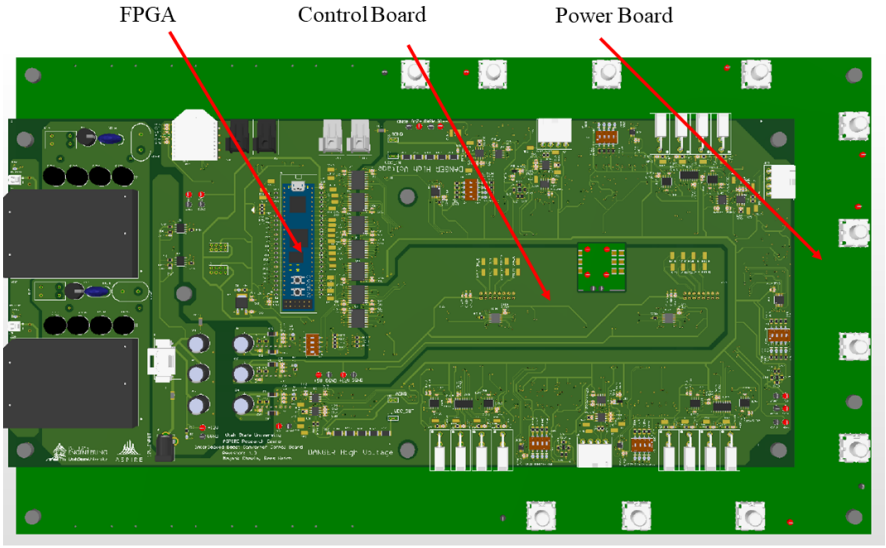


Fig. 7.2: Control board PCB design stacked with power board for multiphase boost converter showing fiber connectors on PCB.

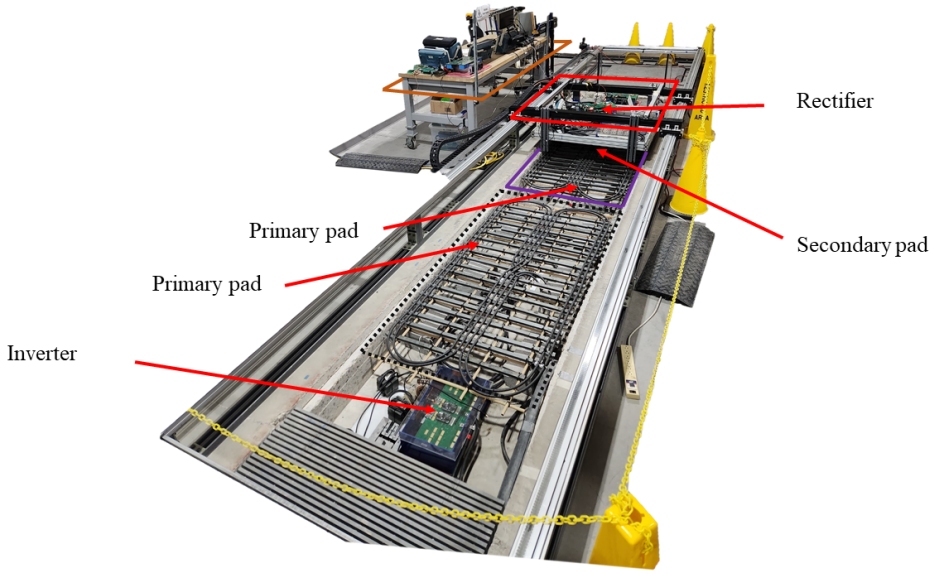


Fig. 7.3: Test setup for future testing with multiple primaries.

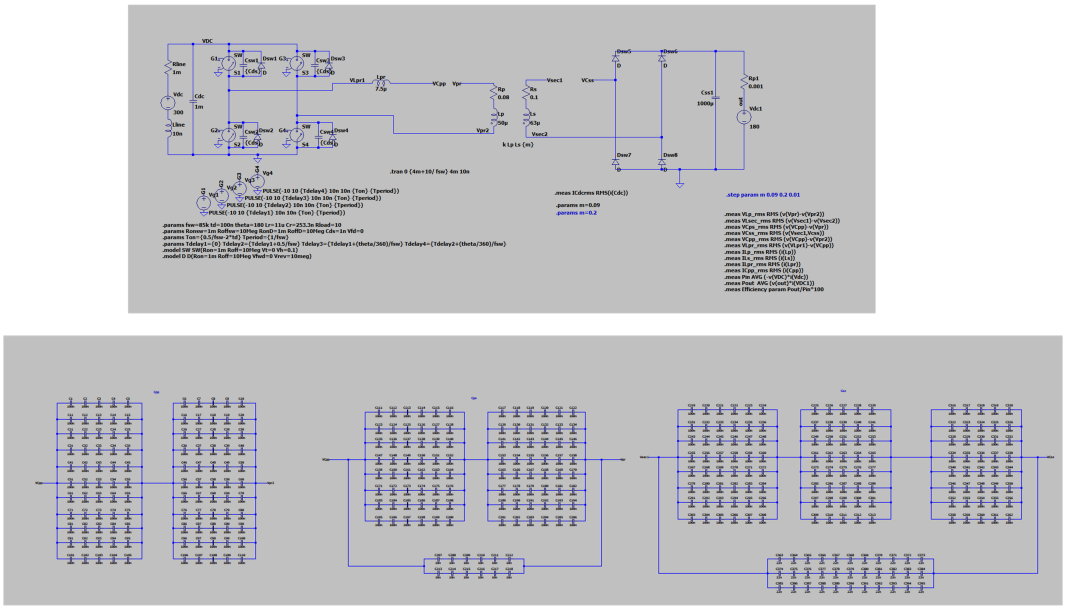


Fig. 7.4: LTspice Simulation including capacitor combinations for future testing

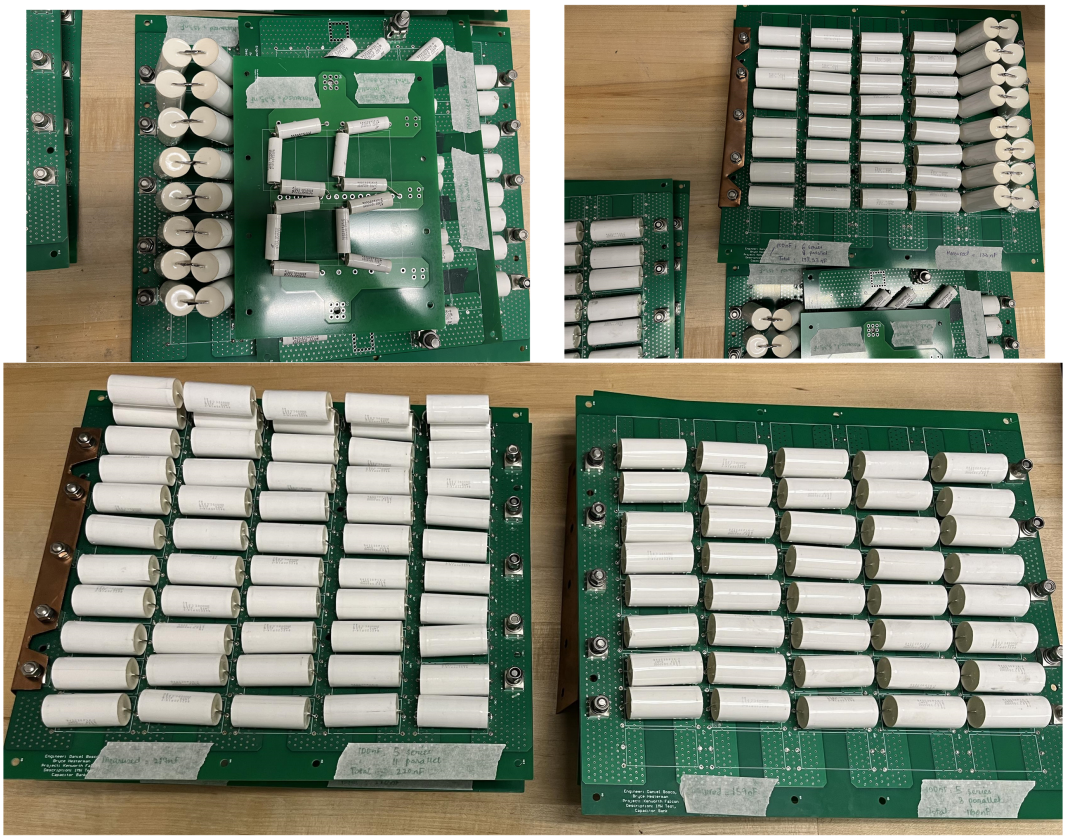


Fig. 7.5: Capacitor combinations for future testing

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APPENDICES

APPENDIX A

Simulations for DC-DC Converter

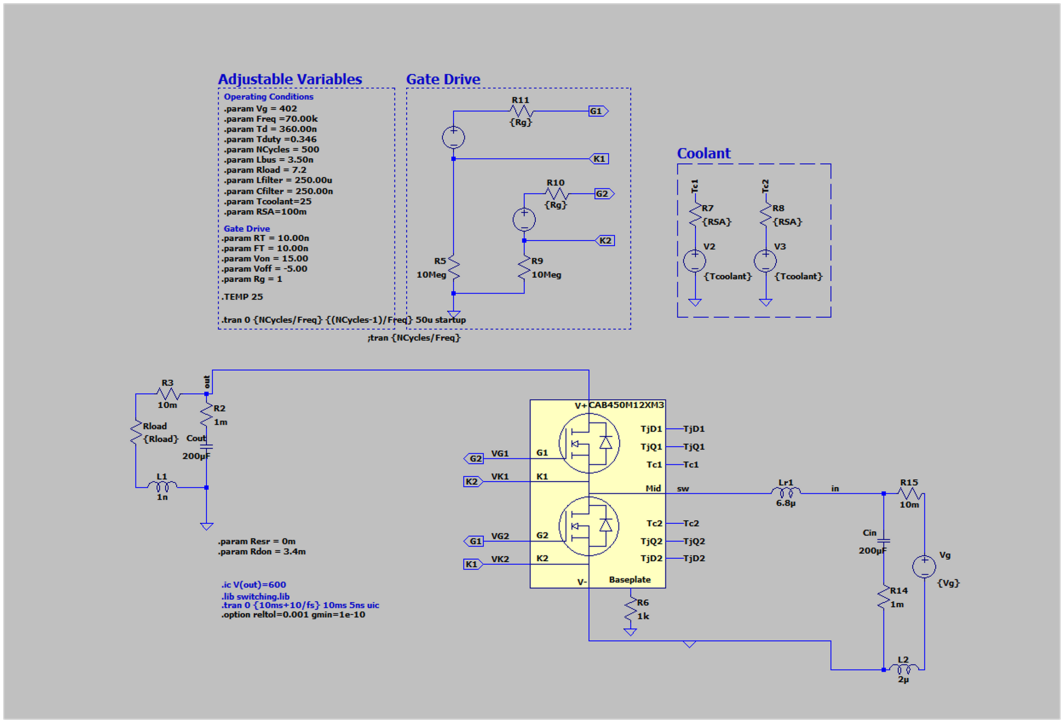


Fig. A.1: LTspice Simulation for DC-DC converter with actual model of module from Wolfspeed [2]

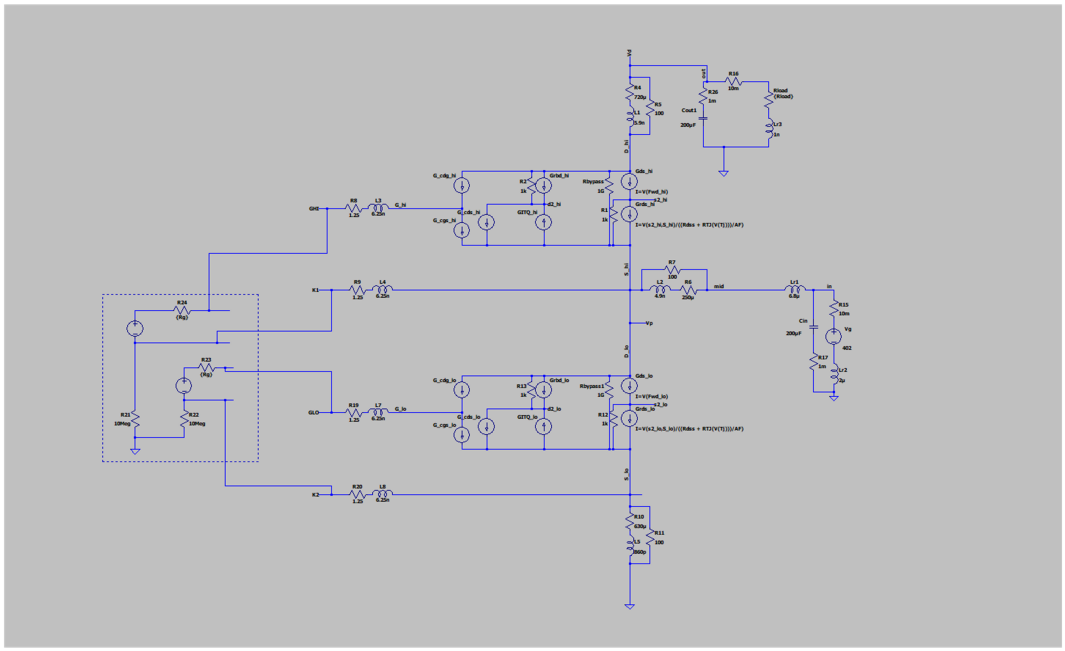


Fig. A.2: LTspice Simulation for DC-DC converter with model created from actual model of module from Wolfspeed

CURRICULUM VITAE

Mayank Chawla

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