DESIGN, CONTROL, AND OPTIMIZATION OF UNFOLDING-BASED AC-DC TOPOLOGIES WITH THREE-PORT RESONANT CONVERTERS FOR ELECTRIC VEHICLE BATTERY CHARGING APPLICATIONS

by

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ABSTRACT

Design, Control, and Optimization of Unfolding-Based AC-DC Topologies with Three-Port Resonant Converters for Electric Vehicle Battery Charging Applications

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The global push to reduce greenhouse gas emissions and dependence on fossil fuels has made electric mobility a key strategy for a sustainable future. This transition drives demand for efficient grid-tied ac-dc converters, which are essential for EV charging as well as for integrating renewable sources such as solar, fuel cells, and battery storage into the grid. Given the high power demands, converters must operate efficiently, reliably, and cost-effectively. Conventional high-power chargers typically use a two-stage architecture with an AFE PFC stage followed by a dc-dc stage. While effective, this approach reduces power density and increases switching losses. To address these challenges, single-stage converters are being explored for both conductive charging and WPT applications.

The first part of this thesis examines a single-stage topology employing a 3-ϕ 480 V Unfolder with a T-type bridge-based three-port dc-dc converter to achieve efficient EV battery charging over the 649–755 V range. This configuration enables simultaneous PFC and output power regulation, allowing efficient ac-dc conversion within a single stage. The topology is proposed for WPT charging infrastructure for heavy-duty EVs and is realized using a modular 21 kW building block. The performance of the charger is further optimized

by: (i) introducing a PWM technique that enhances ZVS of the T-type bridge to minimize switching losses, resulting in 96.51% ac-dc efficiency and reducing radiated EMI by 6 dB; (ii) improving grid current quality and reducing THD; and (iii) increasing control bandwidth without passive damping to improve system performance. Furthermore, accurate small-signal modeling of the 85 kHz HF T-type bridge-based dc-dc converter is carried out to enhance controllability.

Secondly, this research addresses the limited energy generation capacity amid the rapid expansion of EV charging. A multiport unfolding-based system is proposed to integrate battery storage and renewable energy with the grid for EV charging over the 200–800 V range. A 5 kW prototype with a multi-winding transformer and a 100 kHz HF TAB-based converter achieves 98.3% peak efficiency. A paralleling approach is proposed to scale the system to 10 kW, demonstrating its practicality for high-power EV charging.

(316 pages)

PUBLIC ABSTRACT

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Aditya Zade

The global effort to reduce greenhouse gas emissions and reliance on fossil fuels has made electric mobility a cornerstone of sustainable transportation. This transition is driving demand for advanced charging infrastructure and more efficient power conversion systems. Power converters play a central role, not only in enabling reliable EV charging but also in integrating renewable energy sources with the grid. Because of the large amount of power involved, these converters must operate efficiently, reliably, and at low cost. Conventional high-power chargers often use two stages of conversion, which are effective but limited by size and energy losses. To overcome these challenges, there is growing interest in single-stage converters that can handle EV charging and grid integration in a more compact and efficient way.

The first part of this research develops an efficient converter designed for wireless EV charging that performs grid interfacing and battery charging in a single stage. The system improves efficiency, enhances grid power quality, enables stable operation, and does not require large passive components. Advanced control and modulation methods are introduced to strengthen the soft-switching performance of the converter, while modeling approaches are developed to support accurate control and reliable operation.

The second part of this work addresses the challenge of limited energy generation capacity as EV adoption grows. A multiport converter system is proposed that allows renewable energy and battery storage to be integrated directly with the grid and charging infrastructure. This system improves energy management, supports grid stability, and

demonstrates scalability for higher-power charging. Together, these innovations support the development of faster, more compact, efficient, and reliable EV charging solutions.

To my family...

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ACRONYMS

ADC	Analog-to-Digital Converter
AFE	Active Front-End
DAB	Dual Active Bridge
EET	Extra Element Theorem
EMI	Electromagnetic Interference
EV	Electric Vehicle
FEA	Finite Element Analysis
FHA	Fundamental Harmonic Approximation
GSSA	Generalized State-Space Averaging
HF	High Frequency
IGBT	Insulated Gate Bipolar Transistor
iGSE	Improved Generalized Steinmetz Equation
IPOP	Input-Parallel and Output-Parallel
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LPF	Low-Pass Filter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
PCB	Printed Circuit Board
PFC	Power Factor Correction
PI	Proportional-Integral
PLL	Phase-Locked Loop
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SAE	Society of Automotive Engineers
SAR	Successive Approximation Register
SPI	Serial Peripheral Interface
TAB	Triple Active Bridge
THD	Total Harmonic Distortion
WPT	Wireless Power Transfer
ZVS	Zero-Voltage Switching

CHAPTER 1

INTRODUCTION

The global drive to reduce greenhouse gas emissions and decrease dependence on fossil fuels has positioned electric mobility as a key strategy for achieving a sustainable future [1,2]. This transition has intensified the demand for advanced grid-connected charging infrastructure and high-efficiency grid-tied ac-dc power converters. Such converters are essential not only for enabling reliable EV charging but also for the seamless integration of renewable energy sources such as photovoltaic modules, fuel cells, and battery storage systems into the grid [3]. Given the substantial power demands from the grid, grid-tied converters must process power efficiently, reliably, and cost-effectively [4].

Conventionally, a two-stage architecture is employed [5–7], involving an AFE PFC converter [8, 9] and a dc-dc converter with an HF isolation transformer [10, 11]. The intermediate stiff dc link in this architecture facilitates simplified system design and enables excellent dynamic control. However, the AFE in this setup often suffers from relatively high switching and reverse recovery losses, constraining its maximum operating switching frequency. This limitation necessitates a larger filter size, contributing to elevated system costs. Furthermore, employing two successive full-power processing stages leads to a decrease in the overall efficiency of the system [12]. To overcome these challenges, there is increasing interest in single-stage ac-dc converters for both conductive charging and WPT applications [12–22]. The architectures of the two-stage and single-stage topologies are depicted in Fig. 1.1.

Among these, unfolding-based topologies have emerged as promising candidates, as they allow the concurrent execution of PFC and regulated dc output with efficient ac-dc power delivery within a single conversion stage [12, 18–30]. These architectures employ a 3-ϕ Unfolder operating in open loop at a maximum of twice the grid frequency to invert the negative half-cycles of the ac input, producing two unipolar pulsating dc-link voltages.

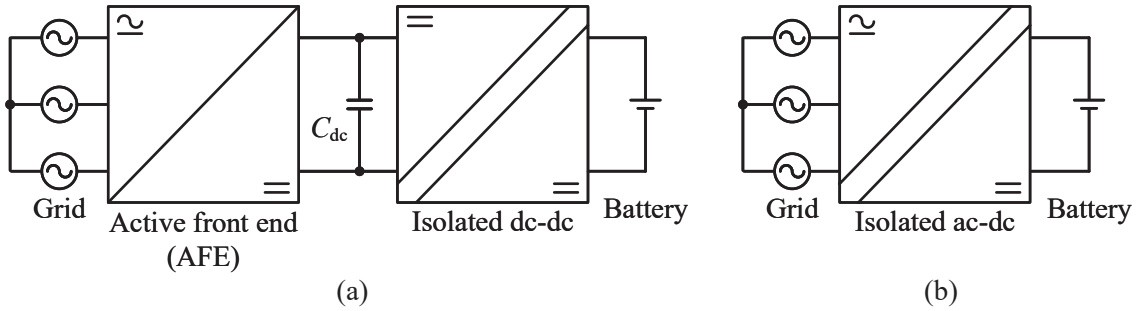


Fig. 1.1: Architecture of (a) a two-stage topology; and (b) a single-stage topology.

The dc-dc converter in this unfolding-based topology is precisely controlled to maintain balanced loading across these pulsating dc-link voltages, resulting in sinusoidal grid currents and a regulated net power output to the load. Operating the Unfolder at a maximum of twice the grid frequency with negligible switching losses, while performing all the control-related tasks using the dc-dc converter, results in improved power density, efficiency, and design simplicity. Moreover, by eliminating the intermediate stiff dc link with its large capacitors, and by reducing the requirement for external grid-side inductive filters since the grid inductance is sufficient for PFC, unfolding-based converters provide a more compact and efficient solution for high-power applications compared with conventional two-stage topologies. In this unfolding-based topology, the power from the two pulsating dc-link voltages can be processed using a dual-input converter, such as a 3-level buck/boost [18–20], a pair of H-bridges [21,22], or a T-type bridge [12,23–31], thereby establishing the foundation for a wide range of single-stage unfolding-based ac-dc architectures.

Chapters 2–5 of this thesis employ an unfolding-based single-stage ac-dc topology with a T-type bridge-based dc-dc converter. The T-type bridge integrates two H-bridges into a single three-port converter that connects to the pulsating dc-link voltages at the output of the Unfolder, enabling efficient utilization of semiconductor devices. Additionally, the T-type bridge allows the use of a single galvanic isolation for dc-dc conversion. As a result, it offers a power-dense solution well-suited for unfolding-based ac-dc architectures. The design and operation of the unfolding-based ac-dc converter rated at 21 kW output power are presented in Chapter 2. To demonstrate the advantages of the proposed unfolding-

Table 1.1: Comparison between the proposed unfolding-based single-stage and conventional two-stage topologies (V_{gm} - peak line-line grid voltage, P_{out} - output power, and ω_g - angular grid frequency).

Component	**Parameter**	**Scaling factor**	**Conventional two-stage (AFE+H-bridge)**	**Proposed single-stage (Unfolder+T-type)**
AFE/Unfolder	Semiconductor device count	-	6	12
	Voltage stress	V_{gm}	1.18	1, 0.433
	Current stress (rms)	P_{out}/V_{gm}	0.216, 0.535	0.56, 0.139
H-bridge/T-type	Semiconductor device count	-	4	8
	Voltage stress	V_{gm}	1.18	1, 0.866
	Current stress (average rms)	P_{out}/V_{gm}	0.693	0.89, 0.4
Grid-side inductive filter	Value (mH)	$V_{gm}^2/(\omega_g P_{\text{out}})$	10.31	0
Dc/soft-dc link capacitor	Value (mF)	$P_{\text{out}}/(\omega_g V_{gm}^2)$	827.23	3×20.68

based single-stage topology over the conventional two-stage architecture, a quantitative performance comparison has been done. As discussed above, the unfolding-based topology utilizes a T-type bridge-based dc-dc converter. On the other hand, the two-stage topology is typically designed with a grid-tied HF AFE followed by an H-bridge-based dc-dc converter. Both topologies use a diode-bridge rectifier on the secondary side connected to a battery load. To perform the comparison, a case study is carried out at the output power level of $P_{\text{out}} = 21$ kW, with input and output voltages of $V_{gm} = 480\sqrt{2}$ V and $V_{\text{batt}} = 730$ V, respectively. The AFE converter is switched at 100 kHz with an appropriate inductive filter to match the grid current THD with the unfolding-based topology. An HF grid-tied

Table 1.2: Loss comparison between the proposed single-stage and conventional two-stage topologies (P_{out} - output power).

Component	**Parameter**	**Scaling factor**	**Conventional two-stage (AFE+H-bridge)**	**Proposed single-stage (Unfolder+T-type)**
AFE/Unfolder	Conduction losses	$P_{\text{out}}/100$	0.95	0.62
	Switching losses	$P_{\text{out}}/100$	0.97	0
H-bridge/T-type	Conduction losses	$P_{\text{out}}/100$	0.47	0.61
	Switching losses	$P_{\text{out}}/100$	0	0.14
-	Total power losses	$P_{\text{out}}/100$	2.39	1.37

converter designed in [32] is considered for reference. The AFE is controlled using space vector PWM, while the H-bridge operates at a maximum modulation index with square wave pulses to achieve complete soft-switched transitions. The control strategy for the T-type bridge used in the unfolding-based topology is detailed in Chapter 2. Table 1.1 provides the comparison between the two topologies in terms of the device count, voltage and current stresses, and filter requirements. It can be observed that the proposed topology provides a significant reduction in the demand for inductive and capacitive filtering in the conversion process at the cost of more semiconductor devices. Table 1.2 presents a comparison of analytical power losses between the two topologies calculated using the analysis presented in Chapter 2 and [33]. The conventional H-bridge demonstrates higher efficiency compared to the T-type bridge due to its lower switch count, resulting in reduced conduction losses. It also benefits from complete soft-switching capability. However, the Unfolder in the proposed topology exhibits significant power loss reduction when compared to the AFE converter, mainly due to its negligible switching losses. Consequently, the proposed topology delivers superior overall efficiency in the conversion process. Moreover, the efficiency of the proposed unfolding-based topology can be improved further by minimizing the switching losses of the T-type bridge, as discussed in Chapter 3.

While the unfolding-based ac-dc topology presented in Chapter 2 demonstrates significant advantages, further refinement and optimization are required to enhance its performance. The next two chapters of this thesis address these refinements. Chapter 3 proposes a robust closed-loop control architecture, an appropriate modulation strategy, and an accurate tank design that together ensure soft-switching operation of the T-type bridge in the unfolding-based ac-dc topology across the entire grid cycle, thereby reducing switching losses, improving efficiency, and reducing EMI. Chapter 4 proposes a current emulation-based active damping technique that improves the quality of the grid currents by reducing their THD, enhances system stability, and enables high-bandwidth closed-loop control, thereby improving the overall operation of the unfolding-based ac-dc topology. To ensure the stability and robustness of closed-loop control in the proposed unfolding-based ac-dc topology, accurate small-signal modeling is required to derive the plant transfer functions and calculate the controller parameters. A detailed small-signal model of the T-type bridge-based dc-dc converter, developed using the phasor transformation technique, is presented in Chapter 5.

Finally, attention is directed toward the constraint of limited electricity generation capacity amidst the rapidly expanding EV charging infrastructure. In 2023, the United States consumed approximately 137 billion gallons of gasoline and 46 billion gallons of diesel, corresponding to an energy demand of about 6.36 trillion kWh for transportation [34]. In contrast, the nation's total electricity generation during the same year was approximately 4.25 trillion kWh [35], underscoring the immense gap between transportation energy consumption and available electricity supply. The distribution of energy sources is illustrated in Fig. 1.2. This disparity highlights the challenge of transitioning to fully electric mobility systems, as electrifying the entire vehicle fleet would far exceed current generation capacity. Therefore, alongside the development of EV charging infrastructure, it is imperative to concurrently enhance electricity generation and grid support. A promising approach that has gained significant attention involves integrating renewable generation and battery energy storage with the grid to support large-scale EV charging [36]. A conceptual representation

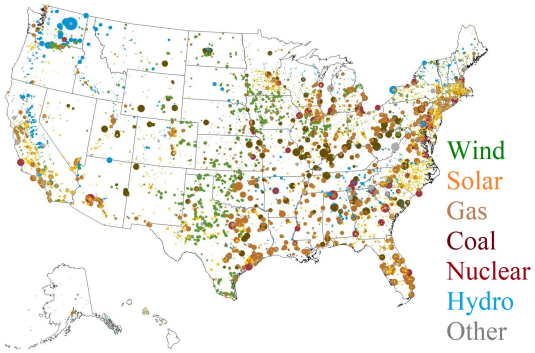


Fig. 1.2: Energy generation sources in the USA in 2023 (source: EIA).

Fig. 1.3: Conceptual image of the integration of battery storage/renewable energy generation with the grid for EV charging infrastructure (source: Mobility Outlook).

of this integration is depicted in Fig. 1.3.

Chapter 6 focuses on the design, control, and optimization of a multiport system that leverages the unfolding-based grid connection to integrate battery storage and renewable energy sources with the grid for EV battery charging. While Chapters 2–5 concentrate on single-stage unfolding-based topologies for direct and efficient grid-to-EV power transfer, the final objective of this thesis broadens the scope to system-level integration challenges. In particular, large-scale EV adoption requires not only efficient converters but also architectures capable of coordinating with renewables and battery storage. To address this, Chapter 6 introduces a multiport architecture that employs the Unfolder for grid interfacing together with a current injection circuit [44, 45] and a TAB-based dc-dc converter [46, 47].

Table 1.3: Performance comparison of the proposed 3-ϕ grid-tied multiport converter with prior 3-ϕ grid-tied multiport converters.

Work	**Ports**	**Grid-side converter**	**No. of devices**	**No. of passives**	**Control complexity**	**Power**	**Efficiency (maximum)**	**Grid current THD**	**Battery voltage**
[37]	5 (1 ac and 4 dc, non isolated)	AFE (HF, hard-switched)	13	19	High	0.1 kW	96.83%	–	12 V
[38]	3 (1 ac and 2 dc, isolated)	Matrix (HF)	20	19	High	2 kW	93.5%	2.65%	200 V
[39]	3 (1 ac and 2 dc, non isolated)	AFE (HF, hard-switched)	16	22	High	3.7 kW	–	2.5%	240 V
[40]	3 (1 ac and 2 dc, isolated)	AFE (HF, hard-switched)	24	21	Moderate	10 kW	96.4%	2.95%	50–500 V
[41]	3 (1 ac and 2 dc, isolated)	Matrix (HF)	42	13	High	40 kW	92%	–	400 V
[42]	3 (1 ac and 2 dc, isolated)	Current source inverter (HF)	14	15	Moderate	3 kW	97% (theoretical)	–	125 V
[43]	4 (1 ac and 3 dc, partially isolated)	AFE (HF, hard-switched)	16	17	Moderate	2 kW	–	–	48 V
This work	**3 (1 ac and 2 dc, isolated)**	**Unfolder (low frequency, negligible switching losses)**	**26**	**13***	**Moderate**	**5 kW (scalability shown at 10 kW)**	**98.3%**	**2%**	**200–800 V**

– Data not reported in the respective work.

* Because of the low-frequency operation of the Unfolder, external grid-side inductors are not required, and the inherent grid inductance is sufficient to achieve PFC. The dc blocking capacitors used in the TAB-based dc-dc converter are included in the component count.

Through this combination, the system effectively integrates the battery storage/renewables with the grid for EV battery charging. This architecture is distinct from the single-stage approaches of earlier chapters, yet it still retains the advantages of the unfolding-based grid connection, such as negligible switching losses, simplified grid interfacing, and compact filtering requirements. The proposed multiport system demonstrates how unfolding-based principles can be scaled to more complex system-level architectures essential for future EV charging infrastructure.

Moreover, the performance of the proposed 3-ϕ unfolding-based grid-tied multiport converter is compared with prior 3-ϕ grid-tied multiport converters in Table 1.3. It can be observed that the proposed system surpasses prior work in key parameters, achieving higher efficiency through a low-frequency-switched Unfolder and an optimized TAB tank, lower THD, and reliable operation over a wide EV battery voltage range of 200–800 V. In addition, the use of an Unfolder, which minimizes grid-side filtering requirements with grid inductance sufficient for PFC, together with the integrated three-winding transformer design, reduces the overall count of passive components in the system. The scalability of the proposed converter is also demonstrated in Chapter 6 through 50 kW simulation results and 10 kW hardware tests, supporting its potential for practical high-power EV charging infrastructure.

The remainder of this thesis is organized as follows:

- Chapter 2 presents the design and operation of the proposed unfolding-based grid-tied ac-dc topology for WPT applications, rated at 21 kW output power.
- Chapter 3 develops a robust closed-loop control architecture, an appropriate modulation strategy, and a precise tank design that together ensure soft-switching operation of the T-type bridge in the unfolding-based topology across the entire grid cycle, thereby reducing switching losses, improving efficiency, and reducing EMI.
- Chapter 4 introduces a current emulation-based active damping technique that reduces grid-current THD, enhances system stability, and enables high-bandwidth closed-loop control for improved overall performance of the unfolding-based ac-dc topology.

- Chapter 5 presents a detailed small-signal model of the T-type bridge-based dc-dc converter in the unfolding-based ac-dc topology, which serves as the foundation for accurate control design and stability analysis.

- Chapter 6 proposes the design and operation of an unfolding-based grid-tied multiport system that integrates battery storage and renewable energy sources with the grid for EV battery charging. A modular approach is adopted, with a single module designed for a 5 kW power level and scalability demonstrated in hardware at a 10 kW power level.

- Chapter 7 presents the conclusions.

CHAPTER 2

DESIGN AND OPERATION OF AN UNFOLDING-BASED AC-DC TOPOLOGY

2.1 Introduction

This chapter presents a single-stage topology for a WPT system [48–51] that consists of a 3-ϕ Unfolder followed by a T-type converter-based soft-dc to dc system. The Unfolder operates close to the grid frequency in order to invert the negative segment of the input ac voltages to the positive polarity. These positive pulsating voltages are referred to as soft dc-link voltages in this chapter. The T-type converter is chosen to connect to the Unfolder due to its dual-input voltage processing capability, which enables efficient utilization of semiconductor devices and improves system efficiency and power density. The T-type converter is switched at a frequency of 85 kHz to ensure interoperability with charging equipment from various manufacturers, as suggested by the WPT standard J2954 established by the SAE [52]. To mitigate the control-related complications, this chapter presents a decoupled control strategy aimed at overcoming the constraints associated with high bandwidth control and minimizing grid current THD. The proposed control approach enables the management of input PFC without the need for grid-side current sensors, while simultaneously providing output power regulation. To ensure proper control of the battery current, a phasor transformation technique is used to model the T-type converter-based soft-dc to dc system. In addition, a modular structure of the T-type converter is proposed for efficient power scalability to develop a WPT infrastructure capable of charging heavy-duty EV batteries in under an hour with a power rating of 1 MW. A board measuring 26.2 in (L) $\times$ 13.2 in (W) $\times$ 4.5 in (H), including the cold plate, is designed to accommodate three T-type converters, each capable of producing 21 kW of output power. A single Unfolder rated for 1 MW is developed to interface with multiple parallel-connected T-type converter modules.

The chapter provides comprehensive design guidelines and presents hardware results

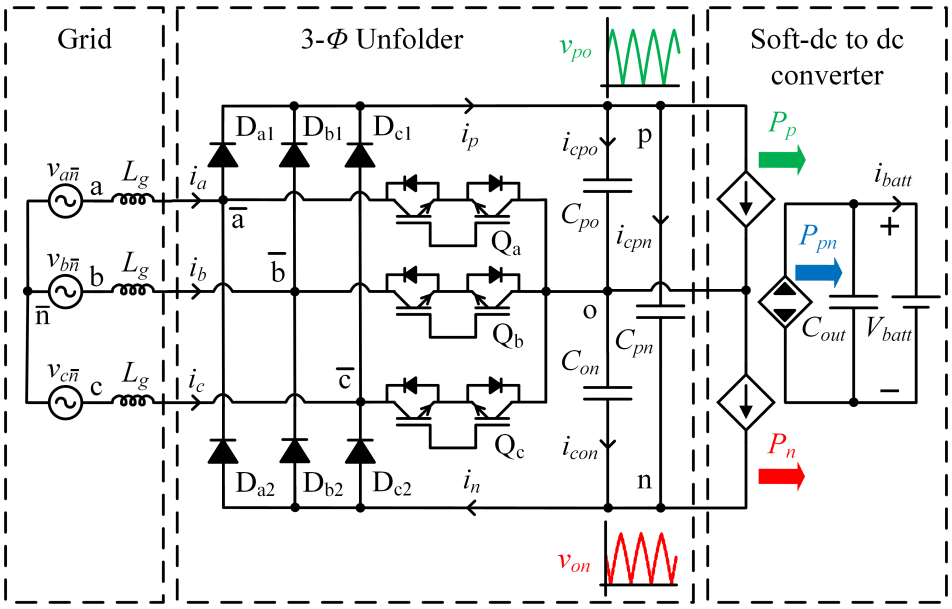


Fig. 2.1: The circuit configuration of a buck-type PFC 3-ϕ Unfolder followed by a generalized soft-dc to dc converter.

for a 21 kW prototype based on a single T-type module. The prototype achieves an ac-dc efficiency of ∼96% in the conversion process from the grid to the battery and a grid current THD of 1.27%. The modular structure for multiple T-type converters operated in tandem is demonstrated by testing six T-type converter modules in parallel, and corresponding hardware results are also presented.

2.2 Circuit Configuration and Operation of the Proposed AC-DC Converter

The unfolding-based ac-dc conversion system, as illustrated in Fig. 2.1, is composed of ac-side grid inductances, a conventional 3-ϕ diode bridge rectifier along with a third-harmonic injection network (Q_x, $x \in \{a, b, c\}$), soft dc-link capacitors, and a soft-dc to dc conversion system. In an Unfolder, the input ac phases are connected to the positive, negative, or midpoint of the soft dc-link based on the specific switching sequence outlined in Fig. 2.2(d). The phases with the maximum and minimum instantaneous voltages are linked to the positive (p) and negative (n) nodes of the soft dc-link, respectively, while the remaining phase is linked to the midpoint (o). As a result, the injection network's switches Q_a, Q_b, and Q_c operate with twice the grid frequency, while the rectifier switches D_{a1}, D_{a2},

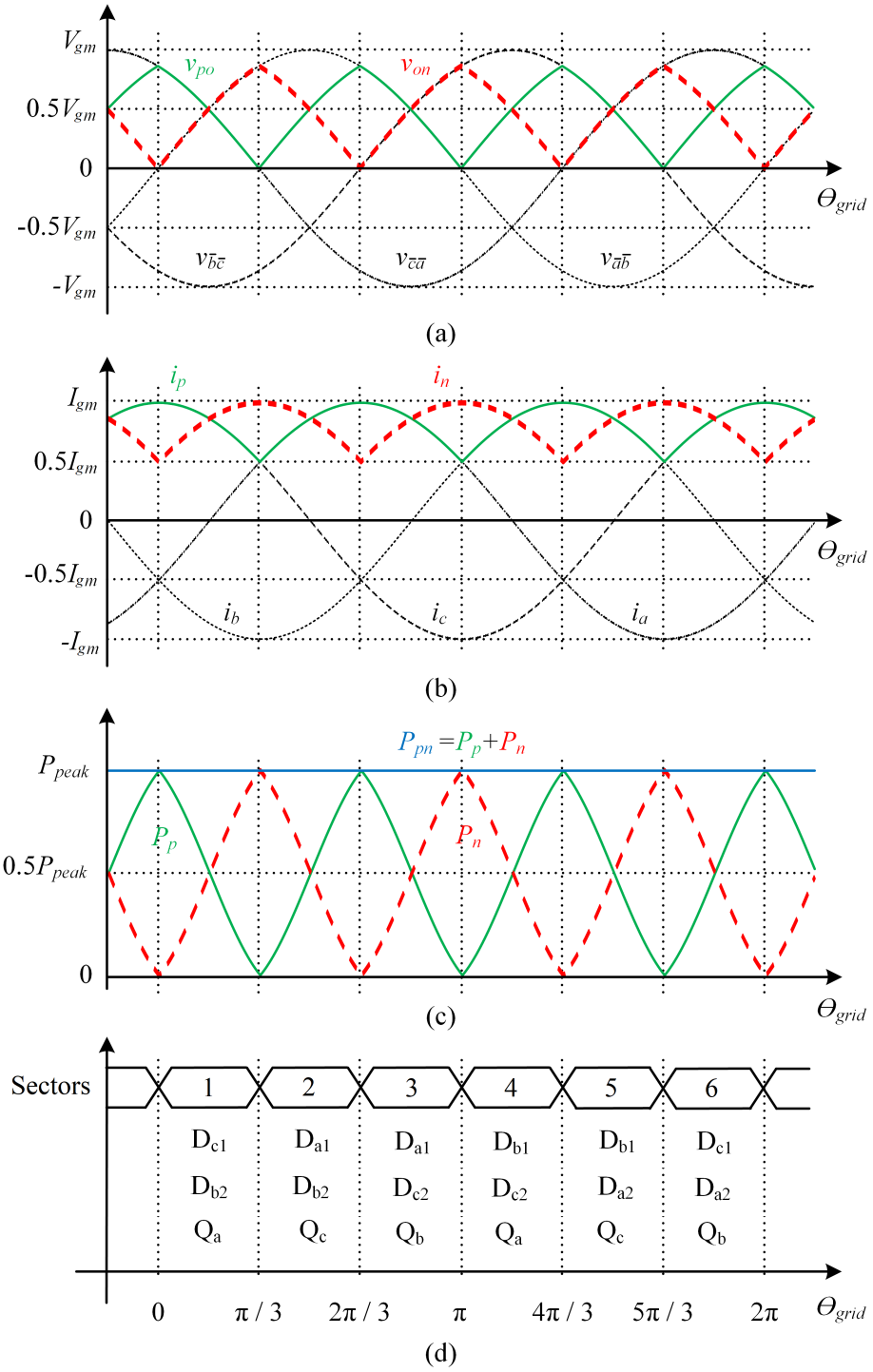


Fig. 2.2: (a) Unfolder input ac voltages are converted to pulsating soft dc-link voltages, v_{po} and v_{on}, (b) sinusoidal grid currents are shaped piece-wise by i_p and i_n, (c) pulsating two ports powers P_p and P_n combined to give a constant overall output power P_{pn}, and (d) switching sequence of the Unfolder devices in accordance with ac voltage sectors.

D_{b1}, D_{b2}, D_{c1}, and D_{c2} operate with the grid frequency. This switching scheme results in the soft dc-link voltages, v_{po} and v_{on}, depicted in Fig. 2.2(a), time-varying from 0 to $(\sqrt{3}/2)V_{gm}$, where V_{gm} is the peak of the line-to-line ac input voltages of the Unfolder. Because of the pulsating soft dc-link voltages, the two output ports of the Unfolder carry pulsating powers, P_p and P_n, as shown in Fig. 2.2(c). It should be noted that although the powers of individual ports are pulsating, the overall power, P_{pn}, is constant as can be seen in Fig. 2.2(c). Additionally, the soft dc-link does not require large capacitance because the voltages are not held constant. Two capacitors, C_{po} and C_{on}, are exclusively necessary and specifically designed to filter out the HF switching ripple produced by the soft-dc to dc converter. However, having only these two capacitors can result in unbalanced capacitive loading on the grid side, leading to imbalanced grid currents. To address this issue, a third capacitor, C_{pn}, is added which creates a balanced Δ-connected capacitor configuration.

The soft-dc to dc system must possess dual-input voltage processing capability to manage the two soft dc-link voltages and handle two pulsating powers, P_p and P_n. One approach utilized in converter topologies, such as dual active bridge [21], phase-shifted full bridge [22], and triple active bridge [53,54], involves using two H-bridges to connect to the two soft dc-link voltages. However, both of these H-bridges need to have a peak power rating of P_{peak}, which is twice the average power processed by each H-bridge converter. Additionally, employing two H-bridges necessitates the use of two wireless coils. These factors contribute to a decrease in the efficiency and power density of the soft-dc to dc system. Another solution is the 3-level buck/boost converter [18–20,55,56], which integrates with the two soft dc-link voltages. However, this topology fails to provide soft-switching for a majority of the grid angles, leading to a reduction in system efficiency.

The T-type converter, as shown in Fig. 2.3, overcomes these challenges by merging the two H-bridges into a single three-port converter, efficiently utilizing the semiconductor devices. It consists of two input ports to integrate with the two soft dc-link voltages and one output port that requires only one wireless coil. Consequently, the T-type converter, with most of its semiconductor devices capable of soft-switching for a majority of the grid

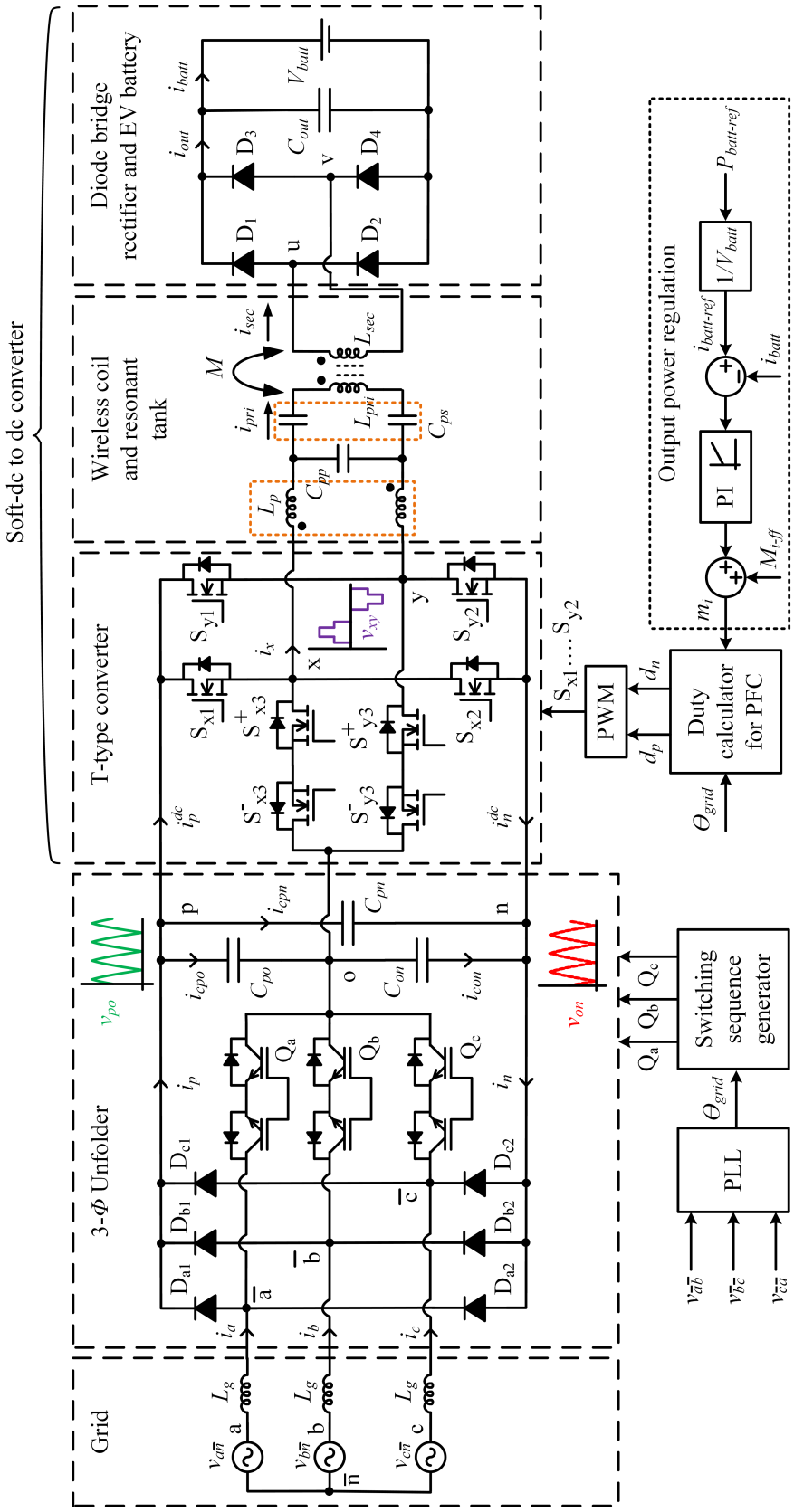


Fig. 2.3: Circuit schematic and control architecture of the PFC and output power regulation of an Unfolder with a T-type converter-based soft-dc to dc system.

angles, enables an efficient and power-dense solution for the unfolding-based single-stage topology. The T-type converter emulates balanced loads across the two output ports of the Unfolder, resulting in sinusoidal currents on the grid side, as presented in Fig. 2.2(b).

The T-type converts the soft dc-link voltages into an HF 5-level voltage, as illustrated in Figs. 2.4 and 2.5. The converter employs a modulation strategy that regulates the switching averages of the currents i_p^{dc} and i_n^{dc} to ensure the grid currents are piece-wise sinusoidal for PFC. Furthermore, the fundamental component of the resonant tank voltage v_{xy} is regulated over the entire grid cycle to control the output power. An LCC network is utilized to extract the fundamental component from the T-type output voltage v_{xy}. The HF current i_{sec} is rectified using a full-bridge rectifier on the secondary side and an output filter capacitor C_{out} to charge the battery of an EV. While a typical WPT system commonly consists of an LCC network on both the primary and secondary sides of the wireless coil [48–50, 57], in this study, the WPT system is emulated by incorporating a 1:1 isolation transformer in conjunction with the primary LCC resonant network.

2.3 Center-Aligned Modulation Strategy for the T-type Bridge

The T-type converter is operated at the WPT system's operating frequency of 85 kHz. Figs. 2.4 and 2.5 depict the switching sequence for the T-type converter for two cases: $d_p > d_n$ and $d_p < d_n$, where d_p and d_n represent the duty ratios corresponding to the soft dc-link voltages v_{po} and v_{on}, respectively. Two quasi-square voltage waveforms generated corresponding to v_{po} and v_{on} are center-aligned. To achieve input PFC and regulate output power, the duty ratios d_p and d_n of the T-type converter are modulated. In steady-state operation, the LCC network, diode bridge rectifier, and connected EV battery collectively act as a passive load given by the FHA. As a result, the output power can be controlled directly by adjusting the magnitude of the fundamental component of v_{xy}. The voltages v_{po} and v_{on} fluctuate at three times the grid frequency, as shown in Fig. 2.2(a). Henceforth, a mathematical evaluation is carried out solely for two sectors, 1 and 2, and subsequent analysis for other sectors can be conducted through a similar procedure. For the analysis, it is assumed that using a resonant tank with a suitable quality factor results in sinusoidal

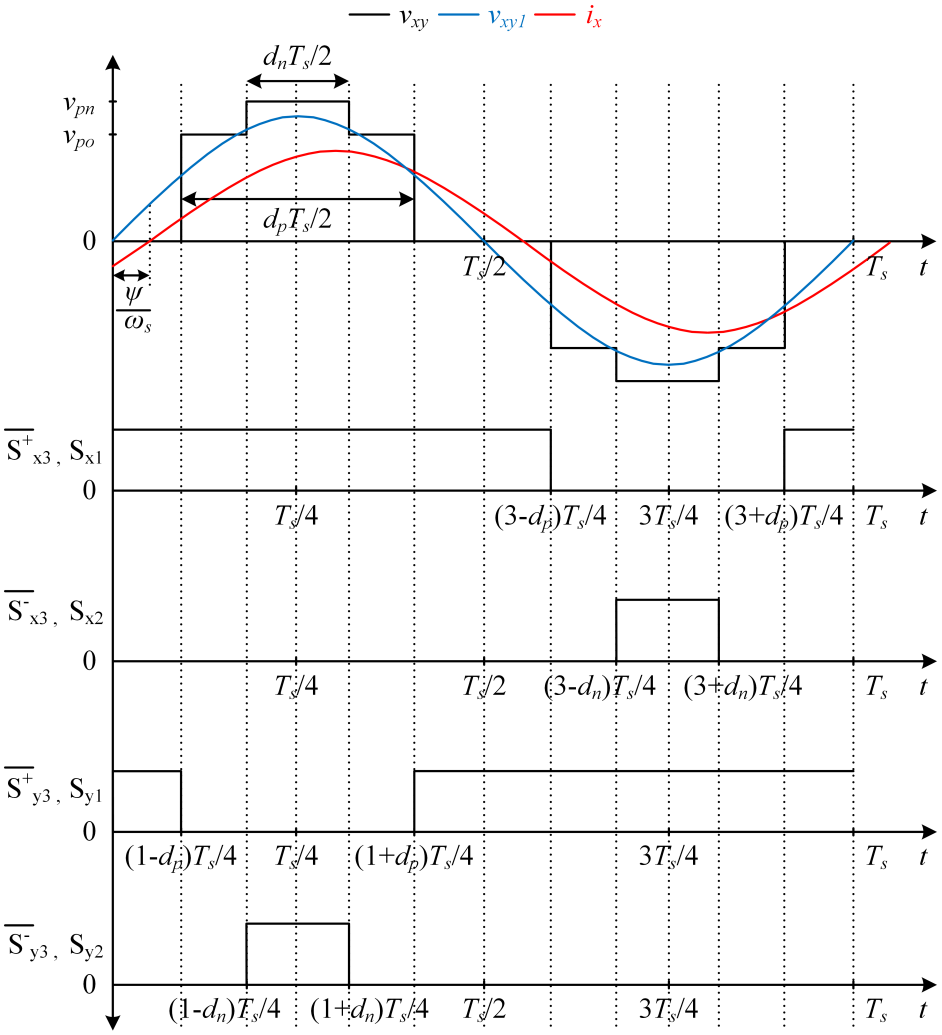


Fig. 2.4: Switching patterns of the T-type converter when d_p is greater than d_n. The modulation technique used aligns the two quasi-square voltages generated with respect to d_p and d_n in a symmetrical manner around the center. The 5-level T-type output voltage consists of a fundamental component, v_{xy1}, and a sinusoidal lagging current, i_x, is generated using an LCC network-based resonant tank.

current and voltage waveforms on both the primary and secondary sides of the soft-dc to dc system. As a result, the tank current i_x is considered a smooth sinusoid for further analysis. The fundamental component of the resonant tank voltage v_{xy} and the tank current i_x are

$$v_{xy1} = \frac{4}{\pi}\left[v_{po}\sin\left(\frac{\pi d_p}{2}\right) + v_{on}\sin\left(\frac{\pi d_n}{2}\right)\right]\sin\left(\omega_s t\right)\ , \tag{2.1}$$

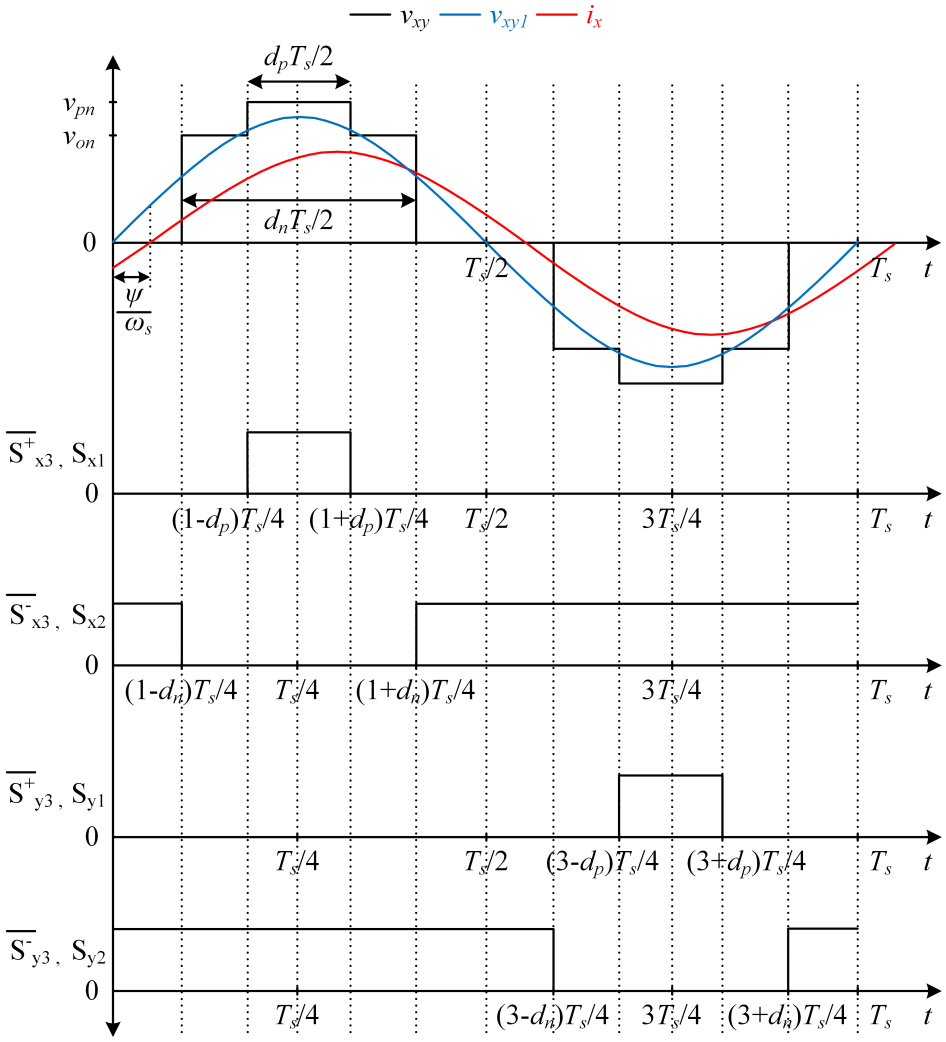


Fig. 2.5: Switching patterns of the T-type converter when d_p is less than d_n. The modulation technique used aligns the two quasi-square voltages generated with respect to d_p and d_n in a symmetrical manner around the center. The 5-level T-type output voltage consists of a fundamental component, v_{xy1}, and a sinusoidal lagging current, i_x, is generated using an LCC network-based resonant tank.

$$i_x = I_{xm} \sin(\omega_s t - \psi) \ , \tag{2.2}$$

where ω_s is the angular switching frequency of the T-type converter, I_{xm} is the amplitude of the tank current i_x, and ψ is the phase angle difference between the fundamental component of the tank voltage, v_{xy1}, and tank current, i_x.

Now, the expressions for d_p and d_n are derived through a three-step procedure:

1. For input PFC, the average values of i_p^{dc} and i_n^{dc} over a switching cycle are equated to the instantaneous values of required i_p and i_n, respectively. Maintaining the appropriate three-pulse i_p and i_n on the output of the Unfolder makes sure that the grid currents, which are shaped piece-wise by i_p and i_n, are sinusoidal. This step accounts for the currents flowing into the soft dc-link capacitors due to the three-pulse soft dc-link voltages across them and guarantees a unity power factor on the input side. It should be noted that the midpoint current of the Unfolder output does not need to be regulated as maintaining i_p and i_n inherently handles the midpoint current in accordance with KCL. This step results in

$$\left.\begin{aligned} \langle i_p^{dc}\rangle_{T_s} &= i_p - \langle i_{cpo} + i_{cpn}\rangle_{T_s}\,, \\ \langle i_n^{dc}\rangle_{T_s} &= i_n - \langle i_{con} + i_{cpn}\rangle_{T_s}\,. \end{aligned}\right\} \tag{2.3}$$

2. The average values of i_p^{dc} and i_n^{dc} are determined in terms of d_p and d_n by satisfying the power balance between the input ports and the output port of the T-type converter, as mentioned below:

$$\left.\begin{aligned} \langle i_p^{dc}\rangle_{T_s} &= \frac{2}{\pi} I_{xm}\cos(\psi)\sin\left(\frac{\pi d_p}{2}\right)\,, \\ \langle i_n^{dc}\rangle_{T_s} &= \frac{2}{\pi} I_{xm}\cos(\psi)\sin\left(\frac{\pi d_n}{2}\right)\,. \end{aligned}\right\} \tag{2.4}$$

3. The average values of i_p^{dc} and i_n^{dc} obtained from the previous two steps are equated to obtain d_p and d_n, as given below:

$$\left.\begin{aligned} d_p &= \frac{2}{\pi}\sin^{-1}\left(\frac{\pi I_{gcm}}{2I_{xm}\cos(\psi)}\sin(f_p(\theta_{grid},\alpha))\right)\,, \\ d_n &= \frac{2}{\pi}\sin^{-1}\left(\frac{\pi I_{gcm}}{2I_{xm}\cos(\psi)}\sin(f_n(\theta_{grid},\alpha))\right)\,, \end{aligned}\right\} \tag{2.5}$$

where

$$\left.\begin{aligned} I_{gcm} &= \sqrt{I_{gm}^2 + I_{cm}^2}\,, \\ \alpha &= \tan^{-1}\left(I_{cm}/I_{gm}\right)\,, \\ I_{cm} &= \sqrt{3}V_{gm}\omega_g C_{soft\text{-}dc}\,, \end{aligned}\right\} \tag{2.6}$$

where I_{gm} represents the peak of grid currents, V_{gm} is the peak of line-to-line ac input voltages, ω_g denotes the angular grid frequency, $C_{soft\text{-}dc}$ is the soft dc-link capacitance (C_{po}, C_{on}, and C_{pn}), and $f_{p,n}$ are the functions with respect to the grid angle (θ_{grid}) obtained from the PLL [9] and α introduced by $C_{soft\text{-}dc}$.

The equations of d_p and d_n are further simplified by introducing a term called steady-state modulation index (M_i) as defined below:

$$M_i = \frac{v_{xy1\text{-}rms}}{V_{xy1\text{-}rms\text{-}max}} = \frac{\pi v_{xy1\text{-}rms}}{\sqrt{6}V_{gm}\cos(\alpha)} = \frac{\pi I_{gcm}}{2I_{xm}\cos(\psi)}\,. \tag{2.7}$$

The resulting expressions for d_p and d_n, provided in Table 2.1 for sectors 1 and 2, ensure input PFC. If the soft dc-link capacitive currents, resulting from the three-pulse soft dc-link voltages applied across them, are much lower than the grid currents $\left(\sqrt{3}V_{gm}\omega_g C_{soft\text{-}dc} \ll I_{gm}\right)$, angle $\alpha \approx 0$. The simplified steady-state modulation index is then given by

$$M_i = \frac{v_{xy1\text{-}rms}}{V_{xy1\text{-}rms\text{-}max}} = \frac{\pi v_{xy1\text{-}rms}}{\sqrt{6}V_{gm}} = \frac{\pi I_{gm}}{2I_{xm}\cos(\psi)}\,. \tag{2.8}$$

As mentioned earlier, the magnitude of voltage v_{xy1}, which is determined by the modulation index, directly controls the output power and battery current. Therefore, a PI controller-based closed-loop control architecture, as shown in Fig. 2.3, is developed that calculates the required modulation index to achieve a certain power level by regulating the battery current. Subsequently, the calculations of d_p and d_n are done, which inherently take care of the input PFC, based on the appropriate modulation index required for the output power. Therefore, the proposed modulation strategy and closed-loop control architecture handle both the control tasks required for battery charging applications. It should be noted

Table 2.1: Calculation of d_p and d_n for sectors 1 and 2 (analysis of the other sectors can be conducted through a similar procedure).

Parameter	**Sector 1** $[\mathbf{0 \leq \theta_{grid} < \pi/3}]$	**Sector 2** $[\mathbf{\pi/3 \leq \theta_{grid} < 2\pi/3}]$
v_{po}	$V_{gm} \sin(\theta_{grid} + 2\pi/3)$	$V_{gm} \sin(\theta_{grid} - \pi/3)$
v_{on}	$V_{gm} \sin(\theta_{grid})$	$V_{gm} \sin(\theta_{grid} + \pi/3)$
$\langle i_p^{dc} \rangle_{T_s}$ $= i_p - \langle i_{cpo} + i_{cpn} \rangle_{T_s}$	$(2/\pi)\, I_{xm} \cos(\psi) \sin(\pi d_p/2)$ $= I_{gm} \sin(\theta_{grid} + \pi/2) - I_{cm} \cos(\theta_{grid} + \pi/2)$	$(2/\pi)\, I_{xm} \cos(\psi) \sin(\pi d_p/2)$ $= I_{gm} \sin(\theta_{grid} - \pi/6) - I_{cm} \cos(\theta_{grid} - \pi/6)$
$\langle i_n^{dc} \rangle_{T_s}$ $= i_n - \langle i_{con} + i_{cpn} \rangle_{T_s}$	$(2/\pi)\, I_{xm} \cos(\psi) \sin(\pi d_n/2)$ $= I_{gm} \sin(\theta_{grid} + \pi/6) - I_{cm} \cos(\theta_{grid} + \pi/6)$	$(2/\pi)\, I_{xm} \cos(\psi) \sin(\pi d_n/2)$ $= I_{gm} \sin(\theta_{grid} + \pi/6) - I_{cm} \cos(\theta_{grid} + \pi/6)$
d_p	$(2/\pi) \sin^{-1}(M_i \sin(\theta_{grid} + \pi/2 - \alpha))$	$(2/\pi) \sin^{-1}(M_i \sin(\theta_{grid} - \pi/6 - \alpha))$
d_n	$(2/\pi) \sin^{-1}(M_i \sin(\theta_{grid} + \pi/6 - \alpha))$	$(2/\pi) \sin^{-1}(M_i \sin(\theta_{grid} + \pi/6 - \alpha))$

that the calculations of d_p and d_n are decoupled even though the voltage v_{xy1} is a function of both d_p and d_n as mentioned in (2.1). Additionally, the proposed modulation strategy elegantly handles input PFC without the need to sense input grid currents or soft dc-link p and n ports currents.

2.4 ZVS Operation and Motivation for the Modular T-type Architecture

As mentioned in [13, 58], in order to achieve ZVS of the MOSFETs, it is necessary for the converter output current to be sufficiently negative during positive transitions of the converter output voltage, and conversely, for the current to be sufficiently positive during negative voltage transitions. Typically, such desired current polarities are achieved by a certain degree of inductive loading of the converter. This ensures two important aspects: (i) prior to turning on the MOSFET, its output capacitor (C_{oss}) is discharged, and (ii) when the MOSFET is turned off[1], the device current is shifted to its C_{oss} for charging. This phenomenon, which is also known as soft-switching, effectively avoids overlap and C_{oss} discharging/charging related switching losses.

To understand the soft-switched or hard-switched nature of the T-type converter MOSFETs, the scenario when $d_p > d_n$ is considered, while a similar analysis can be done for $d_p < d_n$. Fig. 2.6 depicts the analytical waveforms of the T-type converter's output voltage, v_{xy}, and output current, i_x, for two scenarios: (i) when d_p is close to unity, and (ii) when d_p is much smaller than unity. In both scenarios, it is observed that all four trailing edge transitions consistently exhibit ZVS due to the presence of the appropriate output current polarity and magnitude during these transitions. However, the second and fourth leading edge transitions always occur in a hard-switched manner. The ZVS nature of the first and third leading edge transitions is conditional based on the following observations: (i) Fig. 2.6(a) illustrates that when d_p is closer to unity, the output current polarity and magnitude enable ZVS of the MOSFETs during these transitions, and (ii) Fig. 2.6(b) demonstrates that when d_p is much smaller than unity, the MOSFETs undergo hard-switching during these

[1]To achieve ZVS during turn-off, the MOSFET's turn-off time needs to be sufficiently fast so that the device current shifts to its C_{oss} swiftly. Otherwise, the device experiences some degree of overlap losses.

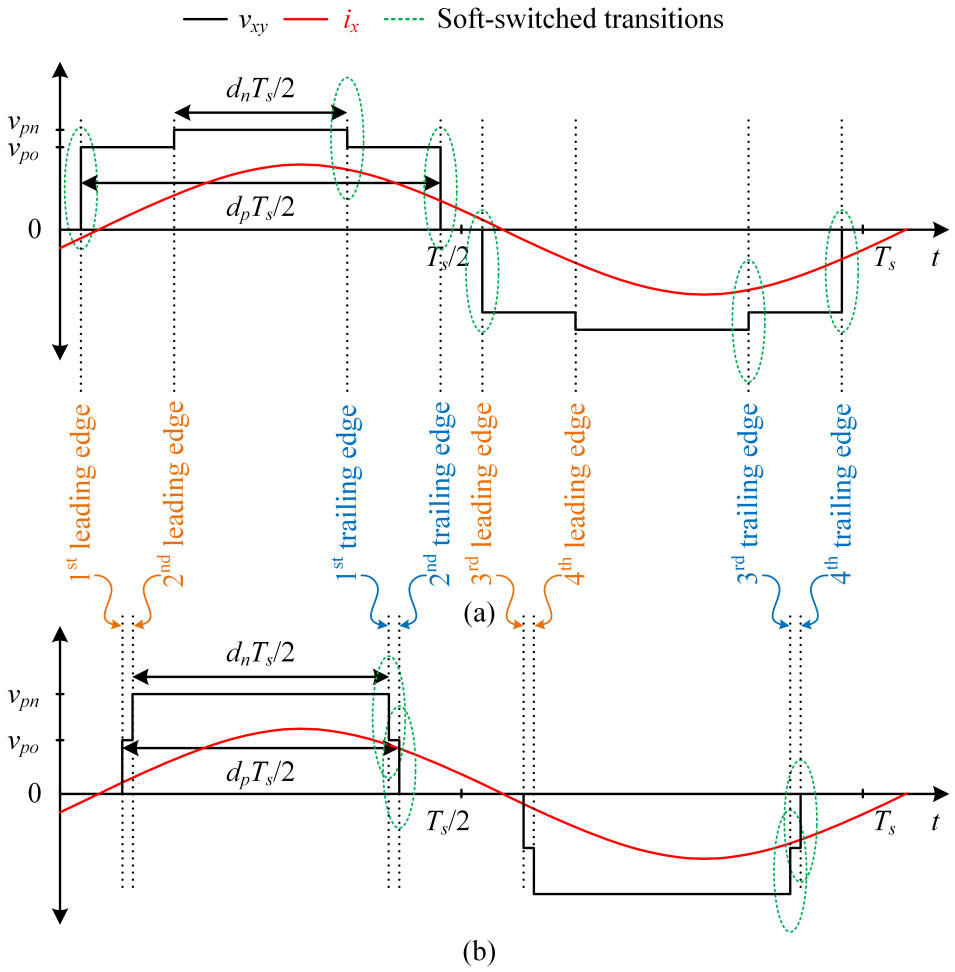


Fig. 2.6: Analytical v_{xy} and i_x with (a) $d_p = 0.9$ and $d_n = 0.43$ which leads to more ZVS transitions of MOSFETs including the first and third leading edge transitions as the value of d_p is higher and closer to unity, (b) $d_p = 0.69$ and $d_n = 0.64$ which leads to hard-switched leading edges as both the duties are much smaller than unity. Trailing edge transitions in both cases always have ZVS. Higher magnitudes of d_p or d_n are favorable for soft-switching.

transitions. The criterion for achieving ZVS of the MOSFETs during the first and third leading edge transitions, expressed in (2.9), depends on the minimum values of d_p or d_n. The increasing amount of MOSFETs experiencing ZVS transitions during the first and third leading edge transitions throughout the grid cycle as d_p or d_n approaches a magnitude of unity is depicted in Fig. 2.7. The classification of all the T-type converter MOSFETs into soft-switched or hard-switched categories during different transitions is summarized in

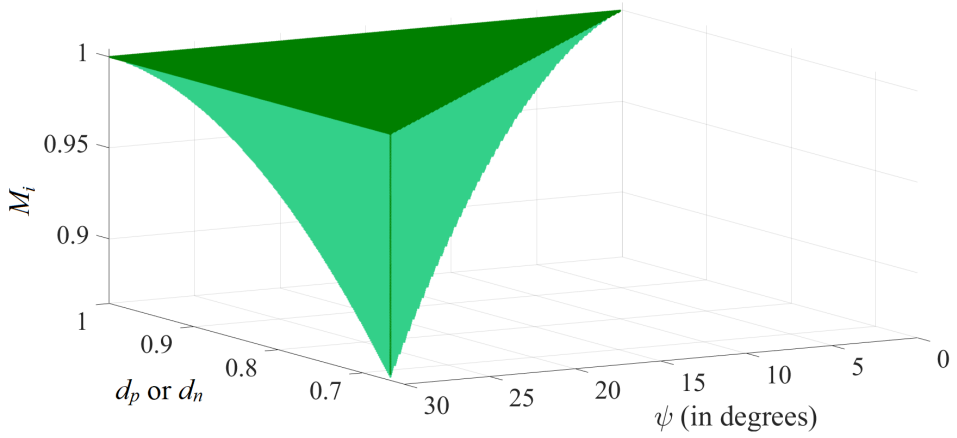


Fig. 2.7: Various duty ratios, d_p or d_n, are indicated in green, representing the values at which the first and third leading edge transitions undergo ZVS of the MOSFETs. As the modulation index, M_i, increases at a specific phase shift between v_{xy1} and i_x, ψ, ZVS is possible for more values of duty ratios. Consequently, an increase in the modulation index directly correlates to a greater extent of soft-switching.

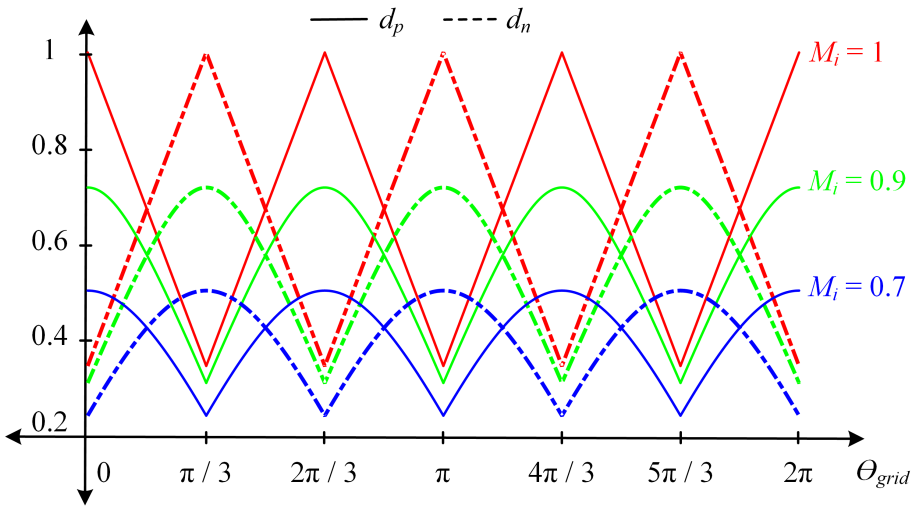


Fig. 2.8: Variation of d_p and d_n with different steady-state modulation indices.

Tables 2.2 and 2.3. The ZVS conditions are

$$\left.\begin{aligned} d_p &> 1 - \frac{2\psi}{\pi} \quad ...(d_p > d_n)\,, \\ d_n &> 1 - \frac{2\psi}{\pi} \quad ...(d_n > d_p)\,. \end{aligned}\right\} \tag{2.9}$$

With most of the MOSFETs soft-switching for higher values of duty ratios throughout the grid cycle, it is required to have a higher modulation index which leads to the attainment

Table 2.2: Nature of the switching of the T-type converter MOSFETs when $d_p > d_n$.

Transition	**MOSFETs switching**	$\boldsymbol{d_p > 1 - \frac{2\psi}{\pi}}$	$\boldsymbol{d_p \leq 1 - \frac{2\psi}{\pi}}$
1^{st} leading edge	S_{y1}, S^{+}_{y3}	ZVS	Hard-switched
2^{nd} leading edge	S_{y2}, S^{-}_{y3}	Hard-switched	Hard-switched
3^{rd} leading edge	S_{x1}, S^{+}_{x3}	ZVS	Hard-switched
4^{th} leading edge	S_{x2}, S^{-}_{x3}	Hard-switched	Hard-switched
1^{st} trailing edge	S_{y2}, S^{-}_{y3}	ZVS	ZVS
2^{nd} trailing edge	S_{y1}, S^{+}_{y3}	ZVS	ZVS
3^{rd} trailing edge	S_{x2}, S^{-}_{x3}	ZVS	ZVS
4^{th} trailing edge	S_{x1}, S^{+}_{x3}	ZVS	ZVS

Table 2.3: Nature of the switching of the T-type converter MOSFETs when $d_p < d_n$.

Transition	**MOSFETs switching**	$\boldsymbol{d_n > 1 - \frac{2\psi}{\pi}}$	$\boldsymbol{d_n \leq 1 - \frac{2\psi}{\pi}}$
1^{st} leading edge	S_{x2}, S^{-}_{x3}	ZVS	Hard-switched
2^{nd} leading edge	S_{x1}, S^{+}_{x3}	Hard-switched	Hard-switched
3^{rd} leading edge	S_{y2}, S^{-}_{y3}	ZVS	Hard-switched
4^{th} leading edge	S_{y1}, S^{+}_{y3}	Hard-switched	Hard-switched
1^{st} trailing edge	S_{x1}, S^{+}_{x3}	ZVS	ZVS
2^{nd} trailing edge	S_{x2}, S^{-}_{x3}	ZVS	ZVS
3^{rd} trailing edge	S_{y1}, S^{+}_{y3}	ZVS	ZVS
4^{th} trailing edge	S_{y2}, S^{-}_{y3}	ZVS	ZVS

of larger duty ratios over a major portion of the grid cycle as shown in Figs. 2.7 and 2.8. This motivates having a modular structure of the T-type converter-based soft-dc to dc system, as shown later in the experimental validation section. With multiple parallelly connected T-type converters, operation at a lower load can be achieved by deactivating some of the converters while maintaining the maximum modulation index for the other operating converters.

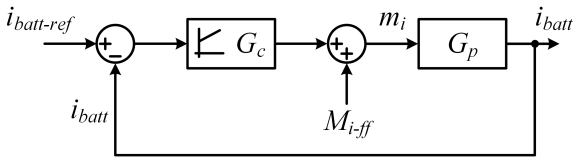


Fig. 2.9: A simplified closed-loop control architecture to regulate battery current (i_{batt}) by controlling the modulation index (m_i). A PI controller (G_c) is used and a feed-forward term $M_{i\text{-}ff}$ is introduced to improve the speed of response. Moreover, the plant's transfer function (G_p) is derived using phasor transformation-based modeling.

2.5 Modeling and Control of the T-type Bridge-Based Soft-DC to DC System

As the T-type converter effectively manages all the control-related tasks, such as input PFC and output power regulation, the modeling and closed-loop control analysis are confined to the soft-dc to dc system, excluding the unfolding part. Moreover, the primary focus is given to the output power regulation task since the PFC is skillfully handled by a previously discussed feed-forward technique, which accurately determines the duty ratios (d_p and d_n) based on the modulation index (m_i) required to produce the desired output power. To accurately regulate the output power and control the battery current (i_{batt}), it is necessary to design a suitable controller for the T-type converter-based soft-dc to dc system with an LCC resonant network[2], secondary diode bridge rectifier, and output capacitive filter. The utilization of a resonant tank with an appropriate quality factor enables the attainment of sinusoidal current or voltage waveforms in the tank. In this scenario, the use of a phasor transformation-based modeling approach, as discussed in Chapter 5 and [25, 60–63], is deemed appropriate.

Since the modulation index serves as a crucial control parameter in determining the duty ratios that ultimately determine the battery current, a small-signal transfer function is derived between $\hat{i}_{batt}$ and $\hat{m}_i$, which acts as a plant (G_p) in the closed-loop control architecture shown in Fig. 2.9. The modeling process involves mainly three steps: (i) steady-state calculation to establish the relationship between I_{batt} and M_i given in (2.10), (ii) derivation of a phasor-transformed stationary circuit for the T-type converter, resonant network, along

[2]This work involves the emulation of a WPT system by employing a tightly coupled transformer. Therefore, a cantilever model is utilized for the purpose of modeling. However, in the case of a system incorporating a wireless coil, it is possible to substitute the cantilever model with a two-coupled inductor model [48, 59, 60]. The remaining steps of the modeling procedure would remain unchanged.

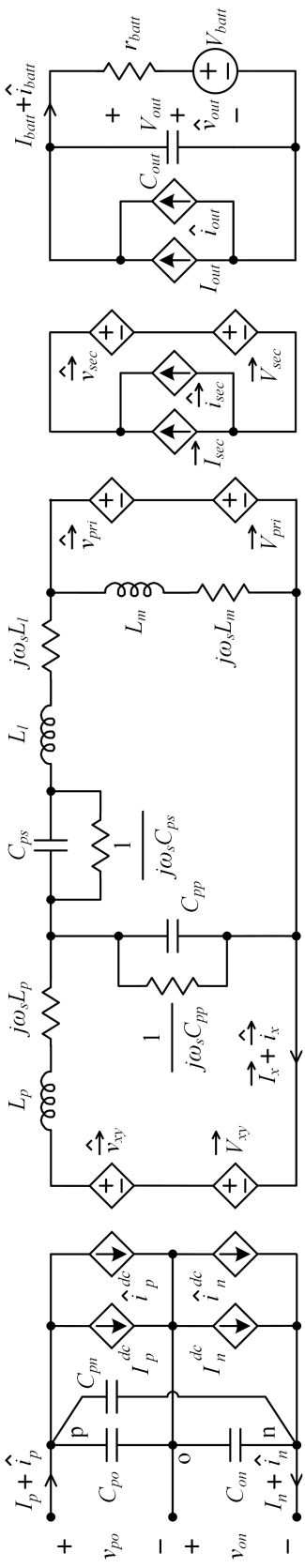


Fig. 2.10: Phasor-transformed stationary circuit for the T-type converter-based soft-dc to dc system with an LCC resonant network, secondary diode bridge rectifier, and output capacitive filter connected to the battery.

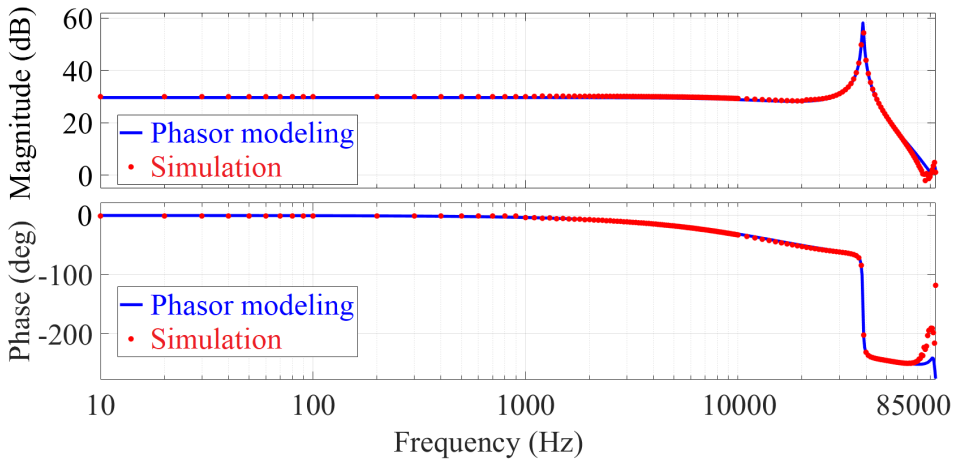


Fig. 2.11: Comparison of the bode plots of the T-type converter-based soft-dc to dc system's plant (G_p) obtained from the phasor transformation-based small-signal modeling and MATLAB/PLECS multitone analysis tool-based simulation.

with the diode bridge on the secondary side, as shown in Fig. 2.10, and (iii) small-signal derivation of the plant's transfer function based on the aforementioned phasor-transformed circuit, as mentioned in (2.11) and (2.12). Equations (2.10), (2.11), and (2.12) are

$$I_{batt} = \frac{4\sqrt{3}M_i V_{gm}}{\pi^2 \omega_s L_p}\,, \tag{2.10}$$

$$H_{i_{out}}^{m_i} = \frac{\hat{i}_{out}}{\hat{m}_i} = \frac{\hat{i}_{out}^{i_{sec\text{-}env}}}{\hat{i}_{sec\text{-}env}^{m_i}} \frac{\hat{i}_{sec\text{-}env}^{m_i}}{\hat{m}_i} + \frac{\hat{i}_{out}^{\theta_{sec}}}{\hat{\theta}_{sec}^{m_i}} \frac{\hat{\theta}_{sec}^{m_i}}{\hat{m}_i}\,, \tag{2.11}$$

$$G_p = H_{i_{batt}}^{m_i} = \frac{\hat{i}_{batt}}{\hat{m}_i} = \frac{H_{i_{out}}^{m_i}}{1 + r_{batt} C_{out} s}\,, \tag{2.12}$$

where $\hat{i}_{out}^{i_{sec\text{-}env}}$ and $\hat{i}_{out}^{\theta_{sec}}$ represent perturbations in the output current (i_{out}) of the diode bridge that are contingent upon the small-signal change in the envelope ($\hat{i}_{sec\text{-}env}^{m_i}$) and phase ($\hat{\theta}_{sec}^{m_i}$) of the diode bridge's input current phasor ($\overrightarrow{i_{sec}}$), respectively. These perturbations arise due to small-signal deviations in m_i. The plant's transfer function, G_p, is evaluated by combining $H_{i_{out}}^{m_i}$ with a first-order pole that originates from the net series resistance of the battery, r_{batt}, and the output capacitive filter, C_{out}.

Fig. 2.11 compares the bode plots of the plant G_p obtained through two different methods: phasor transformation-based modeling and the multitone analysis (MATLAB/PLECS simulation tool) of the soft-dc to dc system. The bode plots derived at the rated load con-

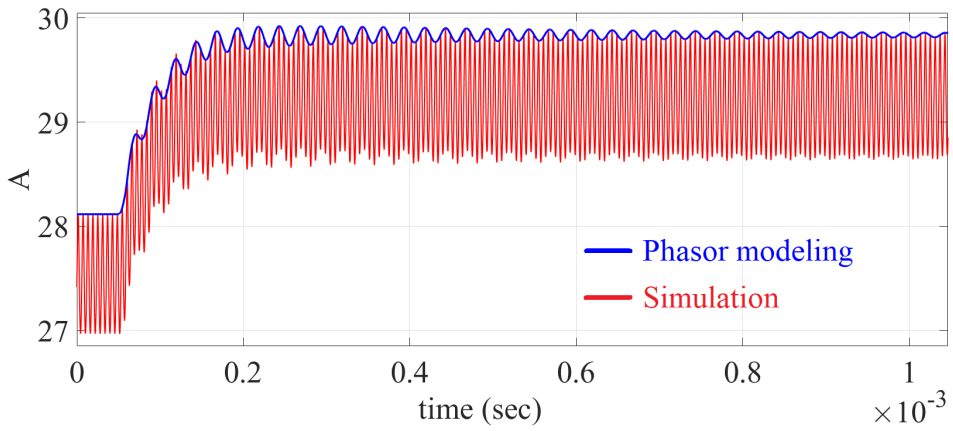


Fig. 2.12: Simulation result of the battery current superimposed upon the envelope predicted by the small-signal model under the step change in modulation index from 0.95 to 1 at time = 0.05 msec.

dition display a close resemblance. In addition, the model-generated envelope curve of the battery current closely matches the simulation result when evaluated under a step change of modulation index from 0.95 to 1, as shown in Fig. 2.12. The soft-dc to dc system exhibits considerable dynamics at higher frequencies, but since the steady-state battery current changes gradually, the closed-loop system's bandwidth is limited to 100 Hz. This analysis is utilized to compute the PI controller's (G_c) parameters and the resulting uncompensated and compensated bode plots are shown in Fig. 2.13. Moreover, the Nyquist plot of the open-loop transfer function (G_cG_p), as given in Fig. 2.14, for the T-type converter-based soft-dc to dc system provides valuable insights into the stability of the controller design. As can be seen in this figure, the Nyquist plot does not encircle the point (-1, j0), without any poles of the open loop transfer function on the right half-plane, indicating a stable controller design [58]. Accurate small-signal analysis of the T-type converter-based soft-dc to dc system assists in regulating the battery current effectively, as demonstrated in the experimental validation section along with the information about the system parameters used for small-signal modeling.

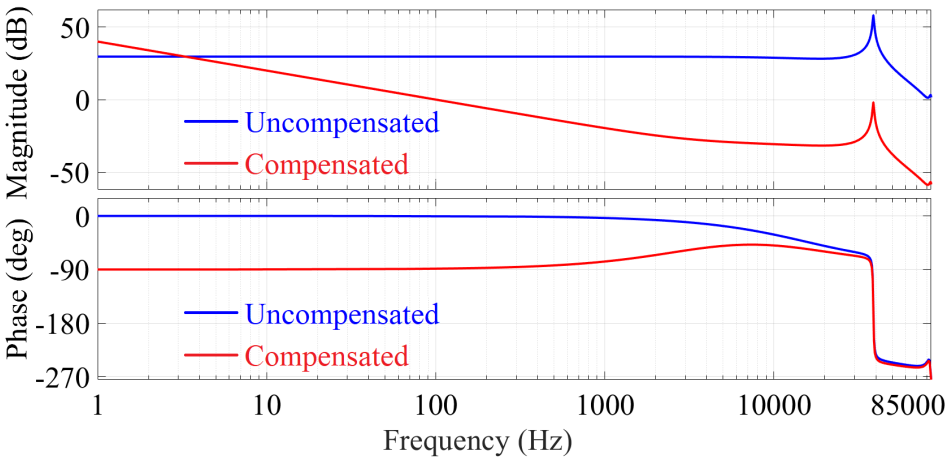


Fig. 2.13: Uncompensated and compensated bode plots of the T-type converter-based soft-dc to dc system's plant (G_p). The closed-loop bandwidth is set to 100 Hz with the help of a PI controller (G_c) with $K_p = 0.001$ and $K_i = 20.7$. Phase margin of 91.4° is obtained.

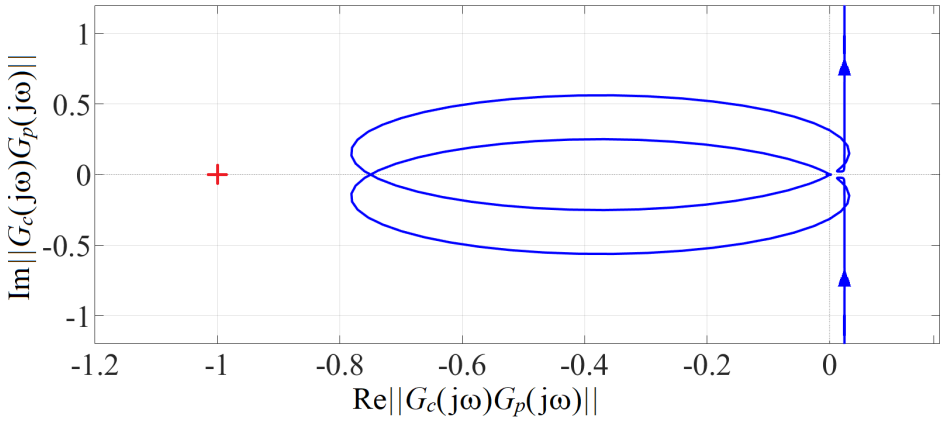


Fig. 2.14: Nyquist plot of the open loop transfer function (G_cG_p) of the T-type converter-based soft-dc to dc system. With no poles of the open loop transfer function on the right half-plane, the Nyquist plot not encircling (-1, j0) point shows a stable controller design.

2.6 Design Guidelines and Analytical Loss Calculation

This section focuses on the design of the crucial components in the proposed single-stage topology. Moreover, loss calculation is provided for the Unfolder and T-type converter.

2.6.1 Soft DC-Link Capacitor Design

The representation of the input current (i_p^{dc}) of the T-type converter as a function of the output current phasor ($\vec{i_x}$) and the switching function phasor ($\vec{s_p}$) can be expressed as,

$$i_p^{dc} = \Re[\vec{s_p}^* \vec{i_x}] + \Re[\vec{s_p}\vec{i_x} e^{2j\omega_s t}]\,, \tag{2.13}$$

which clearly states that the input current has dc and twice the switching frequency components. The HF components flow through the soft dc-link capacitors, which leads to HF ripples in the soft dc-link voltages v_{po}, v_{on}, and v_{pn}. To ensure the voltage ripple ($\Delta v_{c\text{-}soft}$) remains within an acceptable threshold, the soft dc-link capacitors should be sized accordingly. As the soft dc-link capacitors solely serve the purpose of bypassing HF current components, the following factors are considered during the calculation process:

1. Currents flowing into the capacitors due to the low frequency three-pulse soft dc-link voltages are considered negligible.

2. Fundamentally, only two capacitors (C_{po} and C_{on}) are required to bypass the HF current components, and the third capacitor (C_{pn}) is used to create a symmetric Δ-connected configuration for balanced loading purposes. As a result, for the sake of simplifying the calculations, a configuration involving only two capacitors (C_{po} and C_{on}) is considered.

The RMS current of the HF component flowing into C_{po} is given by

$$\left.\begin{aligned} i_{cpo\text{-}rms} &= \sqrt{\left(i_{p\text{-}rms}^{dc}\right)^2 - \left(\langle i_p^{dc}\rangle_{T_s}\right)^2}\,, \\ i_{p\text{-}rms}^{dc} &= \frac{I_{xm}}{\sqrt{2}}\sqrt{d_p + \frac{\cos(2\psi)\sin(\pi d_p)}{\pi}}\,, \\ \langle i_p^{dc}\rangle_{T_s} &= \frac{2}{\pi} I_{xm}\cos(\psi)\sin\left(\frac{\pi d_p}{2}\right)\,. \end{aligned}\right\} \tag{2.14}$$

The variation of $i_{cpo\text{-}rms}$ across the grid cycle is evident from above equations, depending on the value of d_p. The specific value of d_p at which C_{po} carries the highest RMS current is given by

$$d_p|_{I_{cpo\text{-}rms\text{-}max}} = \frac{1}{\pi}\left\{ \tan^{-1}\left(\frac{\pi}{4}\left(1-\tan^2(\psi)\right)\right) + \sin^{-1}\left(\frac{\pi}{\sqrt{16\cos^4(\psi)+\pi^2\cos^2(2\psi)}}\right)\right\}. \tag{2.15}$$

Now, to ensure the peak-peak voltage ripple of the capacitor C_{po} stays within a maximum acceptable limit of $\Delta V_{c\text{-}soft\text{-}max}$, the capacitance is derived below using the equation $Q_{cpo\text{-}max} = C_{po}\Delta V_{c\text{-}soft\text{-}max}$:

$$C_{po} = \frac{2I_{xm}\left(1 - d_p|_{I_{cpo\text{-}rms\text{-}max}}\right)\cos(\psi)\sin\left(\frac{\pi}{2}\, d_p|_{I_{cpo\text{-}rms\text{-}max}}\right)}{\omega_s \Delta V_{c\text{-}soft\text{-}max}}, \tag{2.16}$$

which can be written in terms of the output power, P_{out}, as

$$C_{po} = \frac{2\pi P_{out}\left(1 - d_p|_{I_{cpo\text{-}rms\text{-}max}}\right)\sin\left(\frac{\pi}{2}\, d_p|_{I_{cpo\text{-}rms\text{-}max}}\right)}{\sqrt{3}V_{gm}\omega_s \Delta V_{c\text{-}soft\text{-}max}}. \tag{2.17}$$

Since a symmetric Δ-connected configuration is employed, the two other capacitors, C_{on} and C_{pn}, with the identical capacitance value as determined by (2.17), can be used. Furthermore, the capacitors must have a minimum RMS current rating of $I_{cpo\text{-}rms\text{-}max}$ at twice the switching frequency.

2.6.2 Resonant Tank Design

In this work, the WPT system is emulated using a tightly coupled 1:1 isolation transformer along with the primary LCC resonant network. This setup allows the resonant tank to emulate a load similar to that of a WPT system under this specific configuration. The design of the LCC tank is given below.

Design of L_p

As indicated by (2.10), the battery current and the resulting output power, P_{out}, exhibit an inverse relationship with the inductance L_p. Therefore, the determination of L_p is contingent upon the power requirement for the battery, as described below:

$$L_p = \frac{4\sqrt{3}M_i V_{gm} V_{out}}{\pi^2 \omega_s P_{out}}. \tag{2.18}$$

Design of C_{pp}

Illustrated in Figs. 2.4 and 2.5, v_{xy} represents a 5-level voltage waveform characterized by its fundamental component at the switching frequency. In order to extract this fundamental component while attenuating undesired higher-order frequency components, the capacitance value of C_{pp} is chosen to resonate with L_p at the switching frequency, as defined in (2.19). This ensures that the tank current exhibits a well-defined sinusoidal waveform with a dominant fundamental component. By suppressing the higher-order harmonics of the tank current, the conduction losses in the conversion process are effectively reduced. The value of C_{pp} is calculated as

$$C_{pp} = \frac{1}{\omega_s^2 L_p}\,. \tag{2.19}$$

Design of C_{ps} and L_l

As mentioned earlier, the diode bridge connected to an EV battery on the secondary side functions as a voltage and power-dependent resistive load in steady-state, denoted as R_{eq} in (2.20) and (2.21). In the case of an LCC tank, if the combined impedance of the transformer leakage inductor, L_l, and series capacitor, C_{ps}, matches the impedance of L_p at the operating frequency, the impedance perceived by the T-type converter becomes purely resistive and equal to $\frac{L_p}{R_{eq}C_{pp}}$ [64]. Consequently, to minimize the requirement of C_{ps} and avoid the reactive loading of the converter, the transformer is designed such that L_l closely matches the inductance of L_p. However, in order to achieve ZVS for the maximum number of T-type converter MOSFETs, a certain level of inductive loading is necessary. To attain this inductive loading by introducing a phase lag in the converter output current, denoted by ψ, the value of C_{ps} is derived as

$$C_{ps} = \frac{1}{\omega_s \left(R_{eq}\tan\left(\psi\right) + \omega_s(L_l - L_p)\right)}\,, \tag{2.20}$$

where

$$R_{eq} = \frac{8}{\pi^2}\frac{V_{out}^2}{P_{out}}\,. \tag{2.21}$$

2.6.3 Output Capacitor Design

The output capacitor, C_{out}, carries twice the switching frequency component present in the diode bridge output current. This HF current leads to ripples in the output voltage. To constrain the peak-peak voltage ripple within a maximum acceptable value of $\Delta V_{c\text{-}out\text{-}max}$, the capacitance is calculated as follows considering that C_{out} carries all the HF component. The value of C_{out} is calculated as

$$C_{out} = \frac{P_{out}}{\omega_s V_{out} \Delta V_{c\text{-}out\text{-}max}} \,. \tag{2.22}$$

2.6.4 Analytical Loss Calculation

Unfolder

As mentioned earlier, the Unfolder functions with a maximum of twice the grid frequency. Consequently, the Unfolder's switching losses can be disregarded. The primary impact of the Unfolder lies in the conduction losses, which are dependent on the average and RMS currents passing through the diodes and IGBTs, as given below:

$$\left.\begin{aligned} P_{cond\text{-}loss\text{-}unfolder} = 6\Big\{ & V_{f\text{-}diode} I_{avg\text{-}diode} + R_{f\text{-}diode} I^2_{rms\text{-}diode} + \\ & (V_{ce\text{-}igbt} + V_{f\text{-}apdiode\text{-}igbt}) I_{avg\text{-}igbt} + \\ & (R_{ce\text{-}igbt} + R_{f\text{-}apdiode\text{-}igbt}) I^2_{rms\text{-}igbt} \Big\} \,, \end{aligned}\right\} \tag{2.23}$$

where

$$\left.\begin{aligned} I_{avg\text{-}diode} &= \frac{\sqrt{3} I_{gm}}{2\pi} \,, \\ I_{rms\text{-}diode} &= I_{gm} \sqrt{\frac{1}{6} + \frac{\sqrt{3}}{8\pi}} \,, \\ I_{avg\text{-}igbt} &= \frac{I_{gm}}{\pi} \left(1 - \frac{\sqrt{3}}{2} \right) \,, \\ I_{rms\text{-}igbt} &= I_{gm} \sqrt{\frac{1}{12} - \frac{\sqrt{3}}{8\pi}} \,. \end{aligned}\right\} \tag{2.24}$$

T-type converter

The T-type converter incurs both conduction and switching losses. The conduction losses are determined by the RMS currents that flow through the MOSFETs, as given in (2.25) and (2.26). These equations are applicable when $d_p > d_n$. However, a similar analysis can also be performed for the case when $d_p < d_n$. In the following equations, the term $R_{ds\text{-}hc}$ represents the on-resistance of the MOSFETs carrying higher currents (S_{x1}, S_{x2}, S_{y1}, and S_{y2}). On the other hand, $R_{ds\text{-}lc}$ denotes the on-resistance of the midpoint MOSFETs that carry lower currents (S^{+}_{x3}, S^{-}_{x3}, S^{+}_{y3}, and S^{-}_{y3}). The conduction losses are given as

$$\left.\begin{aligned} P_{cond\text{-}loss\text{-}t\text{-}type} = 2\Big(& i^2_{rms\text{-}sx1,sy1} R_{ds\text{-}hc} + i^2_{rms\text{-}sx2,sy2} R_{ds\text{-}hc} + \\ & i^2_{rms\text{-}sx3+,sx3\text{-}} R_{ds\text{-}lc} + i^2_{rms\text{-}sy3+,sy3\text{-}} R_{ds\text{-}lc}\Big), \end{aligned}\right\} \tag{2.25}$$

where

$$\left.\begin{aligned} i_{rms\text{-}sx1,sy1} &= \frac{I_{xm}}{2}\sqrt{(2-d_p) - \frac{\cos(2\psi)\sin(\pi d_p)}{\pi}}, \\ i_{rms\text{-}sx2,sy2} &= \frac{I_{xm}}{2}\sqrt{d_n + \frac{\cos(2\psi)\sin(\pi d_n)}{\pi}}, \\ i_{rms\text{-}sx3+,sx3\text{-}} &= \frac{I_{xm}}{2}\sqrt{(d_p-d_n) + \frac{2}{\pi}\cos(2\psi)\cos\left(\frac{\pi}{2}(d_p+d_n)\right)\sin\left(\frac{\pi}{2}(d_p-d_n)\right)}, \\ i_{rms\text{-}sy3+,sy3\text{-}} &= \frac{I_{xm}}{2}\sqrt{(d_p-d_n) + \frac{2}{\pi}\cos(2\psi)\cos\left(\frac{\pi}{2}(d_p+d_n)\right)\sin\left(\frac{\pi}{2}(d_p-d_n)\right)}. \end{aligned}\right\} \tag{2.26}$$

As mentioned in Tables 2.2 and 2.3, all the trailing edge transitions of the T-type converter exhibit soft-switching characteristics. On the other hand, depending on the magnitude of d_p or d_n, either two or all four of the leading edge transitions demonstrate hard-switching behavior, as discussed earlier. The switching losses associated with these hard-switched transitions can be computed by utilizing the specified turn-on and turn-off energy losses provided in the datasheet. It is necessary to scale these energy values based on the voltage and current levels at which the switching of the MOSFETs happens, as well as the chosen gate resistance within the circuit. Moreover, additional C_{oss}-related losses must be taken into account for the MOSFET that is not actively turning on or off, but experiences

a voltage change across its C_{oss} due to the switching transitions of the other MOSFETs in the same leg. This phenomenon has been explained in detail in [29, 65, 66]. The following equations have been derived for the scenario where $d_p > d_n$. However, it is also possible to conduct a similar analysis for the case when $d_p < d_n$.

When $d_p > 1 - \frac{2\psi}{\pi}$,

$$\left.\begin{aligned} P_{sw\text{-}loss\text{-}t\text{-}type} &= P_{2^{nd}\text{-}leading\text{-}edge} + P_{4^{th}\text{-}leading\text{-}edge} \\ &= 2f_s(E_{on\text{-}scaled\text{-}sy2} + E_{off\text{-}scaled\text{-}sy3\text{-}} + E_{coss\text{-}sy1})\,. \end{aligned}\right\} \tag{2.27}$$

When $d_p \leq 1 - \frac{2\psi}{\pi}$,

$$\left.\begin{aligned} P_{sw\text{-}loss\text{-}t\text{-}type} &= P_{1^{st}\text{-}leading\text{-}edge} + P_{2^{nd}\text{-}leading\text{-}edge} + \\ &\quad P_{3^{rd}\text{-}leading\text{-}edge} + P_{4^{th}\text{-}leading\text{-}edge} \\ &= 2f_s(E_{off\text{-}scaled\text{-}sy1} + E_{on\text{-}scaled\text{-}sy3+} + E_{coss\text{-}sy2} + \\ &\quad E_{on\text{-}scaled\text{-}sy2} + E_{off\text{-}scaled\text{-}sy3\text{-}} + E_{coss\text{-}sy1})\,. \end{aligned}\right\} \tag{2.28}$$

In the above equations,

$$\left.\begin{aligned} E_{coss\text{-}sy1} &= (Q_{oss}|_{v_{pn}} - Q_{oss}|_{v_{po}})v_{pn} - (E_{oss}|_{v_{pn}} - E_{oss}|_{v_{po}})\,, \\ E_{coss\text{-}sy2} &= (E_{oss}|_{v_{pn}} - E_{oss}|_{v_{on}}) - (Q_{oss}|_{v_{pn}} - Q_{oss}|_{v_{on}})v_{on}\,, \end{aligned}\right\} \tag{2.29}$$

where $Q_{oss}|_{v_k}$ and $E_{oss}|_{v_k}$ represent the charge and energy stored in the C_{oss} of S_{y1} and S_{y2} at voltage v_k, as defined in [30, 65, 66].

By examining (2.25)-(2.29), it becomes evident that the conduction and switching losses exhibit variations dependent on the duty ratios. However, in order to obtain a consistent and single value, the average of both losses can be computed over the entirety of the grid cycle.

Table 2.4: Hardware parameters of the ac-dc conversion system with a single T-type converter module.

Parameter	Value
Nominal input voltage	480 V (l-l), 60 Hz ac 3-ϕ
Battery voltage	649 V - 755 V
Nominal output power	21 kW
Unfolder switching frequency	Diodes - 60 Hz, IGBTs - 120 Hz
T-type converter switching frequency	85 kHz

2.7 Experimental Validation

A hardware prototype of an ac-dc conversion system based on a single T-type converter module is demonstrated in Fig. 2.15(a) with a power rating of 21 kW. The hardware parameters are summarized in Table 2.4, while Table 2.5 provides a detailed list of the semiconductor devices and passive components utilized in the prototype. The Unfolder[3] employs IXYS W1263YC200 diodes and Infineon FZ1200R17KF6C-B2 IGBTs, while the T-type converter uses NVH4L020N120SC1 and NVH4L040N120SC1 SiC MOSFETs from Onsemi. The midpoint switches ($S^{+}_{x3}, S^{-}_{x3}, S^{+}_{y3}$, and S^{-}_{y3}) carry lower RMS currents, as given by (2.26), so lower current devices are used to reduce the cost of the system. The use of a TO-247-4L package with a Kelvin source connection helps to reduce gate ringing and switching losses. Body diodes of CREE CCS050M12CM2 MOSFETs are utilized for the diode bridge rectifier on the secondary side. The California Instruments MX-30 and NH Research 9300 are used to emulate the grid and EV battery, respectively.

In order to facilitate the efficient paralleling of multiple modules and optimize the usage of the TMDSCNCD28379D microcontroller used in this system, a circuit board measuring 26.2 in (L) $\times$ 13.2 in (W) $\times$ 4.5 in (H) has been developed, as shown in Fig. 2.15(b), featuring three T-type converter modules rated for 21 kW output power each. The circuit board incorporates a cold plate for liquid cooling purposes [67]. To evaluate the functionality of this modular configuration when multiple T-type converters are operated together, six T-type converter modules are connected in parallel and subjected to testing at a 21 kW output

[3]Unfolder is designed for a 1 MW of output power which is the end goal of the project.

Table 2.5: List of components employed in the prototype.

Component	**Description**
Unfolder diodes	IXYS W1263YC200 (2000 V, 1263 A)
Unfolder IGBTs	Infineon FZ1200R17KF6C-B2 (1700 V, 1200 A)
T-type converter MOSFETs	Onsemi NVH4L020N120SC1 (1200 V, 102 A) Onsemi NVH4L040N120SC1 (1200 V, 58 A)
Secondary bridge diodes	CREE CCS050M12CM2 (1200 V, 87 A)
Grid inductance	600 μH (5% impedance of 50 kVA grid)
Soft dc-link capacitance (C_{po}, C_{on}, and C_{pn})	4.5 μF
L_p Single T-type module testing Six T-type modules testing	 28.3 μH 64.5 μH
C_{pp} Single T-type module testing Six T-type modules testing	 123.1 nF 54.3 nF
C_{ps}	160.3 nF
Transformer parameters L_l L_m	 37.5 μH 996.2 μH
C_{out}	161.5 μF
r_{batt}	60 mΩ

power level, as shown in Fig. 2.15(c). It should be emphasized that the six T-type converter modules have a combined output power of 126 kW. While testing is currently limited to 21 kW of output power, the current testing results provide valuable insights and pave the way for higher output power in the future. Moreover, as the Unfolder mainly contributes to the conduction losses, an approach utilizing a single high-power Unfolder interfaced with multiple parallel-connected T-type converter modules is employed to effectively minimize these losses by leveraging high-current, low-resistance semiconductor devices.

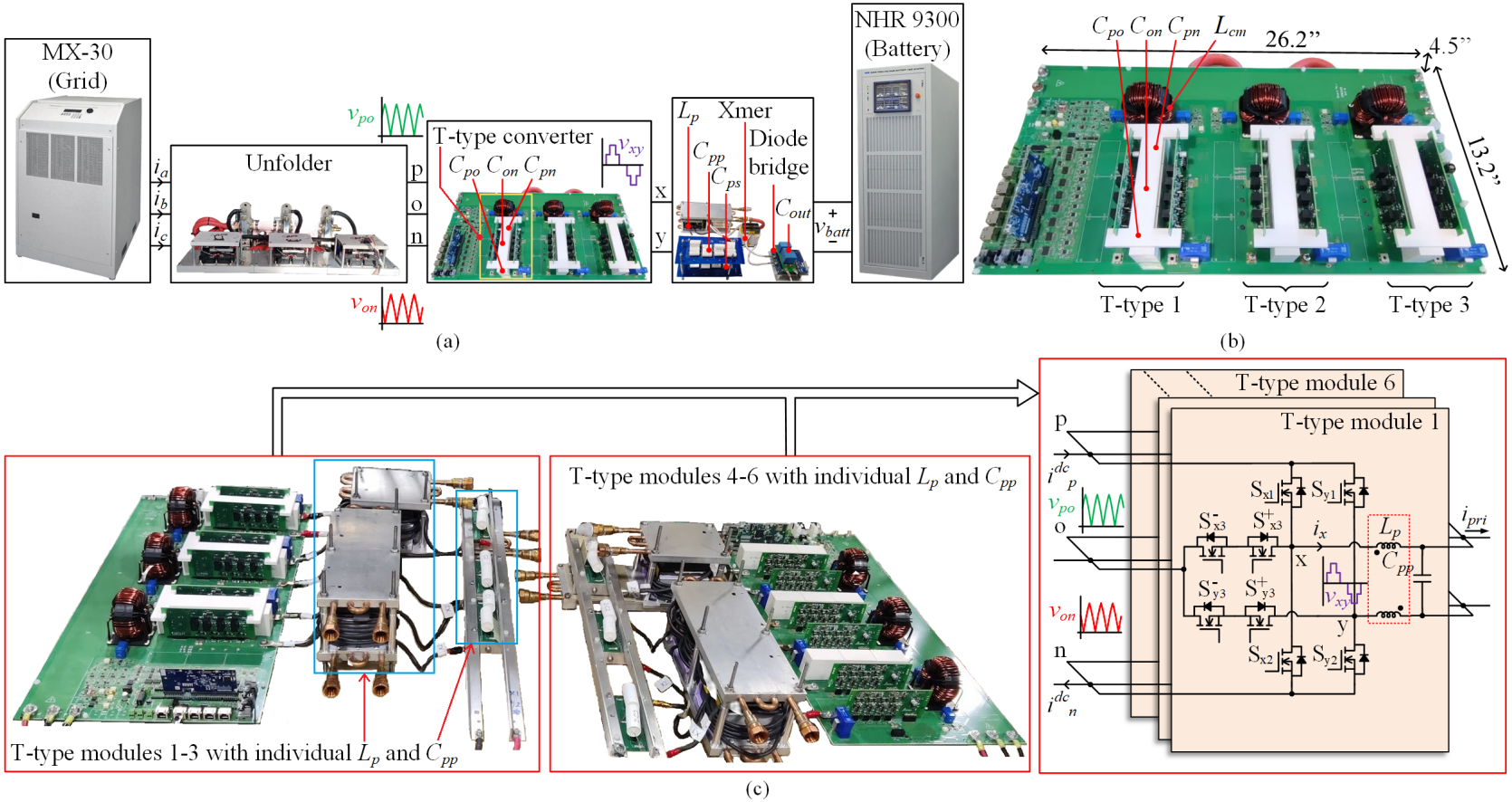


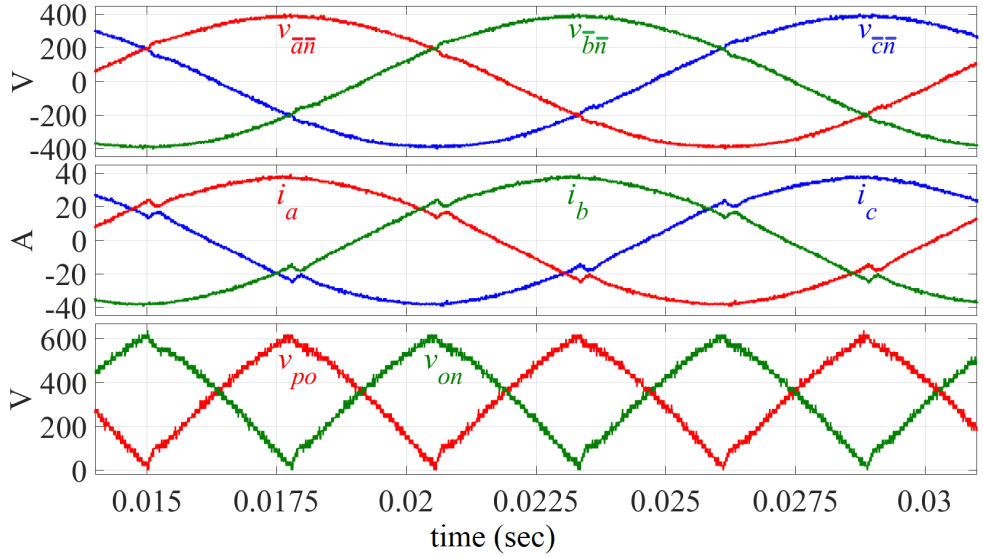
Fig. 2.15: (a) 21 kW hardware prototype of an ac-dc conversion system with a single T-type converter module, (b) a circuit board comprising of three T-type converter modules each rated for 21 kW output power with the dimensions of 26.2 in (L) × 13.2 in (W) × 4.5 in (H) (including the cold plate), and (c) hardware verification of the modular configuration with six T-type converter modules connected in parallel feeding 21 kW of output power to the battery.

2.7.1 Hardware Results

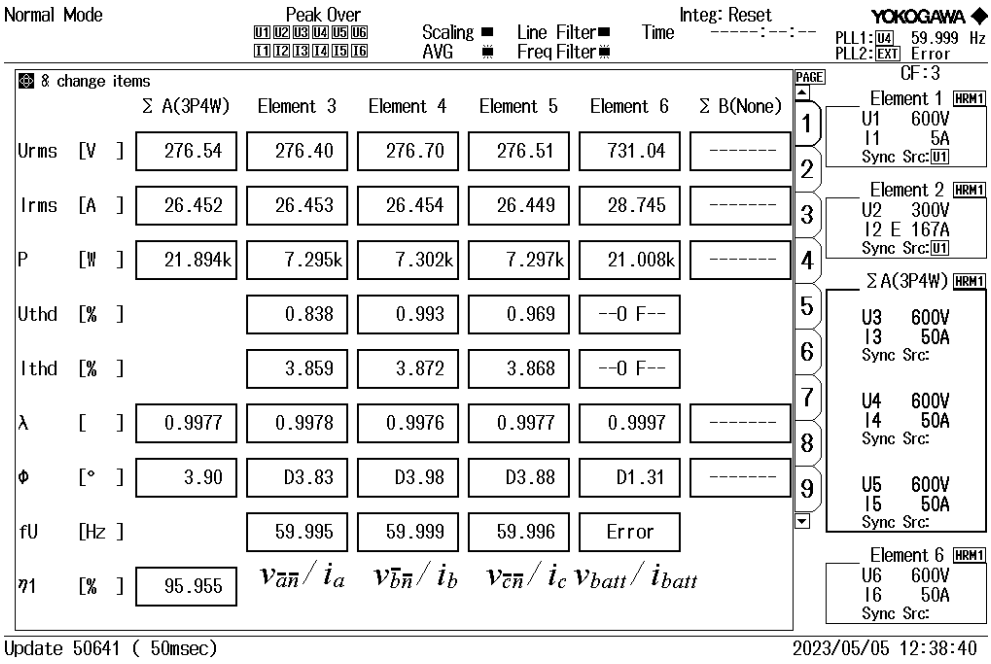
Fig. 2.16(a) presents the hardware results of the 3-ϕ grid voltages, currents, and their corresponding soft dc-link voltages of an ac-dc conversion system based on a single T-type converter module. The figure also shows that a higher THD of 3.86% is observed in the grid current, as depicted in Fig. 2.16(b). This increase in THD is caused by the periodic current distortions that occur during the sector boundaries of the grid voltage associated with each sector of the unfolding action during a line cycle. The HF operation of the T-type converter gives rise to the HF currents, which are bypassed by the soft dc-link capacitors. These currents lead to HF ripples in the soft dc-link voltages which cause undesirable turn-on of the Unfolder diodes, mainly leading to this phenomenon. A detailed analysis of these distortions and their mitigation technique can be found in Chapter 4 and [68]. The distortion mitigation technique has resulted in improved grid currents, as shown in Fig. 2.17(a), with a lower current THD of 1.27% given in Fig. 2.17(b). Fig. 2.18 illustrates the output voltage of the T-type converter and the battery current when supplying 21 kW of power to the battery. The T-type converter's output voltage exhibits a six-pulse waveform but, its fundamental magnitude is consistently maintained by regulating the widths of the T-type converter's duty ratios, d_p and d_n. This control method ensures appropriate output power regulation. Fig. 2.19 shows the variation in the grid current THD as the output power changes. Consistent with expectations, a decrease in power level correlates with an increase in THD.

Figs. 2.20 and 2.21 present the transient response analysis of the controller in relation to dynamic load and grid voltage variations. Fig. 2.20 demonstrates the controller's response in effectively adjusting the battery current to accommodate a 20% step change in output power, transitioning from 17.5 kW to 21 kW. Furthermore, as depicted in Fig. 2.21, the controller regulates the battery current when the grid phase voltage experiences a 10.8% increase from 250 V to 277 V.

The waveforms of the T-type converter's output voltage and current are displayed in greater detail in Fig. 2.22. It is evident from Fig. 2.22(a) that when d_p exceeds d_n by a



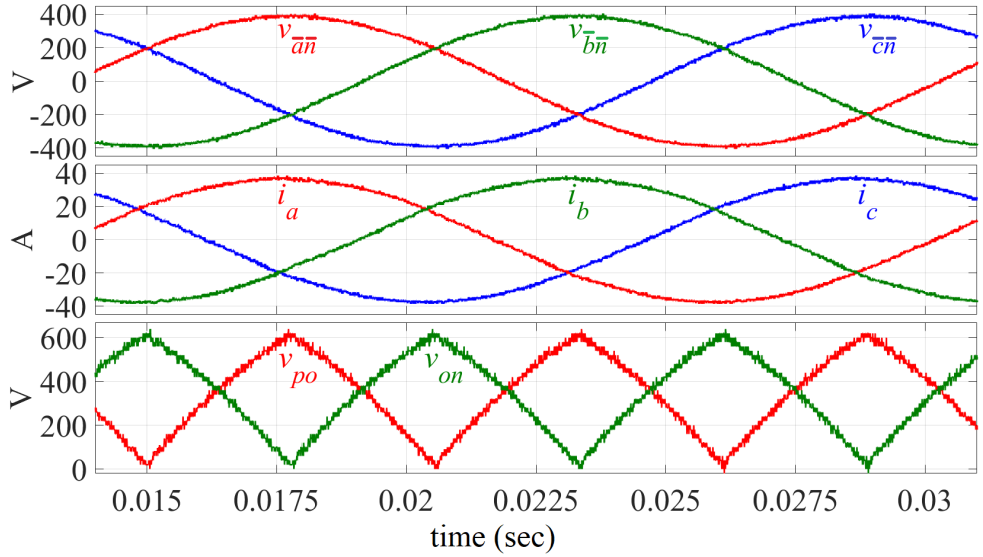
(a)



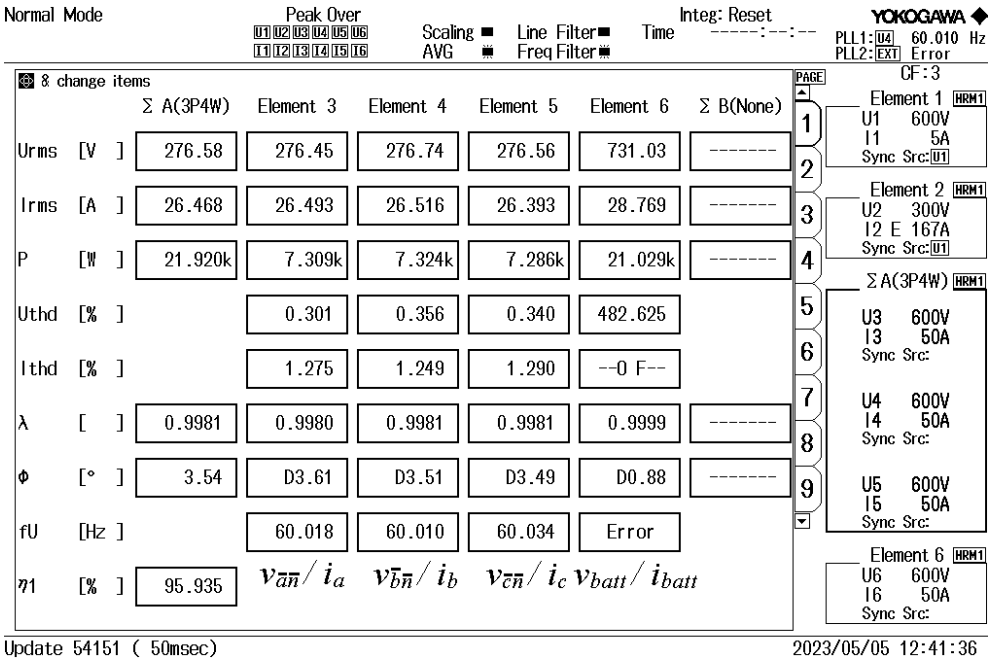
(b)

Fig. 2.16: Experimental results showing (a) grid voltages, currents, and soft dc-link voltages and (b) a higher grid current THD of 3.86% measured with Yokogawa WT1806E power analyzer at 21 kW of output power caused by the presence of periodic distortions in the grid currents. An ac-dc efficiency of 95.95% is achieved.

significant amount, or vice versa, the MOSFETs during the first, third leading edges and all trailing edges undergo ZVS as discussed earlier, while the second and fourth leading



(a)



(b)

Fig. 2.17: Experimental results showing (a) grid voltages, improved currents, and pulsating soft dc-link voltages and (b) a lower grid current THD of 1.27% measured with the power analyzer at 21 kW of output power attributed to the application of control-based current distortion mitigation logic. An ac-dc efficiency of 95.94% is achieved.

edges are hard-switched at higher current levels. When d_p is closer to d_n, as depicted in Fig. 2.22(b), all the leading edges are hard-switched, while all trailing edges are soft-

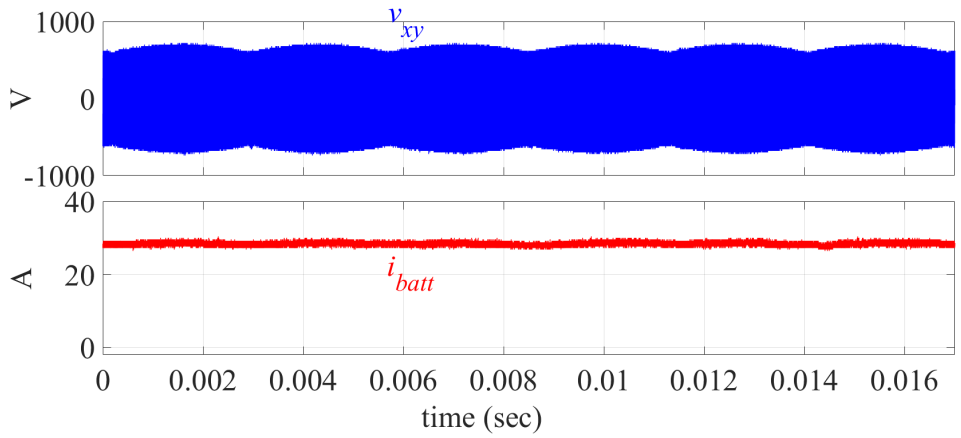


Fig. 2.18: Experimental results of the T-type converter's output voltage and battery current at 21 kW of output power. The output voltage has a six-pulse waveform, but the magnitude of its fundamental is maintained by controlling the duty ratios of the converter. This ensures that the battery current is regulated as shown.

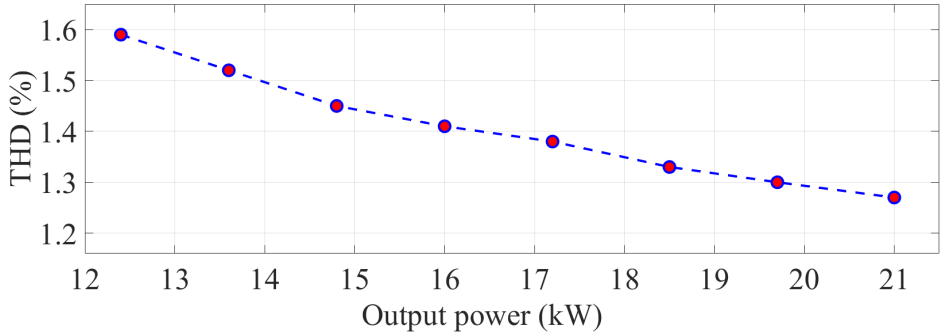


Fig. 2.19: The variation in the grid current THD is measured experimentally at different output power levels using a single T-type converter module. A minimum THD of 1.27% is observed at a rated power of 21 kW.

switched. Thus, the proposed topology is capable of achieving soft-switching over a significant portion of the grid cycle at higher modulation indices when d_p and d_n can attain higher values. This phenomenon is illustrated in Figs. 2.23 and 2.24, which show the increase in the T-type converter's contribution to the overall system losses as the power level drops from 21 kW to 12.4 kW by reducing the modulation index. The rise in this contribution to overall losses is caused by the increase in switching losses when the power level is brought down. Meanwhile, the contribution of other system components to overall losses decreases as the power level decreases. Fig. 2.25 displays the efficiency characteristics of the proposed ac-dc conversion system utilizing a single T-type converter module. The system attains a

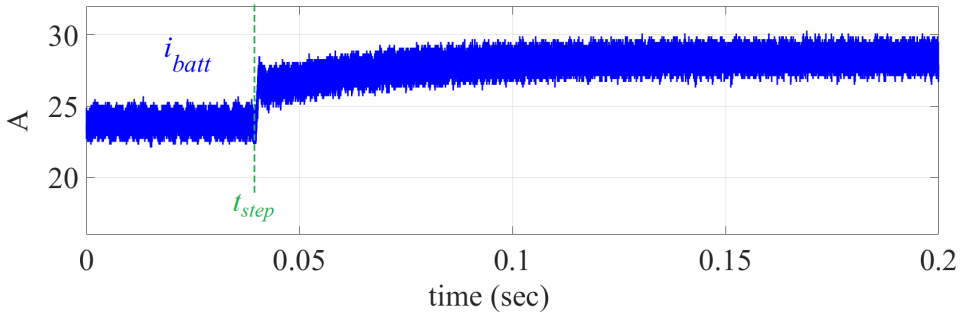


Fig. 2.20: An experimental step change in the load is given from 17.5 kW to 21 kW (20% rise) by changing the battery current (i_{batt}) from 24 A to 28.6 A. The controller exhibits its capability to accurately track the battery current, highlighting its proficiency in effectively managing transient load variations.

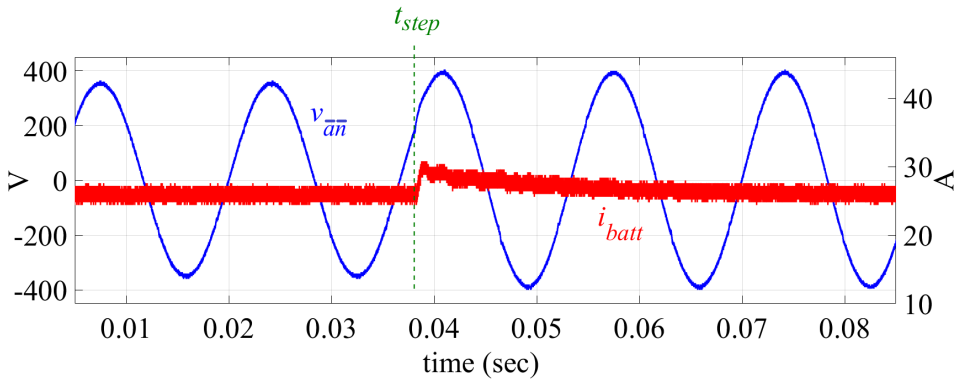


Fig. 2.21: Experimental results upon subjecting the grid voltage ($v_{\bar{a}\bar{n}}$) to a step change of 10.8% from 250 V to 277 V. The controller maintains the battery current (i_{batt}) while ensuring an acceptable response time.

full-load ac-dc efficiency of 95.94%, while delivering 94% efficiency at 59% load (12.4 kW).

Fig. 2.24 shows some differences between the analytical and experimental T-type converter losses. Mainly two factors contribute to this inconsistency. Firstly, the energy loss measurements provided in the datasheet are typically acquired using a two-level half-bridge double pulse tester [69], which introduces errors when calculating losses for the multi-level T-type converter. To accurately determine energy loss, it is imperative to directly record switching transients with the T-type converter across various commutation voltages, currents, and temperatures [70]. Secondly, the turn-off of the MOSFETs during the soft-switched transitions is considered completely lossless, which may not be the case in the actual hardware, as it depends upon the turn-off time of the MOSFETs [58]. However, de-

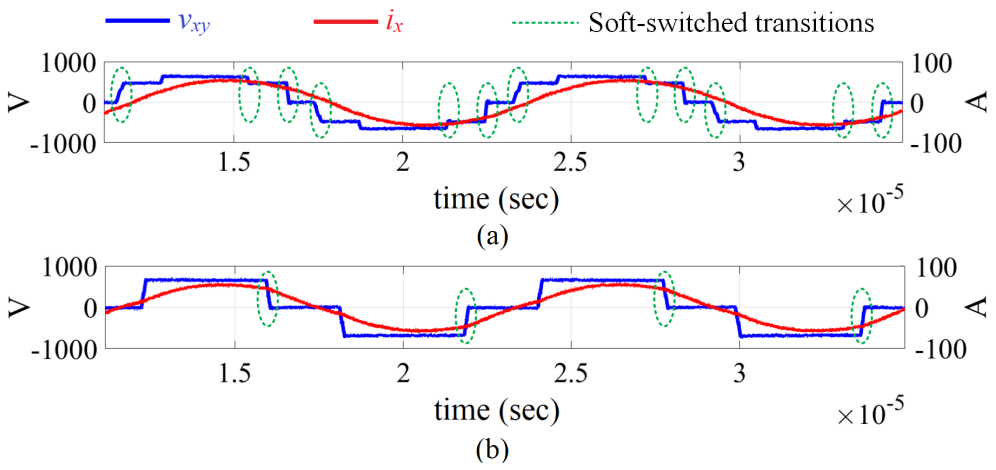


Fig. 2.22: A detailed view of the T-type converter's experimental output voltage and current at two operating conditions. (a) At the first condition, d_p is much higher than d_n, which facilitates ZVS of the MOSFETs during the first and third leading edges. A similar phenomenon can be observed when d_n is much higher than d_p. (b) At the second operating condition, d_p equals d_n, resulting in a three-level waveform with hard-switched leading edges. The trailing edges in both operating conditions always exhibit ZVS.

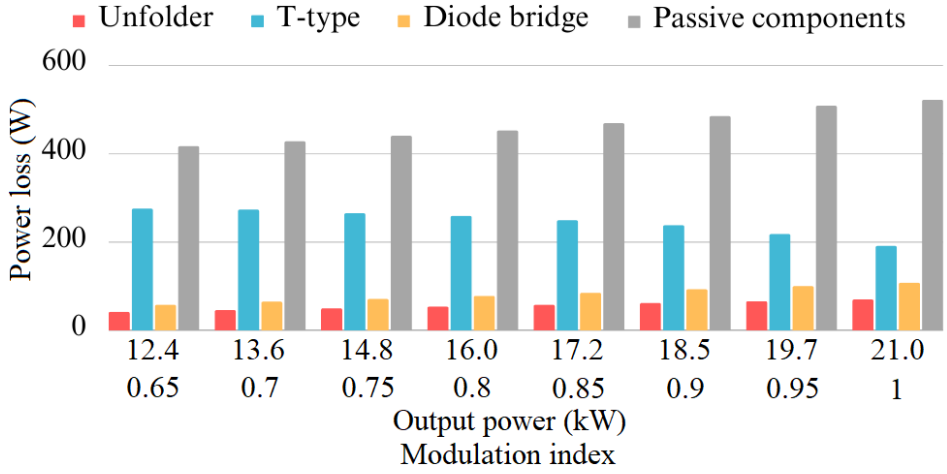


Fig. 2.23: The loss distribution of the ac-dc conversion system with a single T-type converter module.

spite the observed discrepancy in loss values, the analytical loss calculation offers valuable insights into the anticipated losses during experimentation, enabling informed selection of MOSFETs.

Figs. 2.26 and 2.27 depict the results obtained from a paralleling test of six T-type converter modules. To restrict output power to 21 kW at the moment, the experiment

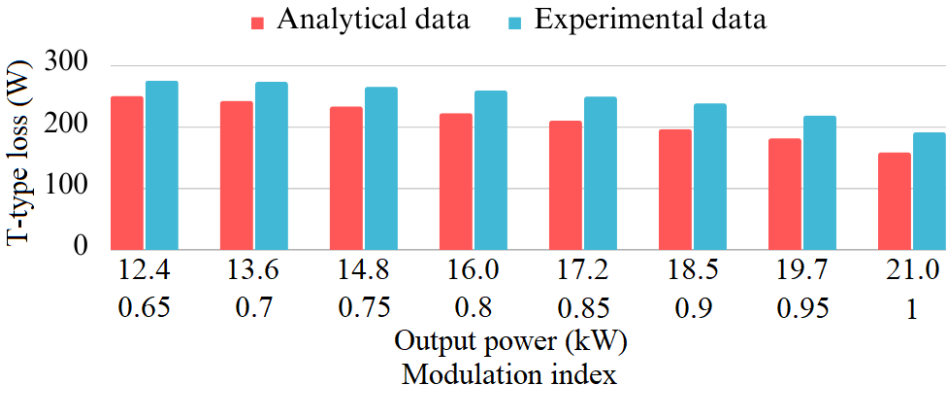


Fig. 2.24: Analytical and experimental power losses of the T-type converter.

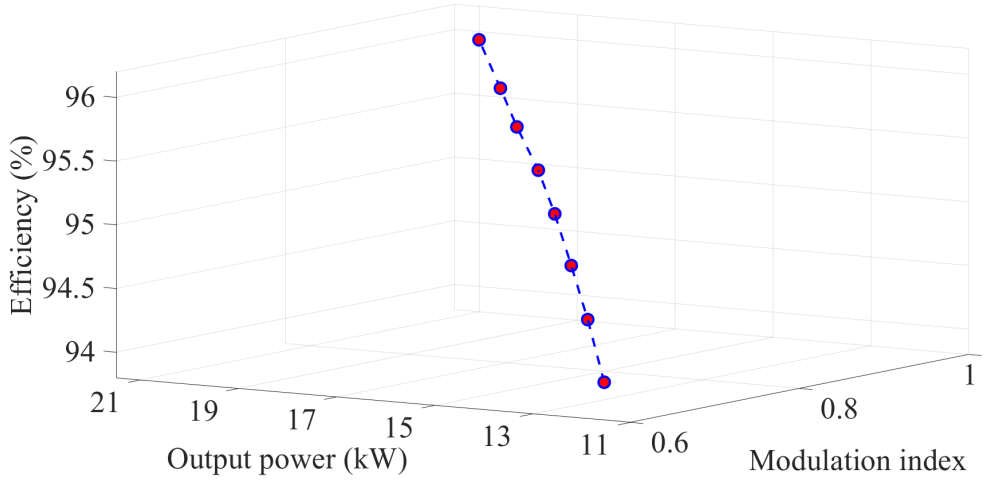


Fig. 2.25: An efficiency curve for the ac-dc conversion system using a single T-type converter module is obtained through experimentation. A peak efficiency of 95.94% is achieved at 21 kW of output power.

is conducted at a reduced grid voltage of 330 V (line-line) as shown in Fig. 2.26(a). The output voltages and currents of all six T-type converters are shown in Fig. 2.26(b). The modules exhibit nearly equal power-sharing with a maximum deviation below 1%. The slight variations in tank inductance L_p primarily contribute to this deviation. The experiment reveals a grid current THD of 4.1% and an ac-dc efficiency of 94%, as shown in Fig. 2.27. However, the efficiency achieved is lower than the full load efficiency of the ac-dc conversion system with a single T-type module, due to higher switching losses. This is because all six modules operate at a lower power of 3.5 kW each in this test.

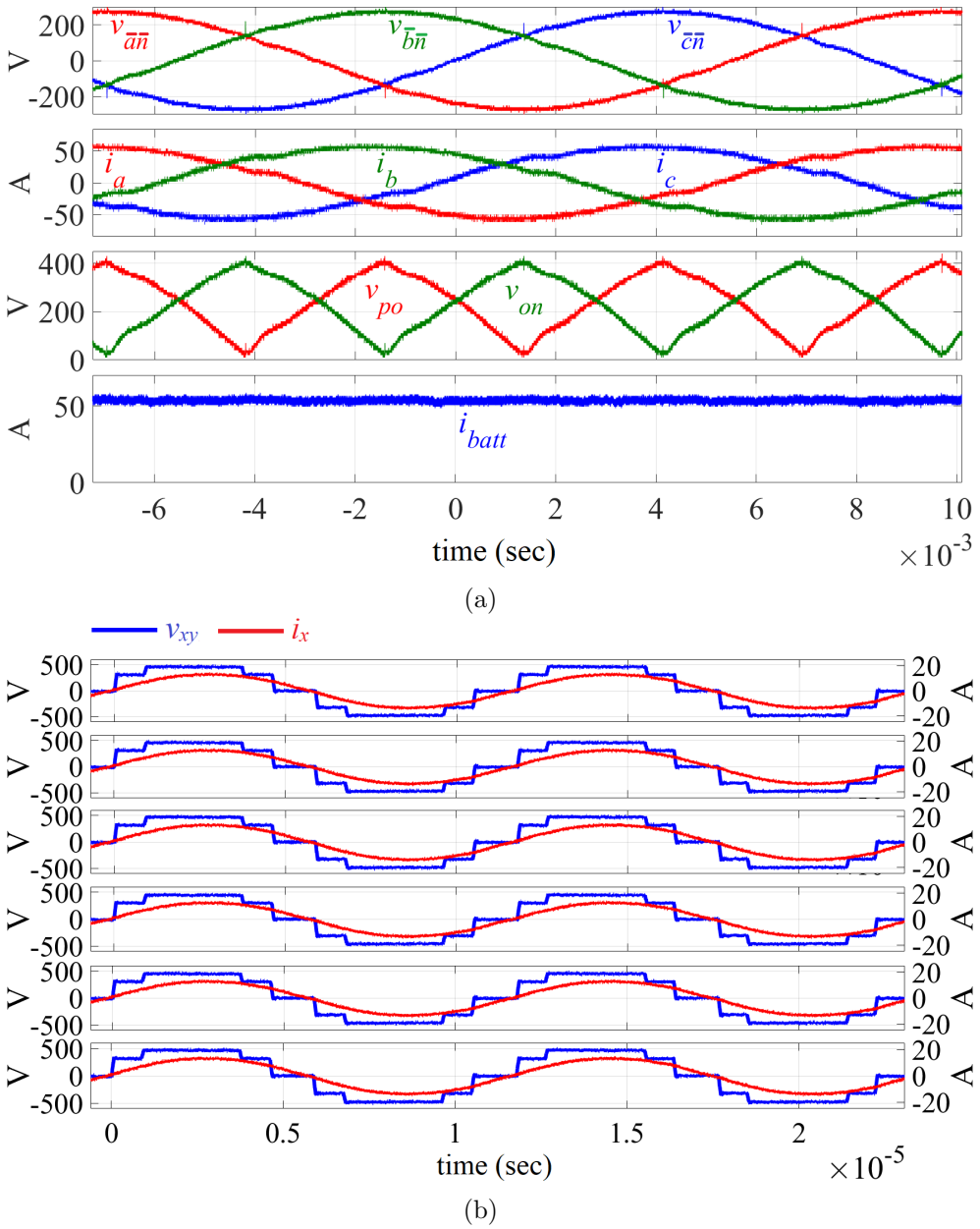


Fig. 2.26: Experimental results showing (a) grid voltages, currents, soft dc-link voltages, and battery current when six T-type converter modules are tested together in a parallel configuration and (b) T-type output voltages and currents sharing approximately equal power of 3.5 kW each.

2.7.2 Analysis and Mitigation of the Incorrect Switching Pattern for $d_p = d_n$

In the context of the TMDSCNCD28379D microcontroller, the PWM peripheral generates two complementary PWM signals with the necessary dead band [71]. These PWM

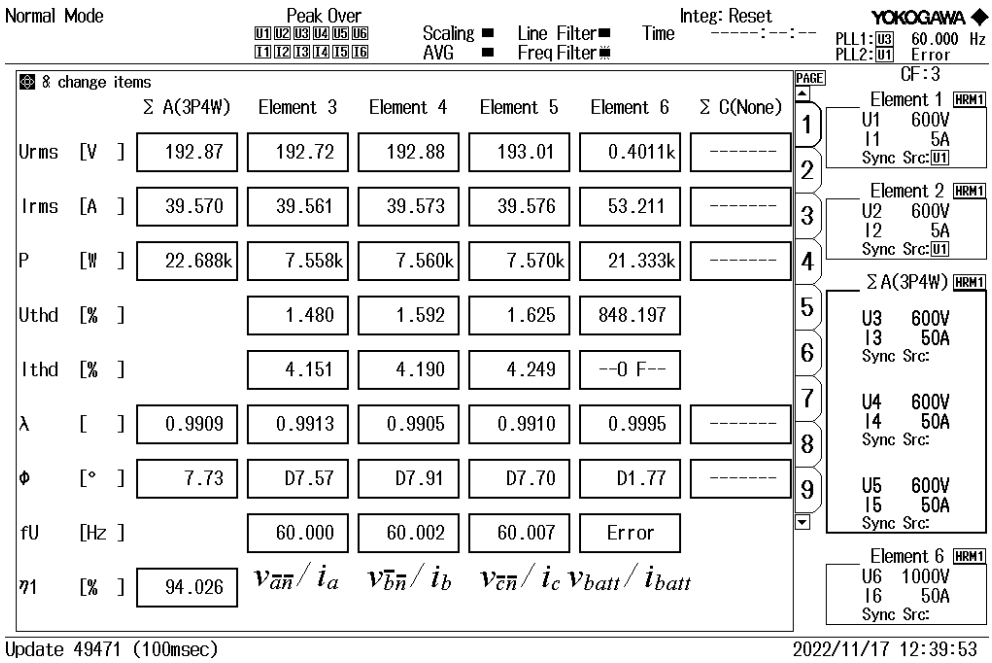


Fig. 2.27: Paralleling testing results with a grid current THD of 4.1% measured using Yokogawa WT1806E power analyzer. An ac-dc efficiency of 94% is achieved. To limit the output power to 21 kW, testing is done with a lower 330 V grid voltage (line-line) and 400 V battery voltage.

signals are used to drive four pairs of MOSFETs in a T-type converter: (i) S_{x1}, S^{+}_{x3}, (ii) S_{x2}, S^{-}_{x3}, (iii) S_{y1}, S^{+}_{y3}, and (iv) S_{y2}, S^{-}_{y3}. The switching patterns for these MOSFETs, as shown in Figs. 2.4 and 2.5, are generated using two modulating signals per MOSFET pair (eight modulating signals in total) which are functions of d_p and d_n, and are compared with the carrier signal generated by the microcontroller. For example, as shown in Figs. 2.28 and 2.29, in the case of the third pair, S_{y1} and S^{+}_{y3}, when the modulating signal $MS^{\uparrow}_{iii}$ is equal to the carrier signal, the PWM signal for S_{y1} is switched high while the PWM signal for S^{+}_{y3} is switched low. Conversely, when the modulating signal $MS^{\downarrow}_{iii}$ is equal to the carrier signal, the PWM signal for S_{y1} is switched low while the PWM signal for S^{+}_{y3} is switched high. Similar comparisons between modulating signals and the carrier signal are made for the other MOSFET pairs to determine the corresponding high or low switching of PWM signals.

Now, two different scenarios are being considered for analysis: (a) carrier starting from

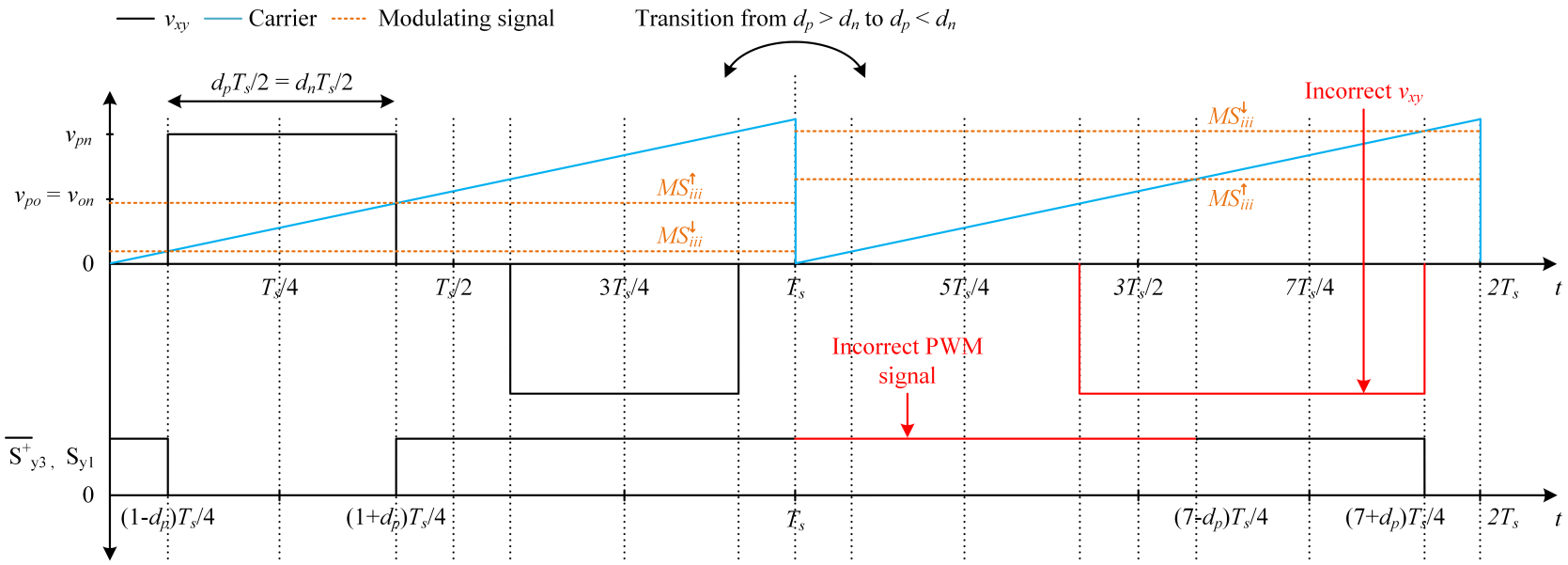


Fig. 2.28: Switching patterns of the T-type converter's MOSFET pair S_{y1} and S^{+}_{y3} when d_p is equal to d_n. Incorrect switching pattern during the transition from $d_p > d_n$ to $d_p < d_n$ when the carrier is aligned in such a way that its zero crossing occurs at $t = 0$ which leads to inaccurate voltage v_{xy}.

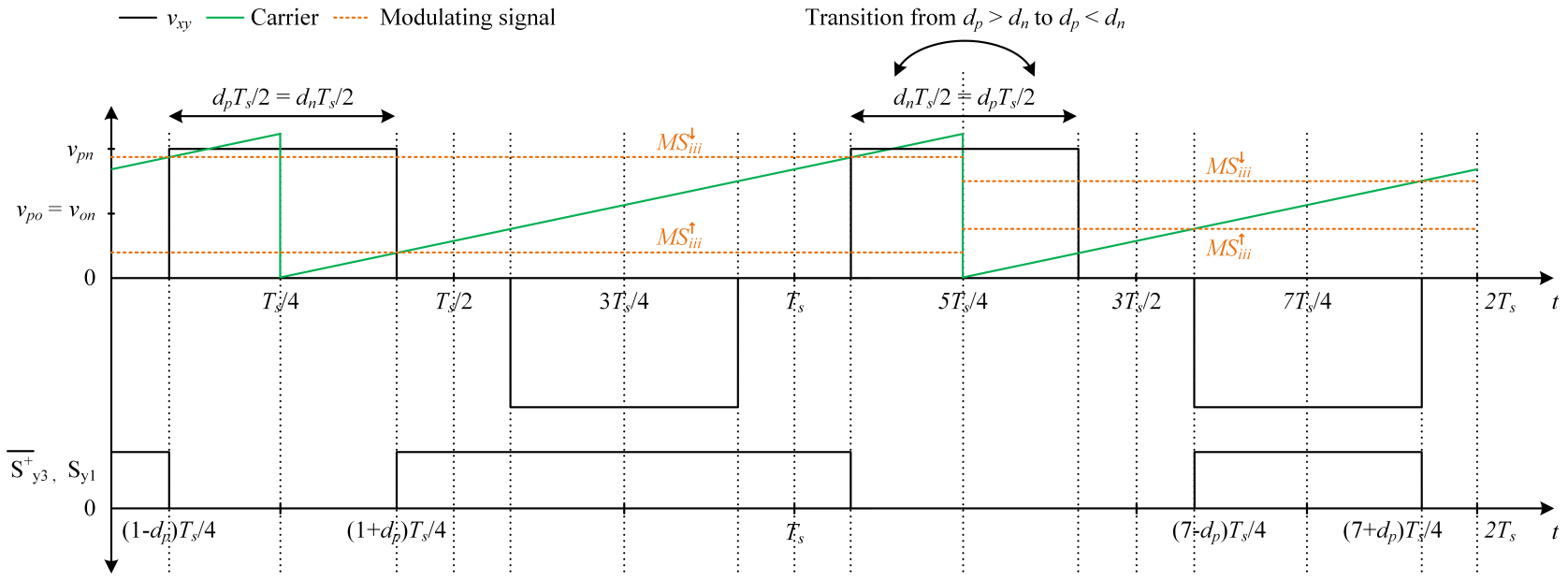


Fig. 2.29: Switching patterns of the T-type converter's MOSFET pair S_{y1} and S^+_{y3} when d_p is equal to d_n. Correct switching pattern during the transition from $d_p > d_n$ to $d_p < d_n$ when the carrier is aligned such that its zero crossing is lagging by 90°, occurring at $t = {}^{T_s}/_4$.

$t = 0$ of the switching period, as depicted in Fig. 2.28, and (b) carrier starting from $t = {}^{T_s}/_4$ of the switching period, as shown in Fig. 2.29. In scenario (a), during the transition of the switching pattern from $d_p > d_n$ to $d_p < d_n$, it is observed that MOSFET S_{y1} remains turned on at the beginning of the next switching period, which is not the desired behavior as S_{y1} should have been turned off at the start of the switching period when $d_p < d_n$, as illustrated in Fig. 2.28. As a result, S_{y1} remains turned on for a longer duration, and S^+_{y3} remains turned off for a longer duration than intended. Similar inaccuracies in switching patterns can also be observed for other pairs of MOSFETs during the transition. These inaccuracies result in an erroneous output voltage v_{xy} for the T-type converter.

On the contrary, in scenario (b), where the switching pattern transitions from $d_p > d_n$ to $d_p < d_n$, as illustrated in Fig. 2.29, the MOSFET S_{y1} remains turned off and S^+_{y3} remains turned on as intended, as the transition occurs at $t = {}^{5T_s}/_4$. Similarly, the switching patterns for other pairs of MOSFETs are also accurate in this scenario when the carrier is shifted by 90°. This ensures that the waveshape of the voltage v_{xy} remains correct. Thus, by aligning the carrier in such a manner that its zero crossing occurs at the time when the PWM signals for all the MOSFETs remain the same just before and after the transition from $d_p > d_n$ to $d_p < d_n$ and $d_p < d_n$ to $d_p > d_n$, erroneous switching patterns and incorrect T-type output voltage during these transitions can be avoided.

2.7.3 Comparison with the Conventional Two-Stage Topology

A detailed comparative analysis is conducted between the proposed single-stage topology and the conventional two-stage configuration, which comprises a grid-tied AFE followed by a dc-dc converter. The dc-dc converter utilizes an active H-bridge on the primary side and a diode bridge rectifier on the secondary side. To perform the comparison, a case study is carried out at the same output power level of $P_{out} = 21$ kW, with input and output voltages of $V_{gm} = 480\sqrt{2}$ V and $V_{batt} = 730$ V, respectively. The AFE converter is switched at 100 kHz with an appropriate inductive filter to match the grid current THD with the single-stage topology. An HF grid-tied converter designed in [32] is considered for reference. The AFE is controlled using space vector PWM, while the H-bridge is operated at

Table 2.6: Comparison between the proposed unfolding-based single-stage and conventional two-stage topologies (V_{gm} - peak line-line grid voltage, P_{out} - output power, and ω_g - angular grid frequency).

Component	**Parameter**	**Scaling factor**	**Conventional two-stage (AFE+H-bridge)**	**Proposed single-stage (Unfolder+T-type)**
AFE/Unfolder	Semiconductor device count	-	6	12
	Voltage stress	V_{gm}	1.18	1, 0.433
	Current stress (rms)	P_{out}/V_{gm}	0.216, 0.535	0.56, 0.139
H-bridge/T-type	Semiconductor device count	-	4	8
	Voltage stress	V_{gm}	1.18	1, 0.866
	Current stress (average rms)	P_{out}/V_{gm}	0.693	0.89, 0.4
Grid-side inductive filter	Value (mH)	$V_{gm}^2/(\omega_g P_{out})$	10.31	0
Dc/soft-dc link capacitor	Value (mF)	$P_{out}/(\omega_g V_{gm}^2)$	827.23	3×20.68

a maximum modulation index with square wave pulses to achieve complete soft-switched transitions. Table 2.6 provides the comparison between the two topologies in terms of the device count, voltage and current stresses, and filter requirements. It can be observed that the proposed topology provides a significant reduction in the demand for inductive and capacitive filtering in the conversion process at the cost of more semiconductor devices.

Table 2.7 presents a comparison of analytical power losses between the two topologies calculated using (2.25)-(2.29) and [33]. As the 1 MW rated Unfolder used in this work benefits from reduced conduction losses due to the use of higher current devices, a 21 kW Unfolder with lower current diodes and IGBTs is considered for the purpose of unbiased

Table 2.7: Loss comparison between the proposed single-stage and conventional two-stage topologies (P_{out} - output power).

Component	**Parameter**	**Scaling factor**	**Conventional two-stage (AFE+H-bridge)**	**Proposed single-stage (Unfolder+T-type)**
AFE/Unfolder	Conduction losses	$P_{out}/100$	0.95	0.62
	Switching losses	$P_{out}/100$	0.97	0
H-bridge/T-type	Conduction losses	$P_{out}/100$	0.47	0.61
	Switching losses	$P_{out}/100$	0	0.14
-	Total power losses	$P_{out}/100$	2.39	1.37

power loss comparison. The conventional H-bridge demonstrates higher efficiency compared to the T-type converter due to its lower switch count, resulting in reduced conduction losses. Furthermore, the H-bridge has the advantage of a complete soft-switching capability. However, the Unfolder in the proposed topology exhibits significant power loss reduction when compared to the AFE converter, mainly due to its negligible switching losses. Consequently, the proposed topology showcases better efficiency in the overall conversion process. Moreover, the efficiency of the proposed unfolding-based topology can be improved further by minimizing the switching losses of the T-type converter, as discussed in Chapter 3.

2.8 Conclusion

The utilization of a single-stage ac-dc converter has the potential to enhance the efficiency and power density of WPT systems for battery charging applications. This chapter presents a single-stage topology and control scheme for an ac-dc conversion system that employs a 3-ϕ Unfolder and a T-type converter. The proposed topology eliminates the need for an input inductive filter as the grid inductance is sufficient for PFC. The T-type converter is capable of handling pulsating dc input voltages, resulting in a smaller capacitive soft dc-link filter. These advantages contribute to a high power-dense and efficient ac-dc

conversion system compared to the conventional two-stage approach. A mathematical analysis of the modulation strategy that takes into account the reactive power of the soft dc-link capacitors is presented which also gives the benefit of performing PFC without any current sensors. Small-signal modeling of the conversion system for the proper regulation of the output power is discussed and comprehensive design guidelines are presented, accompanied by analytical loss equations, to facilitate the selection and optimization of various components within the topology. Hardware results of a 21 kW prototype with a single T-type converter module demonstrate an ac-dc efficiency of 95.94% from the grid to the battery and a grid current THD of 1.27%. The modular structure of the proposed system allows for efficient power scalability. In addition, the modular nature of the system is exemplified through the parallel operation of six T-type converter modules.

In summary, the analysis and results indicate that the proposed system is capable of achieving high efficiency, high power density, low grid current THD, and appropriate output power regulation, making it suitable for wireless charging applications. Furthermore, the proposed modular architecture can be used to achieve power-level scalability, making it a versatile solution for a wide range of applications.

CHAPTER 3

MODULATION, CONTROL, AND TANK DESIGN FOR ZVS OF THE T-TYPE BRIDGE IN AN UNFOLDING-BASED TOPOLOGY

3.1 Introduction

This chapter focuses on ZVS of the resonant T-type bridge in an unfolding-based ac-dc conversion system shown in Fig. 3.1. As the Unfolder operates at a low switching frequency in open loop, it cannot perform any control tasks. Furthermore, since a passive diode bridge rectifier is employed on the secondary side of the isolation, control parameters such as the phase shift between the primary and secondary bridges and the duty cycle of the secondary bridge are not available. In this scenario, all key control tasks, including grid-side sinusoidal current shaping for PFC and output power regulation, must be handled entirely by the HF switched T-type bridge. Since the T-type bridge is operated at HF, achieving ZVS of the MOSFETs is essential to minimize switching losses and EMI. Managing all control requirements while maintaining ZVS, therefore, becomes a significant challenge. This chapter proposes a modulation strategy with closed-loop control and an appropriately designed resonant tank, guided by accurate ZVS analysis that accounts for the nonlinear behavior of MOSFET output capacitance, to simultaneously accomplish these control tasks and ensure ZVS of the MOSFETs throughout the grid cycle.

The T-type bridge, which is a series combination of two H-bridges, is modulated using two duty ratios across the grid cycle. These duty ratios generate two quasi-square voltages at the T-type bridge output, and their relative alignment critically determines whether the MOSFETs achieve ZVS. In Chapter 2 and [12, 23], center-aligned modulation is used, which results in the T-type bridge output voltage waveform shown in Fig. 3.2(a). As detailed in Chapter 2, center-aligned modulation simplifies control by allowing analytical derivation of the duty ratios. However, as shown in Fig. 3.2(a) and discussed in Chapter 2, the

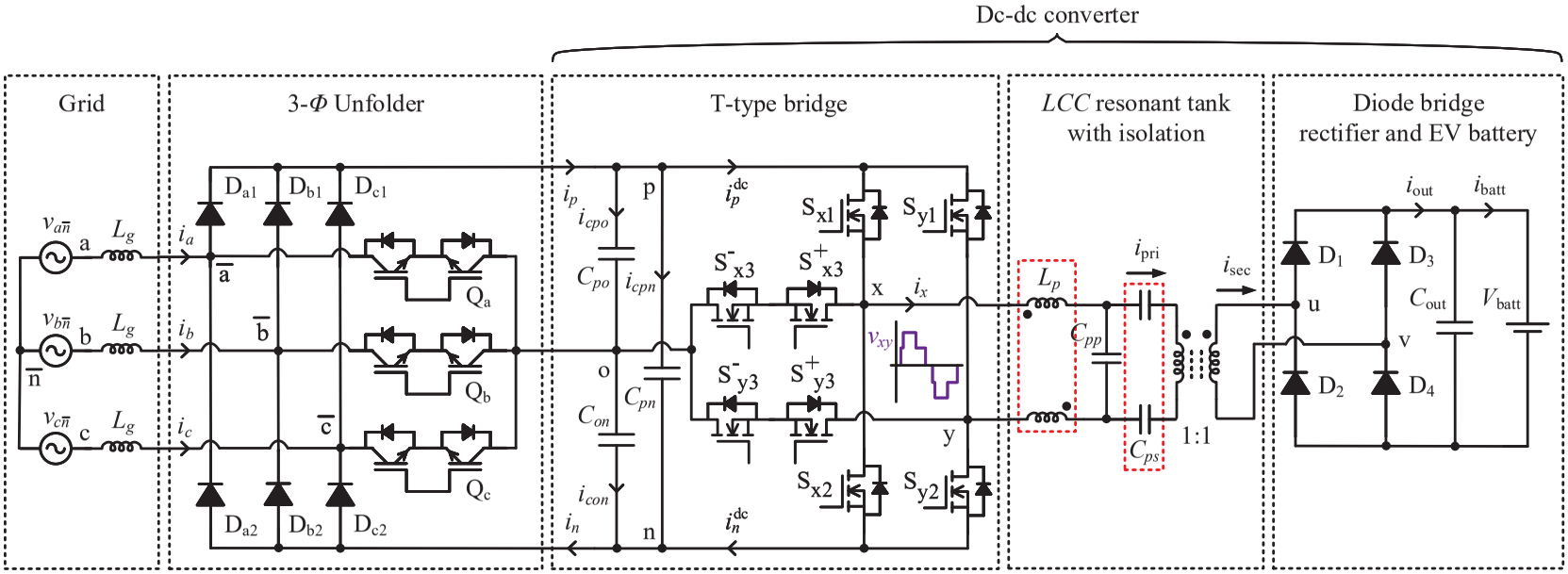


Fig. 3.1: Circuit schematic of the unfolding-based ac-dc system with a T-type primary bridge-based dc-dc converter, consisting of an *LCC* resonant tank and a secondary-side diode bridge rectifier connected to an EV battery load.

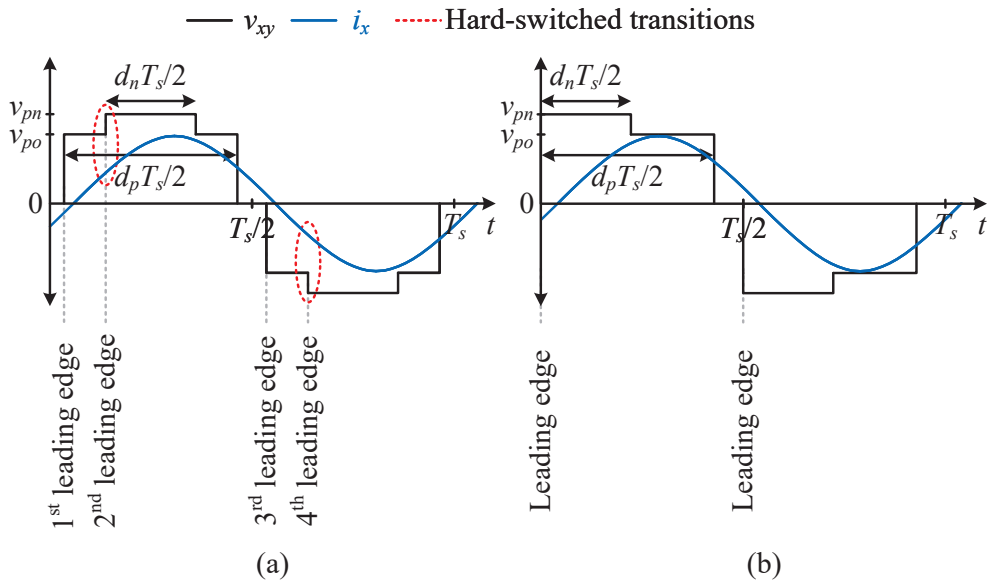


Fig. 3.2: T-type bridge output voltage, v_{xy}, and current, i_x, when controlled using (a) center-aligned modulation and (b) leading-edge-aligned modulation.

second and fourth leading edges, highlighted in red, consistently encounter hard-switching due to incorrect tank current polarity. Additionally, the first and third leading edges may also face hard-switching when the duty ratio reduces at certain grid angles. This hard-switching behavior leads to increased switching losses and higher radiated EMI, both of which are undesirable in HF converters. To address these limitations and ensure ZVS of the MOSFETs throughout the grid cycle, the leading-edge-aligned modulation aligns the leading edges of the two quasi-square voltages to maintain correct tank current polarity and sufficient magnitude at the switching transitions, as shown in Fig. 3.2(b) [24, 26–30].

In [28], leading-edge-aligned modulation is used with phase-shift control between the primary and secondary active bridges for output power regulation and adjustment of the ratio of the T-type bridge input currents to shape sinusoidal grid currents. However, these strategies are not applicable in this study. The proposed ac-dc converter is designed for WPT applications, where a passive diode bridge rectifier on the secondary side is used due to isolation requirements, making phase-shift control infeasible. Furthermore, input current ratio control does not facilitate output power regulation in the proposed configuration. A ZVS analysis is also not provided in this previous work. In [24], leading-edge-aligned modulation

is implemented using analytically derived feedforward duty ratios, without closed-loop regulation of the T-type bridge input currents that shape the grid currents. While this simplifies implementation, it results in poor dynamic regulation of the grid currents and increased sensitivity to variations in grid voltages and load conditions. The study also employs an active secondary bridge with phase-shift control to achieve ZVS, which is unsuitable for this work, as a passive diode bridge is used on the secondary side. Furthermore, the ZVS analysis in [24] is incomplete, as it considers only the polarity of the tank current while neglecting the required current magnitude calculation necessary to ensure reliable ZVS. In [26], the T-type bridge is also operated with leading-edge-aligned modulation based on analytically derived feedforward duty ratios, without closed-loop regulation of the input currents that shape the grid currents. This results in relatively high grid current distortion, with THD of about 5% at rated power. Furthermore, the ZVS analysis neglects the nonlinear behavior of the MOSFET output capacitance, reducing the accuracy of the prediction. In [27], the T-type bridge is controlled with a leading-edge-aligned modulation strategy combined with hybrid frequency control (40–200 kHz). This approach, however, is not applicable to the proposed ac-dc converter in this work, which is designed for WPT applications where the dc-dc converter switching frequency is constrained to 81.39–90 kHz (typically fixed at 85 kHz) [52]. Moreover, both [26] and [27], discussed above, use an inductor between the primary and secondary bridges of the dc-dc converter for power transfer. However, this approach is not suitable for the WPT application considered in this work, as it requires a higher-order resonant tank, such as an LCC tank [48, 49], thereby introducing additional challenges in ZVS analysis.

It should also be noted that, to achieve complete ZVS of all T-type bridge MOSFETs, the leading edges of the two quasi-square output voltages must have a time delay on the order of the dead time and should not be perfectly aligned. This phenomenon is analyzed in detail in this study, but has been overlooked in the prior works discussed above [24, 26–28]. While [29, 30] address the ZVS operation of the T-type bridge using leading-edge-aligned modulation, key aspects such as the overall ac-dc converter operation, duty ratio calculation,

closed-loop control implementation, small-signal modeling, and tank component selection based on ZVS remain unaddressed. In response to the limitations identified in prior works, this study presents a comprehensive study of an unfolding-based ac-dc system incorporating a T-type bridge-based dc-dc converter operated with leading-edge-aligned modulation to achieve ZVS of the MOSFETs. A closed-loop control architecture is developed to simultaneously realize grid-side PFC and output power regulation, and small-signal modeling is presented to ensure robust dynamic performance. Additionally, a detailed ZVS analysis is presented, taking into account the nonlinear behavior of the MOSFET output capacitance. Based on this analysis, combined with conduction loss calculations, an optimized tank component design is provided.

Moreover, the proposed leading-edge-aligned modulation and control structure are experimentally validated using a 20 kW, 480 V, 3-ϕ grid-tied ac-dc hardware prototype. The results demonstrate complete ZVS operation over the grid cycle, a peak ac-dc efficiency of 96.51%, and a low grid current THD of 2.3% at the rated output power. Additionally, the hardware results are compared with those of a center-aligned modulation strategy, which suffers from hard-switching, using the same hardware prototype. This comparison demonstrates that the proposed approach achieves 0.76% higher efficiency and a 6 dB reduction in radiated EMI.

3.2 Overview of the Circuit Configuration and Operation of the Unfolding-Based Converter

Fig. 3.1 illustrates the circuit schematic of the unfolding-based ac-dc converter employed in this work. The architecture comprises ac-side grid inductances, a conventional 3-ϕ diode bridge rectifier equipped with a third-harmonic injection network, dc-link capacitors, and a T-type bridge-based dc-dc converter. In the Unfolder circuit, the input ac phases connect to either the positive (p), negative (n), or midpoint (o) of the dc-link based on the switching sequence shown in Fig. 3.3(c). As observed in the figure, the injection network switches, Q_a, Q_b, and Q_c, operate at twice the grid frequency, while the rectifier diodes, D_{a1}, D_{a2}, D_{b1}, D_{b2}, D_{c1}, and D_{c2}, operate at the grid frequency. This switching sequence

results in time-varying Unfolder dc output voltages, v_{po} and v_{on}, as depicted in Fig. 3.3(a) and expressed as

$$v_{po}(\theta_{\text{grid}}) = \begin{cases} V_{gm}\sin\left(\theta_{\text{grid}} + \frac{2k\pi}{3}\right) & \text{for odd } k; \\ V_{gm}\sin\left(\theta_{\text{grid}} + \frac{(2k+1)\pi}{3}\right) & \text{for even } k; \end{cases} \tag{3.1}$$

and

$$v_{on}(\theta_{\text{grid}}) = \begin{cases} V_{gm}\sin\left(\theta_{\text{grid}} + \frac{2(k-1)\pi}{3}\right) & \text{for odd } k; \\ V_{gm}\sin\left(\theta_{\text{grid}} + \frac{(2k-3)\pi}{3}\right) & \text{for even } k; \end{cases} \tag{3.2}$$

where θ_{grid} is the angle of the line-to-line Unfolder input voltage $v_{\bar{a}\bar{b}}$, determined by the PLL, which varies within the range $\frac{(k-1)\pi}{3} \leq \theta_{\text{grid}} < \frac{k\pi}{3}$ for the k^{th} Unfolder sector, and V_{gm} denotes the peak value of the Unfolder's line-to-line ac input voltages. The pulsating nature of the dc-link voltages reduces the need for energy storage and, consequently, large dc-link capacitors. Instead, relatively small capacitors, C_{po}, C_{on}, and C_{pn}, are employed to bypass the HF switching current ripple introduced by the dc-dc conversion system. To interface with these two time-varying dc-link voltages, the dc-dc conversion system may consist of either two independent converters or a unified converter topology capable of processing power from both pulsating dc voltages.

This work utilizes a three-port dc-dc converter based on a T-type bridge, as shown in Fig. 3.1, to process power from the Unfolder output. The T-type bridge architecture integrates two H-bridges into a unified three-port topology, enabling efficient semiconductor utilization and allowing the use of a single HF transformer for galvanic isolation, thereby improving overall system efficiency. The T-type bridge converts the pulsating dc-link voltages into an HF five-level output voltage, v_{xy}. As the proposed ac-dc converter is designed for WPT applications, an LCC resonant tank, which is typically employed in such applications [48, 49], is used to attenuate higher-order harmonics and achieve a near-sinusoidal tank current, i_x. Moreover, the HF secondary current, i_{sec}, is rectified through a diode bridge and filtered by the output capacitor, C_{out}. The resulting rectified current, i_{batt}, is then used to charge the EV battery load. Since the Unfolder operates at a low switching

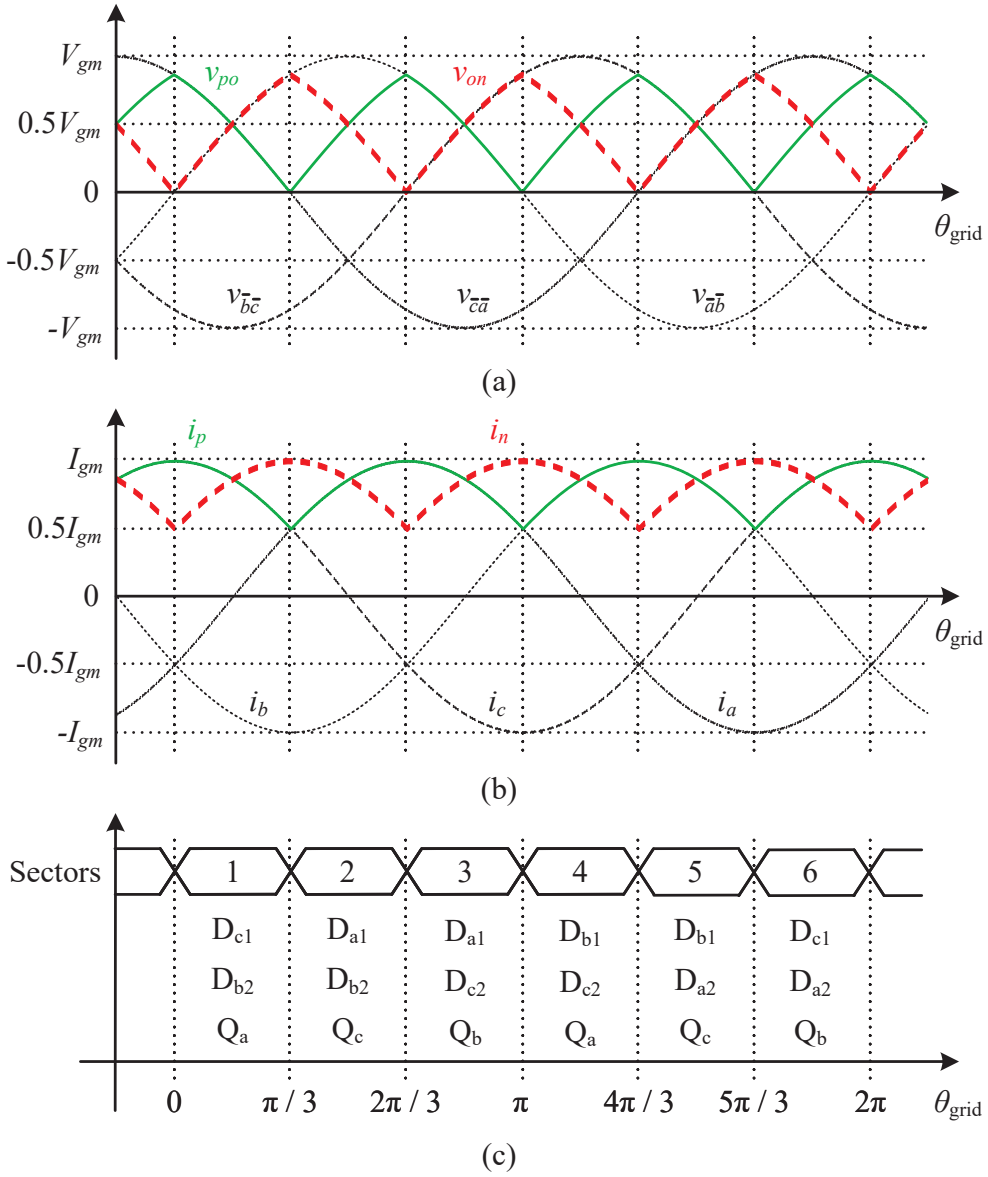


Fig. 3.3: (a) 3-ϕ ac input voltages are converted to pulsating dc-link voltages, v_{po} and v_{on}, by the Unfolder; (b) sinusoidal grid currents are shaped piece-wise by controlling the p-port and n-port output currents of the Unfolder, i_p and i_n; and (c) switching sequence of the Unfolder devices is determined based on the ac voltage sectors.

frequency, control tasks such as grid-side sinusoidal current shaping for PFC and output power regulation are handled through the closed-loop control of the T-type bridge-based dc-dc converter.

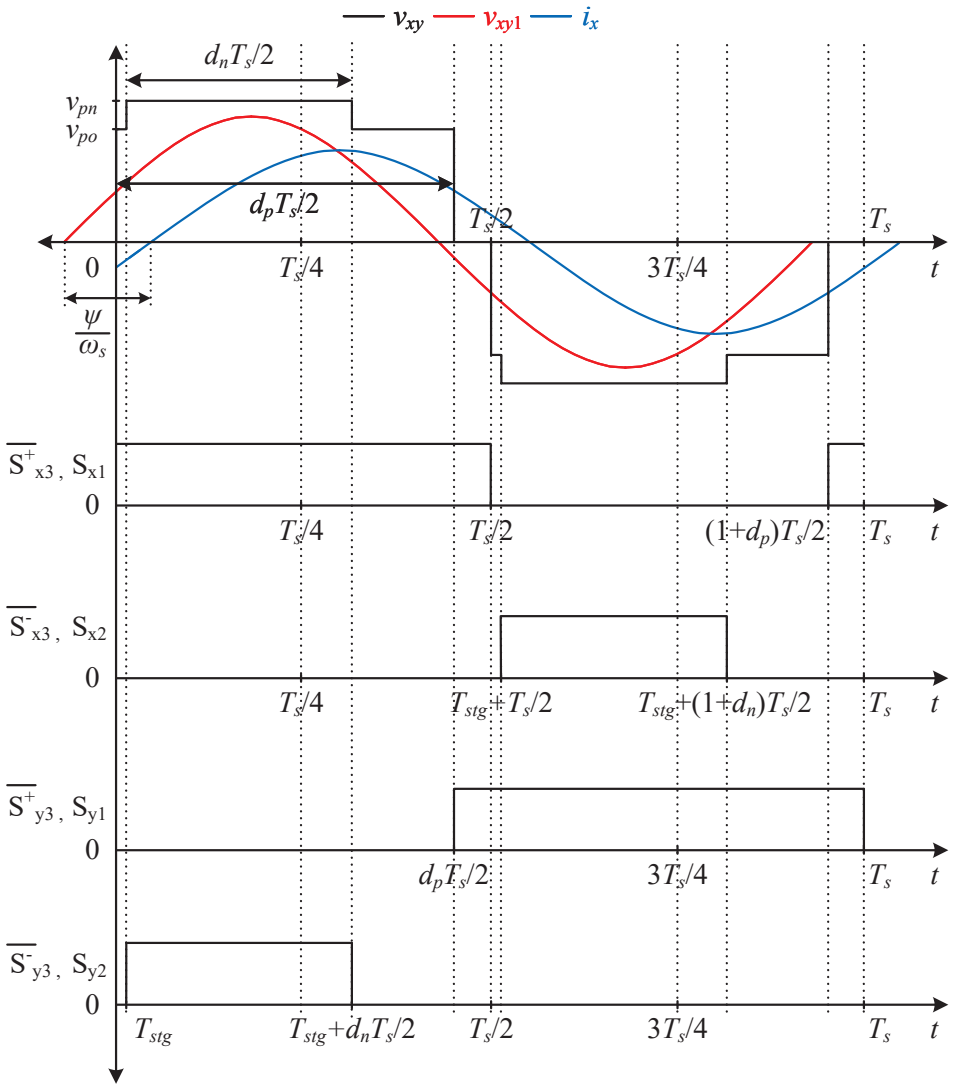


Fig. 3.4: Switching pattern of the T-type bridge when $d_p > d_n$. The proposed leading-edge-aligned modulation strategy closely aligns the leading edges of the two quasi-square voltages, generated with respect to d_p and d_n, with an intentionally introduced time delay, T_{stg}. The five-level T-type bridge output voltage contains a fundamental component, v_{xy1}. Moreover, a near-sinusoidal lagging tank current, i_x, is obtained.

3.3 Proposed Leading-Edge-Aligned Modulation for the T-Type Bridge

The switching sequence for the proposed leading-edge-aligned modulation applied to the T-type bridge is shown in Figs. 3.4 and 3.5 for both cases: $d_p > d_n$ and $d_p < d_n$, where d_p and d_n denote the duty ratios corresponding to the dc-link voltages v_{po} and v_{on}, respectively. To achieve ZVS by ensuring the desired polarity and magnitude of the tank current

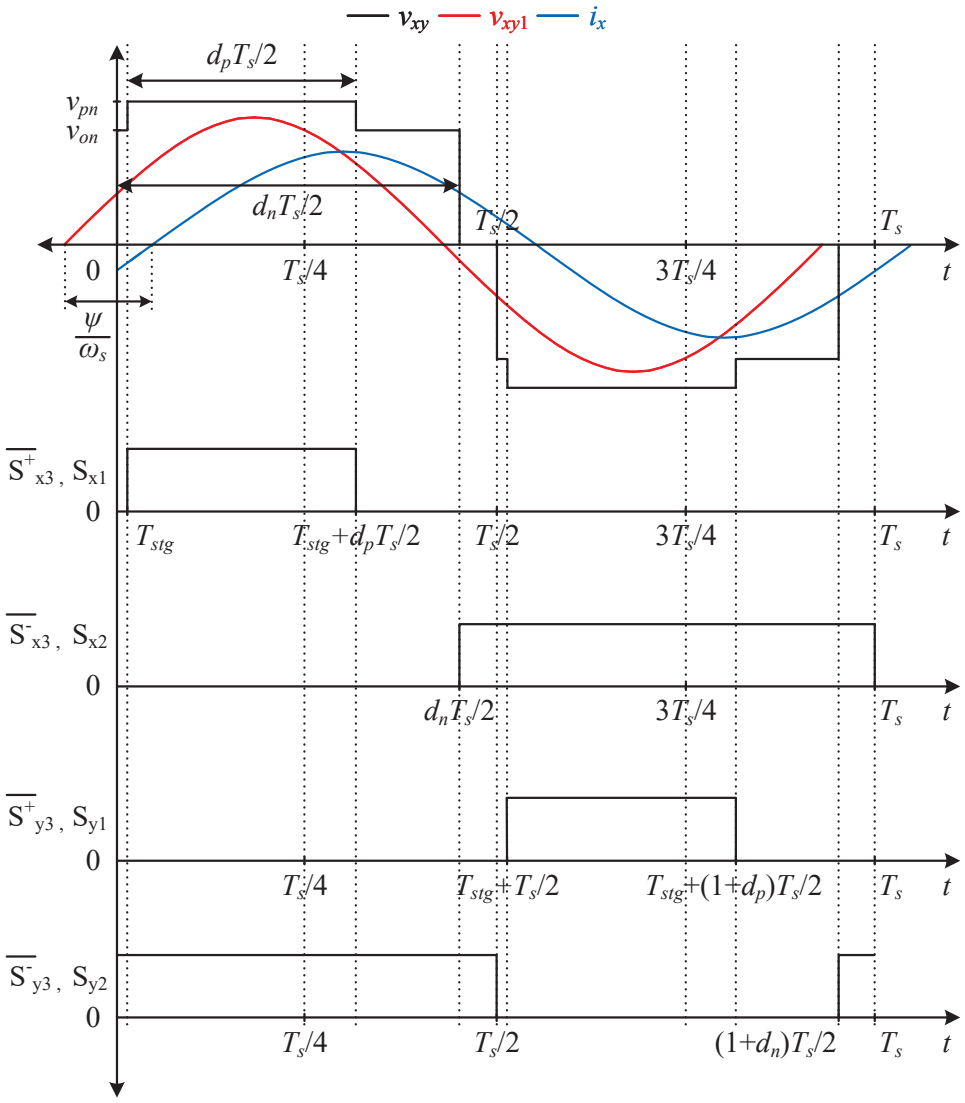


Fig. 3.5: Switching pattern of the T-type bridge when $d_p < d_n$. The proposed leading-edge-aligned modulation strategy closely aligns the leading edges of the two quasi-square voltages, generated with respect to d_p and d_n, with an intentionally introduced time delay, T_{stg}. The five-level T-type bridge output voltage contains a fundamental component, v_{xy1}. Moreover, a near-sinusoidal lagging tank current, i_x, is obtained.

during switching transitions, the leading edges of the two quasi-square voltages, generated with d_p and d_n, are closely aligned with an intentionally introduced time delay, T_{stg}. Additional details regarding the ZVS operation and time delay are provided in Section 3.5. The fundamental component of the T-type bridge output voltage, v_{xy1}, shown in Figs. 3.4 and 3.5, is formed by the sum of the fundamental components of the two quasi-square voltages,

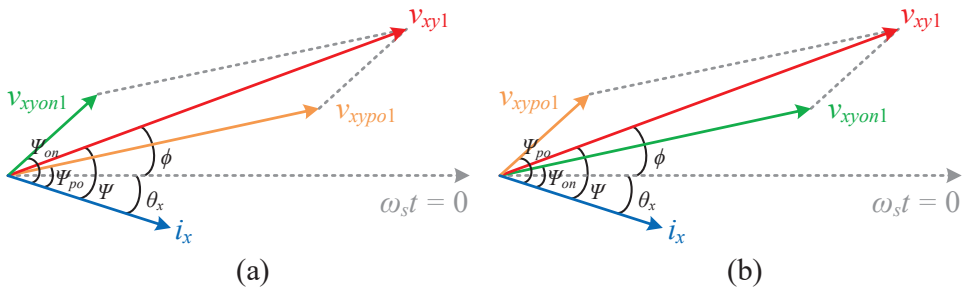


Fig. 3.6: Phasor diagram of the fundamental T-type bridge output voltage, v_{xy1}, and its components: v_{xypo1} and v_{xyon1}. The output tank current phasor, i_x, lags behind v_{xy1} by an angle ψ, determined by the tank design. The figure illustrates the phasor diagram for two cases: (a) $d_p > d_n$ and (b) $d_p < d_n$.

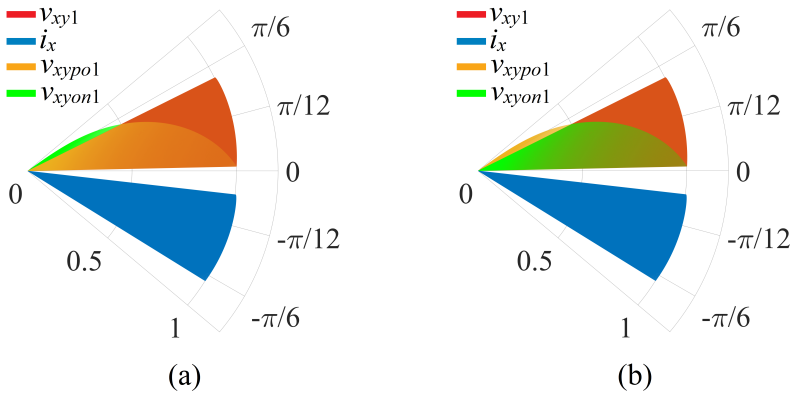


Fig. 3.7: Contour of various phasors over the grid cycle for (a) $d_p > d_n$ and (b) $d_p < d_n$, including the fundamental voltage phasor v_{xy1} and its components: v_{xypo1} and v_{xyon1}. The tank current phasor, i_x, consistently lags behind v_{xy1} by an angle ψ. The peak of v_{xy1} is maintained constant throughout the grid cycle for a given output power.

given by

$$\left.\begin{aligned} v_{xy1} &= v_{xypo1} + v_{xyon1} \\ &= \frac{4}{\pi} v_{po} \sin\left(\frac{\pi d_p}{2}\right) \sin\left(\omega_s t + \frac{\pi}{2}(1-d_p)\right) + \\ &\quad \frac{4}{\pi} v_{on} \sin\left(\frac{\pi d_n}{2}\right) \sin\left(\omega_s t + \frac{\pi}{2}(1-d_n)\right) \\ &= V_{xy1\text{-}m} \sin(\omega_s t + \phi)\,, \end{aligned}\right\} \tag{3.3}$$

where ω_s is the angular switching frequency of the T-type bridge, and $V_{xy1\text{-}m}$ denotes the peak value of its fundamental output voltage. Due to the higher-order nature of the *LCC* tank, which filters out higher-order harmonics, a near-sinusoidal tank current is obtained

at the output of the T-type bridge, given by

$$i_x = I_{xm} \sin(\omega_s t - \theta_x)\,, \tag{3.4}$$

where I_{xm} is the peak of the tank current. Phasor diagrams of the T-type bridge voltages and the corresponding current for both cases, $d_p > d_n$ and $d_p < d_n$, are presented in Fig. 3.6. Moreover, during steady-state operation, the LCC resonant tank network, diode bridge rectifier, and connected EV battery collectively behave as a passive load as characterized by the FHA. As a result, the output power can be directly controlled by adjusting the peak of the fundamental component of the T-type bridge output voltage, v_{xy1}. For a certain power flow, the peak of v_{xy1} must be kept constant throughout the grid cycle via closed-loop control. This constant-peak characteristic of v_{xy1}, maintained by the leading-edge-aligned modulation-based closed-loop control architecture for a given output power, is illustrated in Figs. 3.7(a) and 3.7(b). These figures show the contours of the per-unit v_{xy1} and i_x phasors, along with the components of v_{xy1}, namely v_{xypo1} and v_{xyon1}, throughout the grid cycle for both $d_p > d_n$ and $d_p < d_n$. It can also be observed from these figures that the tank design, as detailed in Section 3.5, ensures that the current i_x remains lagging with respect to $\omega_s t = 0$, which corresponds to the angle of the first leading edge shown in Figs. 3.4 and 3.5, so that the ZVS of the T-type bridge MOSFETs is maintained throughout the grid cycle.

The duty ratios d_p and d_n are modulated throughout the grid cycle to generate the desired 180 Hz p-port and n-port currents, i_p and i_n, as shown in Fig. 3.3(b), which shape the grid currents to be sinusoidal. The analytical duty ratios can be derived through a four-step procedure:

1. For input PFC, the average values of i_p^{dc} and i_n^{dc} over a switching cycle are equated to the instantaneous values of the desired i_p and i_n. These Unfolder output currents, i_p and i_n, shape the grid currents sinusoidal in a piecewise manner. This step also accounts for the currents flowing into the dc-link capacitors due to the dc-link voltages

Table 3.1: Values of f_p and f_n used to calculate d_p and d_n for different ac-voltage sectors.

Sector	**Grid angle ($\angle v_{\bar{a}\bar{b}}$)**	$\boldsymbol{f_p}$	$\boldsymbol{f_n}$
1	$0 \leq \theta_{\text{grid}} < {}^{\pi}/_{3}$	$\theta_{\text{grid}} + {}^{\pi}/_{2} - \alpha$	$\theta_{\text{grid}} + {}^{\pi}/_{6} - \alpha$
2	${}^{\pi}/_{3} \leq \theta_{\text{grid}} < {}^{2\pi}/_{3}$	$\theta_{\text{grid}} - {}^{\pi}/_{6} - \alpha$	$\theta_{\text{grid}} + {}^{\pi}/_{6} - \alpha$
3	${}^{2\pi}/_{3} \leq \theta_{\text{grid}} < \pi$	$\theta_{\text{grid}} - {}^{\pi}/_{6} - \alpha$	$\theta_{\text{grid}} - {}^{\pi}/_{2} - \alpha$
4	$\pi \leq \theta_{\text{grid}} < {}^{4\pi}/_{3}$	$\theta_{\text{grid}} - {}^{5\pi}/_{6} - \alpha$	$\theta_{\text{grid}} - {}^{\pi}/_{2} - \alpha$
5	${}^{4\pi}/_{3} \leq \theta_{\text{grid}} < {}^{5\pi}/_{3}$	$\theta_{\text{grid}} - {}^{5\pi}/_{6} - \alpha$	$\theta_{\text{grid}} - {}^{7\pi}/_{6} - \alpha$
6	${}^{5\pi}/_{3} \leq \theta_{\text{grid}} < 2\pi$	$\theta_{\text{grid}} + {}^{\pi}/_{2} - \alpha$	$\theta_{\text{grid}} - {}^{7\pi}/_{6} - \alpha$

across them and ensures unity power factor at the input. This step results in the following expressions:

$$\begin{aligned} \langle i_p^{\text{dc}} \rangle_{T_s} &= i_p - \langle i_{cpo} + i_{cpn} \rangle_{T_s} \\ &= I_{gcm} \sin(f_p(\theta_{\text{grid}}, \alpha)) \,, \end{aligned} \tag{3.5}$$

$$\begin{aligned} \langle i_n^{\text{dc}} \rangle_{T_s} &= i_n - \langle i_{con} + i_{cpn} \rangle_{T_s} \\ &= I_{gcm} \sin(f_n(\theta_{\text{grid}}, \alpha)) \,, \end{aligned} \tag{3.6}$$

where

$$I_{gcm} = \sqrt{I_{gm}^2 + I_{cm}^2} \,, \tag{3.7}$$

$$\alpha = \tan^{-1}\left({}^{I_{cm}}/_{I_{gm}}\right) \,, \tag{3.8}$$

$$I_{cm} = \sqrt{3} V_{gm} \omega_{\text{grid}} C_{\text{dc}} \,, \tag{3.9}$$

where I_{gm} represents the peak of the grid currents, ω_{grid} denotes the angular grid frequency, and C_{dc} refers to the dc-link capacitors (C_{po}, C_{on}, and C_{pn}) connected at the Unfolder output. The functions f_p and f_n depend on θ_{grid} and the phase α introduced by C_{dc}, as specified in Table 3.1.

2. The average values of i_p^{dc} and i_n^{dc} are expressed in terms of d_p and d_n as

$$\langle i_p^{\text{dc}} \rangle_{T_s} = \frac{2}{\pi} I_{xm} \cos(\psi_{po}) \sin\left(\frac{\pi d_p}{2}\right) , \tag{3.10}$$

$$\langle i_n^{\text{dc}} \rangle_{T_s} = \frac{2}{\pi} I_{xm} \cos(\psi_{on}) \sin\left(\frac{\pi d_n}{2}\right) , \tag{3.11}$$

where ψ_{po} and ψ_{on} denote the phase lags of the current i_x with respect to the voltages v_{xypo1} and v_{xyon1}, respectively, as shown in Fig. 3.6.

3. The average values of i_p^{dc} and i_n^{dc} obtained from the previous two steps are equated to obtain d_p and d_n, as given below:

$$d_p = \frac{2}{\pi} \sin^{-1}\left(\frac{\pi I_{gcm}}{2 I_{xm} \cos(\psi_{po})} \sin(f_p(\theta_{\text{grid}}, \alpha))\right) , \tag{3.12}$$

$$d_n = \frac{2}{\pi} \sin^{-1}\left(\frac{\pi I_{gcm}}{2 I_{xm} \cos(\psi_{on})} \sin(f_n(\theta_{\text{grid}}, \alpha))\right) . \tag{3.13}$$

4. The equations for d_p and d_n are further simplified by introducing the p-port and n-port modulation indices, m_p and m_n, respectively. These modulation indices are the outputs of the PI controllers in the proposed closed-loop control architecture detailed in Section 3.4. The simplified duty ratios are given in the following:

$$d_p = \frac{2}{\pi} \sin^{-1}\left(m_p \sin(f_p(\theta_{\text{grid}}, \alpha))\right) , \tag{3.14}$$

$$d_n = \frac{2}{\pi} \sin^{-1}\left(m_n \sin(f_n(\theta_{\text{grid}}, \alpha))\right) , \tag{3.15}$$

where

$$m_p = \frac{\pi I_{gcm}}{2 I_{xm} \cos(\psi_{po})} = \frac{\pi V_{xy1\text{-}m} \cos(\psi)}{2\sqrt{3} V_{gm} \cos(\alpha) \cos(\psi_{po})} , \tag{3.16}$$

$$m_n = \frac{\pi I_{gcm}}{2 I_{xm} \cos(\psi_{on})} = \frac{\pi V_{xy1\text{-}m} \cos(\psi)}{2\sqrt{3} V_{gm} \cos(\alpha) \cos(\psi_{on})} , \tag{3.17}$$

where ψ is the phase lag of the tank current i_x with respect to the voltage v_{xy1}.

As discussed in Section 3.2, the unfolding-based ac-dc topology utilized in this work requires

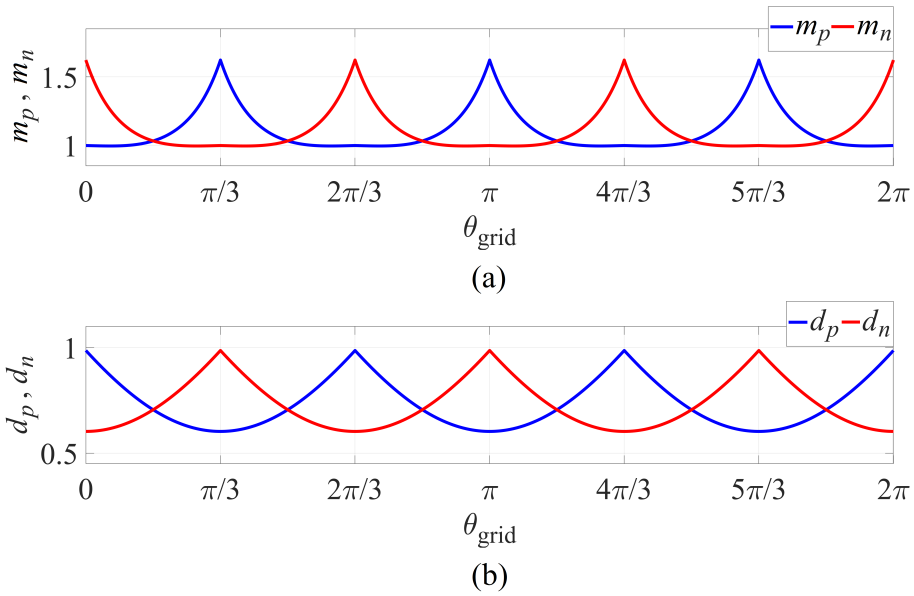


Fig. 3.8: (a) Modulation indices, m_p and m_n, and (b) duty ratios, d_p and d_n, over the grid cycle, considering $\alpha \approx 0$ and operation at rated output power.

smaller dc-link capacitors. Therefore, the currents flowing into these capacitors, due to the voltages across them, are typically lower than the grid currents ($I_{cm} \ll I_{gm}$). This results in the angle $\alpha \approx 0$, as derived in (3.8). The analytical values of the modulation indices, m_p and m_n, and the corresponding duty ratios, d_p and d_n, considering $\alpha = 0$ and operation at rated output power, are illustrated in Fig. 3.8 throughout the grid cycle.

3.4 Modeling and Control of the T-Type Bridge-Based DC-DC Converter

As discussed earlier, the Unfolder operates in an open-loop mode at a low frequency. Consequently, tasks such as grid-side sinusoidal current shaping for PFC and output power regulation are handled simultaneously by the closed-loop controlled T-type bridge-based dc-dc converter. The proposed control strategy is illustrated in Fig. 3.9(a). In this architecture, the outer loop regulates the power delivered to the battery load by controlling the battery current, i_{batt}, while two inner loops ensure sinusoidal grid current shaping by regulating the p-port and n-port output currents of the Unfolder, i_p and i_n. Based on the output power demand, the PI controller of the outer loop determines the peak value of the current references, I_{gm}, for the inner loops controlling i_p and i_n. Using this value of I_{gm} along with

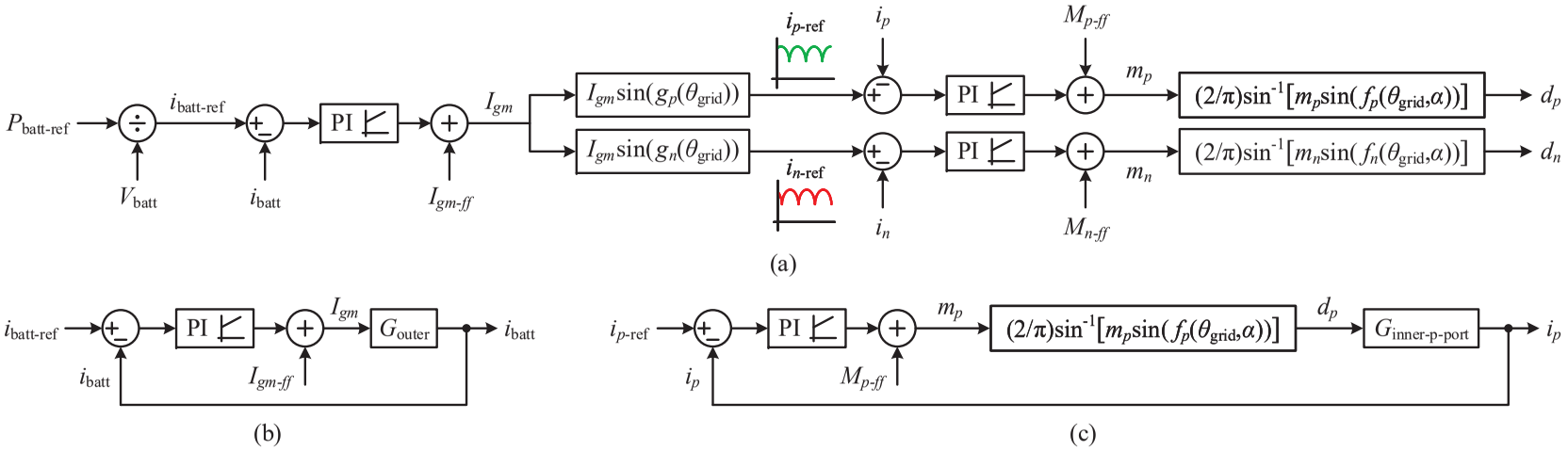


Fig. 3.9: (a) The proposed control architecture for leading-edge-aligned modulation, consisting of an outer loop for output power regulation and two inner loops to shape the grid currents sinusoidal for PFC; (b) simplified control architecture of the outer loop to regulate output power by controlling the battery load current, i_{batt}; and (c) simplified control architecture of the p-port inner loop to shape the grid currents sinusoidal by controlling the current i_p. Since the relationship between m_p and d_p is nonlinear, a small-signal linearization of this relationship, as provided in (3.26), is necessary to calculate the loop gain of the inner p-port control loop. A similar simplified control architecture can be derived for the n-port inner loop, which controls the current i_n.

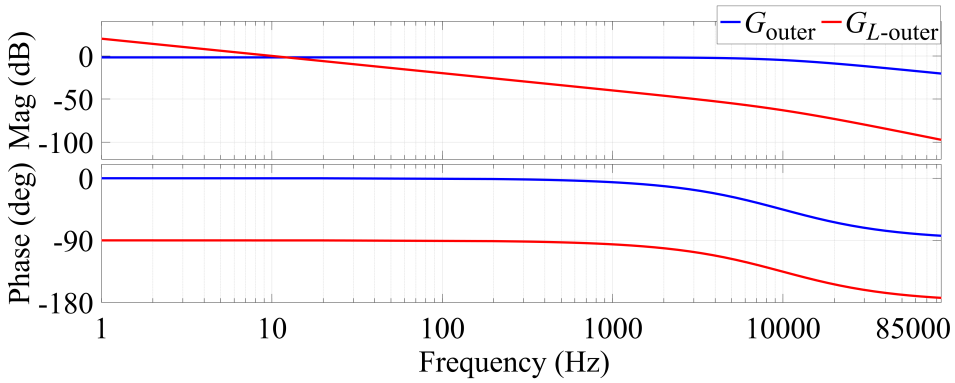


Fig. 3.10: Bode plots of the uncompensated outer-loop plant, G_{outer}, and the compensated plant with the PI controller, $G_{L\text{-outer}}$. A closed-loop bandwidth of 10 Hz is selected for the outer loop, and the corresponding PI controller parameters are $K_{p\text{-PI}} = 0$, $K_{i\text{-PI}} = 76.4$.

the functions g_p and g_n, defined as

$$g_p(\theta_{\text{grid}}) = f_p(\theta_{\text{grid}}, \alpha)\big|_{\alpha=0}\,, \tag{3.18}$$

$$g_n(\theta_{\text{grid}}) = f_n(\theta_{\text{grid}}, \alpha)\big|_{\alpha=0}\,, \tag{3.19}$$

the current references for regulating i_p and i_n are generated. The inner loops then accurately track these current references by modulating the duty ratios, d_p and d_n, throughout the grid cycle. These duty ratios are determined based on the modulation indices, m_p and m_n, generated by the PI controllers of the inner loops. The simplified control architectures of the outer and inner loops are illustrated in Figs. 3.9(b) and 3.9(c), respectively.

It is important to note that the controlled currents, i_p and i_n, are 180 Hz quantities, corresponding to three times the grid frequency, f_{grid}, as illustrated in Fig. 3.3(b). To ensure effective regulation of these currents under both steady-state and dynamic conditions, the control bandwidth of the inner loops should be designed to be significantly greater than 180 Hz. In addition, to achieve proper decoupling between the inner and outer loops, the outer loop can be designed with a lower bandwidth. The appropriate selection of control bandwidths requires the derivation of the plant transfer functions for the control loops. The plant transfer function for the outer loop is derived by satisfying the power balance between

the input grid side and the output battery load side, which is expressed as follows:

$$G_{\text{outer}} = \frac{\hat{i}_{\text{batt}}}{\hat{i}_{gm}} = \frac{\sqrt{3}}{2} \frac{V_{gm}}{V_{\text{batt}}(1 + r_{\text{batt}} C_{\text{out}} s)} , \tag{3.20}$$

where $\hat{i}_{\text{batt}}$ and $\hat{i}_{gm}$ denote the small-signal variations in the battery load current and the peak of the grid current, respectively. Moreover, r_{batt} represents the net series resistance of the battery load, and C_{out} denotes the output filter capacitor. The loop transfer function of the outer loop is given by

$$G_{L\text{-outer}} = G_{\text{PI-outer}} \, G_{\text{outer}} , \tag{3.21}$$

where $G_{\text{PI-outer}}$ represents the PI controller used in the outer loop for closed-loop control. The Bode plots of the uncompensated outer-loop plant, G_{outer}, and the compensated plant with the PI controller, $G_{L\text{-outer}}$, are shown in Fig. 3.10, along with the corresponding controller parameters.

Now, given the symmetry between the p-port and n-port inner control loops, the subsequent analysis primarily focuses on the p-port current control. A similar approach can be applied to the n-port current control as well. In this control architecture, the plant transfer function of the inner p-port current control loop, denoted as $G_{\text{inner-p-port}}$, relates the small-signal p-port current $\hat{i}_p$ to the small-signal p-port duty ratio $\hat{d}_p$, and is expressed as

$$G_{\text{inner-p-port}} = \frac{\hat{i}_p}{\hat{d}_p} . \tag{3.22}$$

The implementation of a higher-order LCC resonant network with an appropriate quality factor enables the realization of sinusoidal current or voltage waveforms within the tank. In this context, employing a small-signal modeling approach based on phasor transformation is considered suitable [25, 60–62]. The modeling procedure for calculating $G_{\text{inner-p-port}}$ primarily involves three steps:

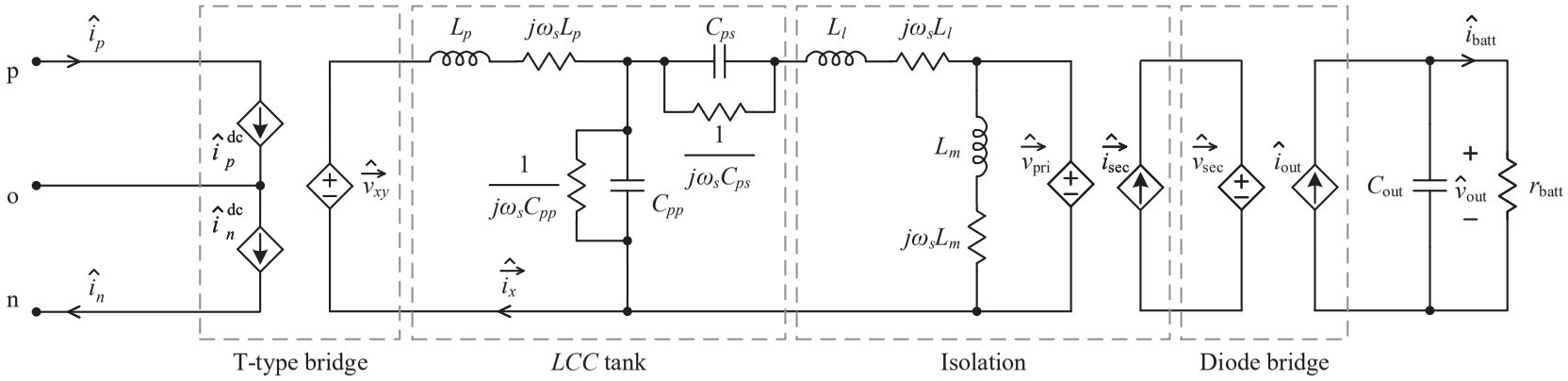


Fig. 3.11: Phasor-transformed small-signal circuit of the T-type bridge-based dc-dc converter, incorporating an *LCC* resonant tank with cantilever-modeled isolation, a secondary-side diode bridge, and an output capacitive filter. The net series resistance of the battery is considered in the small-signal domain.

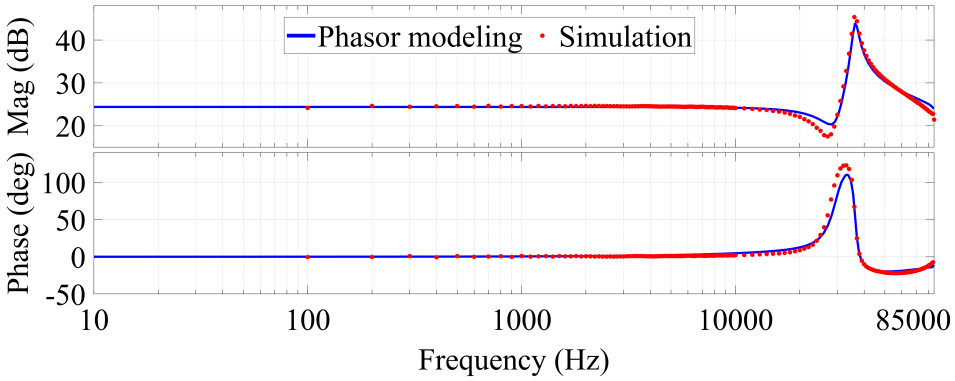


Fig. 3.12: Comparison of the Bode plots of the p-port inner-loop plant, $G_{\text{inner-p-port}} = \hat{i}_p/\hat{d}_p$, of the T-type bridge-based dc-dc conversion system, obtained using phasor transformation-based small-signal modeling and simulations with the PLECS multitone analysis tool.

1. A steady-state analysis is conducted to derive the relationship between the steady-state p-port current, I_p, and the corresponding steady-state p-port duty ratio, D_p, as given below:

$$I_p = \frac{2}{\pi} I_{xm} \cos\left(\frac{\pi}{2}(1 - D_p) + \Theta_x\right) \sin\left(\frac{\pi D_p}{2}\right), \tag{3.23}$$

where I_{xm} and Θ_x represent the steady-state quantities of the T-type bridge-based dc-dc conversion system, evaluated at a specific grid angle at which the plant transfer function, $G_{\text{inner-p-port}}$, is derived.

2. The small-signal phasor-transformed circuit is derived for the T-type bridge-based dc-dc converter, incorporating an LCC resonant tank with isolation and a diode bridge on the secondary side, as illustrated in Fig. 3.11.

3. The plant transfer function is calculated using the phasor-transformed small-signal circuit, as given below:

$$G_{\text{inner-p-port}} = \frac{\hat{i}_p^{i_{x\text{-env}}}}{\hat{i}_{x\text{-env}}^{d_p}} \frac{\hat{i}_{x\text{-env}}^{d_p}}{\hat{d}_p} + \frac{\hat{i}_p^{\theta_x}}{\hat{\theta}_x^{d_p}} \frac{\hat{\theta}_x^{d_p}}{\hat{d}_p} + \frac{\hat{i}_p^{d_p}}{\hat{d}_p}, \tag{3.24}$$

where $\hat{i}_p^{i_{x\text{-env}}}$ and $\hat{i}_p^{\theta_x}$ represent the perturbations in the p-port current, i_p, of the T-type bridge, which arise due to small-signal changes in the envelope ($\hat{i}_{x\text{-env}}^{d_p}$) and phase ($\hat{\theta}_x^{d_p}$) of the T-type bridge output tank current phasor ($\hat{\vec{i}_x}$), respectively. These per-

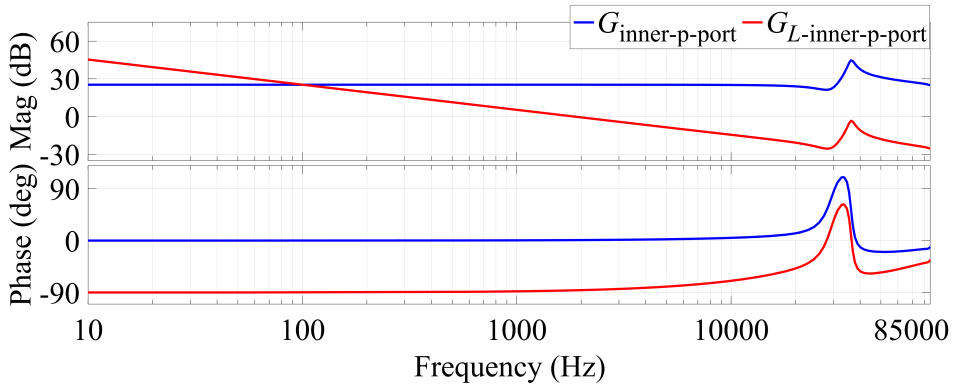


Fig. 3.13: Bode plots of the uncompensated inner-loop plant, $G_{\text{inner-p-port}}$, and the compensated plant with the PI controller, $G_{L\text{-inner-p-port}}$. A closed-loop bandwidth of 1.8 kHz is selected for the inner loop, and the corresponding PI controller parameters are $K_{p\text{-PI}} = 0.001$, $K_{i\text{-PI}} = 251.4$.

turbations are caused by small-signal variations introduced in the p-port duty ratio, d_p. Additionally, $\hat{i}_p^{d_p}$ captures the direct effect of the small-signal change in d_p on the p-port current, i_p.

The loop transfer function of the p-port inner loop is given by

$$G_{L\text{-inner-p-port}} = G_{\text{PI-inner}}\, K_{m_p}^{d_p} G_{\text{inner-p-port}}\,, \tag{3.25}$$

where $G_{\text{PI-inner}}$ represents the PI controller used in the p-port inner loop for closed-loop control and $K_{m_p}^{d_p}$ is the small-signal gain that relates $\hat{d}_p$ and $\hat{m}_p$ as

$$K_{m_p}^{d_p} = \frac{\hat{d}_p}{\hat{m}_p} = \frac{2}{\pi}\frac{\sin(f_p(\theta_{\text{grid}}, \alpha))}{\cos\left(\frac{\pi}{2}D_p\right)}\,, \tag{3.26}$$

which is derived by linearizing (3.14). Here, $K_{m_p}^{d_p}$ represents a linearized, constant gain evaluated at the steady-state operating point. The Bode plots of $G_{\text{inner-p-port}}$, obtained from the phasor transformation-based modeling, are validated through comparison with those obtained via multitone analysis using the PLECS simulation tool, as illustrated in Fig. 3.12. The Bode plots of the uncompensated p-port inner-loop plant, $G_{\text{inner-p-port}}$, and the compensated plant with the PI controller, $G_{L\text{-inner-p-port}}$, are shown in Fig. 3.13. Further details on the small-signal phasor modeling are provided in Chapter 5.

3.5 Selection of Tank Components

The selection of the LCC resonant tank in the T-type bridge-based dc-dc converter is based on three primary design criteria: (i) satisfying the power requirements of the battery load, (ii) achieving an appropriate lagging characteristic of the tank current to ensure the desired current magnitude and polarity during switching transitions for ZVS of the T-type bridge MOSFETs, and (iii) minimizing conduction losses at the rated output power. The tank inductor, L_p, is selected based on the first design criterion, which is satisfying the power requirement of the battery load. Its value is calculated as

$$L_p = \frac{2V_{xy1\text{-}m}V_{\text{batt}}}{\pi\omega_s P_{\text{batt}}}\,. \tag{3.27}$$

The capacitor C_{pp} is selected such that it resonates with L_p at the switching frequency. This resonance helps establish a current-source characteristic for the LCC tank, which is necessary for WPT-based battery charging applications. The value of C_{pp} is calculated as

$$C_{pp} = \frac{1}{\omega_s^2 L_p}\,. \tag{3.28}$$

As discussed earlier, during steady-state operation, the diode bridge rectifier and the connected EV battery collectively behave as a passive load, as characterized by FHA. The value of this passive resistive load is given as

$$R_{\text{eq}} = \frac{8}{\pi^2}\frac{V_{\text{batt}}^2}{P_{\text{batt}}}\,. \tag{3.29}$$

In an LCC tank, when the combined impedance of the isolation leakage inductor, L_l, and the series capacitor, C_{ps}, matches the impedance of L_p at the switching frequency, the impedance seen by the T-type bridge becomes purely resistive and is given by $L_p/(R_{\text{eq}}C_{pp})$. Consequently, to minimize the required value of C_{ps} and reduce the reactive loading of the T-type bridge for lower conduction losses, the tank isolation is designed such that L_l closely matches the inductance of L_p. However, achieving ZVS for the T-type bridge MOSFETs requires a certain level of inductive loading. To achieve this inductive loading,

a phase lag, ψ, is intentionally introduced between the T-type bridge output current, i_x, and the fundamental component of the T-type bridge output voltage, v_{xy1}. Accordingly, the capacitance value of C_{ps} is determined as follows:

$$C_{ps} = \frac{1}{\omega_s \left(R_{\text{eq}} \tan\left(\psi\right) + \omega_s (L_l - L_p)\right)}\,, \tag{3.30}$$

based on the required value of ψ. Now, to select an appropriate value of ψ, and accordingly C_{ps}, a ZVS analysis of the T-type bridge is required to determine the necessary tank current magnitude with the appropriate polarity during the switching transitions. Moreover, a conduction loss analysis of the T-type bridge is also needed to optimize the reactive nature of the tank design and ensure that conduction losses remain at a reasonable level. By combining these analyses, an optimized value of C_{ps} can be selected.

3.5.1 ZVS Analysis of the T-Type Bridge Considering Nonlinear MOSFET Output Capacitance

To accurately calculate the tank current required to charge or discharge the output capacitance, C_{oss}, of the T-type bridge MOSFETs for achieving ZVS, the nonlinear nature of the output capacitance must be considered. To address this, energy- and charge-equivalent capacitors are defined [29, 30, 72, 73], as given below:

$$C_{\text{eq},E}\Big|_0^{v_c} = \frac{2}{{v_c}^2} \int_0^{v_c} v\, C_{\text{oss}}|_v \,\mathrm{d}v\,, \tag{3.31}$$

$$C_{\text{eq},Q}\Big|_0^{v_c} = \frac{1}{v_c} \int_0^{v_c} C_{\text{oss}}|_v \,\mathrm{d}v\,, \tag{3.32}$$

where the energy stored in $C_{\text{eq},E}$ at a voltage v_c is equal to the energy stored when the voltage across C_{oss} rises from 0 to v_c. Similarly, the charge stored in $C_{\text{eq},Q}$ at v_c is equal to the charge stored when charging C_{oss} from 0 to v_c, where v_c can take any value between 0 and the rated operating voltage of the MOSFET. Moreover, the energy- and charge-equivalent

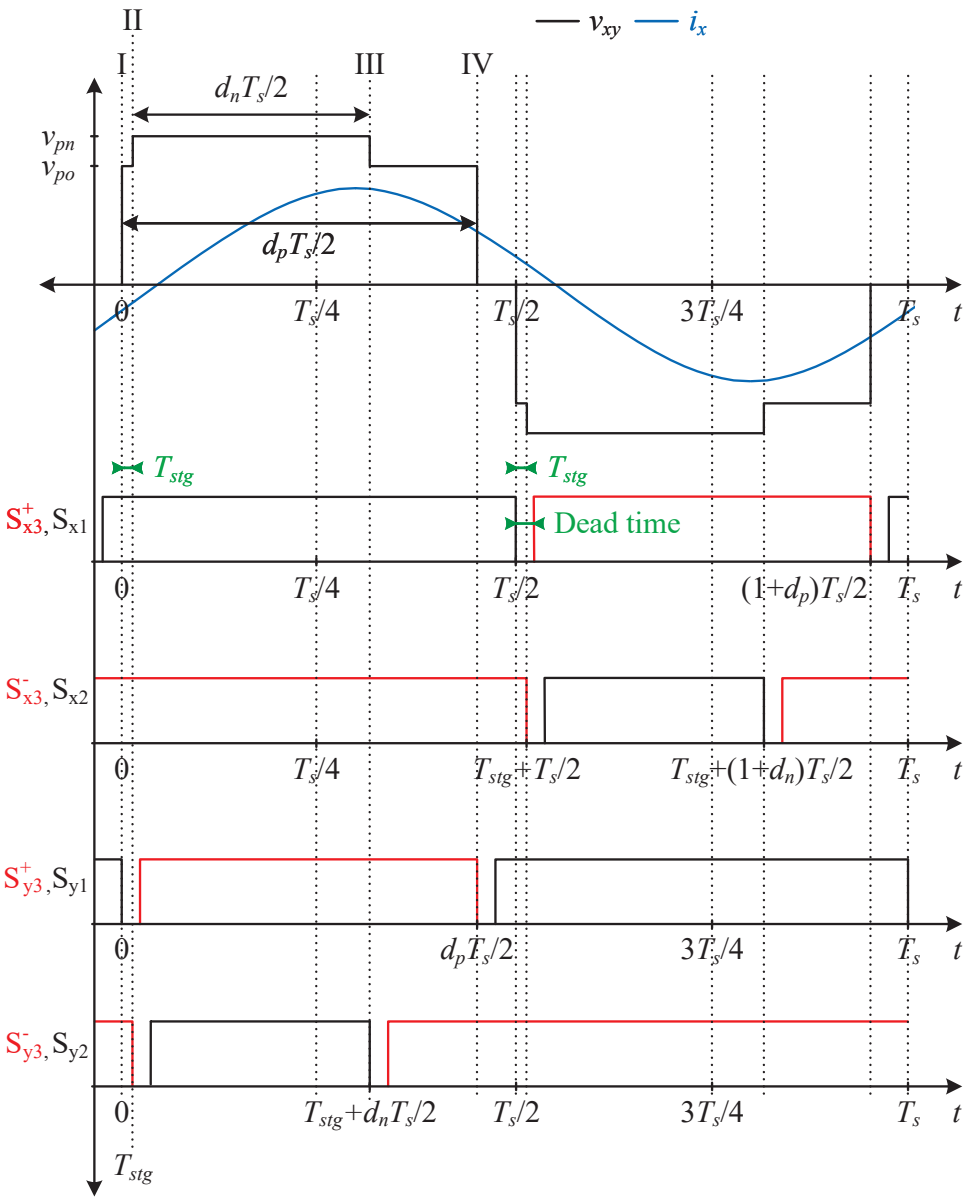


Fig. 3.14: Switching pattern of the T-type bridge when $d_p > d_n$. The leading edges of the two quasi-square voltages are closely aligned with an intentionally introduced time delay of T_{stg}, resulting in four distinct switching transitions.

capacitors for the scenario where C_{oss} charges from v_1 to v_2 is given by

$$C_{\text{eq},E}\Big|_{v_1}^{v_2} = \frac{C_{\text{eq},E}\Big|_0^{v_2} v_2^2 - C_{\text{eq},E}\Big|_0^{v_1} v_1^2}{v_2^2 - v_1^2}, \tag{3.33}$$

$$C_{\text{eq},Q}\Big|_{v_1}^{v_2} = \frac{C_{\text{eq},Q}\Big|_0^{v_2} v_2 - C_{\text{eq},Q}\Big|_0^{v_1} v_1}{v_2 - v_1}, \tag{3.34}$$

Table 3.2: C_{oss} charging and discharging during transitions I and II.

Transition	$\mathbf{S}_{\text{y1}}$	$\mathbf{S}_{\text{y2}}$	$\mathbf{S}^{+}_{\text{y3}}$	$\mathbf{S}^{-}_{\text{y3}}$
I	0 to v_{po}	v_{pn} to v_{on}	v_{po} to 0	-
II	v_{po} to v_{pn}	v_{on} to 0	-	0 to v_{on}

where v_1 and v_2 can be any values from 0 to the rated operating voltage of the MOSFET.

As shown in Figs. 3.4 and 3.5, the switching pattern of the T-type bridge MOSFETs is symmetric for both $d_p > d_n$ and $d_p < d_n$. Therefore, the subsequent analysis focuses on the switching transitions during $d_p > d_n$, while a similar analysis applies for $d_p < d_n$. The leading-edge-aligned switching pattern of the T-type bridge, along with the on/off states of all MOSFETs, is shown in Fig. 3.14 for the case of $d_p > d_n$. It can be observed from this figure that transitions III and IV readily achieve ZVS for the MOSFETs due to the higher magnitude and appropriate polarity of the tank current, i_x, during these intervals. In contrast, transitions I and II are more critical and require careful analysis, as the tank current is relatively low during these transitions. Consequently, the subsequent analysis focuses on these two transitions to determine the minimum required tank current and the duration necessary to achieve ZVS. The equivalent circuits for transitions I and II are shown in Fig. 3.15, while Table 3.2 summarizes the voltage changes across the MOSFET output capacitances. In these circuits, the LCC tank is modeled by an equivalent network consisting of an inductor, L_p, and a voltage source, v_{cpp}, which represents the instantaneous voltage across the capacitor C_{pp} during the switching transition under consideration. Since the capacitor voltage remains nearly constant during the dead time, it is modeled as a constant voltage source in the ZVS analysis. However, different v_{cpp} values are considered for the respective switching transitions and for the variation over the grid cycle.

Transition I

During transition I, the MOSFETs S_{y1}, S_{y2}, and S^{+}_{y3} of the y leg remain part of the active commutation loops. Meanwhile, MOSFET S_{x1} is turned on, connecting the x-leg

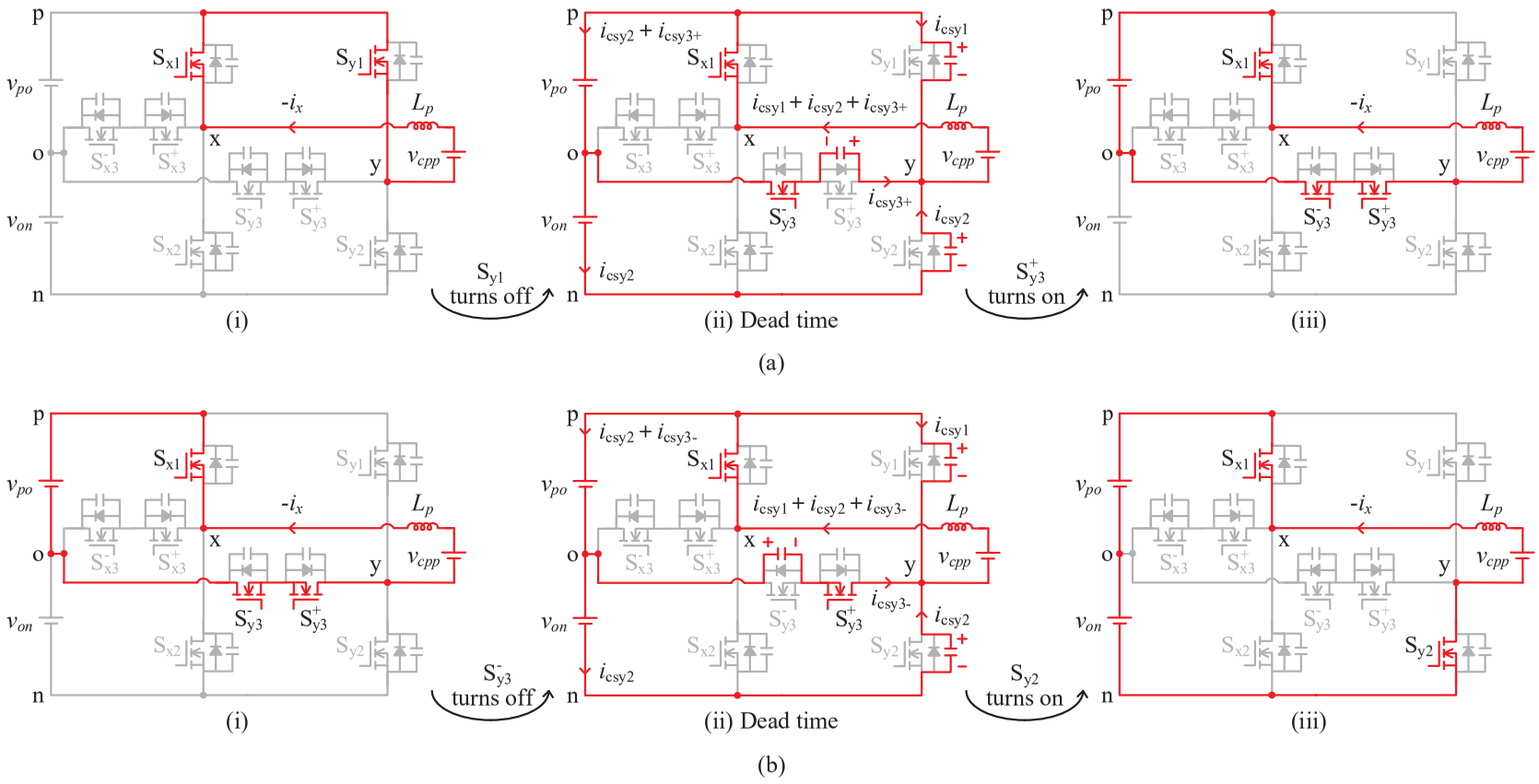


Fig. 3.15: Equivalent circuits of the T-type bridge and the *LCC* tank during (a) transition I and (b) transition II. Dead-time intervals are also shown, during which the MOSFET output capacitances charge or discharge. The *LCC* tank is modeled as an equivalent network with an inductor, L_p, and a voltage source, v_{cpp}, representing the instantaneous voltage across capacitor C_{pp} during the switching transition under consideration.

switch node to the p node of the dc-link. To achieve ZVS during this transition, the tank current, i_x, flowing into the x leg is required. To determine the energy required from the tank inductor, L_p, during this transition for the ZVS of the MOSFETs, the energy contributions from all sources, namely v_{po}, v_{on}, and v_{cpp}, in the circuit shown in Fig. 3.15(a) must be calculated during the dead time, as given below:

$$\left.\begin{aligned} E_{vpo} &= v_{po}\Big(-\int i_{\text{csy2}}\,dt - \int i_{\text{csy3+}}\,dt\Big) \\ &= v_{po}\Big(\int_{v_{pn}}^{v_{on}} C_{\text{oss-sy2}}\,dv + \int_{v_{po}}^{0} C_{\text{oss-sy3+}}\,dv\Big) \\ &= v_{po}\Big((v_{on}-v_{pn})C_{\text{eq},Q\text{-sy2}}\Big|_{v_{pn}}^{v_{on}} + \\ &\qquad\qquad (-v_{po})C_{\text{eq},Q\text{-sy3+}}\Big|_{v_{po}}^{0}\Big) \\ &= v_{po}^2\Big(-C_{\text{eq},Q\text{-sy2}}\Big|_{v_{pn}}^{v_{on}} - C_{\text{eq},Q\text{-sy3+}}\Big|_{v_{po}}^{0}\Big)\,. \end{aligned}\right\} \tag{3.35}$$

Similarly,

$$E_{von} = -v_{on}v_{po}C_{\text{eq},Q\text{-sy2}}\Big|_{v_{pn}}^{v_{on}}, \tag{3.36}$$

$$E_{vcpp} = v_{cpp}v_{po}\Big(C_{\text{eq},Q\text{-sy1}}\Big|_{0}^{v_{po}} + C_{\text{eq},Q\text{-sy2}}\Big|_{v_{pn}}^{v_{on}} + C_{\text{eq},Q\text{-sy3+}}\Big|_{v_{po}}^{0}\Big), \tag{3.37}$$

$$E_{s\text{-trI}} = E_{vpo} + E_{von} + E_{vcpp}\,. \tag{3.38}$$

Following this, the total change in the capacitive energy associated with the MOSFET output capacitances during transition I is determined, as given below:

$$\Delta E_{c\text{-sy1}} = \frac{1}{2}v_{po}^2 C_{\text{eq},E\text{-sy1}}\Big|_{0}^{v_{po}}, \tag{3.39}$$

$$\Delta E_{c\text{-sy2}} = -\frac{1}{2}\left(v_{pn}^2 - v_{on}^2\right) C_{\text{eq},E\text{-sy2}}\Big|_{v_{pn}}^{v_{on}}, \tag{3.40}$$

$$\Delta E_{c\text{-sy3+}} = -\frac{1}{2}v_{po}^2 C_{\text{eq},E\text{-sy3+}}\Big|_{v_{po}}^{0}, \tag{3.41}$$

$$\Delta E_{c\text{-trI}} = \Delta E_{c\text{-sy1}} + \Delta E_{c\text{-sy2}} + \Delta E_{c\text{-sy3+}}\,. \tag{3.42}$$

Now, the energy required from the inductor, L_p, is given by

$$E_{L_p\text{-trI}} = E_{s\text{-trI}} - \Delta E_{c\text{-trI}}\,, \tag{3.43}$$

and finally, the magnitude of the minimum tank current required to achieve ZVS during the switching transition in the T-type bridge is calculated as

$$I_{x\text{-min-zvs-trI}} = \sqrt{\frac{2\left|E_{L_p\text{-trI}}\right|}{L_p}}\,. \tag{3.44}$$

Moreover, the time required to achieve ZVS for the T-type bridge MOSFETs is also a critical design parameter. This calculation plays a critical role in establishing the correct dead time in hardware verification, thereby preventing the MOSFETs from turning on prematurely, before their output capacitance has fully charged or discharged. The ZVS time is evaluated under two scenarios: (i) the magnitude of the tank current, i_x, is equal to $I_{x\text{-min-zvs-trI}}$ and is just sufficient to achieve ZVS, and (ii) the magnitude of the tank current, i_x, exceeds the minimum magnitude required for ZVS. The determination of the ZVS time for transition I involves applying KCL at node y in Fig. 3.15(a), which can be expressed in the form given below:

$$\begin{aligned} -i_x &= i_{\text{csy1}} + i_{\text{csy2}} + i_{\text{csy3+}}\,, \\ &= C_{\text{oss-sy1}}\frac{\mathrm{d}v_{ds\text{-sy1}}}{\mathrm{d}t} - C_{\text{oss-sy2}}\frac{\mathrm{d}v_{ds\text{-sy2}}}{\mathrm{d}t} - C_{\text{oss-sy3+}}\frac{\mathrm{d}v_{ds\text{-sy3+}}}{\mathrm{d}t}\,. \end{aligned} \tag{3.45}$$

Using this, the charge required by the MOSFET output capacitances can be equated to the charge supplied by the tank current, i_x, which corresponds to the area under the current waveform. The required time for ZVS is then calculated as

$$t_{\text{zvs-trI}} = \frac{2\,v_{po}\Big(C_{\text{eq},Q\text{-sy1}}\Big|_0^{v_{po}} + C_{\text{eq},Q\text{-sy2}}\Big|_{v_{pn}}^{v_{on}} + C_{\text{eq},Q\text{-sy3+}}\Big|_{v_{po}}^{0}\Big)}{I_{x\text{-min-zvs-trI}}}. \tag{3.46}$$

Moreover, if the tank current exceeds the minimum ZVS current required during transition I, (3.46) can be modified as

$$t_{\text{ex-zvs-trI}} = \frac{I_{x\text{-trI}} - \sqrt{I_{x\text{-trI}}^2 - \omega_s I_{xm}\, I_{x\text{-min-zvs-trI}}\, t_{\text{zvs-trI}}}}{\omega_s I_{xm}}\,, \tag{3.47}$$

where $I_{x\text{-trI}}$ denotes the tank current at the beginning of transition I.

Transition II

Similar to transition I, the minimum required tank current for ZVS and the duration to achieve it can be calculated for transition II. The energy contributions from all sources, namely v_{po}, v_{on}, and v_{cpp}, in the circuit shown in Fig. 3.15(b) during the dead time must be evaluated, as given below:

$$E_{vpo} = v_{po} v_{on} \Big(- C_{\text{eq},Q\text{-sy2}}\Big|_{v_{on}}^{0} - C_{\text{eq},Q\text{-sy3-}}\Big|_{0}^{v_{on}} \Big)\,, \tag{3.48}$$

$$E_{von} = -v_{on}^2 C_{\text{eq},Q\text{-sy2}}\Big|_{v_{on}}^{0}\,, \tag{3.49}$$

$$E_{vcpp} = v_{cpp} v_{on} \Big(C_{\text{eq},Q\text{-sy1}}\Big|_{v_{po}}^{v_{pn}} + C_{\text{eq},Q\text{-sy2}}\Big|_{v_{on}}^{0} + C_{\text{eq},Q\text{-sy3-}}\Big|_{0}^{v_{on}} \Big), \tag{3.50}$$

$$E_{s\text{-trII}} = E_{vpo} + E_{von} + E_{vcpp}\,. \tag{3.51}$$

Following this, the total change in the capacitive energy associated with the MOSFET output capacitances during transition II is determined, as given below:

$$\Delta E_{c\text{-sy1}} = \frac{1}{2}\left(v_{pn}^2 - v_{po}^2\right) C_{\text{eq},E\text{-sy1}}\Big|_{v_{po}}^{v_{pn}}\,, \tag{3.52}$$

$$\Delta E_{c\text{-sy2}} = -\frac{1}{2} v_{on}^2 C_{\text{eq},E\text{-sy2}}\Big|_{v_{on}}^{0}\,, \tag{3.53}$$

$$\Delta E_{c\text{-sy3-}} = \frac{1}{2} v_{on}^2 C_{\text{eq},E\text{-sy3-}}\Big|_{0}^{v_{on}}\,, \tag{3.54}$$

$$\Delta E_{c\text{-trII}} = \Delta E_{c\text{-sy1}} + \Delta E_{c\text{-sy2}} + \Delta E_{c\text{-sy3-}}\,. \tag{3.55}$$

Now, the energy required from the inductor, L_p, is given by

$$E_{L_p\text{-trII}} = E_{s\text{-trII}} - \Delta E_{c\text{-trII}}\,, \tag{3.56}$$

and finally, the magnitude of the minimum tank current required to achieve ZVS during the switching transition in the T-type bridge is calculated as

$$I_{x\text{-min-zvs-trII}} = \sqrt{\frac{2\left|E_{L_p\text{-trII}}\right|}{L_p}}\,. \tag{3.57}$$

Furthermore, the ZVS time for transition II is expressed as:

$$t_{\text{zvs-trII}} = \frac{2\,v_{on}\left(C_{\text{eq},Q\text{-sy1}}\Big|_{v_{po}}^{v_{pn}} + C_{\text{eq},Q\text{-sy2}}\Big|_{v_{on}}^{0} + C_{\text{eq},Q\text{-sy3-}}\Big|_{0}^{v_{on}}\right)}{I_{x\text{-min-zvs-trII}}}, \tag{3.58}$$

and can be further modified if the tank current exceeds the minimum ZVS current required during transition II, as given below:

$$t_{\text{ex-zvs-trII}} = \frac{I_{x\text{-trII}} - \sqrt{I_{x\text{-trII}}^2 - \omega_s I_{xm}\, I_{x\text{-min-zvs-trII}}\, t_{\text{zvs-trII}}}}{\omega_s I_{xm}}\,, \tag{3.59}$$

where $I_{x\text{-trII}}$ denotes the tank current at the beginning of transition II.

Requirement for Delay Time (T_{stg})

As discussed earlier, an intentional time delay, T_{stg}, is introduced between transitions I and II. If this delay is not provided, the MOSFETs $\mathbf{S}_{\text{y1}}$ and $\mathbf{S}_{\text{y3}}^{-}$ turn off simultaneously, while $\mathbf{S}_{\text{y2}}$ and $\mathbf{S}_{\text{y3}}^{+}$ turn on at the same instant after the dead time. For ZVS turn-on of $\mathbf{S}_{\text{y2}}$ and $\mathbf{S}_{\text{y3}}^{+}$, the output capacitances C_{oss} of these devices must discharge during the dead time prior to switching on. As detailed in Table 3.2, the C_{oss} of $\mathbf{S}_{\text{y2}}$ should discharge from v_{pn} to zero, and that of $\mathbf{S}_{\text{y3}}^{+}$ should discharge from v_{po} to zero. Since $\mathbf{S}_{\text{y3}}^{+}$ is common-source connected with $\mathbf{S}_{\text{y3}}^{-}$, their output capacitances are effectively connected in series. Compared to the single output capacitance on the top and bottom sides of the T-type bridge, this series configuration causes the rate of decrease of $v_{ds\text{-sy3+}}$ to be approximately half that of $v_{ds\text{-sy2}}$. When $v_{po} = v_{on} = {}^{v_{pn}}\!/_{2}$, both $v_{ds\text{-sy3+}}$ and $v_{ds\text{-sy2}}$ can reach zero by discharging their respective C_{oss} using energy from the tank inductor, L_p. However, in the unfolding-based topology, v_{po} and v_{on} are not always equal to ${}^{v_{pn}}\!/_{2}$, as discussed in Section 3.2. When $v_{po} >$

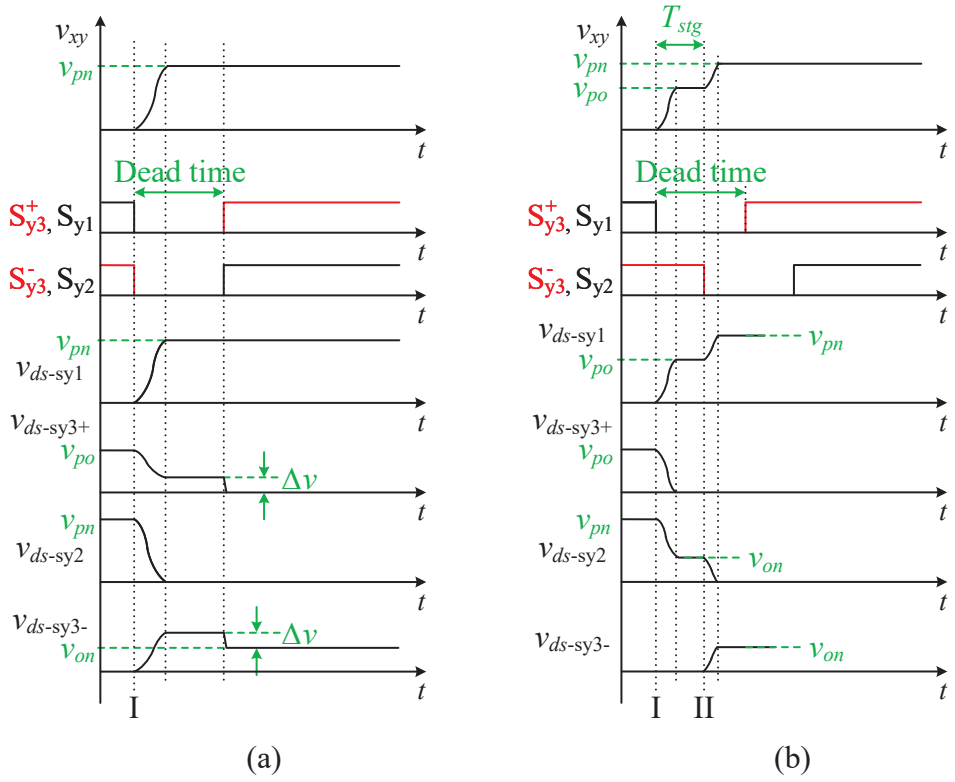


Fig. 3.16: T-type bridge output voltage, v_{xy}, switching pattern, and drain-to-source voltages, v_{ds}, of the leg-y MOSFETs when (a) the delay time, T_{stg}, is disregarded, and transitions I and II overlap, leading to partial ZVS turn-on of $\mathbf{S}^+_{y3}$; and (b) a delay time, T_{stg}, is introduced between transitions I and II, resulting in complete ZVS turn-on of $\mathbf{S}^+_{y3}$.

$v_{pn}/2$, the slower decrease rate of $v_{ds\text{-}sy3+}$ causes $v_{ds\text{-}sy2}$ to reach zero first. This bypasses the tank current through the body diode of $\mathbf{S}_{y2}$ and leads to partial ZVS turn-on of $\mathbf{S}^+_{y3}$, as shown in Fig. 3.16(a).

By introducing a delay time of T_{stg} between transitions I and II, the series-connected MOSFETs $\mathbf{S}^+_{y3}$ and $\mathbf{S}^-_{y3}$ are prevented from turning on/off simultaneously. This ensures that MOSFET $\mathbf{S}^+_{y3}$ undergoes ZVS turn-on first during transition I, followed by MOSFET $\mathbf{S}_{y2}$ during transition II, as depicted in Fig. 3.16(b). The delay time T_{stg} should be greater than the ZVS time required for transition I, given by either $t_{\text{zvs-trI}}$ or $t_{\text{ex-zvs-trI}}$. It should be noted that the delay time T_{stg} is necessary when $v_{po} \neq v_{pn}/2$ and can be set to zero when $v_{po} = v_{on} = v_{pn}/2$, which occurs at grid angles $\theta_{\text{grid}} = \frac{\pi}{6} + (k-1)\frac{\pi}{3}$, as discussed above. Therefore, in this work, a staggered time delay is implemented that is kept greater than

Table 3.3: Analytical RMS currents of the T-type bridge.

Current	**Expression for $d_p > d_n$**
$I_{\text{rms-top}}$	$\left(\frac{I_{xm}}{2}\right)\sqrt{(2-d_p)+\left(\frac{\sin(\pi d_p)\cos(\pi d_p-2\theta_x)}{\pi}\right)}$
$I_{\text{rms-bot}}$	$\left(\frac{I_{xm}}{2}\right)\sqrt{d_n-\left(\frac{\sin(\pi d_n)\cos(\pi d_n-2\theta_x)}{\pi}\right)}$
$I_{\text{rms-mid}}$	$\left(\frac{I_{xm}}{2}\right)\sqrt{(d_p-d_n)-\left(\frac{\cos(\pi(d_p+d_n)-2\theta_x)\sin(\pi(d_p-d_n))}{\pi}\right)}$
Current	**Expression for $d_p < d_n$**
$I_{\text{rms-top}}$	$\left(\frac{I_{xm}}{2}\right)\sqrt{d_p-\left(\frac{\sin(\pi d_p)\cos(\pi d_p-2\theta_x)}{\pi}\right)}$
$I_{\text{rms-bot}}$	$\left(\frac{I_{xm}}{2}\right)\sqrt{(2-d_n)+\left(\frac{\sin(\pi d_n)\cos(\pi d_n-2\theta_x)}{\pi}\right)}$
$I_{\text{rms-mid}}$	$\left(\frac{I_{xm}}{2}\right)\sqrt{(d_n-d_p)-\left(\frac{\cos(\pi(d_n+d_p)-2\theta_x)\sin(\pi(d_n-d_p))}{\pi}\right)}$

$t_{\text{zvs-trI}}$ or $t_{\text{ex-zvs-trI}}$, but is also reduced to zero near the grid angles where $v_{po} = v_{on} = {}^{v_{pn}}\!/_{2}$. Further details on the delay time are given in [30].

3.5.2 Conduction Loss Analysis of the T-Type Bridge

Accurate conduction loss estimation of the T-type bridge is essential for optimizing the reactive behavior of the *LCC* tank and ensuring that conduction losses remain within acceptable limits. This analysis is particularly important for selecting an appropriate capacitor value, C_{ps}, which defines the overall reactive nature of the tank, as given in (3.30). This estimation requires analytical computation of the RMS currents in the T-type bridge. These currents are summarized in Table 3.3 for both $d_p > d_n$ and $d_p < d_n$. Here, $I_{\text{rms-top}}$ corresponds to the RMS current through the top-side MOSFETs, $\mathbf{S}_{\text{x1}}$ and $\mathbf{S}_{\text{y1}}$, while $I_{\text{rms-bot}}$ corresponds to the RMS current through the bottom-side MOSFETs, $\mathbf{S}_{\text{x2}}$ and $\mathbf{S}_{\text{y2}}$. The

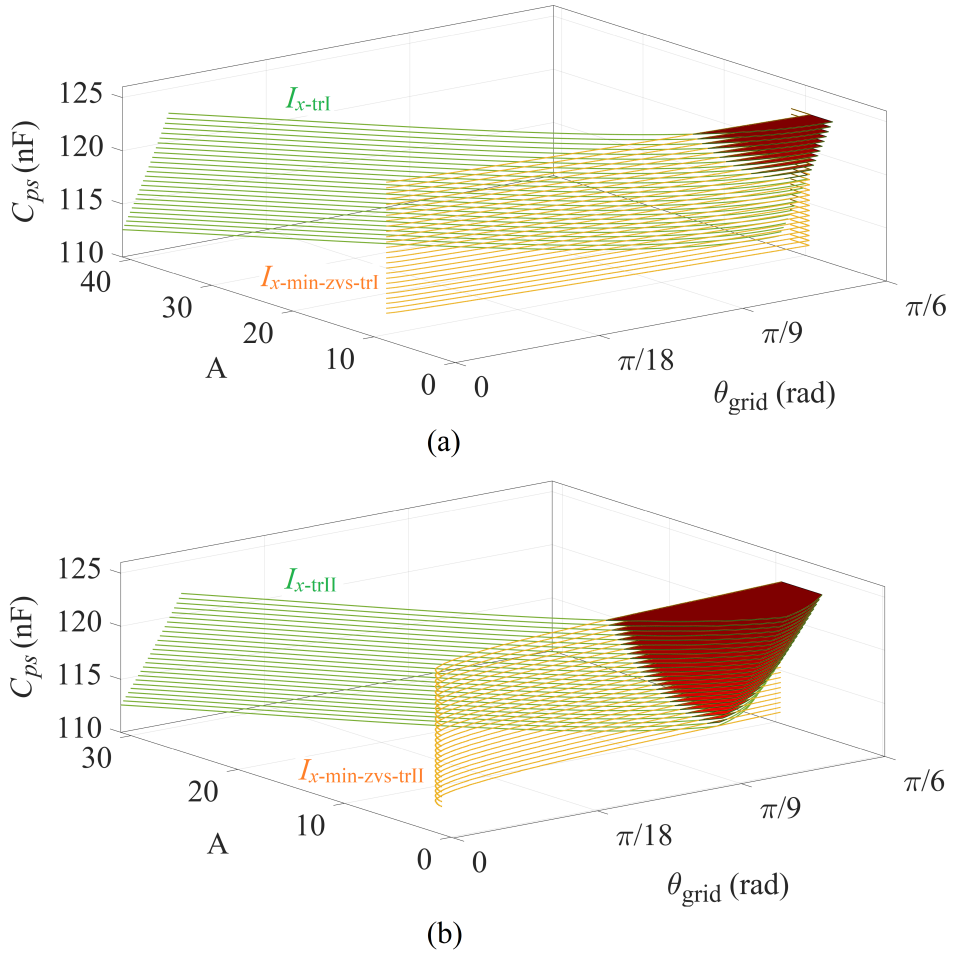


Fig. 3.17: Comparison of the actual tank current magnitude, i_x (green plots), for various values of C_{ps} with the minimum current required (orange plots) to achieve ZVS of the MOSFETs in the T-type bridge during leading-edge transitions: (a) I and (b) II. Red-shaded regions indicate insufficient tank current, resulting in partial ZVS or hard-switching. Based on this analysis, C_{ps} values below 113 nF are found to be suitable for ensuring complete ZVS during both transitions.

term $I_{\text{rms-mid}}$ denotes the RMS current through the common-source-connected MOSFETs, namely $\mathbf{S}^{+}_{\text{x3}}$, $\mathbf{S}^{-}_{\text{x3}}$, $\mathbf{S}^{+}_{\text{y3}}$, and $\mathbf{S}^{-}_{\text{y3}}$.

3.5.3 Optimized Selection of the Capacitor C_{ps}

The ZVS analysis of the T-type bridge during transitions I and II, together with conduction loss estimation, can be used to determine an optimized value for the *LCC* tank capacitor, C_{ps}, which defines the reactive behavior of the tank. To achieve this, the value

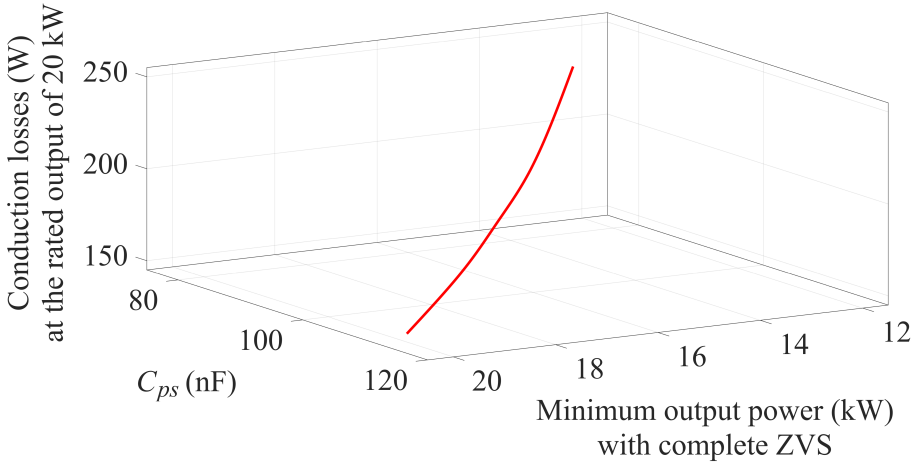


Fig. 3.18: Conduction losses of the T-type bridge at rated output power for various values of C_{ps}, combined with the minimum output power required to achieve ZVS of the T-type bridge MOSFETs. This combined analysis aids in selecting an optimal C_{ps} that ensures ZVS while maintaining acceptable conduction losses.

of C_{ps} is swept, and the corresponding magnitude of the tank current, i_x, during transitions I and II is calculated over the grid cycle using the FHA, since the current remains nearly sinusoidal. Due to the periodic nature of the T-type bridge input dc-link voltages over the grid cycle, as depicted in Fig. 3.3, the tank current behavior also exhibits periodicity over the grid cycle. As a result, the analysis can be limited to the grid angle range $0 \leq \theta_{\text{grid}} < \frac{\pi}{6}$. The computed tank current magnitudes for these transitions are then compared with the minimum currents required to achieve ZVS of the T-type bridge MOSFETs, obtained from (3.44) and (3.57), as shown in Figs. 3.17(a) and 3.17(b) for transitions I and II, respectively. The red-shaded regions in these plots indicate unsuitable values of C_{ps}, where the reactive behavior of the tank is insufficient to achieve ZVS, as the corresponding tank current magnitudes during transitions fall below the required threshold. Based on this analysis, capacitor values below 113 nF are found to be suitable for ensuring ZVS operation during both transitions I and II. To finalize the value of the capacitor, conduction losses of the T-type bridge at the rated output power are calculated for various values of C_{ps}. Additionally, this conduction loss analysis is combined with the minimum output power required to achieve ZVS of the T-type bridge MOSFETs. The combined result is shown in Fig. 3.18. Based on the ZVS and conduction loss analyses presented in Figs. 3.17 and 3.18,

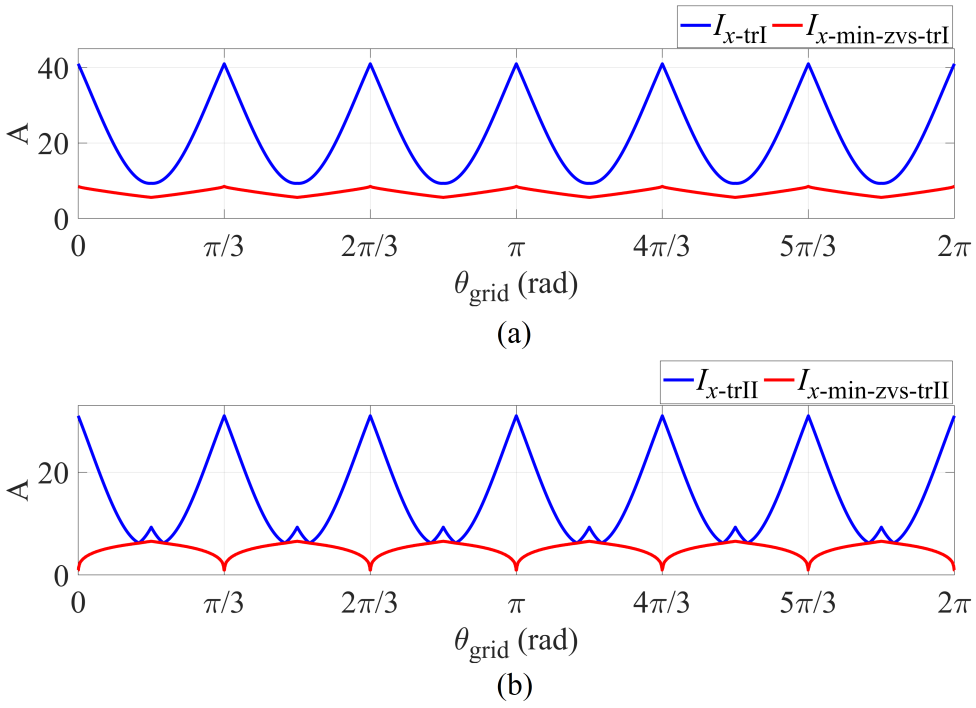


Fig. 3.19: Magnitude of the tank current, i_x, along with the minimum current required to achieve ZVS of the T-type bridge MOSFETs during (a) transition I and (b) transition II, for the selected value of the capacitor C_{ps}.

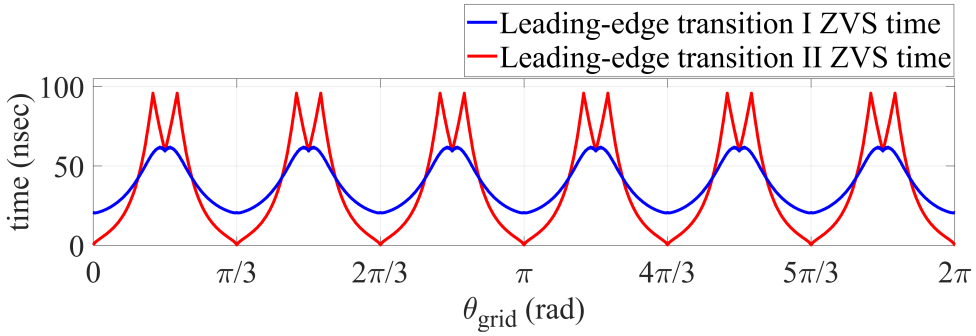


Fig. 3.20: ZVS times during transitions I and II, used to determine suitable values for the dead time and the delay time, T_{stg}, for hardware verification.

an optimized value of C_{ps} is selected as 112.1 nF. This value ensures a suitable reactive behavior of the LCC tank for achieving complete ZVS of the MOSFETs while maintaining acceptable conduction losses at rated output power.

Finally, for the selected value of the capacitor C_{ps}, the magnitude of the tank current, i_x, along with the minimum current required to achieve ZVS of the T-type bridge MOSFETs,

Table 3.4: Hardware parameters of the unfolding-based ac-dc converter.

Parameter	**Value**
Nominal input voltage	480 V (l-l), 60 Hz
Battery voltage	649 V - 755 V
Output power	20 kW
T-type bridge switching frequency	85 kHz
Unfolder switching frequency	Diodes - 60 Hz, IGBTs - 120 Hz
Grid inductance (L_g)	600 μH
Dc-link capacitors (C_{po}, C_{on}, C_{pn})	4.5 μF
L_p	29.3 μH
C_{pp}	120.1 nF
C_{ps}	112.1 nF
Cantilever model-based isolation parameters	L_l = 37.5 μH, L_m = 996.2 μH
C_{out}	161.5 μF

is illustrated in Figs. 3.19(a) and 3.19(b) for transitions I and II, respectively. It can be observed that the tank current remains higher than the minimum required for ZVS throughout the grid cycle for both transitions I and II. In addition, the corresponding ZVS times during these transitions are presented in Fig. 3.20. These ZVS time calculations are particularly important for determining suitable values of the dead time and the delay time, T_{stg}, to be used during the hardware implementation and verification process.

3.6 Experimental Validation

A 20-kW hardware prototype of an unfolding-based ac-dc system incorporating a T-type bridge-based dc-dc converter, as shown in Fig. 3.21, is developed and tested to validate the proposed leading-edge-aligned modulation strategy. The key hardware parameters are summarized in Table 3.4. The 3-ϕ Unfolder is designed using IXYS WT1263YC200 diodes and Infineon FZ1200R17KF6C-B2 IGBTs. The T-type bridge is implemented using Onsemi NVH4L020N120SC1 and NVH4L040N120SC1 MOSFETs, where the NVH4L020N120SC1 devices are employed in the top and bottom positions, and the NVH4L040N120SC1 devices

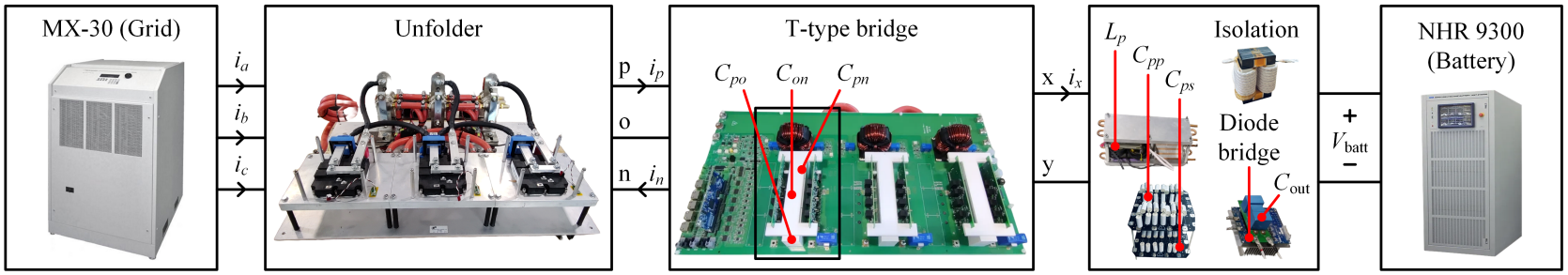


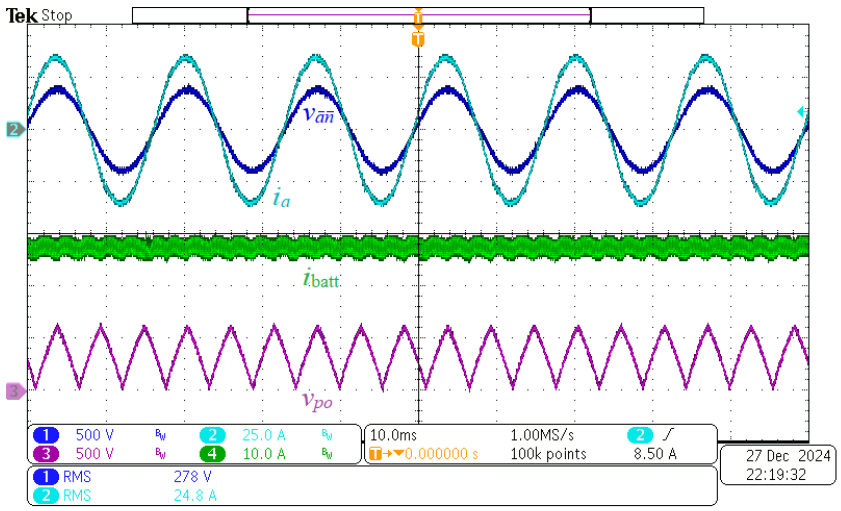
Fig. 3.21: A 20-kW hardware setup of an unfolding-based ac-dc system with a T-type bridge-based dc-dc converter. A California Instruments MX-30 emulates the grid, while an NH Research 9300 functions as the EV battery load.

serve as common-source-connected switches. The body diodes of CREE CCS050M12CM2 MOSFETs are used to construct the secondary-side diode bridge. Grid emulation is carried out using a California Instruments MX-30, while an NH Research 9300, operated in battery mode, emulates the EV battery at the output. The proposed leading-edge-aligned modulation strategy and the corresponding closed-loop control architecture are implemented using the TMS320F28379D microcontroller.

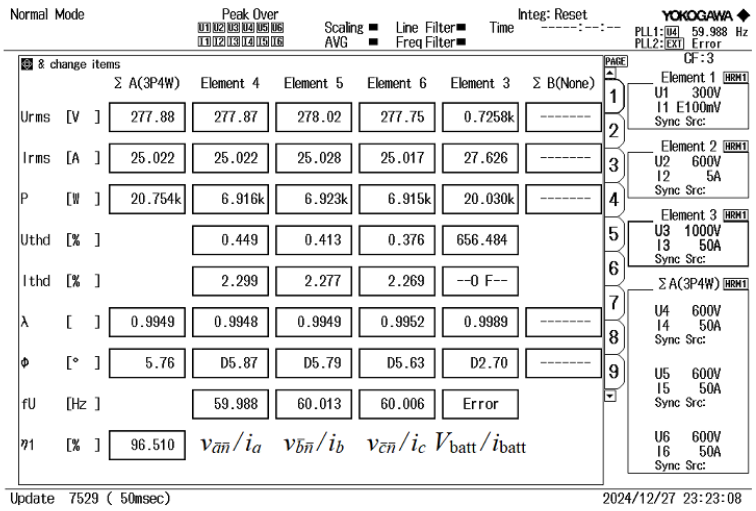
Hardware verification begins with validating the steady-state operation of the proposed leading-edge-aligned modulation strategy by observing the input grid-side, output, and resonant tank waveforms. The ZVS operation of the T-type bridge MOSFETs is also confirmed. Subsequently, the results for ac-dc efficiency and grid current THD are presented. Transient response results are included to evaluate dynamic operation. Finally, the performance of the ac-dc system using the proposed modulation, enabling complete ZVS of the T-type bridge MOSFETs, is compared against the center-aligned modulation previously employed in Chapter 2, which results in hard-switching.

3.6.1 Steady-State Operation

Fig. 3.22(a) presents the steady-state waveforms of the Unfolder input ac phase-a voltage $v_{\bar{a}\bar{n}}$, input phase-a current i_a, dc-link voltage v_{po}, and output battery load current i_{batt} at the rated output power of 20 kW. The corresponding power analyzer data recorded using the Yokogawa WT1806E is shown in Fig. 3.22(b). These results confirm that the proposed leading-edge-aligned modulation strategy, combined with the closed-loop control, achieves a high-quality grid current waveform with 2.3% THD and leads to an ac-dc efficiency of 96.51%. Figs. 3.23(a), 3.23(b), and 3.23(c) depict the T-type bridge output voltage v_{xy} and the tank current i_x for three different dc-link voltage scenarios: (i) $v_{po} = 512$ V and $v_{on} = 130$ V, (ii) $v_{po} = 413$ V and $v_{on} = 260$ V, and (iii) $v_{po} = v_{on} = {}^{v_{pn}}\!/_{2} = 339.5$ V. A time delay, T_{stg}, of 200 ns is introduced between transitions I and II when $v_{po} \neq v_{on} \neq {}^{v_{pn}}\!/_{2}$, and is gradually reduced to zero as v_{po} and v_{on} approach ${}^{v_{pn}}\!/_{2}$. The T-type bridge output voltage, v_{xy}, and current, i_x, over the grid cycle are shown in Fig. 3.24. Although v_{xy} exhibits a 6-pulse waveform due to unfolding operation, its fundamental component, v_{xy1},

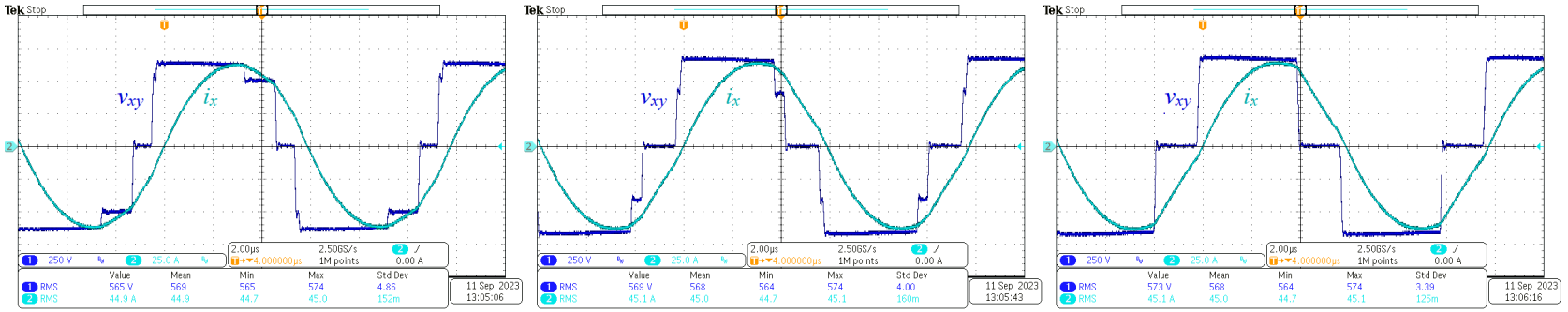


(a)



(b)

Fig. 3.22: (a) Steady-state waveforms of the Unfolder input ac phase-a voltage $v_{\bar{a}\bar{n}}$, input phase-a current i_a, dc-link voltage v_{po}, and output battery load current i_{batt} at the rated output power of 20 kW; (b) power analyzer data obtained using the Yokogawa WT1806E, demonstrating a low grid current THD of 2.3% and an ac-dc efficiency of 96.51% at the rated output power of 20 kW.



(a) (b) (c)

Fig. 3.23: T-type bridge output voltage v_{xy} and the tank current i_x for three different dc-link voltage scenarios: (a) $v_{po} = 512$ V and $v_{on} = 130$ V, (b) $v_{po} = 413$ V and $v_{on} = 260$ V, and (c) $v_{po} = v_{on} = {}^{v_{pn}}/_{2} = 339.5$ V. A time delay, T_{stg}, of 200 ns is introduced between transitions I and II when $v_{po} \neq v_{on} \neq {}^{v_{pn}}/_{2}$, as shown in cases (a) and (b), and is gradually reduced to zero as v_{po} and v_{on} approach ${}^{v_{pn}}/_{2}$, as shown in case (c).

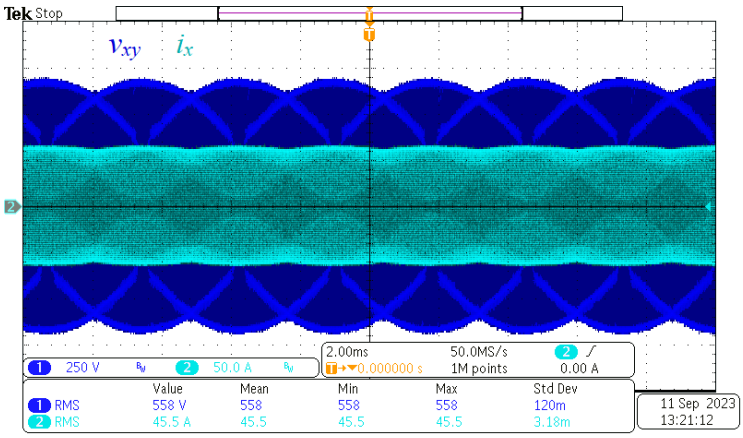


Fig. 3.24: T-type bridge output voltage, v_{xy}, and current, i_x, over the grid cycle.

remains constant for a given power level, as discussed in Section 3.3.

The appropriate magnitude and polarity of the tank current, i_x, achieved using the leading-edge-aligned modulation strategy for various voltage transitions within a switching period, are illustrated in Fig. 3.25. This figure captures the tank waveforms across the entire grid cycle using the infinite persistence mode of the Tektronix MDO3014 oscilloscope. A zoomed-in view highlighting critical transitions I and II is also included, demonstrating the appropriate tank current that enables ZVS for the T-type bridge MOSFETs throughout the grid cycle. Additionally, Fig. 3.25 is represented as a state-plane diagram in Fig. 3.26 to further emphasize the appropriate magnitude and polarity of i_x during switching transitions across the grid cycle. Finally, the ZVS operation of the T-type bridge MOSFETs is verified by simultaneously monitoring the drain-to-source voltage, v_{ds}, and the gate-to-source voltage, v_{gs}, waveforms during transitions I and II, as depicted in Fig. 3.27. It can be observed that $v_{ds\text{-sy3+}}$ and $v_{ds\text{-sy2}}$ fall to zero before the corresponding gate voltages rise to turn on $\mathbf{S}_{\text{y3}}^{+}$ and $\mathbf{S}_{\text{y2}}$, confirming the ZVS operation of the MOSFETs during these two critical transitions.

The ac-dc efficiency curve of the hardware prototype using the proposed leading-edge-aligned modulation at various power levels is shown in Fig. 3.28, demonstrating a peak efficiency of 96.51% at the rated output power of 20 kW. Additionally, the corresponding grid current THD across these power levels is presented in Fig. 3.29. The proposed control

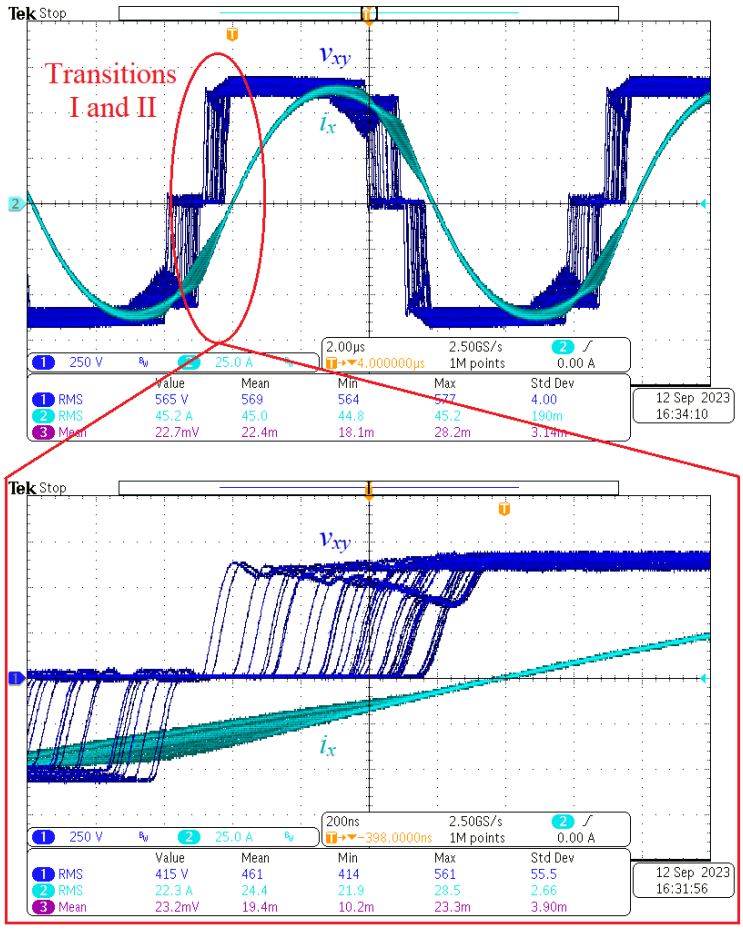


Fig. 3.25: Variation of the T-type bridge output voltage v_{xy} and tank current i_x over a full grid cycle, captured using the infinite persistence mode of a Tektronix MDO3014 oscilloscope. Zoomed-in waveforms of the critical transitions I and II are also shown.

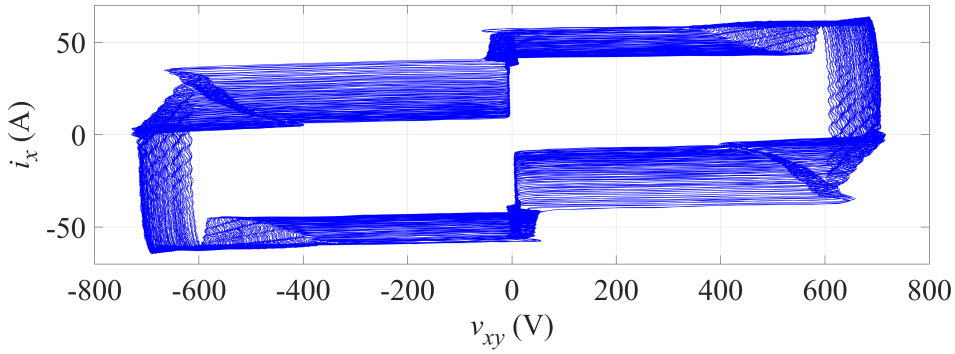


Fig. 3.26: State-plane representation of the tank voltage and current, corresponding to Fig. 3.25, highlighting the proper magnitude and polarity of i_x during switching transitions throughout the grid cycle for ZVS of the T-type bridge.

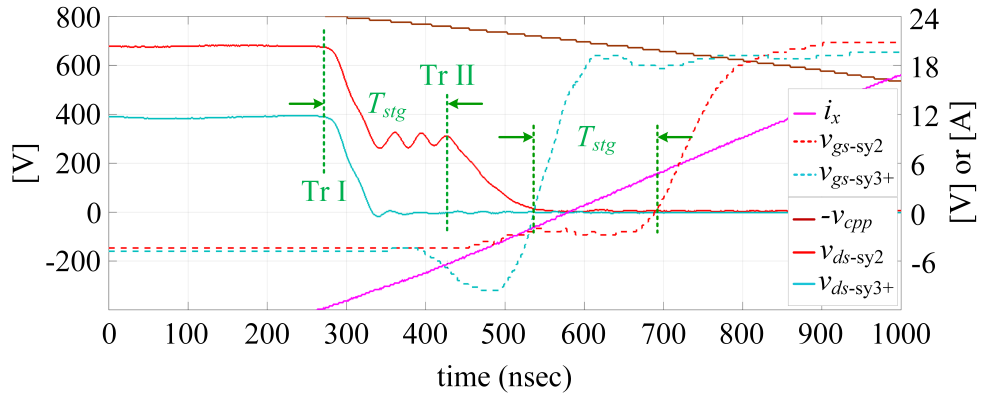


Fig. 3.27: Verification of ZVS operation for the T-type bridge MOSFETs by capturing the drain-to-source voltage, v_{ds}, and gate-to-source voltage, v_{gs}, during transitions I and II.

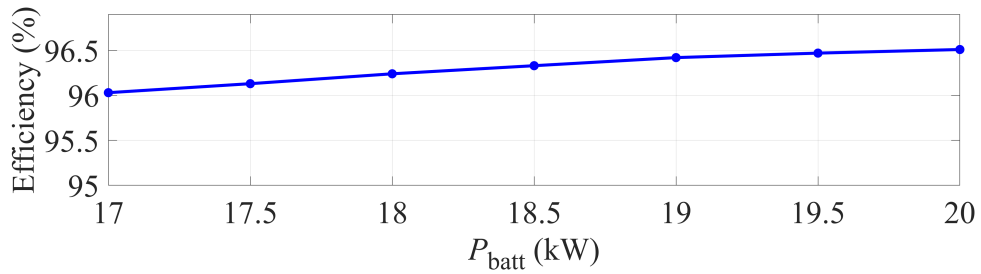


Fig. 3.28: Measured ac-dc efficiency of the hardware prototype using the proposed leading-edge-aligned modulation strategy across various power levels. A peak efficiency of 96.51% is achieved at the rated output power of 20 kW.

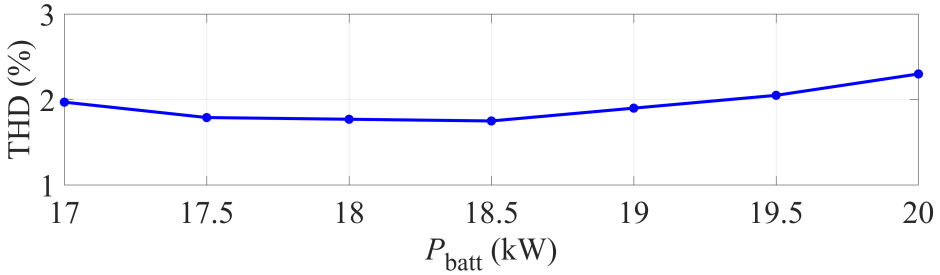
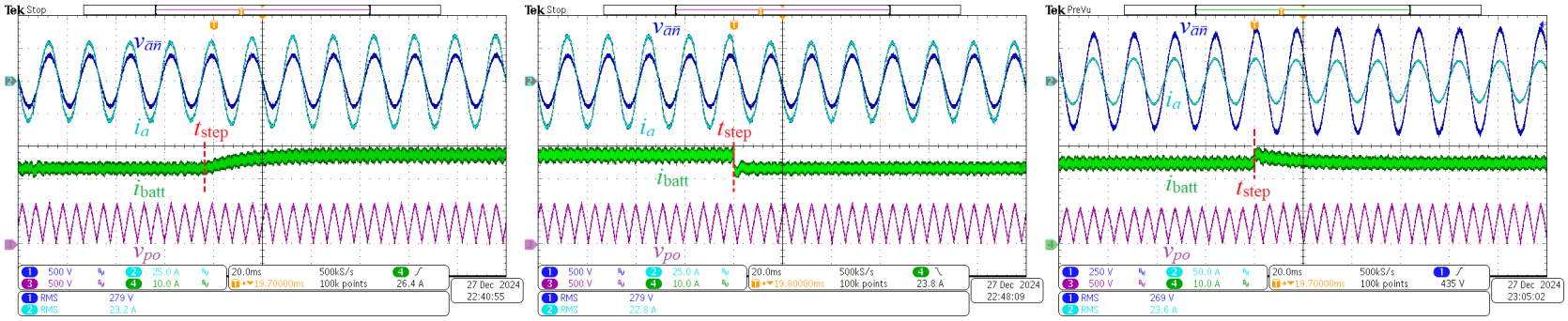


Fig. 3.29: Measured grid current THD of the hardware prototype using the proposed leading-edge-aligned modulation strategy across various power levels. A high-quality grid current waveform is maintained throughout the power variation.

strategy ensures low THD across various power levels, validating the effectiveness of the modulation scheme.



(a) (b) (c)

Fig. 3.30: Transient performance of the proposed closed-loop control architecture is verified by applying: (a) a step change in outer-loop battery current reference, $i_{\text{batt-ref}}$, from 23.6 A to 27.8 A, increasing output power from 17 kW to 20 kW; (b) a step change in the inner-loop reference of the peak grid current, I_{gm}, from 34.8 A to 29.6 A, reducing output power from 20 kW to 17 kW; and (c) a 10.8% step increase in Unfolder phase-a input voltage from 250 V to 277 V, with closed-loop control maintaining i_{batt} and output power properly with acceptable response time.

3.6.2 Transient Responses

To verify the performance of the proposed closed-loop control architecture, designed with appropriate bandwidth levels as shown in Figs. 3.10 and 3.13, the transient responses of the ac-dc system are evaluated under three scenarios. In the first scenario, the battery current reference, $i_{\text{batt-ref}}$, in the outer loop is subjected to a step change from 23.6 A to 27.8 A, resulting in an increase in output power from 17 kW to 20 kW, as shown in Fig. 3.30(a). The hardware response confirms stable outer-loop operation. In the second scenario, the reference for the peak grid current, I_{gm}, is changed from 34.8 A to 29.6 A, reducing the output power from 20 kW to 17 kW. Here, the outer loop is bypassed, and the inner-loop reference is directly modified. The hardware response in Fig. 3.30(b) confirms that the inner loops operate properly under such transient conditions. Finally, in the third scenario, a 10.8% step change is applied to the Unfolder phase-a ac input voltage, increasing it from 250 V to 277 V. The closed-loop control maintains the load current and output power while ensuring acceptable transient response time, as shown in Fig. 3.30(c).

3.6.3 Comparison of Leading-Edge-Aligned and Center-Aligned Modulation Strategies

Fig. 3.31 compares the measured ac-dc efficiency of the proposed leading-edge-aligned modulation, which enables complete ZVS of the T-type bridge MOSFETs, with a previously utilized center-aligned modulation resulting in hard-switching. The efficiency data for the center-aligned modulation is reproduced from Chapter 2. Both modulation strategies have been implemented on the same 20 kW hardware platform. The proposed leading-edge-aligned modulation achieves up to 0.76% higher efficiency at 20 kW output power. This improvement may result from a combination of factors, including reduced switching losses due to ZVS operation of the T-type bridge.

Moreover, the radiated EMI of the T-type bridge-based dc-dc converter within the ac-dc system is measured using an antenna and a Tektronix RSA306B spectrum analyzer, as shown in Fig. 3.32. While the absolute EMI levels may be influenced by measurement bias, the results are primarily intended for comparative analysis between the proposed

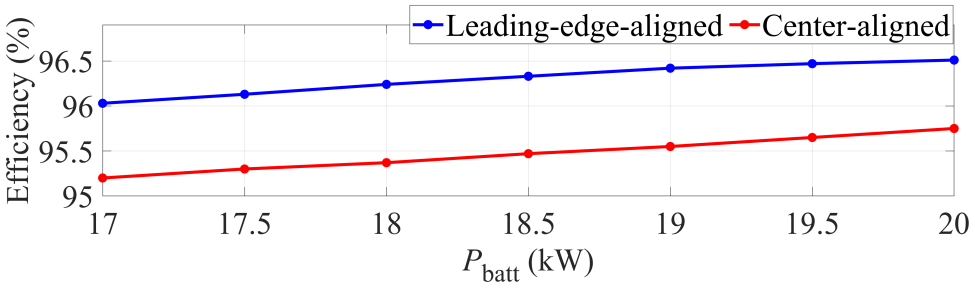


Fig. 3.31: Efficiency comparison between the proposed leading-edge-aligned modulation, which enables ZVS of T-type bridge MOSFETs, and a previously used center-aligned modulation resulting in hard-switching. Data for the center-aligned modulation is reproduced from Chapter 2.

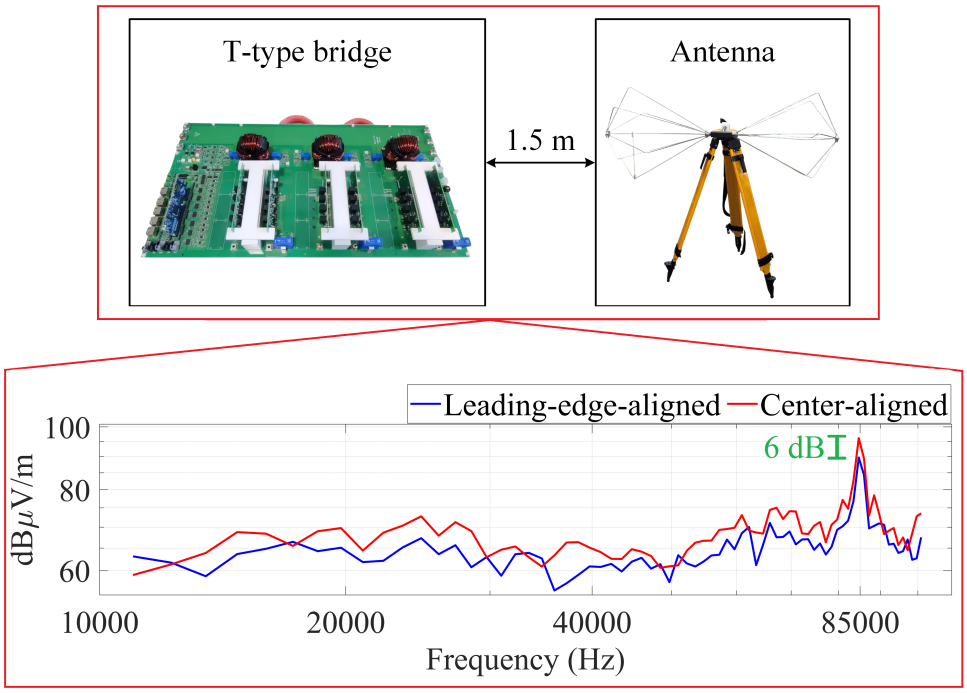


Fig. 3.32: Measured radiated EMI spectra of the T-type bridge-based dc-dc converter with the proposed leading-edge-aligned modulation and the previously used center-aligned modulation. EMI is measured using a Tektronix RSA306B spectrum analyzer and an antenna placed 1.5 m from the converter. While the absolute EMI levels may be affected by measurement biases, the results are primarily intended for comparative analysis.

leading-edge-aligned modulation and the previously used center-aligned modulation. The EMI spectra indicate that the leading-edge-aligned modulation consistently exhibits lower radiated EMI, attributed to the ZVS operation of the T-type bridge. A reduction of approximately 6 dB, equivalent to a twofold decrease, is observed at the 85 kHz switching

frequency.

3.7 Conclusion

This chapter presents a detailed investigation of a leading-edge-aligned modulation strategy in combination with a closed-loop control architecture to achieve ZVS in a resonant T-type bridge used within an unfolding-based ac-dc conversion system for WPT applications. Various modulation strategies, including center-aligned and leading-edge-aligned, are analyzed, highlighting the importance of the leading-edge-aligned approach in enabling ZVS of the T-type bridge MOSFETs. The study confirms that accurate alignment of the leading edges of the T-type bridge output quasi-square voltages is essential for maintaining ZVS throughout the grid cycle. Analytical duty ratio expressions are derived and modulated by a multi-loop closed-loop control architecture to simultaneously achieve PFC and output power regulation through control of the HF T-type bridge operating at 85 kHz. The outer loop regulates output power, while two inner loops maintain sinusoidal grid currents. Small-signal modeling is employed to analyze system dynamics and ensure appropriate bandwidth levels for each control loop, ensuring robust and stable dynamic performance under varying operating conditions. Additionally, a detailed ZVS analysis is presented to examine critical switching transitions, incorporating the nonlinear behavior of the MOSFET output capacitance through energy- and charge-equivalent capacitors. ZVS times are calculated to determine appropriate timing parameters for hardware validation. The tank design is then guided by this accurate ZVS analysis, combined with conduction loss calculations, to ensure correct polarity and sufficient magnitude of the tank current during switching transitions, while also minimizing conduction losses.

Finally, the proposed leading-edge-aligned modulation strategy, along with its control architecture and comprehensive ZVS analysis, is experimentally validated on a 20 kW, 480 V grid-tied ac-dc hardware prototype. The results demonstrate complete ZVS operation throughout the grid cycle, achieving a peak ac-dc efficiency of 96.51% and a low grid current THD of 2.3% at rated output power. Furthermore, a comparison with the center-aligned modulation strategy, which exhibits hard-switching and is implemented on the same

hardware prototype, shows a 0.76% improvement in efficiency and a 6 dB reduction (corresponding to a twofold decrease) in radiated EMI with the proposed leading-edge-aligned modulation.

CHAPTER 4

GRID CURRENT IMPROVEMENT & HIGH-BANDWIDTH CONTROL USING CURRENT EMULATION-BASED ACTIVE DAMPING

4.1 Introduction

Chapter 2 and Chapter 3 have employed an unfolding-based ac-dc system with a T-type bridge-based dc-dc converter due to its dual-input voltage processing capability, which enables efficient utilization of semiconductor devices. The T-type bridge-based dc-dc converter maintains grid-side PFC, regulates output power, and provides galvanic isolation. Operating the Unfolder at a maximum of twice the grid frequency with negligible switching losses, while centralizing all control functions within the dc-dc converter, enhances power density, efficiency, and design simplicity.

Despite their many advantages, unfolding-based topologies encounter two major challenges: input grid current distortion and instability caused by LC-resonance. Grid current distortion arises at the sector boundaries of the grid voltages during each grid cycle, primarily due to the HF operation of the dc-dc converter that generates HF currents bypassed to the dc-link capacitors. These distortions increase the THD of the ac input currents. Prior works [19, 56, 74] have addressed this issue by controlling the Unfolder or its third-harmonic injection network. A passive damping network has also been suggested, which affects the cost, efficiency, and power density of the system. Although effective, these solutions tend to minimize the advantages of the low-frequency-switched Unfolder. In addition, unfolding-based converters are prone to LC-resonance issues arising from the interaction between the grid inductance and dc-link capacitors. This resonance detrimentally affects closed-loop control by reducing the phase margin and rendering the closed-loop system unstable [58]. While the utilization of passive physical damping networks can alleviate this control challenge [75], their integration results in heightened system costs and reduced power

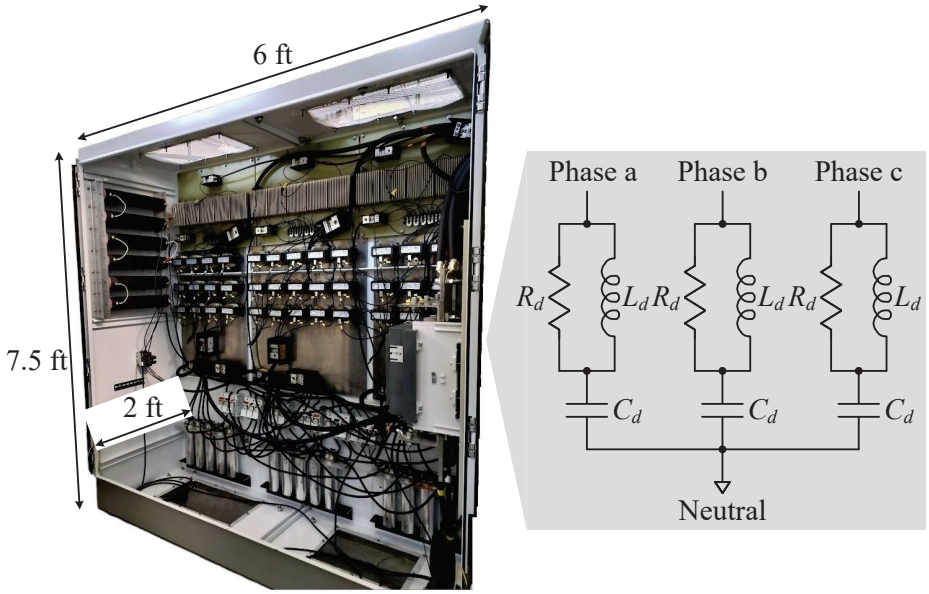


Fig. 4.1: A 3-ϕ passive damping network, incorporating RLC components, utilized in the development of a 1-MW unfolding-based EV charger at Utah State University's power electronics laboratory.

density. Also, the approach of parallel connection of physical damping resistors across input inductive filters, as done in [19,44], becomes unfeasible when utilizing the inherent grid inductance for PFC, rather than incorporating additional inductive filters. Furthermore, the dimensions and costs of such passive networks experience a substantial increase with higher power levels, as exemplified in Fig. 4.1. The figure illustrates a cabinet with a passive damping network comprising RLC components with dimensions of 6 ft (L) $\times$ 2 ft (W) $\times$ 7.5 ft (H), developed for a 1-MW unfolding-based EV-battery charging system [12], without incorporating the contributions presented in this work. The overall cost of this cabinet with a 3-ϕ passive damping network is around \$15,000.

This chapter provides a comprehensive analysis of the fundamental cause of the current distortion problem. An equivalent circuit model is developed to facilitate a better understanding of the issue. Furthermore, a control-based solution is proposed that leverages the HF dc-dc converter through a current emulation technique [55, 76–78] to charge/discharge the dc-link capacitors without disturbing the Unfolder. Moreover, given the severity of the stability-related problem, this chapter undertakes a comprehensive examination of

the unwanted LC resonance through the application of the EET as introduced by R. D. Middlebrook [79–81]. EET is an effective tool for design-oriented analysis, aiding in the examination of complex circuits and systems to derive manageable equations crucial for design purposes. This theorem allows one to quantify the impact of the additional impedance element on any transfer function of interest [58], eliminating the need for re-solving the system. In this study, an unfolding-based topology with a T-type converter and an LCC resonant tank is utilized. This configuration heightens the complexity of deriving the plant transfer function due to the increased number of tank elements and the variation of the pulsating input voltages of the T-type bridge. Additionally, incorporating the interaction between the grid inductance and dc-link capacitors further complicates the process of deriving the plant transfer function. On the other hand, the application of EET helps to derive the modified plant transfer function with the effect of this LC interaction without solving for the plant transfer function all over again [58, 82–85]. Moreover, in unfolding-based topologies, where the dc-dc converter undergoes variations in dc input voltages and corresponding duty ratios throughout the grid cycle, the extent of the LC-resonance effect on the plant transfer function changes accordingly. Consequently, it becomes imperative to assess this LC-resonance effect over the grid cycle. In this scenario, EET facilitates the identification of the worst-case operating point when the impact of the LC interaction is most pronounced [58, 82, 84], thereby minimizing the effort of performing the analysis throughout the grid cycle. Due to these benefits, the EET becomes an effective and beneficial tool for comprehending and mitigating the adverse effects of the LC resonance on the closed-loop control of unfolding-based converters. The application of the EET-based analytical framework involves deriving the plant transfer function along with the EET parameters. This is accomplished through the phasor transformation-based small-signal modeling given in Chapter 5 and [60–62, 86, 87]. In addition to analyzing the stability-related issue, a control-based approach is presented, involving the utilization of the current emulation technique [68, 88–90] to actively damp the LC resonance. This is achieved by modifying the control structure of the HF T-type bridge-based dc-dc converter employed after the Unfolder. This solution eliminates the

requirement for physical damping circuits, thereby enhancing power density and reducing system costs.

The efficacy of the proposed current emulation-based active damping approach in mitigating both problems, grid current distortion and stability-related issues, is evaluated using an EV battery charger circuit based on unfolding technology. Simulation results confirm the stable operation of the overall control structure. Subsequently, a hardware prototype is developed and tested, validating the effectiveness of the proposed solution.

4.2 Analysis and Mitigation of Sector Transition Distortions for Unfolding-Based AC-DC Converters

4.2.1 Analysis of Current Distortions at Sector Boundaries

The transition of the switching state from sector 1 ($0° \leq \theta_{grid} < 60°$) to sector 2 ($60° \leq \theta_{grid} < 120°$) on the unfolding side, as shown in Fig. 2.2(d), is selected to understand the cause of sector transition distortion. Conduction paths for the 3-ϕ grid and dc link capacitors (C_{po}, C_{on}, and C_{pn}) currents during sector 1 are shown in Fig. 4.2(a). Only one of the possible conduction paths on the T-type side is shown, and all others are mentioned in [74].

The phasor representation of the input current (i_s) of a dc-dc converter as a function of the output current (i_o) and the switching function (s) can be expressed as,

$$i_s = \Re[s^* i_o] + \Re[s i_o e^{2j\omega_s t}], \tag{4.1}$$

which clearly states that the input current has dc and twice the switching frequency components. The HF components present in the input currents of p and n ports (i_p^{dc} and i_n^{dc}) flow through the dc link capacitors, which leads to HF ripples in the dc link voltages v_{po}, v_{on}, and v_{pn}. Due to these ripples, the soft dc link voltage v_{po}, which is approaching zero in the vicinity of the sector transition, crosses the cut-in voltage of D_{a1} / body-diode of S_{y1}. This leads to an undesirable turn-on of these diodes, which bypasses the dc link capacitor C_{po}

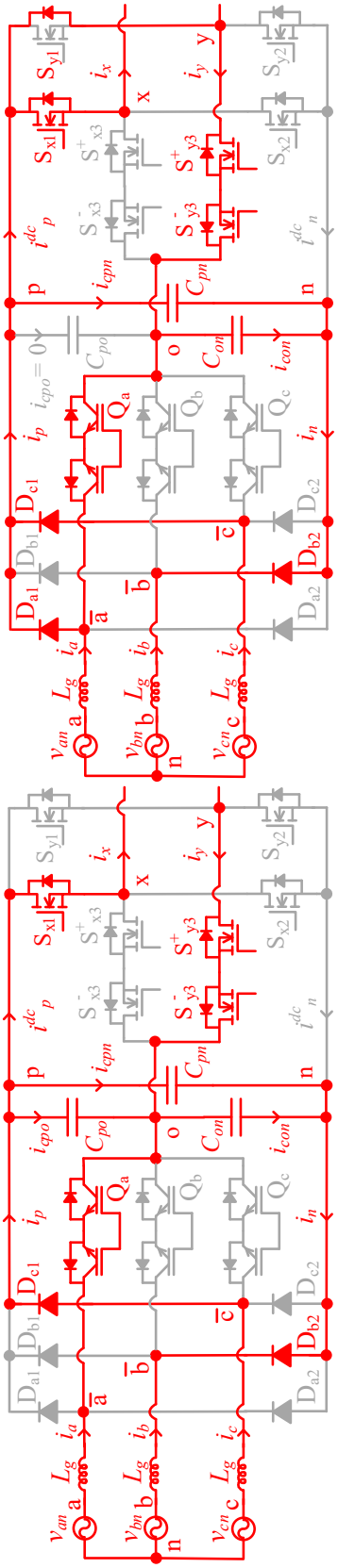


Fig. 4.2: (a) Conduction paths for the 3-ϕ grid, dc link capacitors (C_{po},C_{on}, and C_{pn}), and T-type output currents during sector 1 ($0° \leq \theta_{grid} < 60°$), (b) turn-on of parallel diodes (D_{a1} / body-diode of S_{y1}) during the transition from sector 1 to 2 ($60° \leq \theta_{grid} < 120°$), which bypasses the dc link capacitor (C_{po}) through D_{a1} and Q_a / body-diode of S_{y1}, S^+_{y3}, and S^-_{y3}.

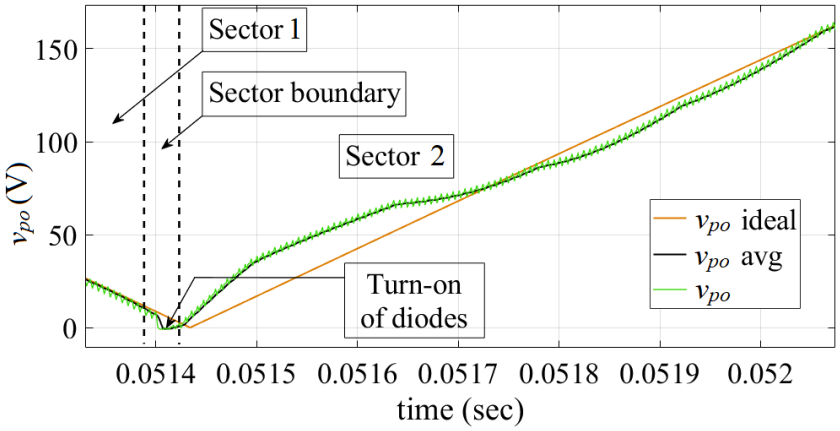


Fig. 4.3: Turn-on of parallel diodes when the dc link voltage (v_{po}) crosses the cut-in voltage of the diodes in the vicinity of the sector transition from 1 to 2. This leads to the bypass of the dc link capacitor (C_{po}), which causes a deviation of the capacitor's average voltage from its ideal value at the sector boundary. Subsequently, the grid voltage charges the capacitor again in sector 2 to track the ideal voltage waveform. This charging current causes oscillations in the dc link voltage.

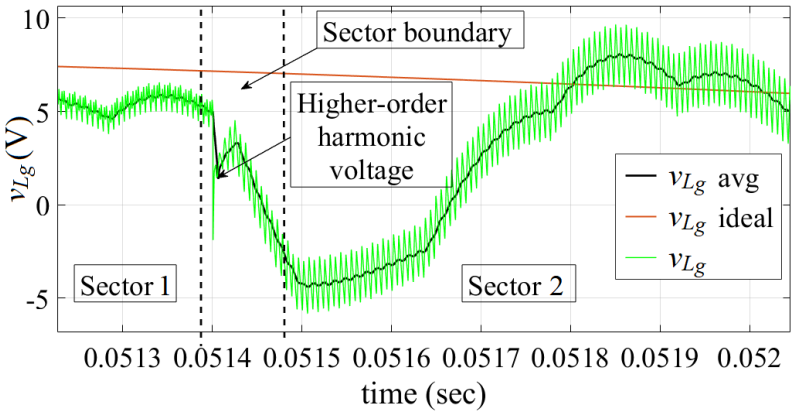


Fig. 4.4: Impression of the higher order harmonic voltage followed by the oscillations in sector 2 on the grid inductor L_g of phase a.

momentarily through D_{a1} and Q_a / body-diode of S_{y1}, S^{+}_{y3}, and S^{-}_{y3}, as shown in Fig. 4.2(b). As the capacitor current becomes zero because of this bypass, it cannot charge/discharge, which leads to a deviation in the capacitor average voltage from its ideal value at the sector boundary, as shown in Fig. 4.3. This gives rise to the following circumstances:

1. The capacitor voltage deviation at the sector boundary impresses higher-order harmonic voltages on the grid-side inductors L_g of phases a and c, as shown in Fig. 4.4.

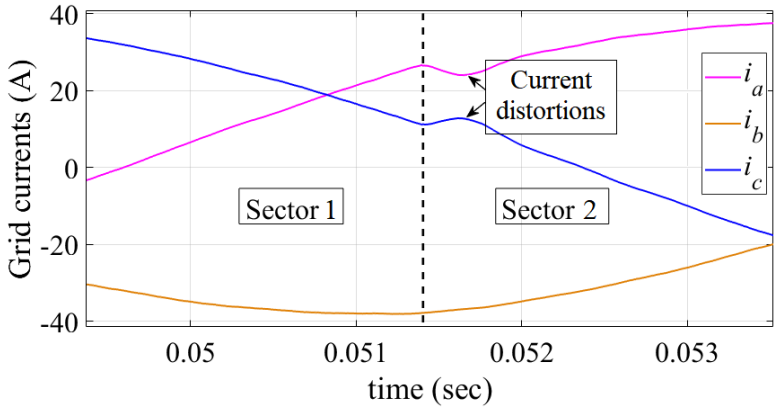


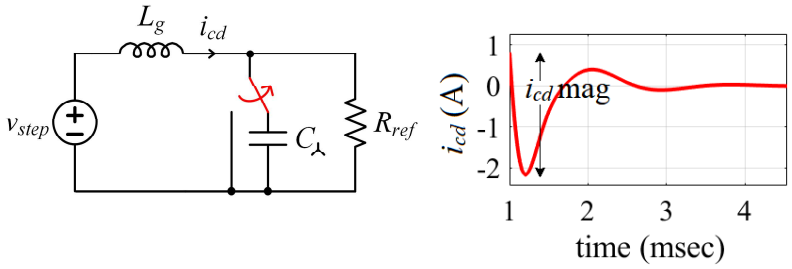
Fig. 4.5: Distortions in grid currents (i_a and i_c) during the sector transition from 1 to 2.

2. As Q_a turns off in sector 2 after the sector boundary, the bypass is removed and the grid voltages charge the capacitor again to track the ideal voltage waveform. The charging current of the capacitor flows through the grid inductors, which leads to second-order system oscillations in the dc link voltage v_{po} shown in Fig. 4.3.

Both of these factors cause oscillations in the grid currents i_a and i_c starting from the sector boundary until they are completely damped by the reflected load resistance. These distortions in grid currents are shown in Fig. 4.5.

An equivalent circuit model with fewer circuit components is developed to understand the correlation between the current distortion magnitude and system parameters, as shown in Fig. 4.6(a). In this model, the dc link capacitor is reflected on the grid side and a voltage source v_{step} is connected, which is equal to the step voltage applied by the grid when the bypass of the capacitor is removed after the sector boundary. This is analogous to the sector transition scenario. Oscillations similar to the sector transition distortion are observed in the inductor current of the circuit model, as shown in Fig. 4.6(b). Moreover, an equation for these oscillations (i_{cd}) is derived below:

$$\left.\begin{aligned} i_{cd} &= \frac{v_{step}}{R_{ref}} e^{-\alpha t}\left(\frac{\beta}{\sqrt{2\beta-1}}\sin(\gamma t+\delta)\right), \\ \alpha &= \frac{1}{2R_{ref}C_{\perp}}, \quad \beta = \frac{2R_{ref}^2 C_{\perp}}{L_g}, \\ \gamma &= \alpha\sqrt{2\beta-1}, \; \delta = \tan^{-1}\left(\frac{\sqrt{2\beta-1}}{1-\beta}\right), \end{aligned}\right\} \tag{4.2}$$



(a) (b)

Fig. 4.6: (a) Equivalent circuit model used to understand the current distortion problem, (b) oscillations in the inductor current of the circuit model similar to the grid current distortion.

Table 4.1: Current distortion magnitude obtained from the simulation of the system for different parameters.

Parameter	**Value**	**Current distortion magnitude (A)**
L_g	100 μH	4.37
($C_{po/on/pn}$ = 7.5 μF,	200 μH	3.93
Output power = 21 kW)	433 μH	3.13
$C_{po/on/pn}$	2 μF	2.53
(L_g = 433 μH,	5 μF	2.75
Output power = 21 kW)	7.5 μF	3.13
Output power	10 kW	1.57
(L_g = 433 μH,	16 kW	2.77
$C_{po/on/pn}$ = 7.5 μF)	21 kW	3.13

where R_{ref} is the reflected load resistance and $C_{\curlywedge}$ is the equivalent $\curlywedge$ connected capacitor reflected on the grid side given by $3C_{po/on}$.

According to (4.2), the magnitude of the current distortion increases with the increase in dc link capacitance, decrease in grid inductance, and increase in load. v_{step} is also a major factor that affects the current distortion. Table 4.1 shows the correlation between the current distortion magnitude and system parameters, obtained from the simulation of the system for different values of the dc link capacitance, grid inductance, and load. It can

be observed that the correlation predicted by (4.2) matches the simulation results.

4.2.2 Mitigation of Current Distortions

The T-type converter connects to the two soft dc link voltages, v_{po} and v_{on}. So, two duty ratios, d_p and d_n, corresponding to v_{po} and v_{on}, respectively, are modulated to achieve the PFC action. Moreover, the T-type output voltage v_{xy} is regulated for an appropriate power transfer. As discussed earlier, sector transition distortion originates from the deviation of the soft dc link voltages from their ideal values. Therefore, to mitigate the problem, dc link voltages are made to track their ideal waveforms by charging/discharging the capacitors as needed. To accomplish this, two current sources/sinks i_{pemu} and i_{nemu} are emulated by controlling the T-type converter such that the capacitors C_{po} and C_{on} can be charged/discharged whenever their voltages deviate from the ideal values. Fig. 4.7 shows the T-type converter supplying power to the load with the current sources i_{P_p} and i_{P_n}, and also emulating the current sources/sinks i_{pemu} and i_{nemu} to mitigate the sector transition distortion.

From Fig. 4.7,

$$i_{cpo} = i_p - i_{P_p} - i_{pemu}. \tag{4.3}$$

The T-type converter is controlled such that the switching average of the current i_{P_p} matches the required wave-shape of i_p over an entire grid cycle. This makes sure that grid currents are piece-wise sinusoidal for PFC. Thus,

$$i_{cpo} = -i_{pemu}. \tag{4.4}$$

So, i_{pemu} can be controlled to charge/discharge the capacitor C_{po} as needed. To match the soft dc link voltage v_{po} closely to its ideal value,

$$i_{pemu} = k_{emu}(v_{po} - v_{poideal}) = k_{emu}\Delta v_{po}, \tag{4.5}$$

where k_{emu} is used to control the magnitude of the capacitive current. It can be observed

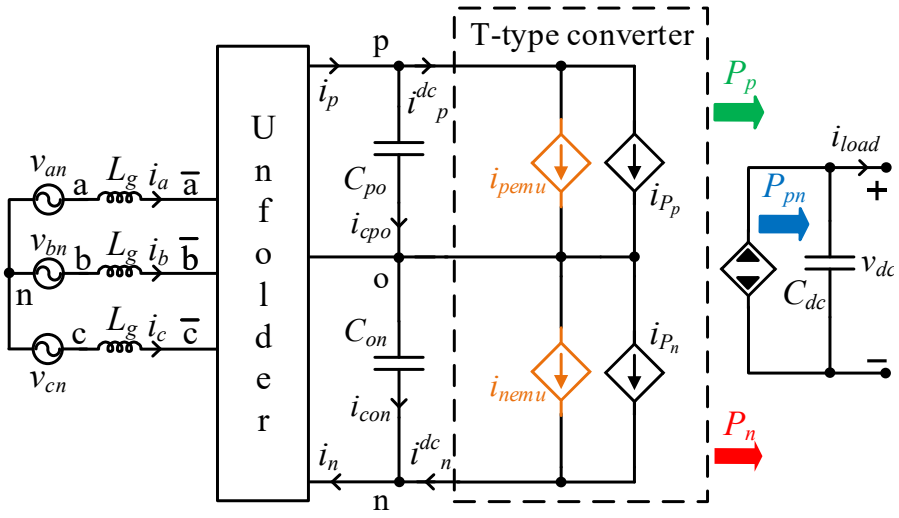


Fig. 4.7: Control of the T-type converter to achieve PFC, output power regulation by regulating i_{P_p} and i_{P_n}, and emulation of the current sources/sinks i_{pemu} and i_{nemu} to mitigate the sector transition distortion.

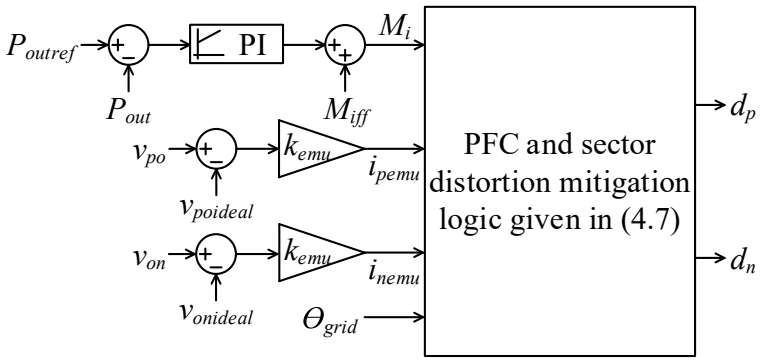


Fig. 4.8: Control architecture of the T-type converter to regulate output power, maintain PFC, and mitigate current distortion.

from (4.5) that when the p port capacitor voltage v_{po} becomes higher than $v_{poideal}$, the capacitor C_{po} is discharged by positive i_{pemu} (i.e. negative i_{cpo}), and vice versa. This makes sure that the capacitor tracks the ideal waveform correctly.

Similarly,

$$i_{nemu} = k_{emu}(v_{on} - v_{onideal}) = k_{emu}\Delta v_{on}, \tag{4.6}$$

which makes sure that the n port capacitor voltage v_{on} does not deviate. Combining the PFC, output power regulation-based calculations given in Chapter 2 (which utilized center-aligned modulation), and the sector transition distortion mitigation technique discussed

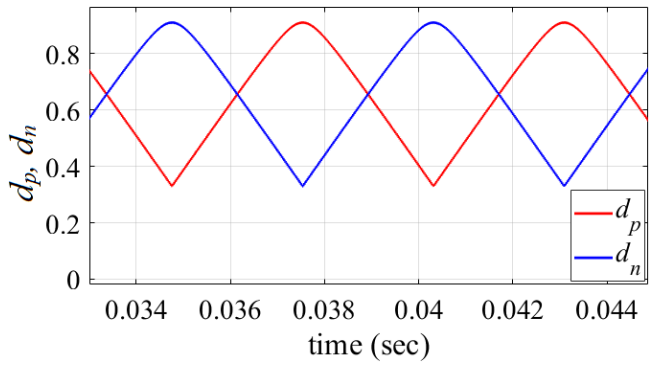


Fig. 4.9: d_p and d_n plots at an output power of 21 kW without the current distortion mitigation logic.

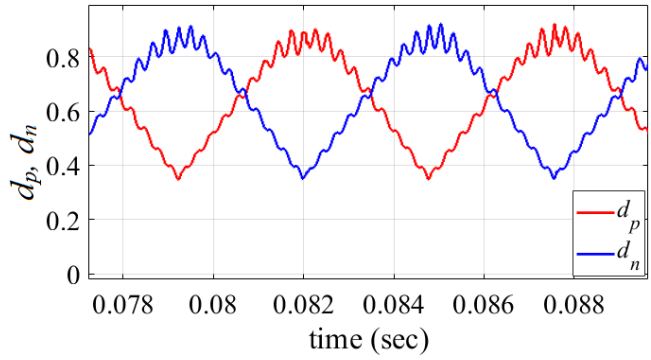


Fig. 4.10: d_p and d_n plots at an output power of 21 kW with the current distortion mitigation logic.

here, the values of d_p and d_n are given as,

$$\left.\begin{aligned} d_p &= \frac{2}{\pi}\sin^{-1}\left(M_i\left(\sin(f_p(\theta_{grid})) + \frac{i_{pemu}}{I_m}\right)\right), \\ d_n &= \frac{2}{\pi}\sin^{-1}\left(M_i\left(\sin(f_n(\theta_{grid})) + \frac{i_{nemu}}{I_m}\right)\right), \end{aligned}\right\} \tag{4.7}$$

where M_i is the modulation index of the T-type converter, θ_{grid} is the angle of v_{ab}, f_p and f_n are the functions with respect to the grid angle, and I_m is the peak of grid currents. The overall control structure of the T-type converter is shown in Fig. 4.8. A PI controller is used to regulate the output power by controlling M_i. Equation (4.7) uses M_i, θ_{grid}, and feed-forward terms i_{pemu} and i_{nemu} to calculate d_p and d_n. The values of d_p and d_n with and without the distortion mitigation logic are shown in Figs. 4.9 and 4.10.

Table 4.2: Simulation and hardware parameters of the grid-tied EV-battery charger system.

Parameter	**Value**
Nominal input voltage	480 V (l-l), 60 Hz ac 3-ϕ
Nominal battery voltage	710 V
Output power	21 kW
Grid inductance	433 μH
Dc link capacitance (C_{po}, C_{on}, and C_{pn})	7.5 μF
L_p	28.42 μH
C_{pp}	129.23 nF
C_{ps}	175.29 nF
Transformer parameters (Cantilever model)	
$L_{leakage}$	34.69 μH
$L_{magnetizing}$	782.76 μH
C_f	157.89 μF
k_{emu}	0.1 A/V

4.2.3 Simulation Results and Experimental Validation

A 21 kW grid-tied unfolding-based EV-battery charger system is simulated in MATLAB with a PLECS blockset. Moreover, a hardware prototype, as shown in Fig. 4.11, is built and tested to prove the proposed control solution for the sector transition distortion problem. The simulation and hardware parameters for the system are listed in Table 4.2. k_{emu} is selected such that the oscillations in d_p and d_n, shown in Fig. 4.10, do not exceed 10% of their peaks. This makes sure that the emulated current sources/sinks do not affect the output power drastically.

Simulation Results

The simulation results of the grid voltages and currents without the sector transition distortion mitigation logic are shown in Fig. 4.12. It can be observed that grid currents

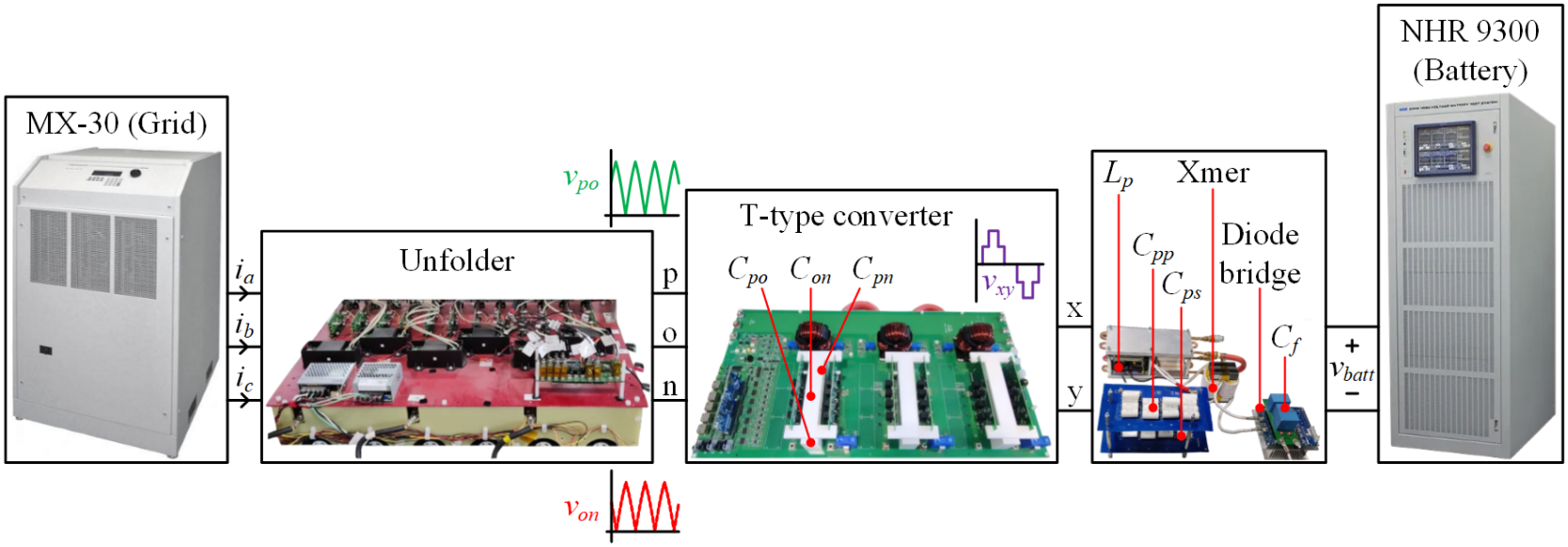


Fig. 4.11: 21 kW battery charger hardware prototype consisting of a grid-tied Unfolder and a T-type bridge-based dc-dc converter.

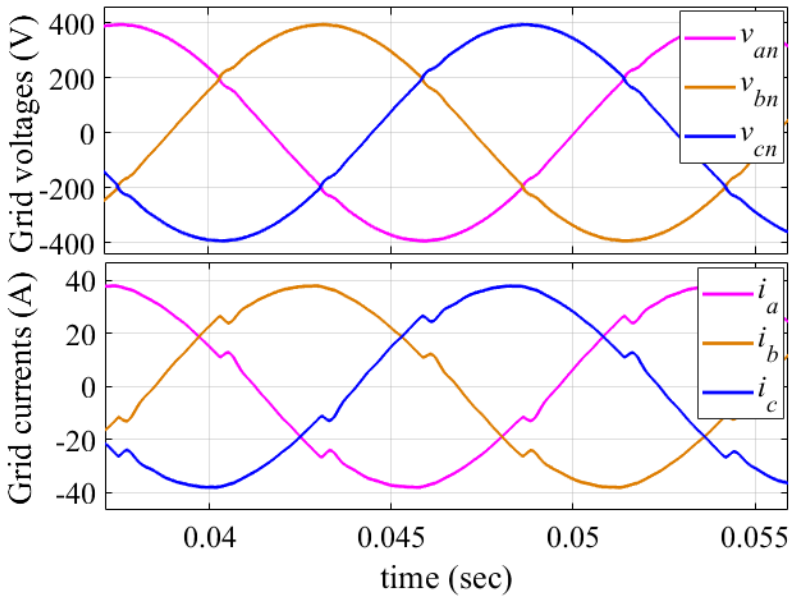


Fig. 4.12: Grid voltages and currents without the current distortion mitigation logic. Distortions can be observed after every 60° interval.

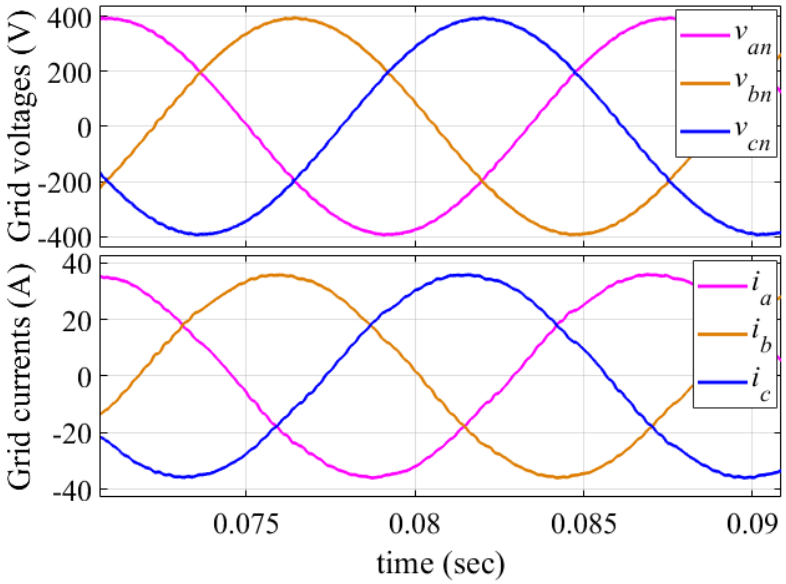


Fig. 4.13: Grid voltages and currents with the current distortion mitigation logic. Reduction in the magnitude of the distortions can be observed.

have undesirable distortions at every mains voltage sector boundaries. After implementing the mitigation logic, the grid current waveforms are improved and are shown in Fig. 4.13.

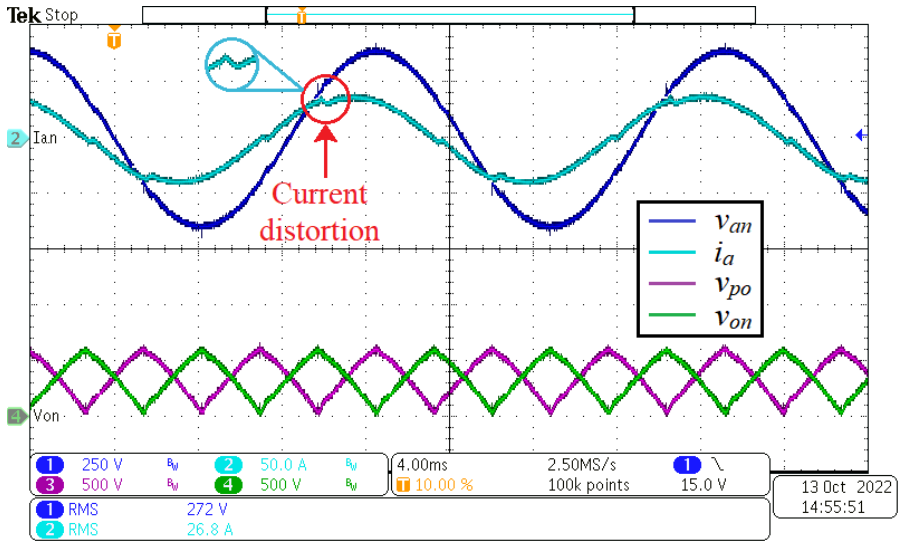


Fig. 4.14: Phase a grid voltage (v_{an}), current (i_a), and soft dc link voltages (v_{po}, v_{on}) without the current sources/sinks emulation at 21 kW output power. Phase a current has significant distortions during sector transitions.

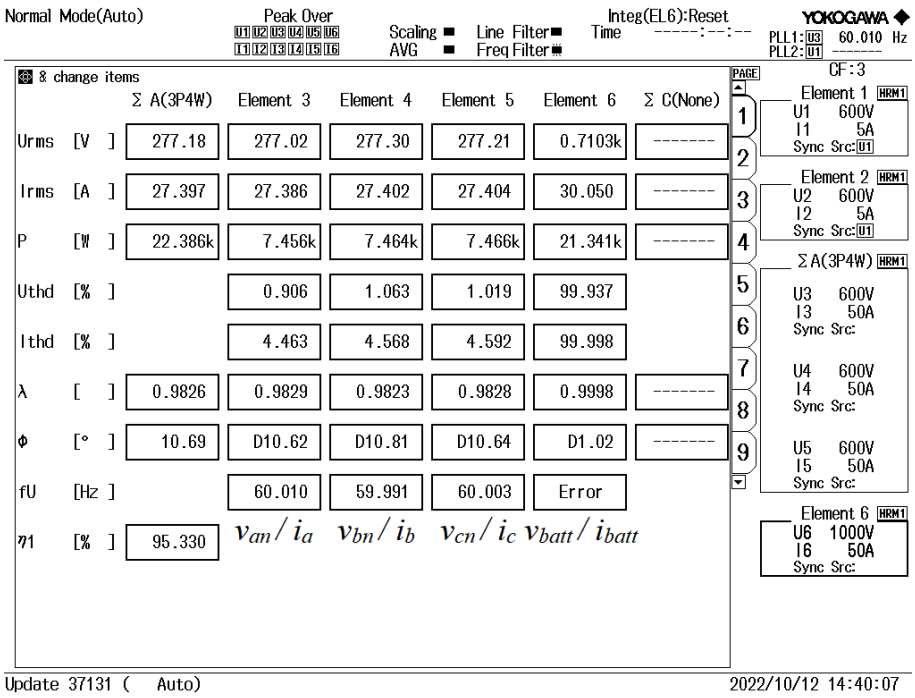


Fig. 4.15: 4.46% THD in phase a current (i_a) is measured with Yokogawa WT1806E power analyser at 21 kW output power without the distortion mitigation logic.

Experimental Validation

QRD6516001 diodes and QIC6508001 IGBTs are used to design the Unfolder. The

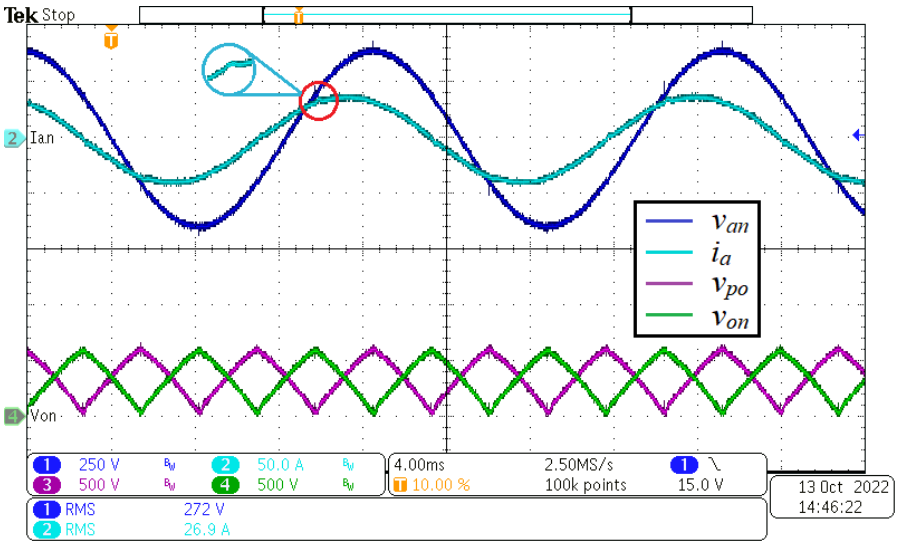


Fig. 4.16: Phase a grid voltage (v_{an}), current (i_a), and soft dc link voltages (v_{po}, v_{on}) with the current sources/sinks emulation at 21 kW output power. Phase a current has lower distortions during sector transitions.

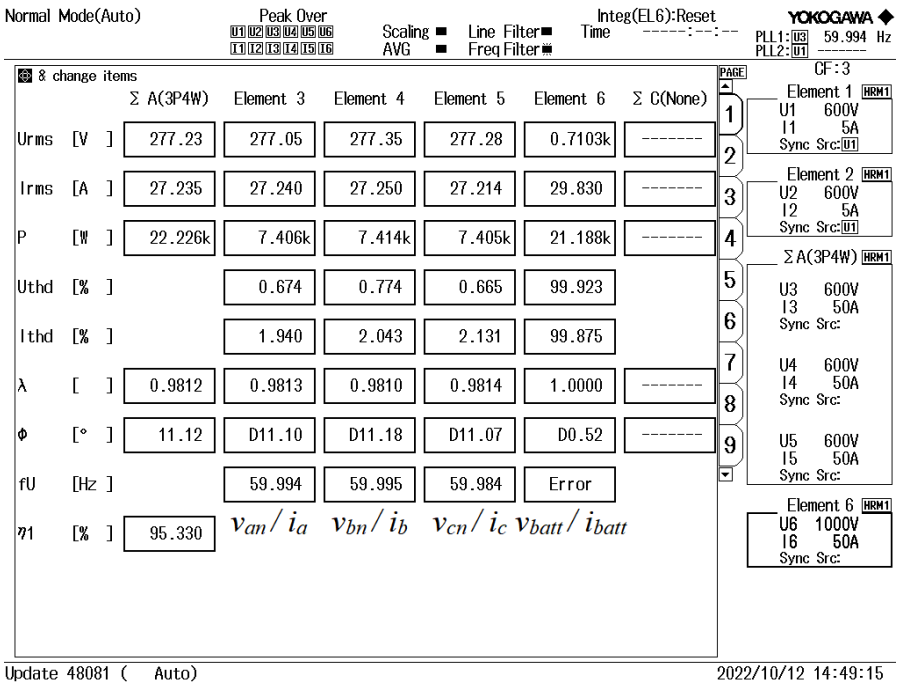


Fig. 4.17: 1.94% THD in phase a current (i_a) is measured with Yokogawa WT1806E power analyser at 21 kW output power with the distortion mitigation logic.

T-type converter is designed using NVH4L020N120SC1 MOSFETs, and body-diodes of CCS050M12CM2 MOSFETs are used for the diode bridge rectifier on the secondary side.

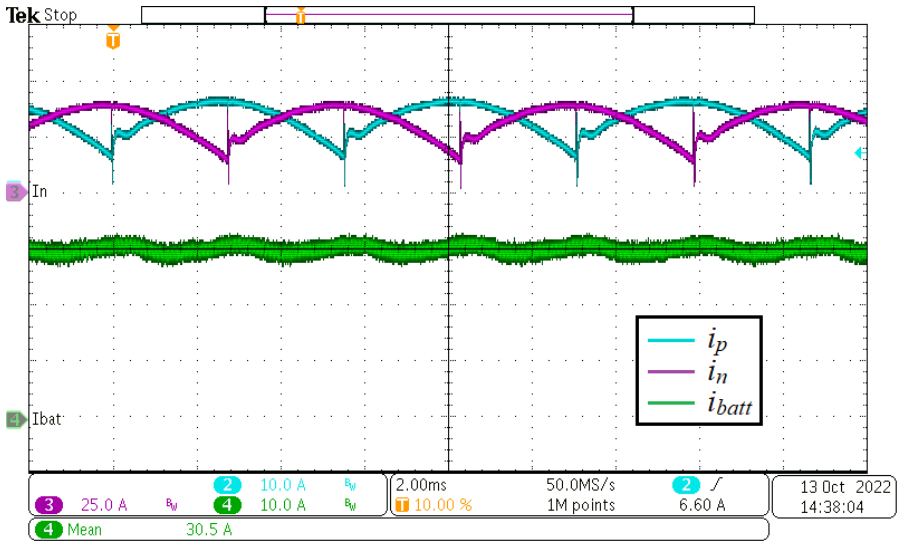


Fig. 4.18: P, n ports currents (i_p, i_n), and battery current (i_{batt}) supplying 21 kW power without the distortion mitigation logic. Battery current has 360 Hz oscillations caused by the deviation of v_{po} and v_{on} affecting the magnitude of v_{xy} fundamental voltage.

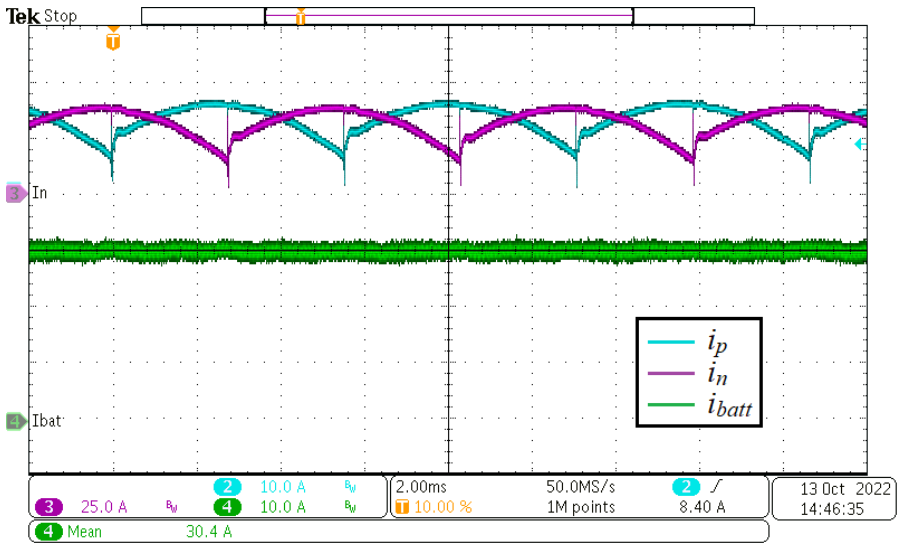


Fig. 4.19: P, n ports currents (i_p, i_n), and battery current (i_{batt}) supplying 21 kW power with the distortion mitigation logic. Battery current has very low 360 Hz oscillations, as the fundamental voltage of v_{xy} is being regulated properly in this case.

California Instruments MX-30 is used to emulate the grid, and NH Research 9300 is used in battery mode to emulate an EV battery, as shown in Fig. 4.11.

The hardware results of the phase a grid voltage, current, and soft dc link voltages without the sector transition distortion mitigation logic are shown in Fig. 4.14. Distor-

tions in phase a current can be observed, which leads to a higher 4.46% THD shown in Fig. 4.15. Fig. 4.16 shows the reduction in the distortions in phase a current when the current sources/sinks emulation logic is turned on. A significant improvement in phase a grid current THD to 1.94% is observed, as shown in Fig. 4.17.

Figs. 4.18 and 4.19 show the p, n ports, and battery currents with and without the current sources/sinks emulation. It can be observed that 360 Hz oscillations in the battery current shown in Fig. 4.18 are reduced due to this emulation technique, as shown in Fig. 4.19. This is because of v_{po} and v_{on} following their ideal values correctly, which helps to accurately regulate the fundamental component of the T-type output voltage v_{xy}.

4.3 High-Bandwidth Control of Unfolding-Based AC-DC Converters

As discussed in Chapter 3, leading-edge-aligned modulation requires high-bandwidth closed-loop control to regulate the Unfolder output currents, i_p and i_n, and shape the grid currents sinusoidal. This section focuses on achieving such high-bandwidth control.

4.3.1 Review of Extra Element Theorem

As previously explained, the Unfolder switches are strategically operated at a maximum of twice the grid frequency, converting every negative segment of ac input voltages into a positive polarity. While advantageous in terms of reducing switching losses, the use of low switching frequency introduces the possibility of LC resonance between the grid inductance (L_g) and dc-link capacitors (C_{po}, C_{on}, and C_{pn}). To better understand this resonance phenomenon, a transformative approach is taken by relocating the Δ-connected dc-link capacitors to the grid side and representing them in a $\curlywedge$-connected configuration ($C_{\curlywedge} = 3C_{po} = 3C_{on} = 3C_{pn}$), as depicted in Fig. 4.20. It is crucial to highlight that the occurrence of the LC resonance and the consequent reconfiguration of dc-link capacitors to the grid side, essential for comprehending this resonance, are both made possible by the lower switching frequency of the Unfolder. This frequency remains well below the LC

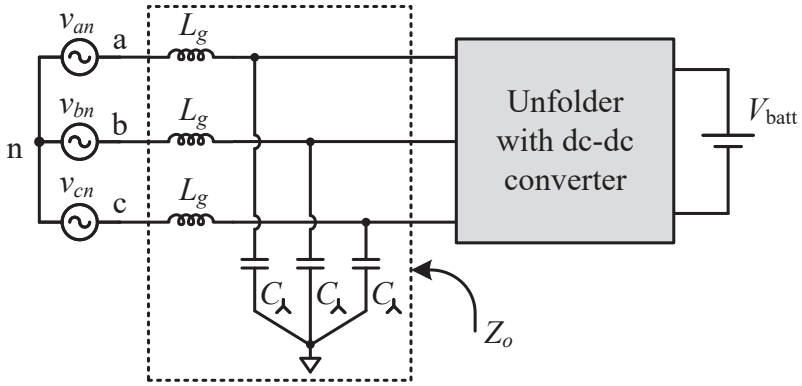


Fig. 4.20: For a clearer understanding of the LC interaction, the Δ-connected dc-link capacitors can be relocated to the grid side and transformed into equivalent 人-connected capacitors. The output impedance of the LC branch, denoted as Z_o, is a parallel combination of L_g and $C_人$.

resonant frequency[1]. On the other hand, such a scenario is not possible for HF-switched grid-tied converters with stiff dc-link voltages. In these systems, the HF switching does not allow sufficient time for the grid inductance and dc-link capacitors to interact with each other, thereby effectively ensuring decoupling between the grid and dc sides.

The LC resonance causes changes in both the magnitude and phase of the plant in the closed-loop control system. These changes can be quantified using the EET [58, 79–81] as

$$G_{\text{plant-modified}} = G_{\text{plant-original}}\, G_{cf}\,, \tag{4.8}$$

where

$$G_{\text{plant-original}} = G_{\text{plant}}|_{Z_o \to 0}\,, \tag{4.9}$$

$$G_{cf} = \frac{\left(1 + \dfrac{Z_o}{Z_n}\right)}{\left(1 + \dfrac{Z_o}{Z_d}\right)}\,. \tag{4.10}$$

In the above equations,

[1]In this study, the Unfolder switches operate at a maximum of 120 Hz, while the LC resonant frequency is 1.77 kHz, as detailed in the experimental validation section.

$$Z_o = sL_g \left\| \left(\frac{1}{sC_{\perp}} \right) \right. = \frac{sL_g}{1 + s^2 L_g C_{\perp}} \tag{4.11}$$

is the output impedance of the parallel-connected grid inductance, L_g, and equivalent $\perp$-connected capacitor on the grid side, $C_{\perp}$, as depicted in Fig. 4.20. Z_n and Z_d are the null double injection driving point impedance and single injection driving point impedance, respectively.

The correction factor, G_{cf}, is a function of Z_o, Z_n, and Z_d. It quantifies the extent to which the original plant transfer function, $G_{\text{plant-original}}$, is modified to $G_{\text{plant-modified}}$ due to the interaction of the output impedance, Z_o, with the null double injection driving point and single injection driving point impedances, Z_n and Z_d. Normally, when the resonance is undamped, the magnitude of Z_o, denoted as $\|Z_o\|$, exceeds $\|Z_n\|$ or $\|Z_d\|$ around the LC resonant frequency, f_{LC}, leading to a deviation of G_{cf} from unity. This leads to unfavorable alterations in the original plant transfer function, causing instability in the closed-loop system due to a decrease in the phase margin. Equations (4.8)-(4.10) suggest that to maintain the plant transfer function unaffected by ensuring $G_{cf} \approx 1$, the magnitude of Z_o must be kept much lower than the magnitudes of Z_n and Z_d. These criteria are given below:

$$\begin{aligned} &\|Z_o\| \ll \|Z_n\|, \text{ and} \\ &\|Z_o\| \ll \|Z_d\|. \end{aligned} \tag{4.12}$$

4.3.2 Plant Transfer Function and EET Parameters of the T-type Bridge-Based DC-DC Converter

Computation of the Plant Transfer Function

As the Unfolder operates in open-loop mode, switching at a maximum of twice the grid frequency, the closed-loop control architecture is designed solely for the HF T-type bridge-based dc-dc converter to modulate the duty ratios, d_p and d_n, as demonstrated in Fig. 3.9. Consequently, this study analyzes the effect of LC resonance on this closed-loop system, which is designed for achieving grid-side PFC and output power regulation. These control

objectives are achieved by maintaining waveshapes and amplitudes of the input p-port and n-port currents (i_p and i_n) of the T-type bridge. By separately controlling i_p and i_n, the grid currents, which are piece-wise functions of these p-port and n-port currents (refer to Fig. 3.3(b)), are kept sinusoidal. Furthermore, maintaining the required amplitudes of i_p and i_n ensures the proper regulation of the output power. Due to the symmetry between p-port and n-port controls, the analysis ahead mainly focuses on the p-port control. However, a similar analysis is applicable to the n-port control as well. In this closed-loop control architecture, a plant transfer function of the p-port ($G_{\text{plant-p-port}}$) is calculated between the small-signal p-port current ($\hat{i}_p$) and the small-signal p-port duty ratio ($\hat{d}_p$), given as

$$G_{\text{plant-p-port}} = \frac{\hat{i}_p}{\hat{d}_p}\,. \tag{4.13}$$

The implementation of an LCC resonant tank with a suitable quality factor facilitates the achievement of sinusoidal current or voltage waveforms on both the primary and secondary sides of the dc-dc conversion system. In this context, employing a small-signal modeling approach based on phasor transformation, as outlined in Chapter 5 and [25,60–62], is considered suitable. The modeling procedure for calculating $G_{\text{plant-p-port}}$ involves mainly three steps:

1. Steady-state analysis to derive the relationship between steady-state p-port current, I_p, and corresponding steady-state p-port duty ratio, D_p, given as

$$I_p = \frac{2}{\pi} I_{xm} \cos\left(\frac{\pi}{2}(1 - D_p) + \Theta_x\right) \sin\left(\frac{\pi D_p}{2}\right)\,. \tag{4.14}$$

2. Derivation of a small-signal phasor-transformed circuit for the T-type bridge, LCC resonant network with a transformer, along with the diode bridge on the secondary side, as shown in Fig. 4.21.

3. Calculation of the plant transfer function using the phasor-transformed small-signal circuit, given as

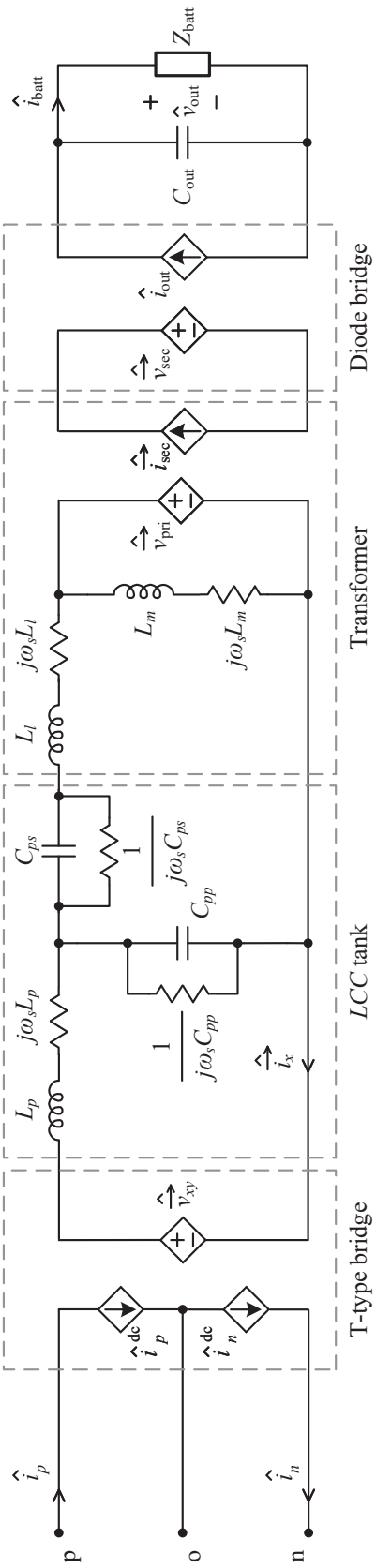


Fig. 4.21: Small-signal circuit in phasor-transformed representation for the T-type bridge-based dc-dc conversion system, incorporating an LCC resonant tank with a cantilever-modeled transformer, secondary diode bridge rectifier, and output capacitive filter. Output battery is represented with its impedance in the small-signal domain.

$$G_{\text{plant-p-port}} = \frac{\hat{i}_p^{i_{x\text{-env}}}}{\hat{i}_{x\text{-env}}^{d_p}} \frac{\hat{i}_{x\text{-env}}^{d_p}}{\hat{d}_p} + \frac{\hat{i}_p^{\theta_x}}{\hat{\theta}_x^{d_p}} \frac{\hat{\theta}_x^{d_p}}{\hat{d}_p} + \frac{\hat{i}_p^{d_p}}{\hat{d}_p}, \tag{4.15}$$

where

$$\frac{\hat{i}_p^{i_{x\text{-env}}}}{\hat{i}_{x\text{-env}}^{d_p}} = \frac{2}{\pi}\cos\left(\frac{\pi}{2}(1-D_p)+\Theta_x\right)\sin\left(\frac{\pi D_p}{2}\right), \tag{4.16}$$

$$\frac{\hat{i}_p^{\theta_x}}{\hat{\theta}_x^{d_p}} = -\frac{2}{\pi} I_{xm}\sin\left(\frac{\pi}{2}(1-D_p)+\Theta_x\right)\sin\left(\frac{\pi D_p}{2}\right), \tag{4.17}$$

$$\frac{\hat{i}_p^{d_p}}{\hat{d}_p} = I_{xm}\sin\left(\pi D_p - \Theta_x\right), \tag{4.18}$$

$$\frac{\hat{i}_{x\text{-env}}^{d_p}}{\hat{d}_p} = \frac{A_0}{B_1 s + B_0}, \tag{4.19}$$

$$\frac{\hat{\theta}_x^{d_p}}{\hat{d}_p} = \frac{C_0}{D_1 s + D_0}. \tag{4.20}$$

Due to the complexity of small-signal modeling for the T-type bridge-based dc-dc system with an LCC tank, this study provides only first-order simplified expressions for $\hat{i}_{x\text{-env}}^{d_p}/\hat{d}_p$ and $\hat{\theta}_x^{d_p}/\hat{d}_p$ to maintain brevity; these quantities, in fact, represent tenth-order behavior. It should be noted that these simplifications still accurately preserve the magnitude and phase of the plant transfer function, $G_{\text{plant-p-port}}$, with precision in the vicinity of the LC resonant frequency, as depicted in Fig. 4.22, providing readers with a valuable tool for analysis. The expressions for A_0, B_0, B_1, C_0, D_0, and D_1 are provided in [25].

In (4.14)-(4.20), D_p, Θ_x, I_{xm}, I_{xr}, I_{xi}, V_{po}, Θ_{sec}, $I_{\text{sec-}m}$, $I_{\text{sec-}r}$, $I_{\text{sec-}i}$, and $V_{\text{sec-}m}$ are the steady-state quantities of the T-type bridge-based dc-dc conversion system calculated at a specific grid angle where the plant transfer function, $G_{\text{plant-p-port}}$, is being derived. Θ_x represents the amount of phase lag of the T-type bridge output current. I_{xm}, I_{xr}, and I_{xi} correspond to the magnitude, real, and imaginary components of the T-type bridge output current phasor ($\vec{I_x}$), respectively. Θ_{sec} denotes the amount of phase lag of the secondary-side current flowing into the diode bridge. $I_{\text{sec-}m}$, $I_{\text{sec-}r}$, and $I_{\text{sec-}i}$ refer to the magnitude, real, and imaginary components of the secondary-side current phasor ($\overrightarrow{I_{\text{sec}}}$), respectively. $V_{\text{sec-}m}$, $V_{\text{sec-}r}$, and $V_{\text{sec-}i}$ are the magnitude, real, and imaginary components of the secondary-side

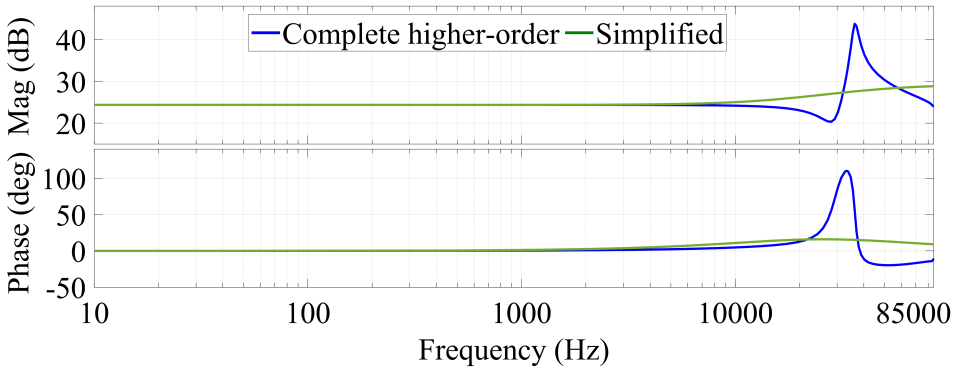


Fig. 4.22: Comparison of Bode plots of the plant ($G_{\text{plant-p-port}} = \hat{i}_p/\hat{d}_p$) of the T-type bridge-based dc-dc conversion system, obtained from the complete higher-order and simplified phasor transformation-based small-signal modeling. It can be observed that the simplified modeling closely preserves the magnitude and phase of the plant transfer function up to 10 kHz. Since the LC resonant frequency typically resides below this value, the simplified phasor transformation-based modeling provides a valuable tool for analysis.

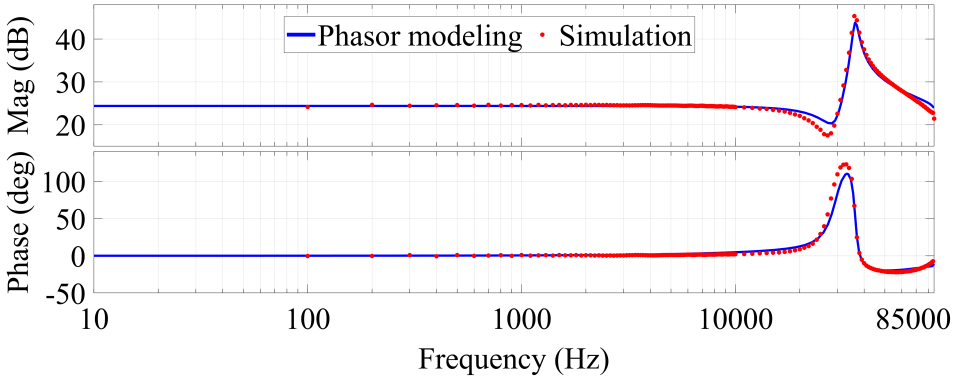


Fig. 4.23: Comparison of Bode plots of the plant ($G_{\text{plant-p-port}} = \hat{i}_p/\hat{d}_p$) of the T-type bridge-based dc-dc conversion system, obtained from the complete higher-order phasor transformation-based small-signal modeling and PLECS multitone analysis-tool-based simulation.

voltage phasor ($\overrightarrow{V_{\text{sec}}}$), respectively.

Moreover, $\hat{i}_p^{i_{x\text{-env}}}$ and $\hat{i}_p^{\theta_x}$ are perturbations in the p-port current, i_p, of the T-type bridge that depend upon small-signal changes in the envelope ($\hat{i}_{x\text{-env}}^{d_p}$) and phase ($\hat{\theta}_x^{d_p}$) of the T-type bridge output tank current phasor ($\overrightarrow{i_x}$), respectively. These perturbations occur due to small-signal deviations introduced in the p-port duty ratio, d_p. Furthermore, $\hat{i}_p^{d_p}$ represents the direct effect of the small-signal change in d_p on p-port current, i_p. The p-port plant transfer function, $G_{\text{plant-p-port}}$, is calculated by combining all these perturbations together,

as given by (4.15).

For a thorough examination, a complete higher-order plant transfer function without any simplifications is considered in subsequent sections for analyzing the effect of the LC resonance phenomenon. The Bode plots of $G_{\text{plant-p-port}}$ derived from the complete higher-order phasor transformation-based modeling are validated by comparison with Bode plots obtained using the multitone analysis (PLECS simulation tool), as illustrated in Fig. 4.23.

Computation of Z_n

Fig. 4.24(a) illustrates the circuit utilized to calculate null double injection driving point impedance, $Z_{n\text{-p-port}}$, for the p-port closed-loop control of the T-type bridge-based dc-dc conversion system. In the presence of $\hat{d}_p$, a current $\hat{i}_{\text{test}}$ is injected at the input p-port of the T-type bridge, and the $\hat{d}_p$ and $\hat{i}_{\text{test}}$ are adjusted in such a way that the output of the plant transfer function ($G_{\text{plant-p-port}}$), which is $\hat{i}_p$, is nulled. Under these conditions, $\hat{v}_{\text{test}}$ is computed, and

$$Z_{n\text{-p-port}} = \left.\frac{\hat{v}_{\text{test}}}{\hat{i}_{\text{test}}}\right|_{\hat{i}_p \xrightarrow{\text{null}} 0} . \tag{4.21}$$

However, in this case where $\hat{i}_{\text{test}}$ equals $\hat{i}_p$, and the latter is nulled to zero, $Z_{n\text{-p-port}}$ remains consistently infinite,

$$Z_{n\text{-p-port}} = \infty . \tag{4.22}$$

Intuitively, as mentioned in [58], the null double injection driving point impedance, $Z_{n\text{-p-port}}$, can be understood as the impedance that would be measured at the input p-port terminals of the T-type bridge if an ideal feedback loop perfectly regulated the p-port current, thus making the disturbance in the current, $\hat{i}_p$, equal to zero.

Computation of Z_d

Fig. 4.24(b) illustrates the circuit utilized to calculate single injection driving point impedance, $Z_{d\text{-p-port}}$, for the p-port closed-loop control of the T-type bridge-based dc-dc conversion system. The input $\hat{d}_p$ is made equal to zero, and the current $\hat{i}_{\text{test}}$ is injected at

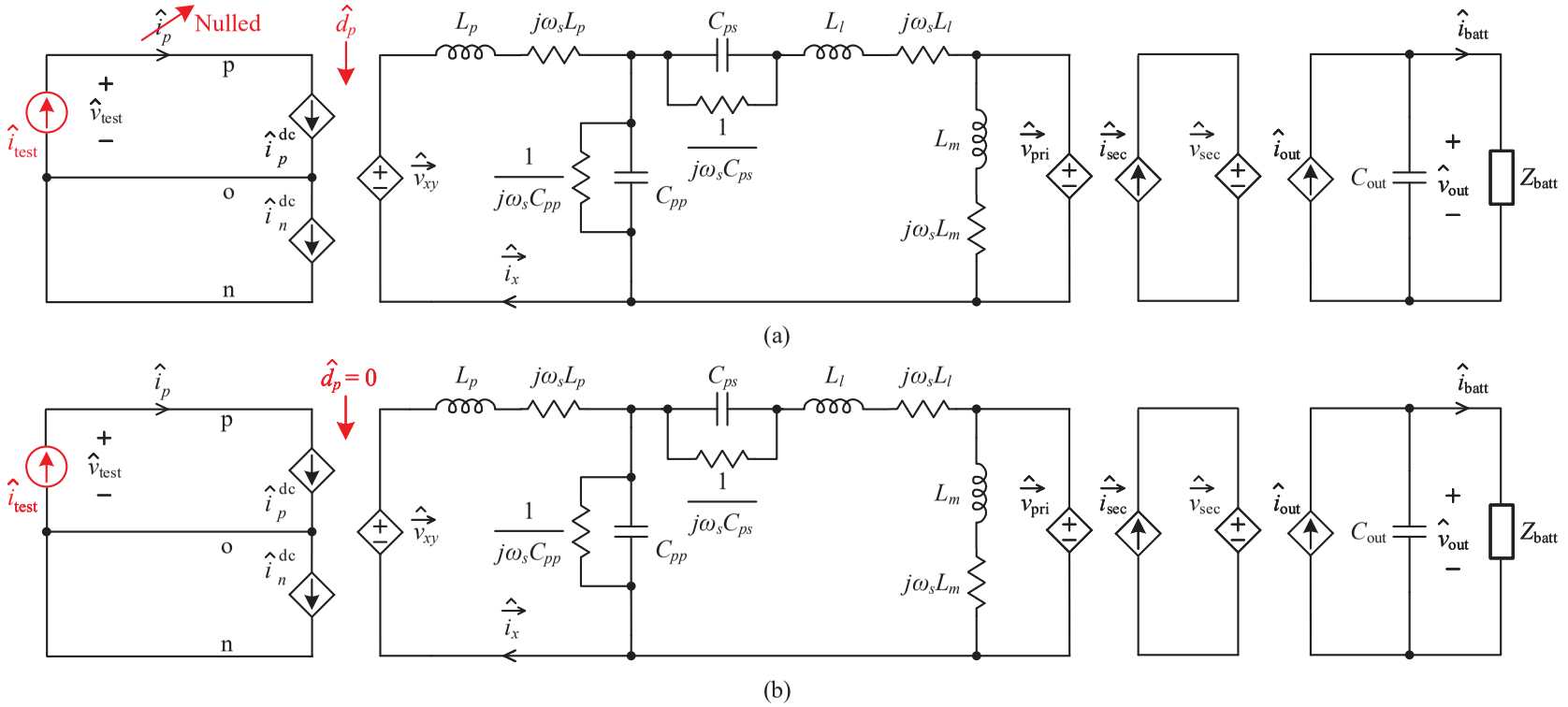


Fig. 4.24: Phasor-transformed small-signal circuits of the T-type bridge-based dc-dc conversion system for the calculation of (a) null double injection driving point impedance, $Z_{n\text{-p-port}}$ and (b) single injection driving point impedance, $Z_{d\text{-p-port}}$.

the input p-port of the T-type bridge. The quantity $Z_{d\text{-p-port}}$ is then derived as

$$Z_{d\text{-p-port}} = \left.\frac{\hat{v}_{\text{test}}}{\hat{i}_{\text{test}}}\right|_{\hat{d}_p=0} . \tag{4.23}$$

Intuitively, as mentioned in [58], the single injection driving point impedance, $Z_{d\text{-p-port}}$, can be understood as the impedance that would be measured at the input p-port terminals of the T-type bridge if the dc-dc converter is operated in open-loop, thus making the disturbance in the duty, $\hat{d}_p$, equal to zero.

The three-step procedure for the phasor transformation-based small-signal modeling discussed earlier is employed to calculate $Z_{d\text{-p-port}}$, as given by

$$Z_{d\text{-p-port}} = \frac{1}{\dfrac{\hat{i}_{\text{test}}^{i_{x\text{-env}}}}{\hat{i}_{x\text{-env}}^{v_{\text{test}}}}\dfrac{\hat{i}_{x\text{-env}}^{v_{\text{test}}}}{\hat{v}_{\text{test}}} + \dfrac{\hat{i}_{\text{test}}^{\theta_x}}{\hat{\theta}_x^{v_{\text{test}}}}\dfrac{\hat{\theta}_x^{v_{\text{test}}}}{\hat{v}_{\text{test}}}}, \tag{4.24}$$

where

$$\frac{\hat{i}_{\text{test}}^{i_{x\text{-env}}}}{\hat{i}_{x\text{-env}}^{v_{\text{test}}}} = \frac{2}{\pi}\cos\left(\frac{\pi}{2}(1-D_p)+\Theta_x\right)\sin\left(\frac{\pi D_p}{2}\right), \tag{4.25}$$

$$\frac{\hat{i}_{\text{test}}^{\theta_x}}{\hat{\theta}_x^{v_{\text{test}}}} = -\frac{2}{\pi}I_{xm}\sin\left(\frac{\pi}{2}(1-D_p)+\Theta_x\right)\sin\left(\frac{\pi D_p}{2}\right), \tag{4.26}$$

$$\frac{\hat{i}_{x\text{-env}}^{v_{\text{test}}}}{\hat{v}_{\text{test}}} = \frac{E_0}{F_0}, \tag{4.27}$$

$$\frac{\hat{\theta}_x^{v_{\text{test}}}}{\hat{v}_{\text{test}}} = \frac{G_0}{H_0}. \tag{4.28}$$

Similar to the procedure for calculating the plant transfer function, deriving $Z_{d\text{-p-port}}$ using phasor transformation-based modeling for the T-type bridge-based dc-dc conversion system involves complexities. Therefore, simplified expressions for $\hat{i}_{x\text{-env}}^{v_{\text{test}}}/\hat{v}_{\text{test}}$ and $\hat{\theta}_x^{v_{\text{test}}}/\hat{v}_{\text{test}}$ are provided to maintain brevity. It is important to note that these simplifications approximately preserve the magnitude of $Z_{d\text{-p-port}}$ around the LC resonant frequency, as depicted in Fig. 4.25, offering readers a valuable tool for analyzing the criteria given in (4.12). The expressions for E_0, F_0, G_0, and H_0 are provided in [25].

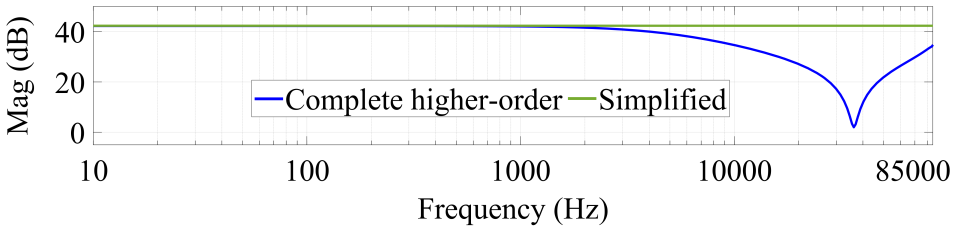


Fig. 4.25: Comparison of the magnitude Bode plots of $Z_{d\text{-p-port}}$ at a grid angle of $\theta_{\text{grid}} = \pi/15$ obtained from the complete higher-order and simplified phasor transformation-based modeling. It can be observed that the simplified modeling closely preserves the magnitude of the single injection driving point impedance at lower frequencies, where the LC resonant frequency typically resides. Therefore, the simplified phasor transformation-based modeling provides a valuable tool for analyzing the criteria given in (4.12).

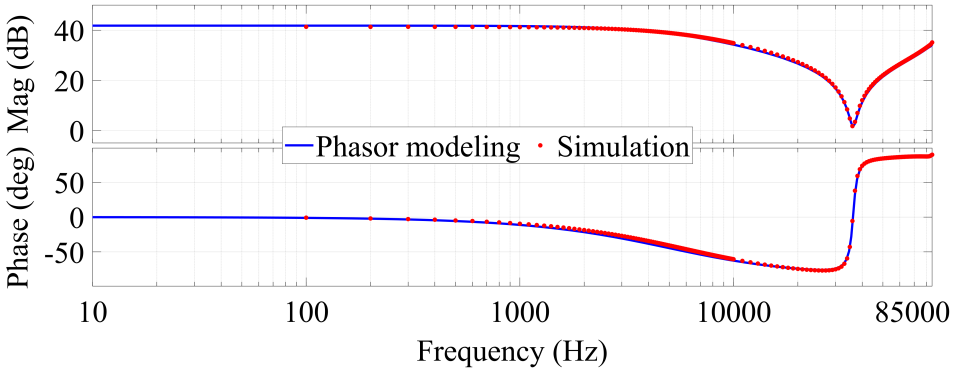


Fig. 4.26: Comparison of Bode plots of the single injection driving point impedance, $Z_{d\text{-p-port}}$, at a grid angle of $\theta_{\text{grid}} = \pi/15$ obtained from the complete higher-order phasor transformation-based small-signal modeling and PLECS multitone analysis-tool-based simulation.

In (4.24)-(4.28), $\hat{i}_{\text{test}}^{i_{x\text{-env}}}$ and $\hat{i}_{\text{test}}^{\theta_x}$ are perturbations in the p-port injected test current (i_{test}) of the T-type bridge that depend upon small-signal changes in the envelope ($\hat{i}_{x\text{-env}}^{v_{\text{test}}}$) and phase ($\hat{\theta}_x^{v_{\text{test}}}$) of the T-type bridge output tank current phasor ($\vec{i_x}$), respectively. These perturbations occur due to small-signal deviations in v_{test}. The p-port single injection driving point impedance, $Z_{d\text{-p-port}}$, is calculated by combining all these perturbations together, as given by (4.24).

For a thorough examination, the analysis ahead utilizes a complete higher-order $Z_{d\text{-p-port}}$ without any simplifications to analyze the effect of the LC resonance phenomenon. The Bode plots of $Z_{d\text{-p-port}}$, derived by the complete higher-order phasor transformation-based modeling, have been verified by comparing them with Bode plots given by multitone analysis

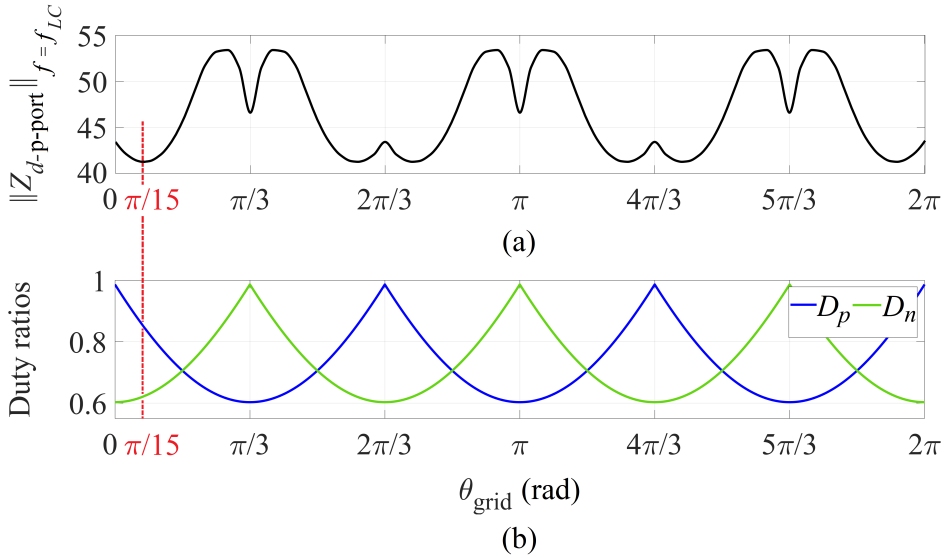


Fig. 4.27: (a) Variation of $\|Z_{d\text{-p-port}}\|$ at $f = f_{LC}$ throughout the grid cycle due to (b) the variation in the steady-state duty ratios, D_p and D_n, of the T-type bridge to maintain PFC and output power regulation.

(using the PLECS simulation tool), as depicted in Fig. 4.26, at a grid angle of $\theta_{\text{grid}} = \pi/15$. Due to the variation of steady-state duty ratios of the T-type bridge across the grid cycle to maintain PFC and output power regulation, as illustrated in Fig. 4.27(b), the magnitude and phase Bode plots of $Z_{d\text{-p-port}}$ also undergo changes throughout this grid cycle. The corresponding variation of $\|Z_{d\text{-p-port}}\|$ at the LC resonant frequency over the grid cycle is depicted in Fig. 4.27(a).

4.3.3 Effect of LC Resonance on Closed-Loop Control of the T-type Bridge-Based DC-DC Conversion System

It can be observed from the criteria given in (4.12) that the plant transfer function gets more significantly influenced by the LC resonance when the $\|Z_n\|$ or $\|Z_d\|$ are lower. Consequently, the subsequent analysis focuses on the worst-case scenario observed over the grid cycle, particularly when $\|Z_{d\text{-p-port}}\|_{f=f_{LC}}$ reaches its minimum value of 41.27 dB at $\theta_{\text{grid}} = (2n\pi/3 \pm \pi/15)$, where $n \in \{0, 1, 2, 3, ...\}$, as illustrated in Fig. 4.27(a). It is crucial to reiterate that $\|Z_{n\text{-p-port}}\|$ maintains an infinite value throughout the grid cycle, thereby eliminating the need for further analysis, as it being infinity consistently satisfies one of the

criteria outlined in (4.12).

In Fig. 4.28(a), the presence of LC resonance is evident from the magnitude plot of Z_o, occurring at the resonant frequency of 1.77 kHz $\left(f_{LC} = 1/\left(2\pi\sqrt{L_g C_{\curlywedge}}\right)\right)$. This resonance interacts with $\|Z_{d\text{-p-port}}\|$ and significantly impacts the correction factor, G_{cf}, causing it to deviate from unity, as calculated below using (4.10)

$$G_{cf} = \frac{\left(1 + \dfrac{Z_o}{Z_{n\text{-p-port}}}\right)}{\left(1 + \dfrac{Z_o}{Z_{d\text{-p-port}}}\right)} \tag{4.29}$$

and shown in Fig. 4.28(b). The deviation in G_{cf} from unity results in modifications to both the magnitude and phase Bode plots of the original plant transfer function, denoted as $G_{\text{plant-p-port-original}}$ in this section and given in (4.15). These modifications are calculated using (4.8) as given below

$$G_{\text{plant-p-port-modified}} = G_{\text{plant-p-port-original}}\, G_{cf} \tag{4.30}$$

and are depicted in Fig. 4.28(c). It is observable that the modified plant transfer function, $G_{\text{plant-p-port-modified}}$, has experienced significant changes as a consequence of the resonance between the grid inductance and dc-link capacitors, leading to an additional '$-360°$' phase shift in the phase Bode plot at the resonant frequency.

The negative phase shift introduced by the LC resonance in the plant transfer function poses challenges for a PI controller in achieving a positive phase margin and, consequently, stable closed-loop control. This challenge becomes particularly pronounced when the control bandwidth closely approaches or exceeds the LC resonant frequency. It is important to note that the controlled currents, i_p and i_n, are 180 Hz quantities (three times the grid frequency, f_{grid}), as illustrated in Fig. 3.3(b). To effectively regulate these currents under both steady-state and dynamic conditions, it is advisable to have a control bandwidth greater than ten times their fundamental frequency of 180 Hz. However, this preference brings the control bandwidth close to the LC resonant frequency, posing challenges for a PI controller to

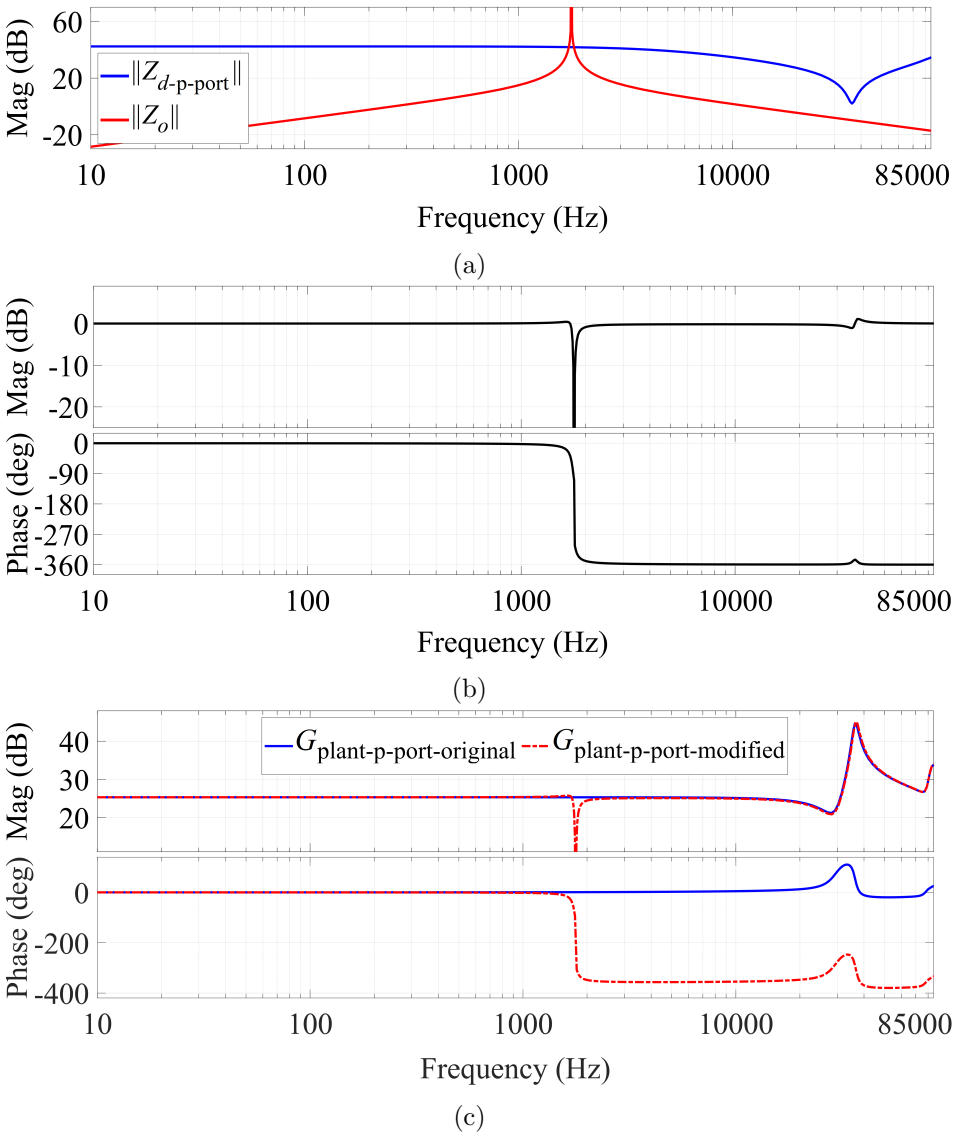


Fig. 4.28: The Bode plots depict: (a) the interaction of LC resonance with the magnitude of $Z_{d\text{-p-port}}$; (b) the correction factor, G_{cf}, showing the deviation from unity attributed to the LC resonance as given by (4.10); and (c) the original plant transfer function ($G_{\text{plant-p-port-original}}$) undergoing significant modifications because of the LC resonance, notably characterized by a '$-360°$' phase shift in the phase Bode plot. The modified plant transfer function is denoted as $G_{\text{plant-p-port-modified}}$.

maintain stable closed-loop operation at such a higher bandwidth level due to the negative phase shift caused by the resonance.

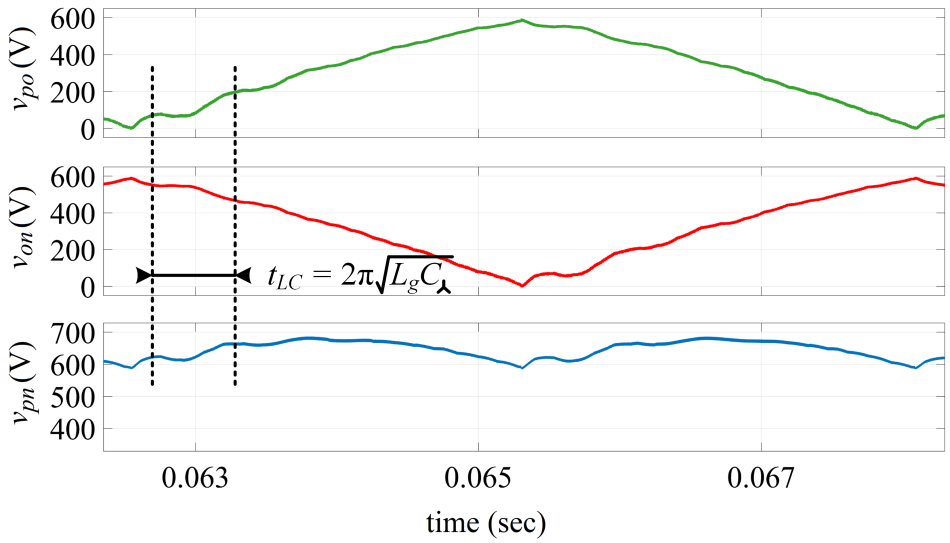


Fig. 4.29: The interaction between the grid inductance and dc-link capacitors leads to LC oscillations in the dc-link voltages, v_{po}, v_{on}, and v_{pn}. The time period of these oscillations is given as $t_{LC} = {}^{1}/_{f_{LC}} = 2\pi\sqrt{L_g C_{\lambda}}$.

4.3.4 Active Damping Using Current Emulation Technique

The interaction between the grid inductance and dc-link capacitors causes oscillations in dc-link voltages, v_{po}, v_{on}, and v_{pn}, as depicted in Fig. 4.29. To actively damp these oscillations, current sources/sinks ($i_{p\text{-emu}}$ and $i_{n\text{-emu}}$) are emulated using the T-type bridge-based dc-dc converter, in conjunction with current sources i_{P_p} and i_{P_n} responsible for powering the output battery. These emulated currents, illustrated in Fig. 4.30(a), either charge or discharge the dc-link capacitors when their voltages deviate from ideal values because of LC oscillations. These current sources/sinks, which help eliminate the LC oscillations in dc-link voltages, are given as

$$i_{p\text{-emu}} = k_{\text{emu}} \left(v_{po\text{-ideal}} - v_{po}\right) = k_{\text{emu}} \Delta v_{po} \,, \tag{4.31}$$

$$i_{n\text{-emu}} = k_{\text{emu}} \left(v_{on\text{-ideal}} - v_{on}\right) = k_{\text{emu}} \Delta v_{on} \,, \tag{4.32}$$

where k_{emu} denotes the proportionality constant. It is important to note that addressing v_{po} and v_{on} inherently takes care of LC oscillations present in v_{pn} as per KVL. The voltages v_{po} and v_{on}, affected by the LC resonance, predominantly consist of the fundamental compo-

nents of $3f_{\text{grid}}$ and f_{LC} frequencies (neglecting switching frequency components caused by the dc-dc converter operation). Additionally, as the $3f_{\text{grid}}$-frequency components of these dc-link voltages closely match the ideal waveforms, and the ideal dc-link voltages do not have f_{LC}-frequency components, (4.31) and (4.32) can be simplified to

$$i_{p\text{-emu}} = k_{\text{emu}} \left(\Delta v_{po}|_{3f_{\text{grid}}} + \Delta v_{po}|_{f_{LC}} \right) = -k_{\text{emu}}\, v_{po}|_{f_{LC}}\,, \tag{4.33}$$

$$i_{n\text{-emu}} = k_{\text{emu}} \left(\Delta v_{on}|_{3f_{\text{grid}}} + \Delta v_{on}|_{f_{LC}} \right) = -k_{\text{emu}}\, v_{on}|_{f_{LC}}\,, \tag{4.34}$$

where $v_{po}|_{f_{LC}}$ and $v_{on}|_{f_{LC}}$ are LC oscillations present in the actual v_{po} and v_{on} voltages. Consequently, the emulated current sources/sinks, $i_{p\text{-emu}}$ and $i_{n\text{-emu}}$, comprise only f_{LC}-frequency components.

Furthermore, by disregarding the negligible grid-frequency voltage drop across the grid inductances[2], the voltages across these inductances primarily exhibit f_{LC}-frequency components. This phenomenon arises due to LC oscillations present in the Unfolder's input line-to-line voltages, which are essentially piece-wise related to the dc-link voltages, v_{po}, v_{on}, and v_{pn}. These voltages across the grid-side inductances are therefore given by

$$v_{j\text{-}L_g}|_{f_{LC}} = -\, v_{\bar{j}n}|_{f_{LC}} \;\ldots j \in \{a, b, c\}\,, \tag{4.35}$$

where $v_{\bar{j}n}$ ($j \in \{a, b, c\}$) are the Unfolder input phase voltages. By combining (4.33)-(4.35) with the understanding that $v_{\bar{j}n}$ are fundamentally related to dc-link voltages, the voltages across grid inductances can be expressed as

$$\begin{aligned} v_{j\text{-}L_g}|_{f_{LC}} &= f(v_{po}|_{f_{LC}}\,, v_{on}|_{f_{LC}}) \\ &= f\left(\frac{i_{p\text{-emu}}}{k_{\text{emu}}}, \frac{i_{n\text{-emu}}}{k_{\text{emu}}} \right)\,. \end{aligned} \tag{4.36}$$

As the T-type bridge-based dc-dc system provides balanced loading at the output of the Unfolder which operates at a much lower frequency than the LC resonant frequency, a

[2]The grid inductance required for PFC in unfolding-based ac-dc topologies is significantly low [12]. Hence, the voltage drop across this inductance, proportional to $\omega_{\text{grid}} L_g$, is considered negligible [19].

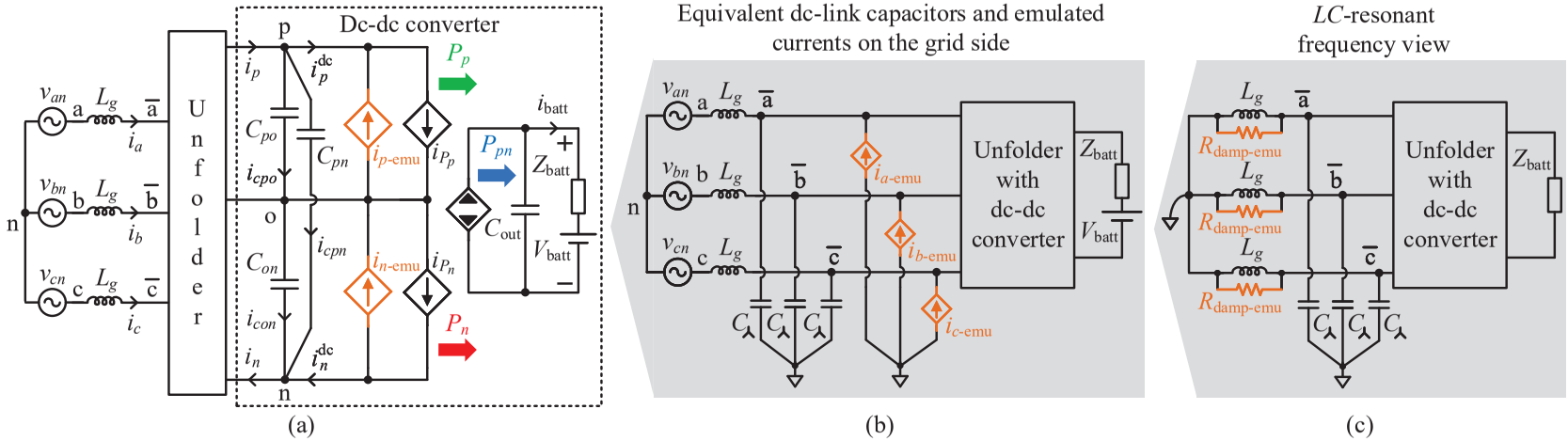


Fig. 4.30: (a) i_{P_p} and i_{P_n} supply power to the output battery, while $i_{p\text{-emu}}$ and $i_{n\text{-emu}}$ are emulated to provide active damping; (b) equivalent $\curlywedge$-connected dc-link capacitors and emulated currents on the grid side; and (c) emulated current sources/sinks can be viewed as damping resistors, $R_{\text{damp-emu}}$, connected across the grid inductances in the f_{LC}-frequency domain.

transformative approach can be taken. This involves relocating the Δ-connected dc-link capacitors along with the emulated currents, $i_{p\text{-emu}}$ and $i_{n\text{-emu}}$, to the grid side and representing them in a $\curlywedge$-connected configuration, as depicted in Fig. 4.30(b). The values of these individual emulated phase currents are

$$i_{a\text{-emu}} = -k_{\text{emu}} \left(v_{\bar{a}\bar{b}}|_{f_{LC}} - v_{\bar{c}\bar{a}}|_{f_{LC}} \right) = 3k_{\text{emu}}\, v_{a\text{-}L_g}\big|_{f_{LC}}\,, \tag{4.37}$$

$$i_{b\text{-emu}} = -k_{\text{emu}} \left(v_{\bar{b}\bar{c}}|_{f_{LC}} - v_{\bar{a}\bar{b}}|_{f_{LC}} \right) = 3k_{\text{emu}}\, v_{b\text{-}L_g}\big|_{f_{LC}}\,, \tag{4.38}$$

$$i_{c\text{-emu}} = -k_{\text{emu}} \left(v_{\bar{c}\bar{a}}|_{f_{LC}} - v_{\bar{b}\bar{c}}|_{f_{LC}} \right) = 3k_{\text{emu}}\, v_{c\text{-}L_g}\big|_{f_{LC}}\,. \tag{4.39}$$

From the above equations, it becomes apparent that the emulated current sources/sinks introduce additional currents into the system, which are directly proportionate to the voltages across the grid inductances. Consequently, these currents mimic virtual resistors placed across the grid inductances by emulating additional currents that should flow into the virtual resistors ($= v_{j\text{-}L_g}\big|_{f_{LC}} / R_{\text{damp-emu}}$). Designated as $R_{\text{damp-emu}}$, the virtual resistor is emulated in the higher f_{LC}-frequency domain and is a function of the parameter k_{emu}. An illustration of this interpretation of the emulated currents is presented in Fig. 4.30(c). Upon examination of (4.37)-(4.39), the value of $R_{\text{damp-emu}}$ can be computed as $1/(3k_{\text{emu}})$.

$i_{p\text{-emu}}$ and $i_{n\text{-emu}}$ are emulated by incorporating feedforward terms in the closed-loop control of the T-type bridge-based dc-dc system, as depicted in Fig. 4.31, while determining the duty ratios d_p and d_n. These modified duty ratios are given as

$$d_p = \frac{2}{\pi} \sin^{-1} \left(m_p \left(\sin(f_p(\theta_{\text{grid}})) - \frac{i_{p\text{-emu}}}{I_{gm}} \right) \right), \tag{4.40}$$

$$d_n = \frac{2}{\pi} \sin^{-1} \left(m_n \left(\sin(f_n(\theta_{\text{grid}})) - \frac{i_{n\text{-emu}}}{I_{gm}} \right) \right), \tag{4.41}$$

where m_p and m_n represent the p-port and n-port modulation indices, respectively, which are outputs of the PI controllers. θ_{grid} is the angle of $v_{\bar{a}\bar{b}}$ determined by the PLL. f_p and f_n denote functions with respect to θ_{grid}, as specified in Table 4.3, and I_{gm} is the peak of grid currents.

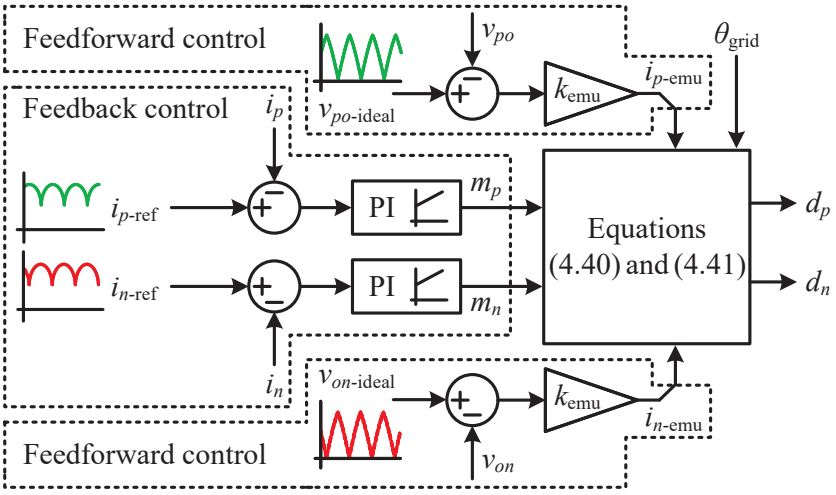


Fig. 4.31: The control structure of the T-type bridge-based dc-dc conversion system, ensuring output power regulation and input PFC through feedback control. Simultaneously, active damping is provided using emulated current sources/sinks via a feedforward technique.

Table 4.3: Values of f_p and f_n used to calculate d_p and d_n for different ac-voltage sectors.

Sector	**Grid angle ($\angle v_{\bar{a}\bar{b}}$)**	$\boldsymbol{f_p}$	$\boldsymbol{f_n}$
1	$0 \leq \theta_{\text{grid}} < \pi/3$	$\theta_{\text{grid}} + \pi/2$	$\theta_{\text{grid}} + \pi/6$
2	$\pi/3 \leq \theta_{\text{grid}} < 2\pi/3$	$\theta_{\text{grid}} - \pi/6$	$\theta_{\text{grid}} + \pi/6$
3	$2\pi/3 \leq \theta_{\text{grid}} < \pi$	$\theta_{\text{grid}} - \pi/6$	$\theta_{\text{grid}} - \pi/2$
4	$\pi \leq \theta_{\text{grid}} < 4\pi/3$	$\theta_{\text{grid}} - 5\pi/6$	$\theta_{\text{grid}} - \pi/2$
5	$4\pi/3 \leq \theta_{\text{grid}} < 5\pi/3$	$\theta_{\text{grid}} - 5\pi/6$	$\theta_{\text{grid}} - 7\pi/6$
6	$5\pi/3 \leq \theta_{\text{grid}} < 2\pi$	$\theta_{\text{grid}} + \pi/2$	$\theta_{\text{grid}} - 7\pi/6$

Utilizing the current emulation-based active damping, the LC resonance between the grid inductance and dc-link capacitors is effectively damped, as illustrated in Fig. 4.32(a). The chosen value of $R_{\text{damp-emu}} = 9\,\Omega$ is considered suitable. This ensures that, over the grid cycle, the magnitude of the damped LC resonance, $\|Z_{o\text{-damped}}\|_{f=f_{LC}} = R_{\text{damp-emu}} = 19.08$ dB, remains at least 20 dB lower (i.e., $1/10^{\text{th}}$) than the minimum value of $\|Z_{d\text{-p-port}}\|_{f=f_{LC}}$ = 41.27 dB (check Fig. 4.27(a)) at the resonant frequency. This meets the criteria[3] out-

[3]In this study, the condition related to $\|Z_{n\text{-p-port}}\|$ is always satisfied due to its infinite value.

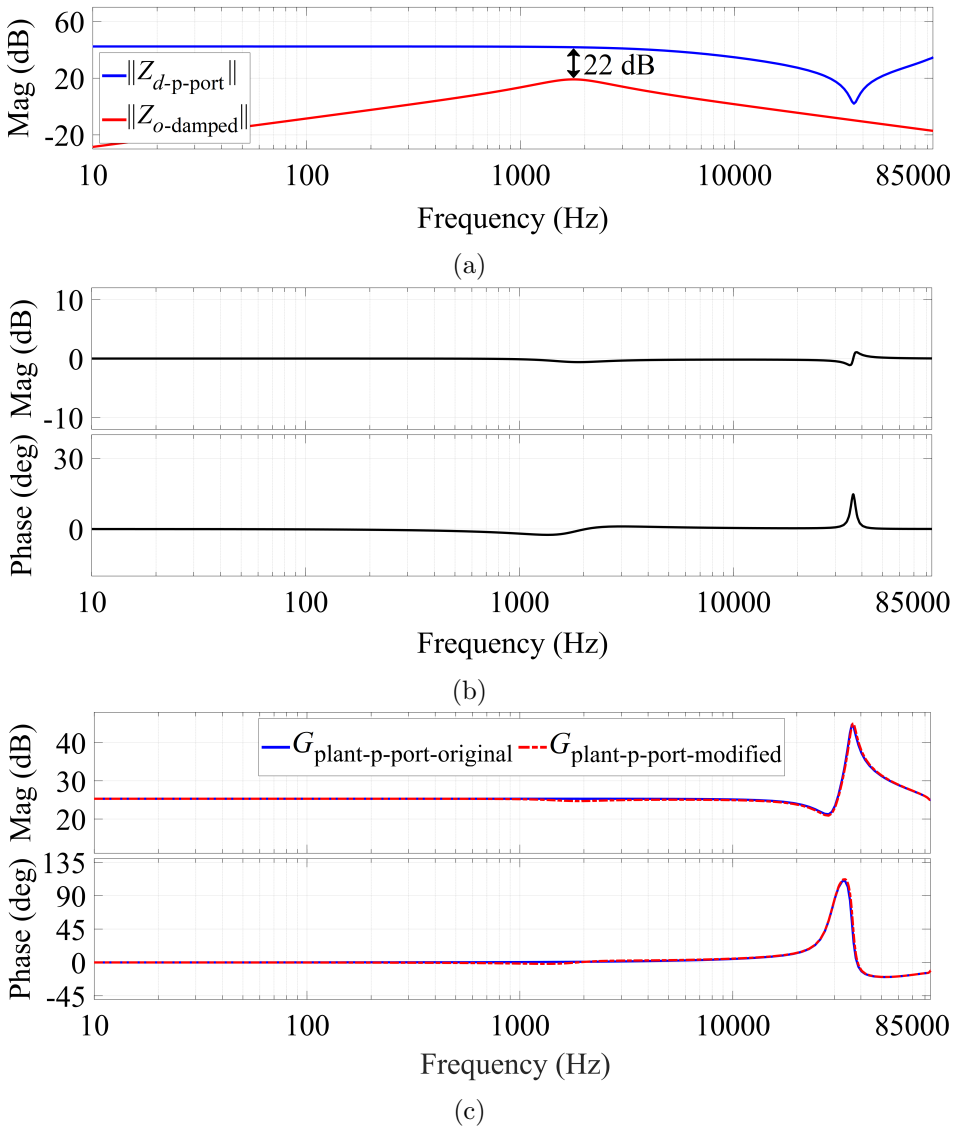


Fig. 4.32: The Bode plots illustrate (a) the damping of the LC resonance using $R_{\text{damp-emu}} = 9\,\Omega$ achieved through the current emulation technique; (b) the correction factor G_{cf} maintained close to unity; and (c) the comparison between the original plant transfer function ($G_{\text{plant-p-port-original}}$) and the modified plant transfer function ($G_{\text{plant-p-port-modified}}$), indicating that the plant is negligibly affected by the LC resonance due to the current emulation-based active damping.

lined in (4.12) and ensures that the correction factor, G_{cf}, stays close to unity (check Fig. 4.32(b)). Consequently, the plant transfer function, $G_{\text{plant-p-port}}$, remains unaffected, as depicted in Fig. 4.32(c). Observing this figure, it becomes apparent that the modified plant transfer function, $G_{\text{plant-p-port-modified}}$, closely matches the original plant transfer func-

Table 4.4: Hardware parameters of the unfolding-based ac-dc converter.

Parameter	**Value**
Nominal input voltage	480 V (l-l), 60 Hz
Battery voltage	649 V - 755 V
Output power	20 kW
T-type bridge switching frequency	85 kHz
Unfolder switching frequency	Diodes - 60 Hz, IGBTs - 120 Hz
Grid inductance (L_g)	600 μH
Dc-link capacitors (C_{po}, C_{on}, C_{pn})	4.5 μF
Equivalent grid-side capacitors ($C_{\perp}$)	13.5 μF
LC resonant frequency (f_{LC})	1.77 kHz
L_p	29.3 μH
C_{pp}	120.1 nF
C_{ps}	112.1 nF
Cantilever model-based isolation parameters	L_l = 37.5 μH, L_m = 996.2 μH
C_{out}	161.5 μF
k_{emu}	0.037 A/V
$R_{\text{damp-emu}}$	9 Ω

Table 4.5: PI controller (G_{PI}) parameters for various closed-loop bandwidth levels.

Bandwidth (Hz)	$\boldsymbol{K_p}$-PI	$\boldsymbol{K_i}$-PI
300	0.001	36.6
1800	0.001	251.4
3000	0.001	380.1

tion, $G_{\text{plant-p-port-original}}$, with negligible magnitude and phase deviations of -0.6 dB and $-1.3°$, respectively, at the resonant frequency. Notably, there is no undesirable '$-360°$' phase shift in the phase Bode plot, as observed in the case without active damping. This allows a PI controller to achieve a positive phase margin and ensure stable closed-loop operation of the T-type bridge-based dc-dc conversion system.

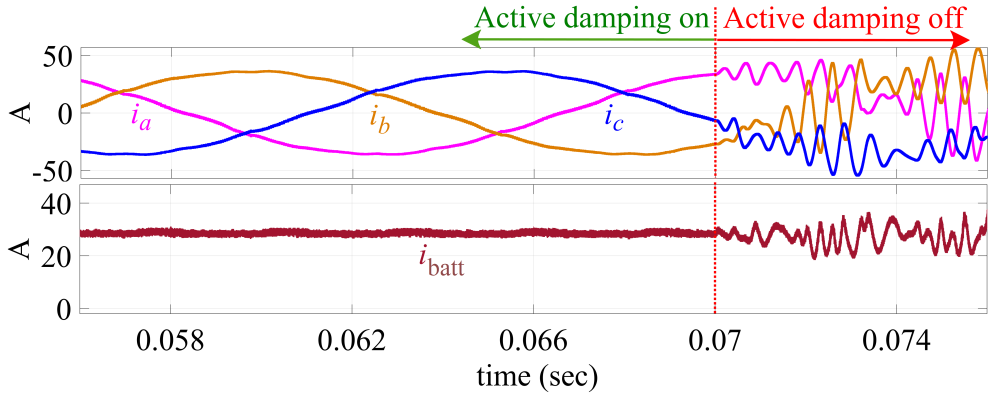


Fig. 4.33: Simulation results of the 20-kW unfolding-based ac-dc system reveal unstable oscillatory responses in both battery and grid currents when the active damping based on current emulation is disabled at $t = 0.07$ sec. In this case, the closed-loop bandwidth is configured to 1.8 kHz, closely aligned with the LC resonance at 1.77 kHz.

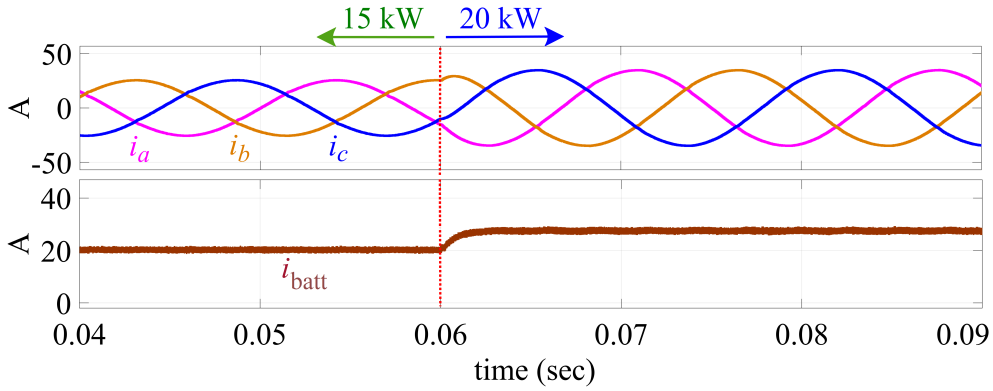


Fig. 4.34: Simulation-based step response of the unfolding-based ac-dc system at the closed-loop bandwidth of 1.8 kHz with active damping enabled. The output power has given a step change from 15 kW to 20 kW at $t = 0.06$ sec.

4.3.5 Simulation Results

A 20-kW grid-tied unfolding-based EV-battery charging system with a T-type bridge-based dc-dc converter is simulated using PLECS. The system parameters used for the simulation are given in Table 4.4. The simulation results, as presented in Fig. 4.33, reveal unstable oscillations in both battery and grid currents when the active damping based on current emulation is turned off. This instability arises due to the observed '$-360°$' phase shift in the phase Bode plot of the plant transfer function, $G_{\text{plant-p-port}}$, when the active damping is disabled. Consequently, a negative phase margin is obtained by utilizing a

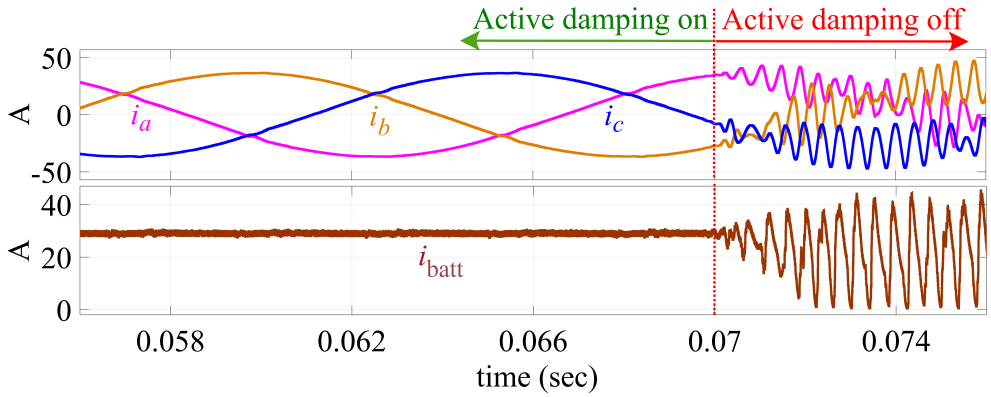


Fig. 4.35: Simulation results of the 20-kW unfolding-based ac-dc system reveal unstable oscillatory responses in both battery and grid currents when the active damping based on current emulation is disabled at $t = 0.07$ sec. In this case, the closed-loop bandwidth is configured to be 3 kHz, which is much higher than the LC resonance at 1.77 kHz.

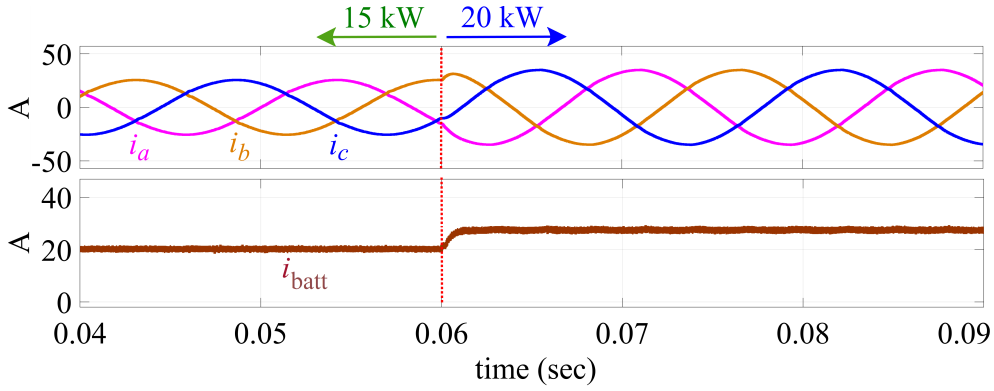


Fig. 4.36: Simulation-based step response of the unfolding-based ac-dc system at the closed-loop bandwidth of 3 kHz with active damping enabled. The output power has given a step change from 15 kW to 20 kW at $t = 0.06$ sec.

PI controller configured (check Table 4.5) to attain a closed-loop bandwidth of 1.8 kHz, slightly above the LC resonant frequency of 1.77 kHz. The stable performance of the active damping is also checked in transient conditions by giving a step change in the output power, from 15 kW to 20 kW, as shown in Fig. 4.34.

Moreover, the active damping is tested at a bandwidth level of 3 kHz, significantly higher than the LC resonant frequency. The corresponding simulation results provided in Fig. 4.35 demonstrate the stable operation of the unfolding-based ac-dc system when the active damping is enabled. A stable transient response at this higher bandwidth level is

depicted in Fig. 4.36, where the output power of the converter undergoes a step change from 15 kW to 20 kW.

4.3.6 Experimental Validation

A 20-kW hardware prototype of an unfolding-based ac–dc system with a T-type bridge-based dc-dc converter, as depicted in Fig. 4.37, is built and tested to validate the proposed control solution of current emulation-based active damping. The corresponding hardware parameters are summarized in Table 4.4. IXYS W1263YC200 diodes and Infineon FZ1200R17KF6C-B2 IGBTs are employed in designing the 3-ϕ Unfolder. The T-type bridge utilized in the three-port dc-dc system is built using Onsemi NVH4L020N120SC1 and NVH4L040N120SC1 MOSFETs, with the body-diodes of CREE CCS050M12CM2 MOSFETs used for the diode bridge on the secondary side. The emulation of the grid is performed using California Instruments MX-30, while NH Research 9300 is employed in battery mode to emulate an EV battery at the output terminal, as illustrated in Fig. 4.37.

Hardware verification begins by testing the unfolding-based ac-dc system at different closed-loop bandwidths without the control-based damping. Following this, the software platform of the TMS320F28379D microcontroller [71] is utilized to implement the current emulation-based active damping logic to damp the LC resonance and test the operation of the ac-dc system at different closed-loop bandwidth levels.

Unfolding-based ac-dc system operation without active damping

The hardware prototype of the unfolding-based ac-dc system is tested at an output power of 20 kW, without the current emulation-based active damping to observe the impact of the LC resonance on the system operation. Initially, the closed-loop bandwidth of the T-type bridge-based dc-dc converter control is set to 300 Hz, a value much lower than the LC resonant frequency of 1.77 kHz. The corresponding PI controller parameters are provided in Table 4.5. In Fig. 4.38(a), hardware results depict the phase a ac input voltage, phase a grid current, dc-link voltage (v_{po}), and the output battery current. Due to the considerably lower bandwidth of 300 Hz compared to the LC resonant frequency, stable

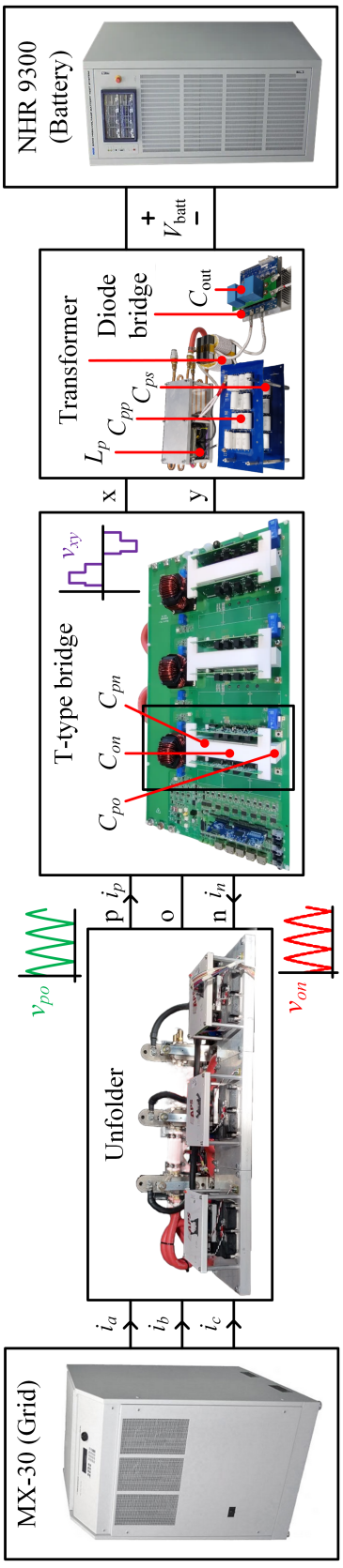
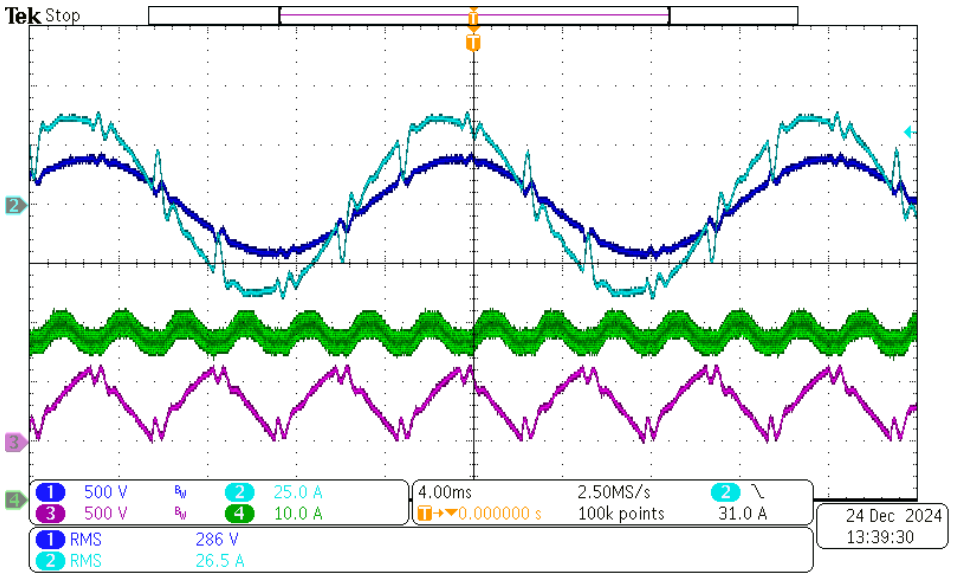
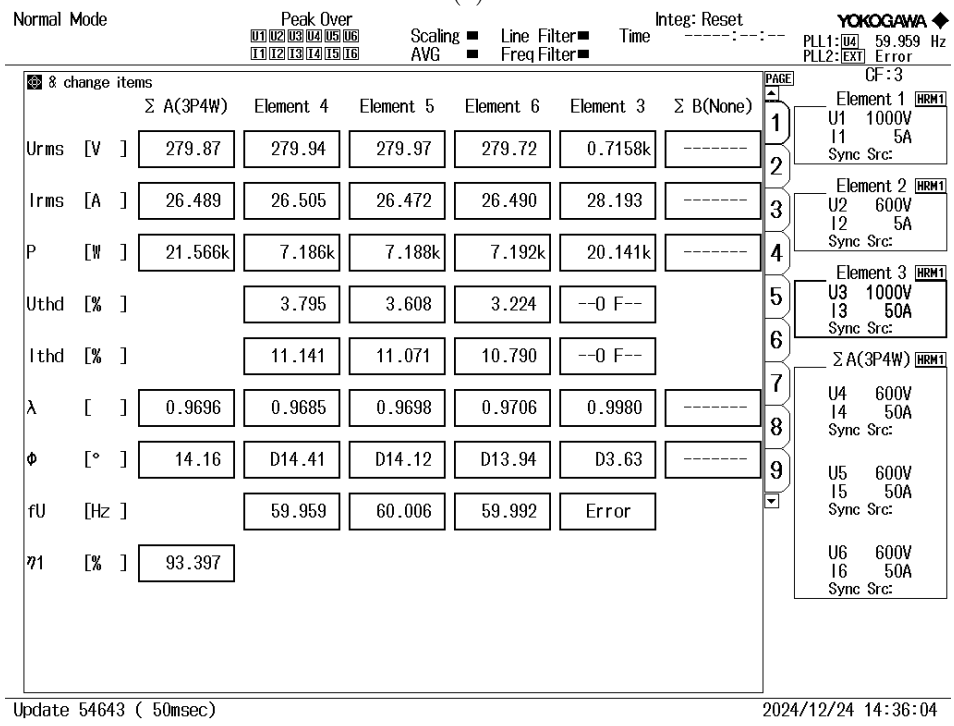


Fig. 4.37: A 20-kW hardware setup of an unfolding-based ac-dc system with a T-type bridge-based dc-dc converter. The California Instruments MX-30 is employed to emulate the grid, and the NH Research 9300 is used as an EV battery.



(a)



(b)

Fig. 4.38: Experimental results of the 20-kW unfolding-based ac-dc system operating at a closed-loop bandwidth of 300 Hz without active damping are illustrated as follows: (a) oscillatory phase a ac input voltage, phase a grid current, dc-link voltage (v_{po}), and output battery current; (b) a high grid current THD of 11.14%, measured using the Yokogawa WT1806E power analyzer.

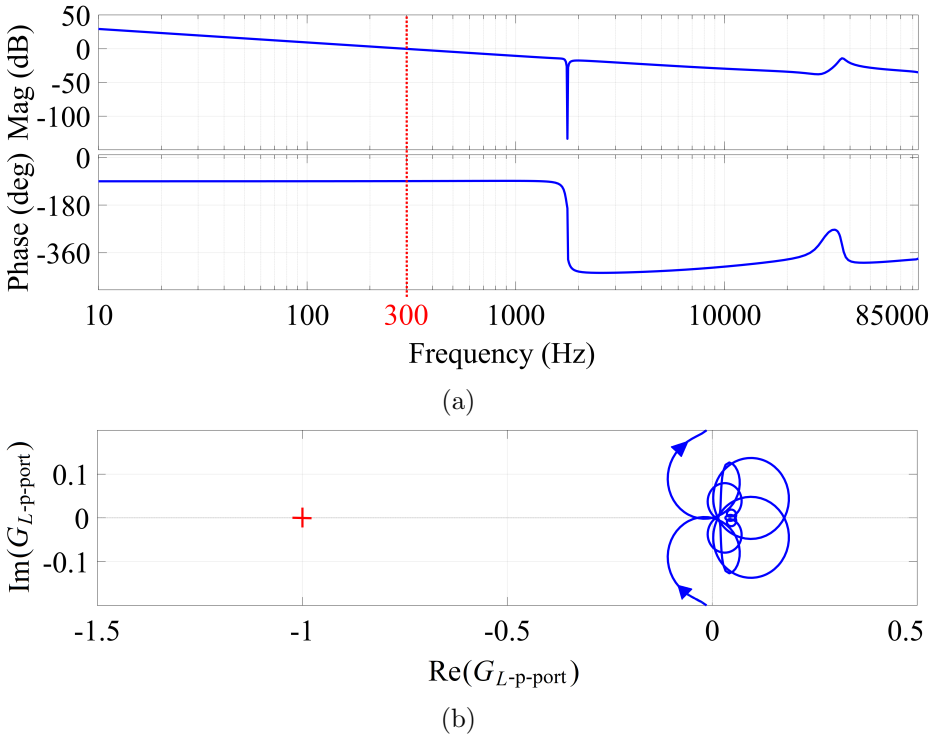


Fig. 4.39: (a) Bode plots of the loop transfer function, $G_{L\text{-p-port}}$, indicating a positive phase margin at the gain crossover frequency of 300 Hz (G_{PI} parameters: $K_{p\text{-PI}} = 0.001$ and $K_{i\text{-PI}} = 36.6$); and (b) the corresponding Nyquist plot, which does not encircle the point $(-1,\ j0)$, confirming a stable closed-loop operation.

closed-loop operation is observed. The corresponding Bode plots of the p-port loop transfer function, calculated as

$$G_{L\text{-p-port}} = G_{\text{PI}} K_{m_p}^{d_p} G_{\text{plant-p-port}}\,, \tag{4.42}$$

are given in Fig. 4.39(a), where G_{PI} represents the PI controller, and $K_{m_p}^{d_p}$ is the small-signal gain of the expression given in (4.40) that relates $\hat{d}_p$ and $\hat{m}_p$ as

$$K_{m_p}^{d_p} = \frac{\hat{d}_p}{\hat{m}_p} = \frac{2}{\pi}\frac{\sin(f_p(\theta_{\text{grid}}))}{\cos\left(\frac{\pi}{2}D_p\right)}\,. \tag{4.43}$$

The value of $K_{m_p}^{d_p}$ at $\theta_{\text{grid}} = \pi/15$ is 2.79. Moreover, the associated Nyquist plot presented in Fig. 4.39(b), which does not encircle the point $(-1,\ j0)$, confirms the stability of the closed-loop operation. Despite the stable ac-dc operation at this lower bandwidth without

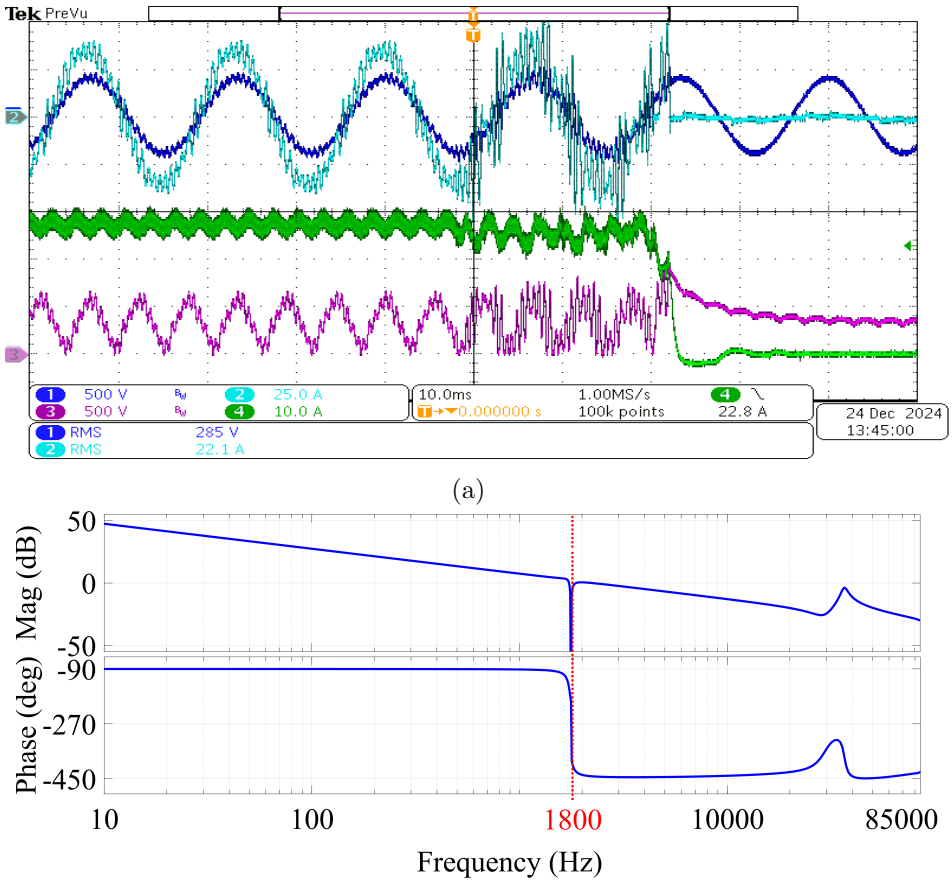
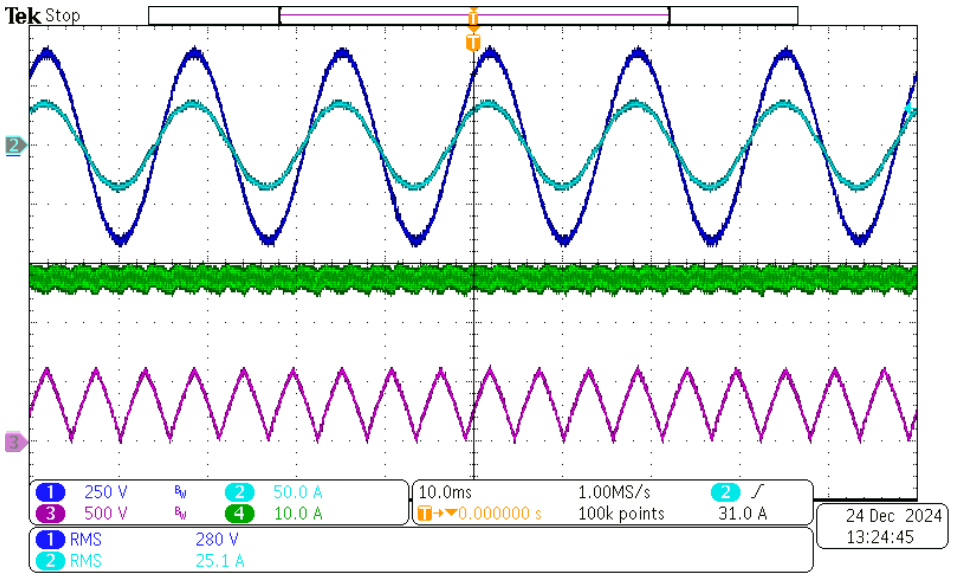


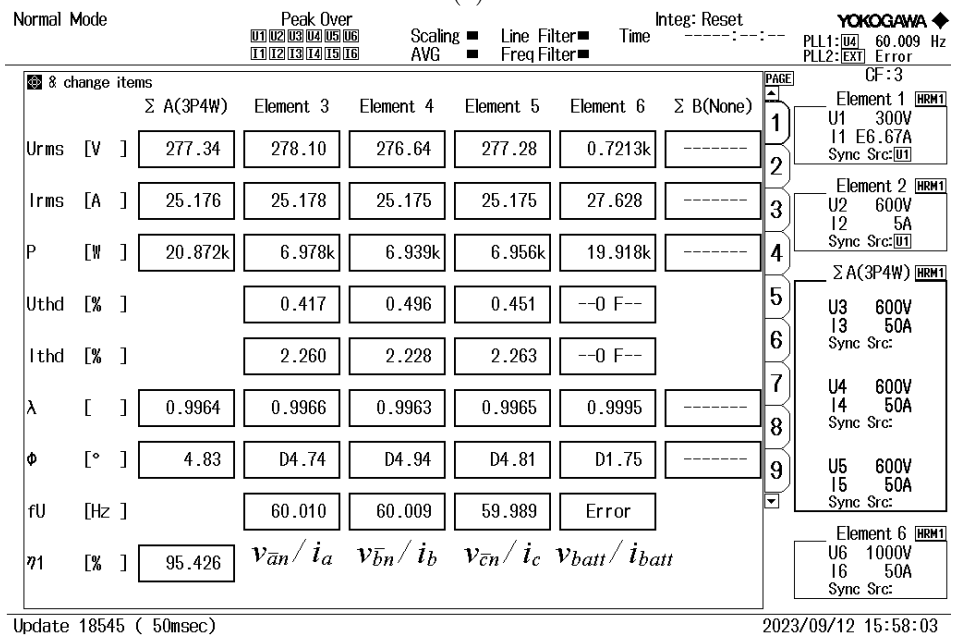
Fig. 4.40: Experimental results of the 20-kW unfolding-based ac-dc system operating at a closed-loop bandwidth of 1.8 kHz without active damping are illustrated as follows: (a) unstable and increasing oscillations in the system waveforms are observed, leading to grid-overcurrent shutdown; (b) Bode plots of the loop transfer function, $G_{L\text{-p-port}}$, indicating a negative phase margin at the gain crossover frequency of 1.8 kHz (G_{PI} parameters: $K_{p\text{-PI}} = 0.001$ and $K_{i\text{-PI}} = 251.4$). A positive phase margin cannot be achieved above the LC resonant frequency with a PI controller in the absence of active damping, leading to instability.

active damping, sustained undesirable LC oscillations are observed in the waveforms, as seen in Fig. 4.38(a). This leads to a high THD of 11.14% in grid currents, as depicted in Fig. 4.38(b), obtained from the Yokogawa WT1806E power analyzer. Such oscillatory response results in poor ac-dc power delivery.

Subsequently, the closed-loop bandwidth of the T-type bridge-based dc-dc converter control is increased to 1.8 kHz, close to the LC resonant frequency. In Fig. 4.40(a), the hard-



(a)



(b)

Fig. 4.41: Experimental results of the 20-kW unfolding-based ac-dc system operating at a closed-loop bandwidth of 1.8 kHz with active damping are illustrated as follows: (a) stable phase a ac input voltage, phase a grid current, dc-link voltage (v_{po}), and output battery current; (b) a low grid current THD of 2.26%, measured using the Yokogawa WT1806E power analyzer.

ware results depict the phase a ac input voltage, phase a grid current, dc-link voltage (v_{po}), and the output battery current. As the phase Bode plot of the plant without any damping

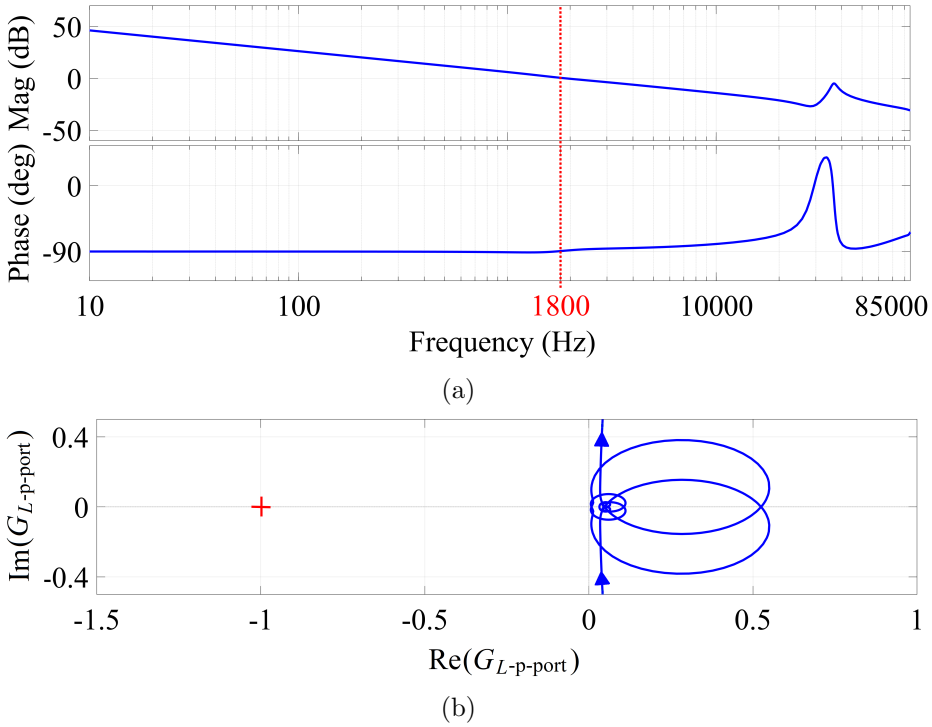
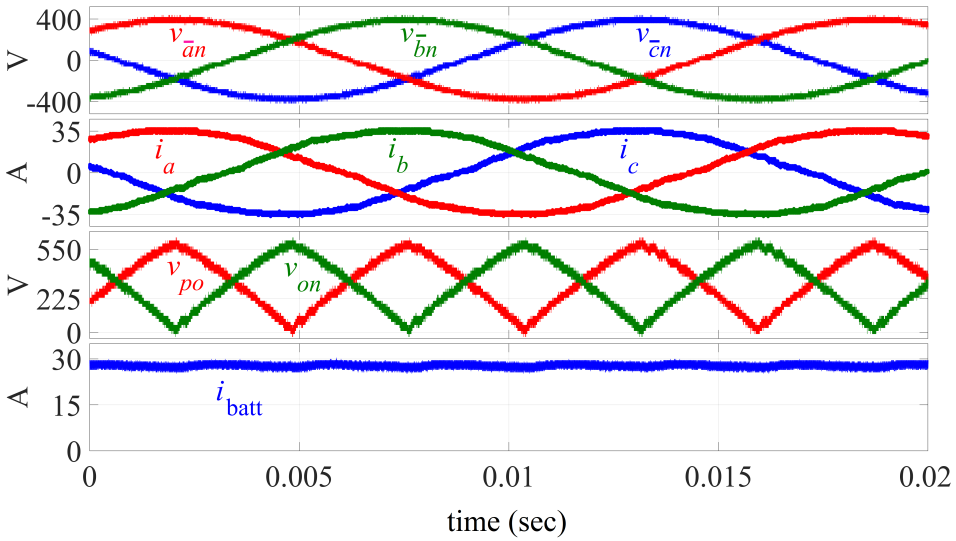


Fig. 4.42: (a) Bode plots of the loop transfer function, $G_{L\text{-p-port}}$, indicating a positive phase margin at the gain crossover frequency of 1.8 kHz (G_{PI} parameters: $K_{p\text{-PI}} = 0.001$ and $K_{i\text{-PI}} = 251.4$); and (b) the corresponding Nyquist plot, which does not encircle the point $(-1, j0)$, confirming a stable closed-loop operation. Active damping is enabled in this case.

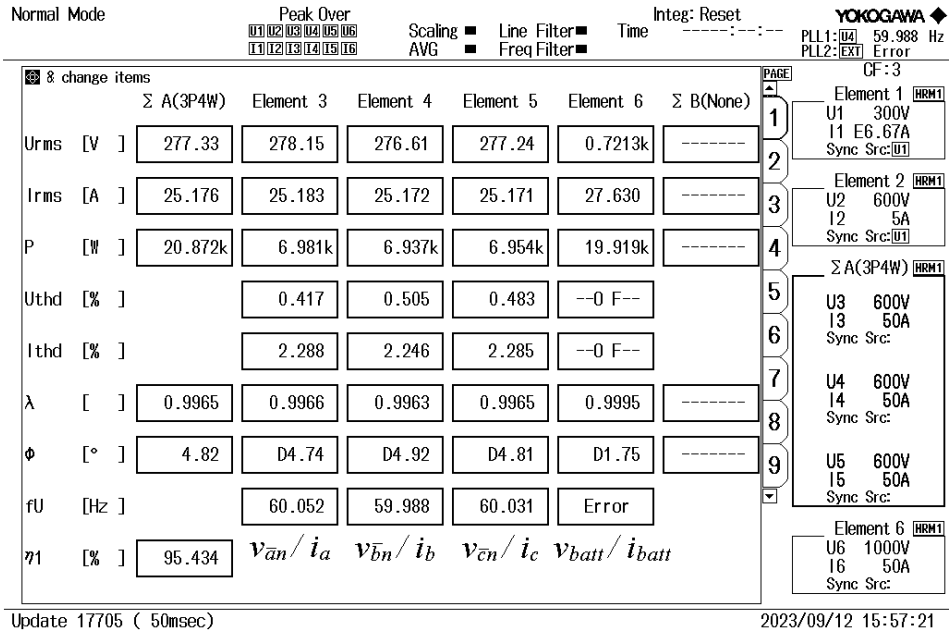
undergoes a '$-360°$' phase shift at the resonant frequency, the PI controller cannot achieve a positive phase margin, as shown in Fig. 4.40(b). This results in an unstable closed-loop operation, leading to growing oscillations in the grid currents, as depicted in Fig. 4.40(a). Consequently, the grid-overcurrent fault, employed for protection purposes, is triggered due to such growing oscillations, resulting in a system shutdown. To summarize, in the absence of active damping, stable operation is not achieved at closed-loop bandwidth levels near the LC resonant frequency. Moreover, undesirable oscillatory ac-dc power delivery is observed, even at a lower 300 Hz closed-loop bandwidth, leading to a higher grid current THD.

Unfolding-based ac-dc system operation with the current emulation-based active damping

The hardware prototype of the unfolding-based ac-dc system is tested at an output



(a)



(b)

Fig. 4.43: Experimental results of the 20-kW unfolding-based ac-dc system operating at a closed-loop bandwidth of 3 kHz with active damping are illustrated as follows: (a) stable 3-ϕ ac input voltages, grid currents, dc-link voltages, and output battery current; (b) a low grid current THD of 2.29%, measured using the Yokogawa WT1806E power analyzer.

power of 20 kW, incorporating current emulation-based active damping ($R_{\text{damp-emu}} = 9\Omega$) to mitigate the effects of LC resonance on power delivery. Initially, the closed-loop bandwidth of the T-type bridge-based dc-dc converter control is set to 1.8 kHz, close to the LC resonant

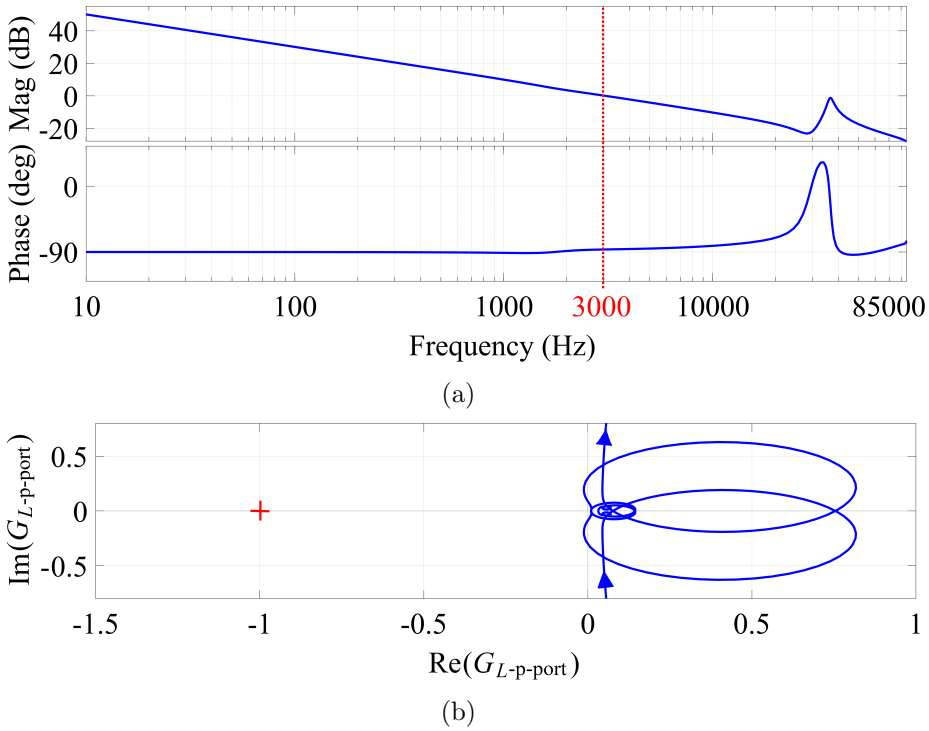


Fig. 4.44: (a) Bode plots of the loop transfer function, $G_{L\text{-p-port}}$, indicating a positive phase margin at the gain crossover frequency of 3 kHz (G_{PI} parameters: $K_{p\text{-PI}} = 0.001$ and $K_{i\text{-PI}} = 380.1$); and (b) the corresponding Nyquist plot, which does not encircle the point $(-1, j0)$, confirming a stable closed-loop operation. Active damping is enabled in this case.

frequency of 1.77 kHz. In Fig. 4.41(a), hardware results depict the stable phase a ac input voltage, phase a grid current, dc-link voltage (v_{po}), and the output battery current. Both the battery and grid currents show significant improvements and do not have any LC oscillations, even with the closed-loop bandwidth maintained in close proximity to the resonance. A low grid current THD of 2.26% is achieved in this case, as shown in Fig. 4.41(b). The corresponding Bode plots of the loop transfer function, $G_{L\text{-p-port}}$, with a gain-crossover frequency of 1.8 kHz and 90.7° phase margin are illustrated in Fig. 4.42(a). The accompanying Nyquist plot presented in Fig. 4.42(b), which does not encircle the point $(-1, j0)$, confirms the stability of the closed-loop operation at a bandwidth level of 1.8 kHz.

Additionally, the closed-loop bandwidth of the T-type bridge-based dc-dc converter control is further extended to 3 kHz. The unfolding-based ac-dc system continues to exhibit stable operation without any LC oscillations in the currents, as depicted in Fig. 4.43(a). A

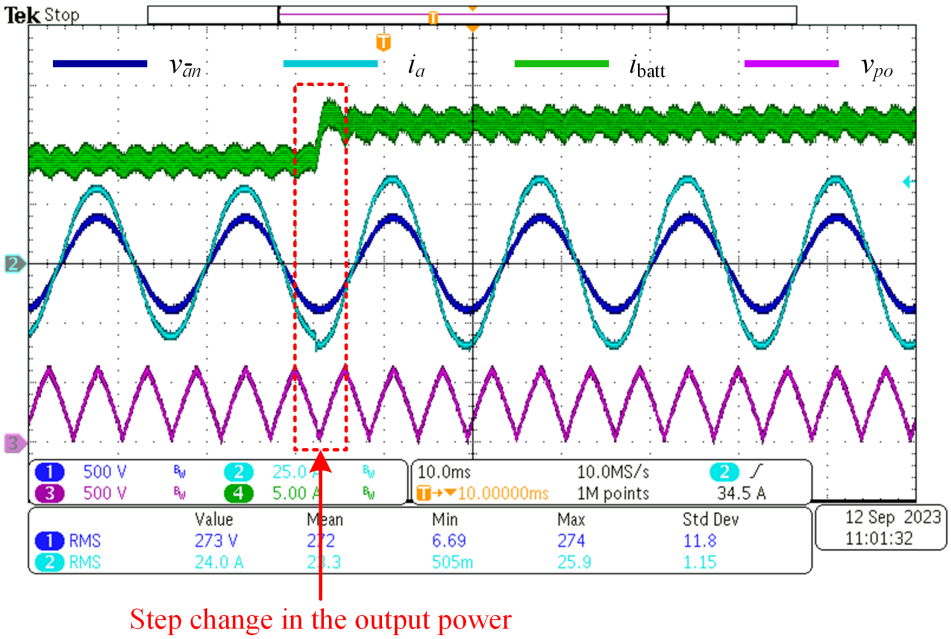


Fig. 4.45: An experimental step change in the output power is given from 17.5 kW to 20 kW by adjusting the amplitudes of the T-type bridge input currents, i_p and i_n, from 30 A to 35 A at the closed-loop bandwidth of 3 kHz. This change causes a step increase in grid currents as well, transitioning from 30 A peak to 35 A peak. The battery current also undergoes a step change from 24.3 A to 27.8 A. A stable transient response is achieved.

low grid current THD of 2.29% is also maintained, as illustrated in Fig. 4.43(b). The corresponding Bode plots of the loop transfer function, $G_{L\text{-p-port}}$, with a gain-crossover frequency of 3 kHz and 93.3° phase margin are presented in Fig. 4.44(a). Moreover, the associated Nyquist plot shown in Fig. 4.44(b), which does not encircle the point $(-1, j0)$, confirms the stability of the closed-loop operation at this high bandwidth level. Furthermore, the transient response of the ac-dc system, operating at a bandwidth level of 3 kHz, is assessed by implementing a step change in the output power from 17.5 kW to 20 kW, as depicted in Fig. 4.45. This adjustment is made by varying the amplitudes of the T-type bridge input currents, i_p and i_n, from 30 A to 35 A. This modification leads to a step change in grid-side currents as well, transitioning from 30 A peak to 35 A peak. The battery current also undergoes a step change from 24.3 A to 27.8 A.

Based on the simulation and experimental results, it can be concluded that stable steady-state and transient responses are achieved at bandwidth levels close to the LC

resonance and well above the LC resonant frequency. This is made possible due to the implementation of current emulation-based active damping. The sensing circuits employed for such high-bandwidth control are detailed in Appendix A.

4.4 Conclusion

In summary, this chapter conducts a comprehensive analysis of two key problems associated with high-efficiency, power-dense single-stage 3-ϕ unfolding-based ac-dc converters: (i) grid current distortions and (ii) the detrimental effects of LC resonance between the grid inductance and dc-link capacitors on closed-loop control. A detailed analysis of the current distortion is presented, and an equation governing the current during sector transitions is derived. To mitigate this issue, a control-based technique requiring no additional hardware is proposed, which utilizes the HF dc-dc converter to emulate current sources and sinks for distortion reduction. The operation of the proposed technique is studied on a grid-tied EV-battery charger circuit, and its effectiveness is verified through simulations and laboratory prototype experiments. A significant reduction in grid current THD is achieved.

Moreover, employing Middlebrook's extra element theorem, a detailed investigation into the characteristics of the LC resonance is carried out to assess its impact on closed-loop control. An in-depth analysis using phasor transformation-based small-signal modeling is performed to derive the necessary transfer functions, and simplified expressions are presented for clarity. A control-based solution is then proposed to damp the LC resonance, utilizing current emulation-based active damping through feedforward control of the HF T-type bridge dc-dc converter. The validity of this solution is confirmed through simulations and hardware verification on an unfolding-based ac-dc system for EV-battery charging applications. The hardware results demonstrate a tenfold increase in closed-loop bandwidth compared to systems without damping. Bandwidth levels higher than the LC resonant frequency are achieved, while maintaining a low grid current THD across all operating conditions with active damping. The proposed approach eliminates the need for physical damping circuits, offering a cost-effective means of suppressing resonance while enhancing power density, efficiency, and overall performance in unfolding-based ac-dc converters.

CHAPTER 5

PHASOR MODELING OF A T-TYPE BRIDGE-BASED DC-DC CONVERTER

5.1 Introduction

As discussed in Chapter 2 and Chapter 3, the unfolding-based ac-dc conversion system with a T-type bridge-based dc-dc converter used in this study is designed for WPT application. WPT systems often use dc-dc resonant converters with single-sided or double-sided *LCC* resonant networks to generate a current source for charging EV batteries [48, 49, 91]. Given the widespread use of *LCC* networks in dc-dc converters, this chapter employs a T-type bridge-based dc-dc converter with both single-sided and double-sided *LCC* resonant networks and conducts a thorough small-signal analysis of the system. In this study, the T-type bridge-based dc-dc resonant converter connects to a grid-tied Unfolder. The Unfolder switches operate at a maximum of twice the grid frequency, converting each negative segment of the ac input voltages into positive polarity, as discussed in previous chapters. With the Unfolder operating in open-loop, the small-signal modeling centers on the T-type bridge-based dc-dc converter, which is closed-loop controlled to regulate the battery load current and ensure grid-side PFC.

The higher-order single-sided or double-sided *LCC* resonant tank, designed with an appropriate quality factor, leads to sinusoidal current or voltage waveforms on both the primary and secondary sides of the dc-dc converter. In this context, the use of a phasor transformation-based small-signal modeling approach, as discussed in [25, 60–62, 86, 87, 92–94], is deemed appropriate. Previously, GSSA has been used for modeling *LCC* tank-based resonant converters [48, 59]. However, GSSA involves complex mathematical analysis and lacks intuitive clarity in the modeling steps, and prior works have not verified *LCC* tank-based modeling in hardware. In contrast, the phasor transformation-based modeling proposed in this chapter offers an intuitive understanding of each step, serving as a valuable

tool for both analysis and closed-loop control design. Moreover, as discussed in previous chapters, this study employs a diode-bridge rectifier on the secondary side of the isolation stage to make the system suitable for practical WPT applications. It has been observed that the conventional approach of modeling the diode bridge as an equivalent resistor using the FHA, as described in [58, 93], results in excessive and inaccurate damping of higher-frequency resonances for a battery load, leading to errors in small-signal modeling. To address this, this chapter introduces an alternative method that models the diode bridge with a battery load as a dependent voltage sink, providing a more accurate representation. This voltage sink experiences phase deviations that align with variations in the diode bridge input current in response to perturbations in the control input, while its magnitude remains constant. The proposed method yields precise small-signal modeling results and effectively captures the higher-frequency resonances.

The proposed small-signal modeling analysis is validated through simulations on a 20 kW T-type bridge-based dc-dc converter incorporating an *LCC* resonant network. Additionally, hardware testing on a 4 kW, 85 kHz battery charger prototype confirms the accuracy of the modeling process for perturbation frequencies up to 55 kHz.

5.2 Notation

In this chapter, small-signal quantities are denoted by lowercase letters with a hat notation (such as $\hat{i}_{\text{load}}$), while steady-state quantities are indicated using capital letters (for instance, I_{load}). Quantities specified with only lowercase letters, without a hat (e.g., $i_{\text{load}} = I_{\text{load}} + \hat{i}_{\text{load}}$), represent full signal quantities, which include both steady-state and small-signal components. Phasors are indicated by an arrow (as in $\overrightarrow{v_{xy}}$), while magnitudes (peak values) are denoted by double bars (such as $\|\vec{i_x}\|$). Additionally, magnitudes are also identified by 'mag' in the subscript. Finally, angled brackets (e.g., $\langle i_{\text{out}} \rangle$) are used for average values.

5.3 Secondary-Side Diode-Bridge Rectifier in the Small-Signal Domain

In resonant dc-dc converters, as shown in Fig. 5.1(a), with an appropriate quality factor

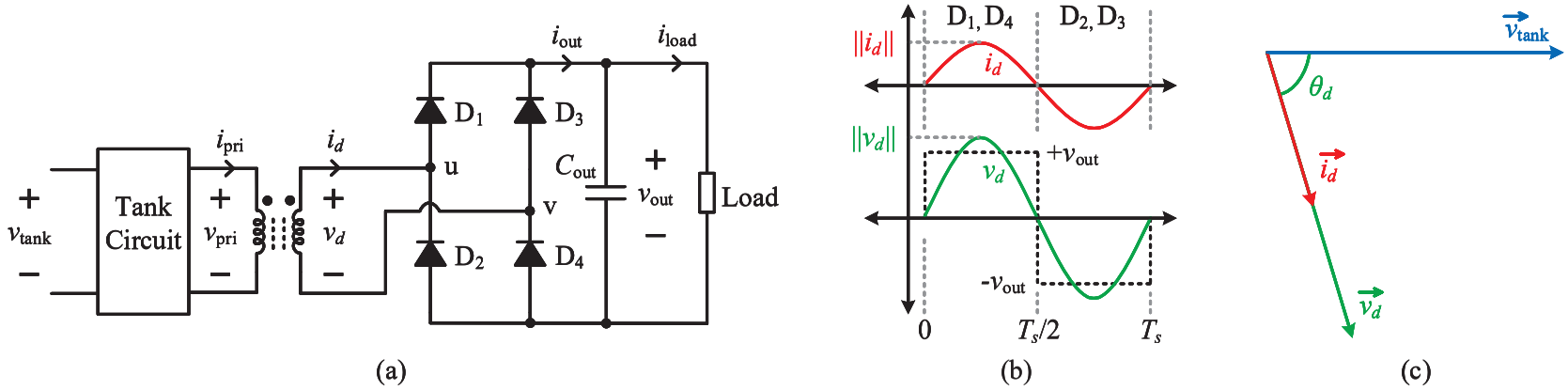


Fig. 5.1: (a) Typical circuit configuration of a resonant dc-dc converter with a diode bridge on the secondary side connected to a generic load; (b) current and voltage waveforms at the input of the diode bridge; and (c) a phasor diagram of current and voltage quantities in the dc-dc converter.

of the tank circuit, the tank current entering the diode-bridge rectifier, denoted as i_d in this work, exhibits a sinusoidal shape [58]. During the positive half-cycle of this current, diodes D_1 and D_4 conduct, resulting in a positive voltage ("$+v_{\text{out}}$") across the input of the diode bridge. On the other hand, during the negative half-cycle of the current, diodes D_2 and D_3 conduct, causing a negative voltage ("$-v_{\text{out}}$") to appear across the input of the diode bridge. As a result, this switching pattern of diodes generates a square-wave voltage at the input of the diode bridge that is in phase with the current i_d, as depicted in Fig. 5.1(b). Furthermore, the sinusoidal fundamental component of this square-wave voltage, denoted as v_d, also remains in phase with the current i_d. Both i_d and v_d can be represented as phasor quantities:

$$\vec{i_d} = \|\vec{i_d}\| e^{-j\theta_d}\,, \tag{5.1}$$

$$\vec{v_d} = \|\vec{v_d}\| e^{-j\theta_d} = \frac{4}{\pi} v_{\text{out}}\, e^{-j\theta_d}\,, \tag{5.2}$$

where v_{out} represents the output dc voltage across the load and θ_d denotes the amount of phase lag of the diode-bridge rectifier input current relative to the voltage applied across the tank input, as illustrated in Fig. 5.1(c). It can be observed from (5.2) that the magnitude of $\vec{v_d}$ depends upon the output dc voltage, while its phase always aligns exactly with the phase of $\vec{i_d}$, as depicted in the phasor diagram given in Fig. 5.1(c).

5.3.1 Resistive Load

In a typical configuration with a resistive load connected to the output of the diode-bridge rectifier, as shown in Fig. 5.2(a), small-signal perturbations introduced in the tank input voltage (by perturbing the duty ratios of the primary bridge) lead to small-signal deviations in both the magnitude and phase of $\vec{i_d}$. These small-signal deviations are also proportionally reflected in the output dc voltage, v_{out}, due to its dependency on $\vec{i_d}$, as given by

$$v_{\text{out}} = i_{\text{load}}\, R_{\text{load}} = \frac{2}{\pi} \|\vec{i_d}\|\, R_{\text{load}}\,. \tag{5.3}$$

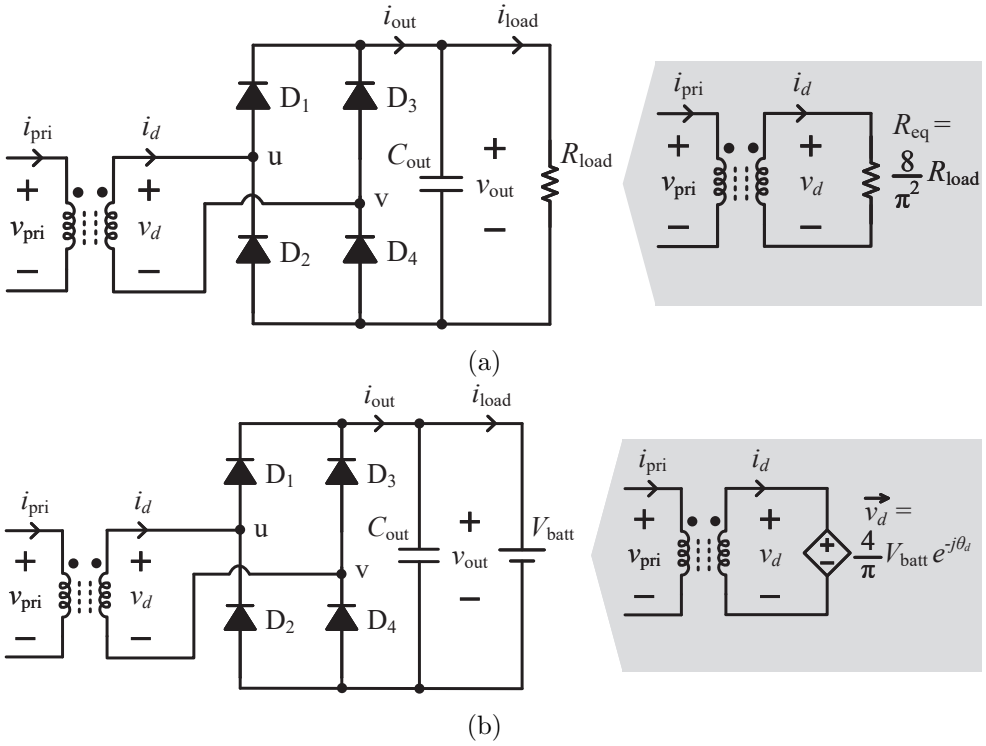


Fig. 5.2: (a) The diode-bridge rectifier with a resistive load can be modeled as an equivalent resistor in the small-signal domain; (b) the diode-bridge rectifier with a battery load needs to be modeled as a dependent voltage sink in the small-signal domain.

Now, using (5.2) and (5.3), $\vec{v_d}$ can be calculated as

$$\left.\begin{aligned} \vec{v_d} &= \frac{8}{\pi^2} R_{\text{load}} \, \|\vec{i_d}\| e^{-j\theta_d} \\ &= R_{\text{eq}} \, \|\vec{i_d}\| e^{-j\theta_d} \\ &= R_{\text{eq}} \, \vec{i_d} \, . \end{aligned}\right\} \tag{5.4}$$

Therefore, the diode bridge input voltage in the small-signal domain, in the case of a resistive load, is given as

$$\hat{\vec{v_d}} = R_{\text{eq}} \, \hat{\vec{i_d}} \, , \tag{5.5}$$

where

$$R_{\text{eq}} = \frac{8}{\pi^2} R_{\text{load}} \, , \tag{5.6}$$

represents the equivalent resistor that can be used to model the diode-bridge rectifier with a resistive load in the small-signal domain, as depicted in Fig. 5.2(a).

5.3.2 Battery Load

In the case where a battery is connected to the output of the diode-bridge rectifier, as depicted in Fig. 5.2(b), small-signal perturbations in the tank input voltage (by perturbing the duty ratios of the primary bridge) induce corresponding small-signal deviations in both the magnitude and phase of $\vec{i_d}$. However, the output dc voltage, v_{out}, exhibits negligible deviation in the small-signal domain due to the significantly higher time constant of the battery State of Charge [95]. Therefore, during small-signal analysis, the battery voltage, which is the output dc voltage, can be considered constant [94]. As a result, the input voltage phasor of the diode bridge, $\vec{v_d}$, given by (5.2), has a constant magnitude, but its phase varies during small-signal analysis,

$$\vec{v_d} = \frac{4}{\pi} V_{\text{batt}}\, e^{-j\theta_d}\,. \tag{5.7}$$

Therefore, in the case of a battery load, the diode bridge input voltage phasor in the small-signal domain is given as

$$\hat{\vec{v}}_d = -j\frac{4}{\pi} V_{\text{batt}}\, e^{-j\Theta_d}\hat{\theta}_d\,, \tag{5.8}$$

where V_{batt} is the battery voltage, and Θ_d is the steady-state phase lag of the diode bridge input current phasor, $\vec{I_d}$, relative to the tank input voltage. It can be observed from (5.8) that the diode bridge circuit cannot be simply modeled as a resistor in the case of a battery-connected load. The circuit needs to be modeled as a dependent voltage sink with a constant magnitude but a variable phase that depends upon the phase deviations of the diode bridge input current. The circuit diagram for this scenario is shown in Fig. 5.2(b). Incorrectly modeling this circuit as a resistor excessively damps higher-frequency resonance, as will be discussed in the experimental results section, leading to inaccuracies in small-

signal modeling. On the other hand, since the phase lag angle, θ_d, of the diode bridge input voltage in a dc-dc converter with a secondary-side diode bridge is not directly regulated by a controller, one might consider treating this angle as a steady-state constant, Θ_d, by neglecting its small-signal variations. This would render the diode bridge input voltage an independent quantity with constant magnitude and phase. However, this approach introduces excessive resonances and leads to inaccurate modeling results, as discussed in the experimental validation section.

5.4 Brief Overview of Circuit Configuration, Modulation Strategy, and Closed-Loop Control

In Fig. 5.3, a circuit diagram of the T-type bridge-based dc-dc converter is illustrated, consisting of either a single-sided or double-sided LCC resonant tank with isolation. As the topology is designed for WPT applications, where communicating control signals to the isolated side is challenging, a diode-bridge rectifier is used on the secondary side to connect to the battery load. The dc-dc converter in this study is connected to a grid-tied Unfolder operating in open-loop mode, switching at a frequency up to twice the grid frequency. The closed-loop control architecture is specifically designed for the HF T-type bridge-based dc-dc converter to regulate the battery load current. The duty calculator, as depicted in Fig. 5.3, accurately calculates the duty ratios (d_p and d_n) based on the modulation index (m_i) obtained from the closed-loop control and the grid angle (θ_{grid}), which is calculated using the PLL. The duty calculator, along with the closed-loop control, ensures the desired load current while maintaining PFC on the grid side. A detailed description of the circuit configuration, modulation strategy, and closed-loop control is provided in Chapter 2. Since the Unfolder operates in open-loop mode, the small-signal analysis in this chapter focuses exclusively on the closed-loop controlled T-type bridge-based dc-dc conversion system, incorporating either a single-sided or double-sided LCC resonant tank. Moreover, in this chapter, the T-type bridge is operated using center-aligned modulation, as discussed in Chapter 2. However, a similar analysis can be performed when the T-type bridge is operated using leading-edge-aligned modulation, as discussed in Chapter 3. Hardware results

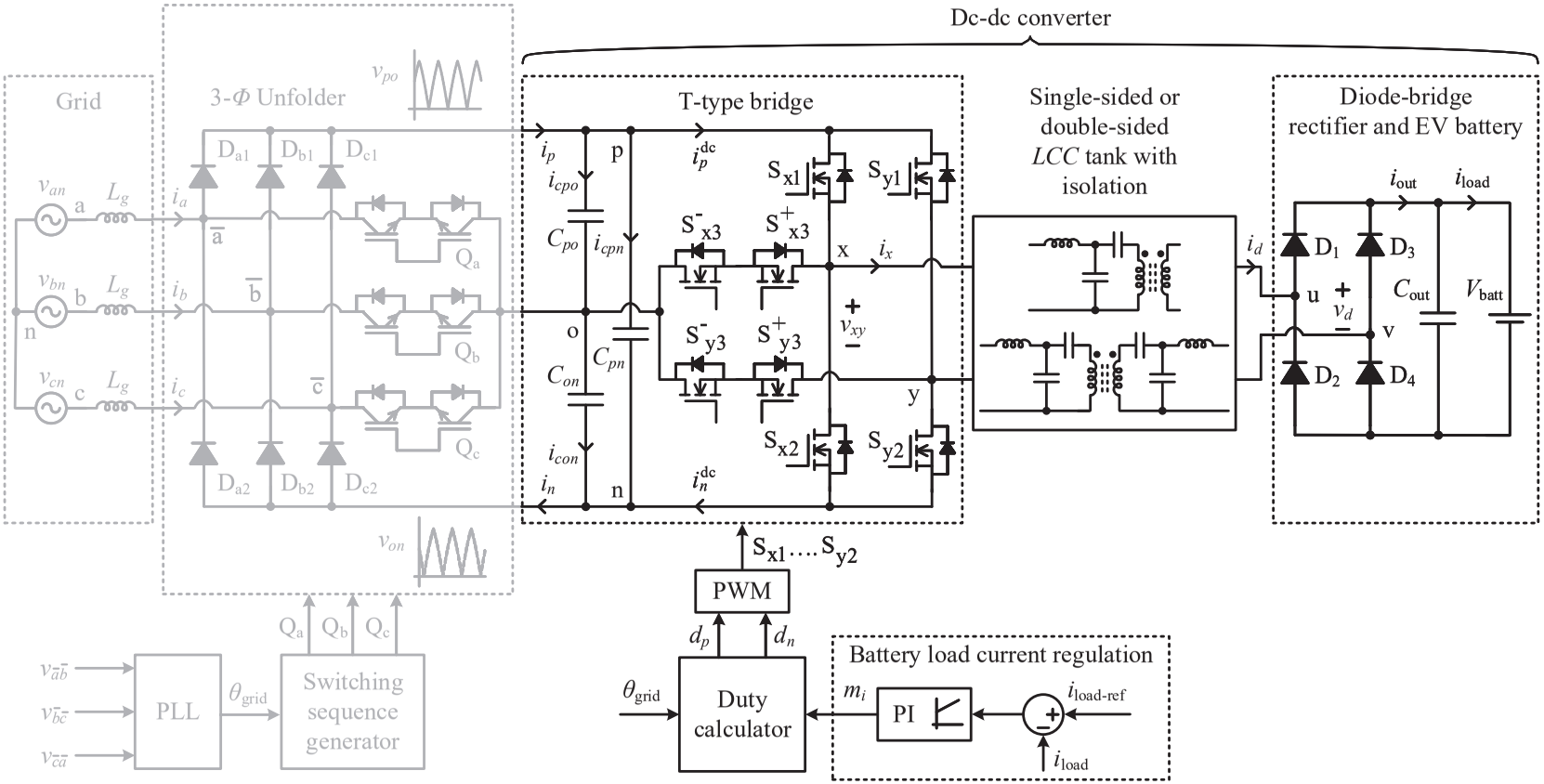


Fig. 5.3: Circuit diagram of a T-type bridge-based dc-dc converter featuring a single-sided or double-sided *LCC* tank with isolation and a diode bridge in an unfolding-based battery charger. The closed-loop control regulates the battery load current.

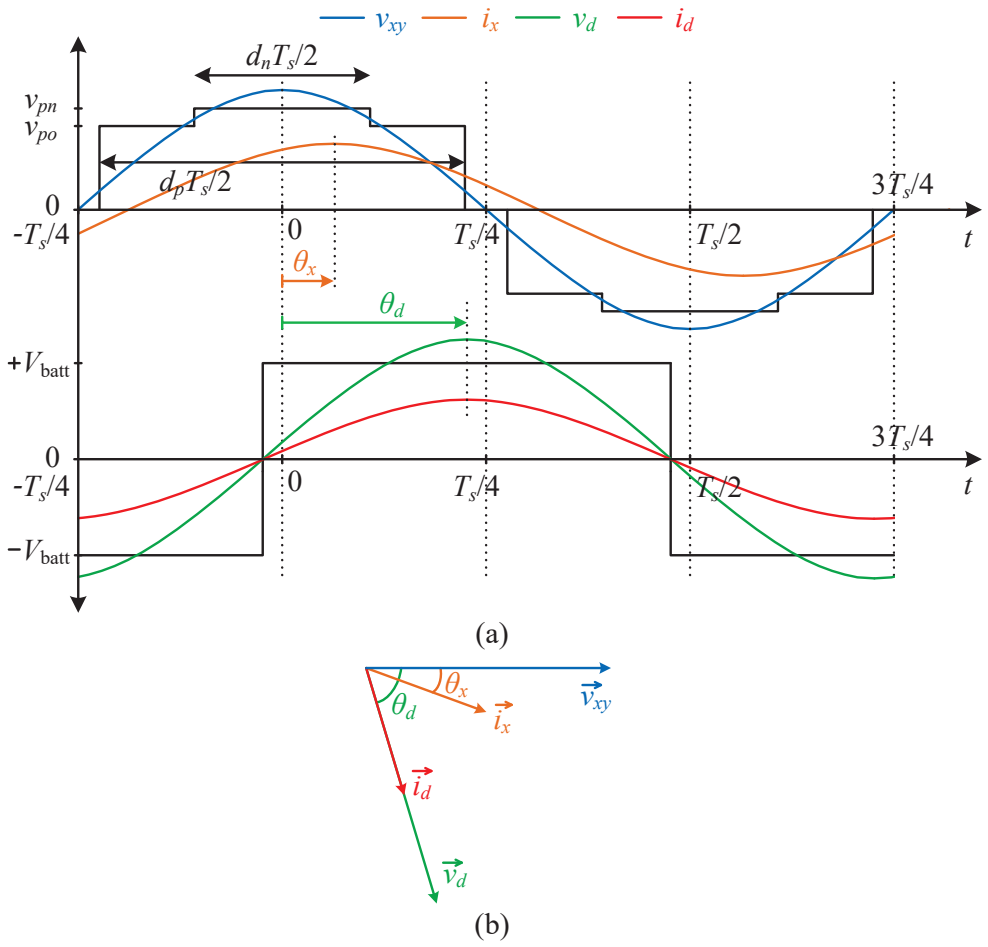


Fig. 5.4: (a) Fundamental components of the T-type bridge output voltage, v_{xy}, and current, i_x, as well as the diode bridge input voltage, v_d, and current, i_d. The operating region where $d_p > d_n$ is shown, and the two quasi-square voltages generated at the output of the T-type bridge using these duty ratios are center-aligned. (b) Phasor diagram of the voltage and current quantities in the T-type bridge-based dc-dc converter.

for both modulation strategies are provided in the experimental validation section.

5.5 Derivation of the Phasor Transformer

The application of the phasor transformer to model switching converters within the resonant dc-dc system has been previously investigated for representing an H-bridge [62]. The derivation established in the prior work has been extended here to represent the T-type bridge and the diode bridge utilized in this analysis. The implementation of a single-sided or double-sided higher-order *LCC* resonant tank with an appropriate quality factor

facilitates the achievement of sinusoidal current or voltage waveforms on both the primary and secondary sides of the dc–dc conversion system. Consequently, the subsequent analysis considers only the fundamental components of the tank voltage and current quantities. The fundamental component of the voltage at the output of the T-type bridge, denoted as v_{xy} and shown in Fig. 5.4(a), is derived from the two dc input voltages, v_{po} and v_{on}, along with their corresponding duty ratios, d_p and d_n:

$$\left.\begin{aligned} v_{xy}(t) &= v_{xy\text{-}po}(t) + v_{xy\text{-}on}(t) \\ &= \frac{4}{\pi}\left[v_{po}\sin\left(\frac{\pi d_p}{2}\right) + v_{on}\sin\left(\frac{\pi d_n}{2}\right)\right]\cos\left(\omega_s t\right) , \end{aligned}\right\} \tag{5.9}$$

where

$$v_{xy\text{-}po}(t) = \frac{4}{\pi} v_{po}\sin\left(\frac{\pi d_p}{2}\right)\cos\left(\omega_s t\right) , \tag{5.10}$$

$$v_{xy\text{-}on}(t) = \frac{4}{\pi} v_{on}\sin\left(\frac{\pi d_n}{2}\right)\cos\left(\omega_s t\right) , \tag{5.11}$$

and ω_s represents the angular switching frequency of the T-type bridge, which remains constant ($f_s = 85$ kHz) for this application in accordance with the WPT standard J2954, established by the SAE [52]. By considering the voltage ratio between the ac and dc sides, two effective turns ratios (or switching functions) for the T-type bridge can be defined as

$$s_{po}(t) = \frac{v_{xy\text{-}po}}{v_{po}} = \frac{4}{\pi}\sin\left(\frac{\pi d_p}{2}\right)\cos\left(\omega_s t\right) , \tag{5.12}$$

$$s_{on}(t) = \frac{v_{xy\text{-}on}}{v_{on}} = \frac{4}{\pi}\sin\left(\frac{\pi d_n}{2}\right)\cos\left(\omega_s t\right) , \tag{5.13}$$

or, equivalently, in phasor form at a constant angular frequency of ω_s, as

$$\overrightarrow{s_{po}} = \frac{4}{\pi}\sin\left(\frac{\pi d_p}{2}\right) , \tag{5.14}$$

$$\overrightarrow{s_{on}} = \frac{4}{\pi}\sin\left(\frac{\pi d_n}{2}\right) . \tag{5.15}$$

By combining the above equations, the voltage at the output of the T-type bridge can be expressed in phasor form using the switching functions as

$$\overrightarrow{v_{xy}} = \overrightarrow{v_{xy\text{-}po}} + \overrightarrow{v_{xy\text{-}on}} = \overrightarrow{s_{po}}\, v_{po} + \overrightarrow{s_{on}}\, v_{on}\,. \tag{5.16}$$

Similarly, the voltage at the input of the diode bridge can be expressed in phasor form as

$$\overrightarrow{v_d} = \overrightarrow{s_d}\, V_{\text{batt}}\,, \tag{5.17}$$

where

$$\overrightarrow{s_d} = \frac{4}{\pi} e^{-j\theta_d}\,. \tag{5.18}$$

Here, θ_d represents the phase lag of the diode bridge input voltage phasor, $\overrightarrow{v_d}$, relative to the T-type bridge output voltage phasor, $\overrightarrow{v_{xy}}$, as shown in Fig. 5.4(b). It is important to note that the phases of the fundamental components of the diode bridge input voltage, v_d, and the diode bridge input current, i_d, always align exactly in both steady-state and small-signal conditions, as discussed earlier. The overlap of these two quantities is illustrated in the phasor diagram provided in Fig. 5.4(b). The diode bridge input current phasor is therefore expressed as

$$\overrightarrow{i_d} = \|\overrightarrow{i_d}\| e^{-j\theta_d}\,. \tag{5.19}$$

By employing the definitions of tank ac voltages derived in (5.16) and (5.17) in relation to the switching functions, the T-type bridge-based dc-dc conversion system can be represented using phasor transformers for both single-sided and double-sided LCC resonant tanks, as depicted in Fig. 5.5. Using the phasor transformers-based circuit diagram, the

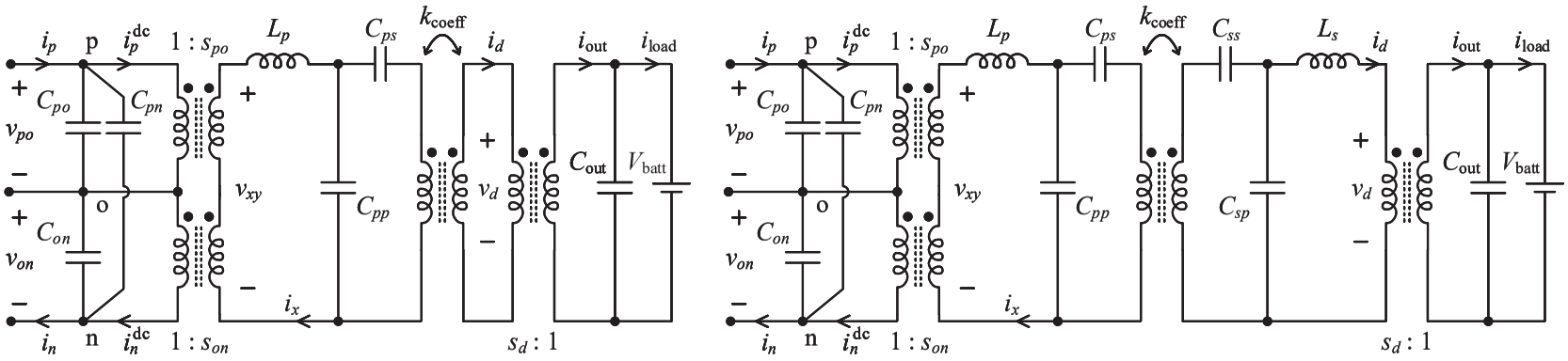


Fig. 5.5: T-type bridge-based dc-dc converter with a primary T-type bridge and secondary diode bridge modeled using phasor transformers, featuring (a) a single-sided *LCC* resonant tank with isolation, and (b) a double-sided *LCC* resonant tank with isolation.

output current of the diode bridge can be calculated as

$$\left.\begin{aligned} i_{\text{out}} = \langle i_{\text{out}} \rangle + i_{\text{out}}^{\text{HF}} &= \Re\big[\vec{s_d}\, e^{j\omega_s t}\big]\Re\big[\vec{i_d}\, e^{j\omega_s t}\big] \\ &= \Re\left[\frac{\vec{s_d}^*}{\sqrt{2}}\frac{\vec{i_d}}{\sqrt{2}}\right] + \Re\left[\frac{\vec{s_d}}{\sqrt{2}}\frac{\vec{i_d}}{\sqrt{2}}\, e^{2j\omega_s t}\right] . \end{aligned}\right\} \tag{5.20}$$

The battery load current, which is the averaged component of the output current of the diode bridge, can now be written as

$$\left.\begin{aligned} i_{\text{load}} = \langle i_{\text{out}} \rangle = \Re\left[\frac{\vec{s_d}^*}{\sqrt{2}}\frac{\vec{i_d}}{\sqrt{2}}\right] &= \Re\left[\left(\frac{4}{\sqrt{2}\pi}e^{-j\theta_d}\right)^* \frac{\|\vec{i_d}\|}{\sqrt{2}}e^{-j\theta_d}\right] \\ &= \frac{2}{\pi}\|\vec{i_d}\| . \end{aligned}\right\} \tag{5.21}$$

Similarly, the input dc currents of the T-type bridge can be calculated as

$$i_p = \langle i_p^{\text{dc}} \rangle = \Re\left[\frac{\vec{s_{po}}^*}{\sqrt{2}}\frac{\vec{i_x}}{\sqrt{2}}\right] = \frac{2}{\pi}\|\vec{i_x}\|\cos(\theta_x)\sin\left(\frac{\pi d_p}{2}\right) , \tag{5.22}$$

$$i_n = \langle i_n^{\text{dc}} \rangle = \Re\left[\frac{\vec{s_{on}}^*}{\sqrt{2}}\frac{\vec{i_x}}{\sqrt{2}}\right] = \frac{2}{\pi}\|\vec{i_x}\|\cos(\theta_x)\sin\left(\frac{\pi d_n}{2}\right) , \tag{5.23}$$

where $\|\vec{i_x}\|$ and θ_x are the magnitude and phase angle, respectively, of the T-type bridge output current phasor, $\vec{i_x}$, as depicted in Fig. 5.4(b).

5.6 Small Signal Analysis

The output voltage of the T-type bridge, as defined in (5.9), can be expressed in phasor form as

$$\vec{v_{xy}} = \frac{4}{\pi}\left[v_{po}\sin\left(\frac{\pi d_p}{2}\right) + v_{on}\sin\left(\frac{\pi d_n}{2}\right)\right]\angle 0 , \tag{5.24}$$

which can be further solved by substituting the following expressions for v_{po}, v_{on}, d_p, and d_n during $0 \le \theta_{\text{grid}} < \pi/3$:

$$v_{po} = V_{g\text{-mag}} \sin\left(\theta_{\text{grid}} + {}^{2\pi}/_{3}\right) , \tag{5.25}$$

$$v_{on} = V_{g\text{-mag}} \sin\left(\theta_{\text{grid}}\right) , \tag{5.26}$$

$$d_p = ({}^{2}/_{\pi}) \sin^{-1}\left(m_i \sin\left(\theta_{\text{grid}} + {}^{\pi}/_{2}\right)\right) , \tag{5.27}$$

$$d_n = ({}^{2}/_{\pi}) \sin^{-1}\left(m_i \sin\left(\theta_{\text{grid}} + {}^{\pi}/_{6}\right)\right) , \tag{5.28}$$

where $V_{g\text{-mag}}$ represents the peak value of the line-to-line ac input voltage of the Unfolder, and m_i is the modulation index that controls the magnitude of the duty ratios. A detailed discussion of the above equations is provided in Chapter 2. By combining (5.24)–(5.28), the T-type bridge output voltage phasor, $\overrightarrow{v_{xy}}$, can be expressed as

$$\overrightarrow{v_{xy}} = \frac{2\sqrt{3}}{\pi} m_i V_{g\text{-mag}} \angle 0 = \frac{2\sqrt{3}}{\pi} m_i V_{g\text{-mag}} \, . \tag{5.29}$$

As the modulation index m_i controls the magnitude of the T-type bridge output voltage, which defines the load current i_{load} charging the battery, a small-signal analysis is conducted on the plant transfer function derived between the small-signal load current $\hat{i}_{\text{load}}$ and the small-signal modulation index $\hat{m}_i$:

$$G_{\text{plant}} = \frac{\hat{i}_{\text{load}}}{\hat{m}_i} \, . \tag{5.30}$$

5.6.1 Single-Sided LCC Tank

Small-signal phasor-transformed circuit

To derive the small-signal phasor-transformed circuit, the tank inductors and capacitors are phasor-transformed as described in [61]. The inductor is represented as a series combination of the dynamic impedance (sL) and the steady-state impedance ($j\omega_s L$) while the capacitor is represented as a parallel combination of the dynamic impedance $\left(\frac{1}{sC}\right)$ and the steady-state impedance $\left(\frac{1}{j\omega_s C}\right)$. The output voltage of the T-type bridge is linearized

around the steady-state value of the control input m_i, allowing the steady-state and small-signal components of $\overrightarrow{v_{xy}}$ to be expressed as

$$\left.\begin{aligned}\overrightarrow{v_{xy}} = \overrightarrow{V_{xy}} + \hat{\overrightarrow{v_{xy}}} &= \overrightarrow{V_{xy}} + \left(\frac{\partial \overrightarrow{v_{xy}}}{\partial m_i}\right)\hat{m}_i \\ &= \frac{2\sqrt{3}}{\pi} M_i V_{g\text{-mag}} + \frac{2\sqrt{3}}{\pi}\hat{m}_i V_{g\text{-mag}}\,.\end{aligned}\right\} \tag{5.31}$$

Therefore,

$$\frac{\hat{\overrightarrow{v_{xy}}}}{\hat{m}_i} = \frac{2\sqrt{3}}{\pi} V_{g\text{-mag}}\,. \tag{5.32}$$

Now, the diode bridge input voltage, written as

$$\overrightarrow{v_d} = \frac{4}{\pi} V_{\text{batt}}\, e^{-j\theta_d}\,, \tag{5.33}$$

can be expressed in terms of the small-signal component by taking the partial derivative with respect to the control input, m_i. The phase lag, θ_d, undergoes small-signal deviations due to perturbations in m_i. The magnitude, which is a function of the battery voltage (V_{batt}), is treated as a constant, as the battery voltage shows a negligible deviation in the small-signal domain due to the significantly higher time constant of the State of Charge [95]. Therefore, the steady-state and small-signal components of the diode bridge input voltage can be expressed as

$$\left.\begin{aligned}\overrightarrow{v_d} = \overrightarrow{V_d} + \hat{\overrightarrow{v_d}} &= \overrightarrow{V_d} + \left(\frac{\partial \overrightarrow{v_d}}{\partial m_i}\right)\hat{m}_i \\ &= \frac{4}{\pi} V_{\text{batt}}\, e^{-j\Theta_d} - j\frac{4}{\pi} V_{\text{batt}}\, e^{-j\Theta_d}\hat{\theta}_d\,.\end{aligned}\right\} \tag{5.34}$$

Therefore,

$$\frac{\hat{\overrightarrow{v_d}}}{\hat{m}_i} = -j\frac{4}{\pi} V_{\text{batt}}\, e^{-j\Theta_d}\frac{\hat{\theta}_d}{\hat{m}_i}\,. \tag{5.35}$$

The overall linearized steady-state and small-signal model of the T-type bridge-based

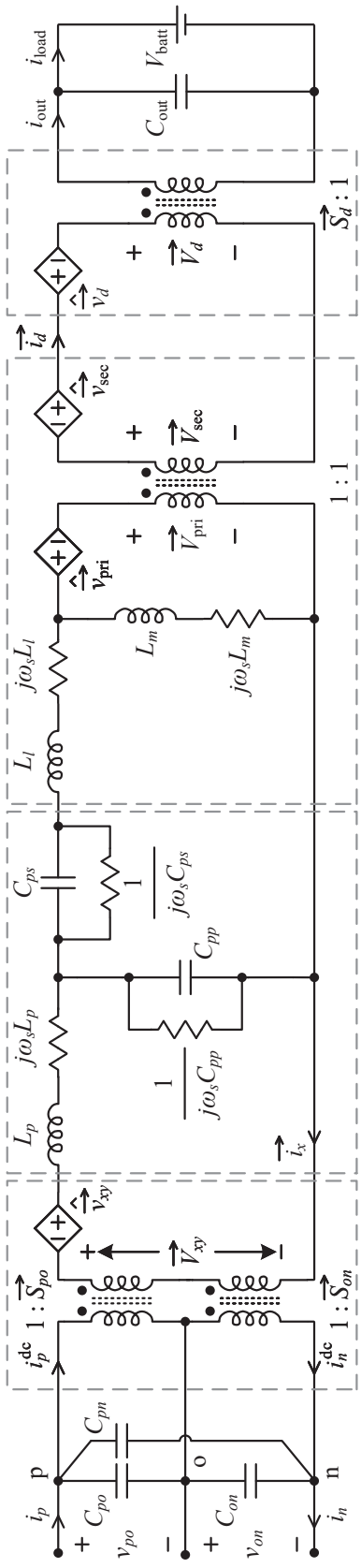


Fig. 5.6: Combined steady-state and small-signal phasor-transformed model of the T-type bridge-based dc-dc system, with a single-sided LCC tank, a diode bridge connected to a battery, and isolation represented by the cantilever model. Parasitic resistances are not shown but are included in the derived expressions.

dc-dc converter with a single-sided LCC tank is illustrated in Fig. 5.6. The isolation is represented using the cantilever model, incorporating leakage and magnetizing inductances. To enhance the accuracy of the model, the parasitic resistances of inductors and capacitors are introduced as series and parallel resistances, respectively, as done while presenting the simulation and experimental results.

Small-signal diode bridge input current

As derived in (5.21), the load current i_{load} is a function of the magnitude of the diode bridge input current i_d. Therefore, to obtain the plant transfer function, the small-signal deviations in the diode bridge input current phasor, $\hat{\vec{i}}_d$, are calculated in relation to perturbations introduced in the control input, $\hat{m}_i$. The small-signal diode bridge input current phasor is calculated using Fig. 5.6 as

$$\hat{\vec{i}}_d = \frac{\left(\hat{\vec{v}}_{xy} - \hat{\vec{v}}_d(f_1 f_3 - f_4)\right)}{f_2 f_3} = \frac{\left(\frac{2\sqrt{3}}{\pi}\hat{m}_i V_{g\text{-mag}} + j\frac{4}{\pi}V_{\text{batt}}\, e^{-j\Theta_d}\hat{\theta}_d(f_1 f_3 - f_4)\right)}{f_2 f_3}, \tag{5.36}$$

where f_1, f_2, f_3, and f_4 are functions of the tank parameters:

$$f_1 = \frac{Z_{ps} + Z_l + Z_m}{Z_m}, \tag{5.37}$$

$$f_2 = Z_{ps} + Z_l, \tag{5.38}$$

$$f_3 = 1 + \frac{Z_p}{Z_{pp}} + \frac{Z_p}{Z_{ps} + Z_l}, \tag{5.39}$$

$$f_4 = \frac{Z_p}{Z_{ps} + Z_l}, \tag{5.40}$$

$$Z_p = sL_p + j\omega_s L_p + r_{L_p}, \tag{5.41}$$

$$Z_{pp} = \frac{r_{C_{pp}}}{1 + r_{C_{pp}}(sC_{pp} + j\omega_s C_{pp})}, \tag{5.42}$$

$$Z_{ps} = \frac{r_{C_{ps}}}{1 + r_{C_{ps}}(sC_{ps} + j\omega_s C_{ps})}, \tag{5.43}$$

$$Z_l = sL_l + j\omega_s L_l + r_{L_l}, \tag{5.44}$$

$$Z_m = sL_m + j\omega_s L_m, \tag{5.45}$$

where r_{L_p}, $r_{C_{pp}}$, $r_{C_{ps}}$, and r_{L_l} represent the parasitic resistances of the tank inductors and capacitors. Equation (5.36) can be modified into a transfer function using (5.32) and (5.35):

$$\left.\begin{aligned}\frac{\hat{\vec{i}}_d}{\hat{m}_i} &= \frac{\left(\frac{\hat{\vec{v}}_{xy}}{\hat{m}_i} - \frac{\hat{\vec{v}}_d}{\hat{m}_i}(f_1 f_3 - f_4)\right)}{f_2 f_3} \\ &= \frac{\left(\frac{2\sqrt{3}}{\pi} V_{g\text{-mag}} + j\frac{4}{\pi} V_{\text{batt}}\, e^{-j\Theta_d} \frac{\hat{\theta}_d}{\hat{m}_i}(f_1 f_3 - f_4)\right)}{f_2 f_3}\,.\end{aligned}\right\} \tag{5.46}$$

An alternative, more useful form of the result (5.46) is derived by splitting this equation into its linearized magnitude and phase components using a first-order Taylor series approximation. This method allows the complex phasor transfer function to be approximated by two transfer functions with real coefficients, representing the magnitude and phase deviations of the diode bridge input current. These transfer functions are calculated as follows:

$$\frac{\hat{i}_{d\text{-mag}}}{\hat{m}_i} = \frac{\Re\left[\frac{\hat{\vec{i}}_d}{\hat{m}_i}\right]\Re[\vec{I}_d] + \Im\left[\frac{\hat{\vec{i}}_d}{\hat{m}_i}\right]\Im[\vec{I}_d]}{\|\vec{I}_d\|}\,, \tag{5.47}$$

$$\frac{\hat{\theta}_d}{\hat{m}_i} = \frac{\Re\left[\frac{\hat{\vec{i}}_d}{\hat{m}_i}\right]\Im[\vec{I}_d] - \Im\left[\frac{\hat{\vec{i}}_d}{\hat{m}_i}\right]\Re[\vec{I}_d]}{\|\vec{I}_d\|^2}\,. \tag{5.48}$$

It is important to note that (5.46) and (5.48) are interdependent and must be solved as simultaneous equations.

Small-signal load current

The output current of the diode bridge is a dc quantity and, therefore, cannot be represented in phasor form. A time-domain analysis is conducted to determine the complete output current, which includes both the dc and HF components. The output current in the time domain can be calculated using the circuit model shown in Fig. 5.6 as

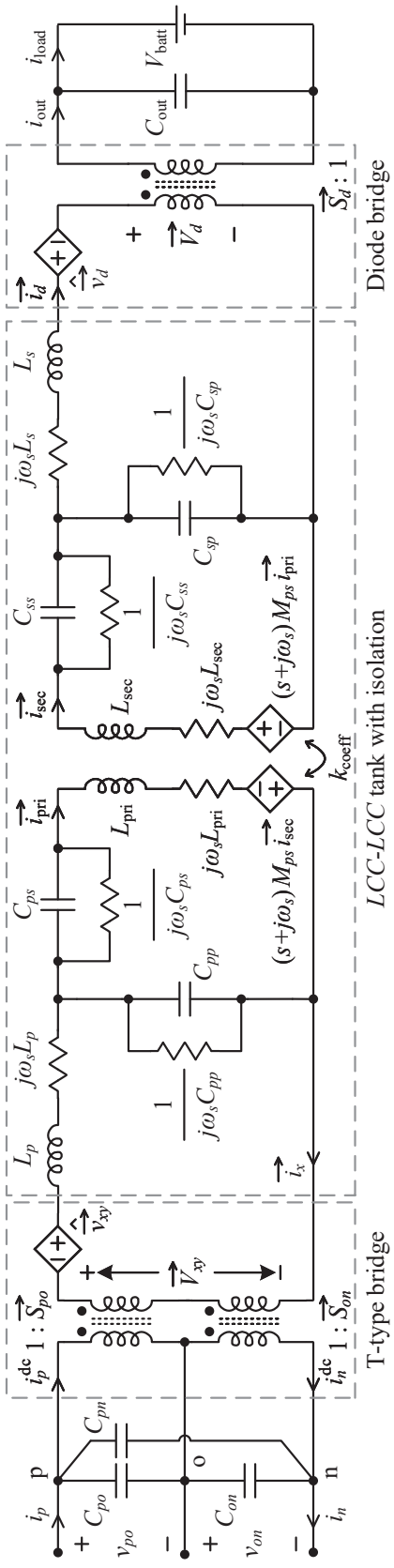


Fig. 5.7: Combined steady-state and small-signal phasor-transformed model of the T-type bridge-based dc-dc converter, featuring a double-sided LCC tank and a diode bridge connected to a battery load. Isolation is represented by a two-coupled inductor model, with k_{coeff} as the coupling coefficient.

$$\left.\begin{aligned} i_{\text{out}}(t) &= s_d(t) i_d(t) \\ &= \frac{4}{\pi}\cos(\omega_s\, t - \theta_d)\, i_{d\text{-mag}} \cos(\omega_s\, t - \theta_d) \\ &= \frac{2}{\pi}(I_{d\text{-mag}} + \hat{i}_{d\text{-mag}})(1 + \cos(2\omega_s\, t - 2\Theta_d - 2\hat{\theta}_d))\,. \end{aligned}\right\} \tag{5.49}$$

The battery load current, which is the averaged component of the output current of the diode bridge, can now be written as

$$i_{\text{load}} = \langle i_{\text{out}} \rangle = I_{\text{load}} + \hat{i}_{\text{load}} = \frac{2}{\pi} I_{d\text{-mag}} + \frac{2}{\pi}\hat{i}_{d\text{-mag}}\,. \tag{5.50}$$

Therefore, the small-signal deviations in i_{load} that directly depend on $\hat{i}_{d\text{-mag}}$ and $\hat{\theta}_d$ are

$$\frac{\hat{i}_{\text{load}}}{\hat{i}_{d\text{-mag}}} = \frac{2}{\pi}\,, \tag{5.51}$$

$$\frac{\hat{i}_{\text{load}}}{\hat{\theta}_d} = 0\,, \tag{5.52}$$

respectively.

Now, by combining (5.47), (5.48), (5.51), and (5.52), the plant transfer function can be calculated as

$$G_{\text{plant}} = \frac{\hat{i}_{\text{load}}}{\hat{m}_i} = \frac{\hat{i}_{\text{load}}}{\hat{i}_{d\text{-mag}}}\frac{\hat{i}_{d\text{-mag}}}{\hat{m}_i} + \frac{\hat{i}_{\text{load}}}{\hat{\theta}_d}\frac{\hat{\theta}_d}{\hat{m}_i}\,. \tag{5.53}$$

5.6.2 Double-Sided *LCC* Tank

The three steps outlined for the small-signal modeling of the single-sided *LCC* tank are similarly applied to the double-sided *LCC* tank.

Small-signal phasor-transformed circuit

Similar to the single-sided *LCC* tank, the linearized steady-state and small-signal model of the T-type bridge-based dc-dc converter with a double-sided *LCC* tank is derived by representing the tank inductors and capacitors in terms of dynamic and steady-state impedances. The T-type bridge output voltage is linearized as given in (5.31), and the

diode bridge input voltage is linearized as derived in (5.34). The complete steady-state and small-signal model is depicted in Fig. 5.7, with isolation modeled using the two-coupled inductor approach commonly employed in WPT systems.

Small-signal diode bridge input current

As explained earlier, since the load current i_{load} is a function of the diode bridge input current i_d, the small-signal deviations in the diode bridge input current phasor, $\hat{\vec{i}}_d$, are calculated in relation to perturbations introduced in the control input, $\hat{m}_i$, as provided below:

$$\left.\begin{aligned}\frac{\hat{\vec{i}}_d}{\hat{m}_i} &= \frac{\frac{\hat{\vec{v}}_{xy}}{\hat{m}_i} - \frac{\hat{\vec{v}}_d}{\hat{m}_i}\left(\left(\frac{f_{p1}f_{s1}}{f_{ps}} - \frac{f_{ps}}{Z_{sp}}\right)f_{p2} + \frac{Z_p f_{s1}}{f_{ps}}\right)}{\left(\frac{f_{p1}f_{s2}}{f_{ps}} - f_{ps}f_{s3}\right)f_{p2} + \frac{Z_p f_{s2}}{f_{ps}}} \\ &= \frac{\frac{2\sqrt{3}}{\pi}V_{g\text{-mag}} + j\frac{4}{\pi}V_{\text{batt}}\,e^{-j\Theta_d}\frac{\hat{\theta}_d}{\hat{m}_i}\left(\left(\frac{f_{p1}f_{s1}}{f_{ps}} - \frac{f_{ps}}{Z_{sp}}\right)f_{p2} + \frac{Z_p f_{s1}}{f_{ps}}\right)}{\left(\frac{f_{p1}f_{s2}}{f_{ps}} - f_{ps}f_{s3}\right)f_{p2} + \frac{Z_p f_{s2}}{f_{ps}}}.\end{aligned}\right\} \tag{5.54}$$

In the above equation,

$$f_{p1} = Z_{ps} + Z_{\text{pri}}\,, \tag{5.55}$$

$$f_{p2} = 1 + \frac{Z_p}{Z_{pp}}\,, \tag{5.56}$$

$$f_{s1} = \frac{Z_{sp} + Z_{\text{sec}} + Z_{ss}}{Z_{sp}}\,, \tag{5.57}$$

$$f_{s2} = Z_{\text{sec}} + Z_{ss} + Z_s\left(\frac{Z_{sp} + Z_{\text{sec}} + Z_{ss}}{Z_{sp}}\right)\,, \tag{5.58}$$

$$f_{s3} = 1 + \frac{Z_s}{Z_{sp}}\,, \tag{5.59}$$

$$f_{ps} = sM_{ps} + j\omega_s M_{ps}\,, \tag{5.60}$$

$$Z_p = sL_p + j\omega_s L_p + r_{L_p}\,, \tag{5.61}$$

$$Z_{pp} = \frac{r_{C_{pp}}}{1 + r_{C_{pp}}(sC_{pp} + j\omega_s C_{pp})}\,, \tag{5.62}$$

$$Z_{ps} = \frac{r_{C_{ps}}}{1 + r_{C_{ps}}(sC_{ps} + j\omega_s C_{ps})}\,, \tag{5.63}$$

$$Z_{\text{pri}} = sL_{\text{pri}} + j\omega_s L_{\text{pri}} + r_{L_{\text{pri}}}\,, \tag{5.64}$$

$$Z_{\text{sec}} = sL_{\text{sec}} + j\omega_s L_{\text{sec}} + r_{L_{\text{sec}}}\,, \tag{5.65}$$

$$Z_{ss} = \frac{r_{C_{ss}}}{1 + r_{C_{ss}}(sC_{ss} + j\omega_s C_{ss})}\,, \tag{5.66}$$

$$Z_{sp} = \frac{r_{C_{sp}}}{1 + r_{C_{sp}}(sC_{sp} + j\omega_s C_{sp})}\,, \tag{5.67}$$

$$Z_s = sL_s + j\omega_s L_s + r_{L_s}\,, \tag{5.68}$$

$$M_{ps} = k_{\text{coeff}}\sqrt{L_{\text{pri}} L_{\text{sec}}}\,, \tag{5.69}$$

where r_{L_p}, $r_{C_{pp}}$, $r_{C_{ps}}$, $r_{L_{\text{pri}}}$, $r_{L_{\text{sec}}}$, $r_{C_{ss}}$, $r_{C_{sp}}$, and r_{L_s} are the parasitic resistances of the tank inductors and capacitors. As described earlier for the single-sided LCC tank, (5.54) can be split into its linearized magnitude and phase components using a first-order Taylor series approximation, as provided in (5.47) and (5.48). This method allows the complex phasor transfer function to be approximated by two transfer functions with real coefficients, representing the magnitude $\left(\frac{\hat{i}_{d\text{-mag}}}{\hat{m}_i}\right)$ and phase $\left(\frac{\hat{\theta}_d}{\hat{m}_i}\right)$ deviations of the diode bridge input current relative to the perturbations in the control input, $\hat{m}_i$.

Small-signal load current

Similar to the single-sided LCC tank, by combining the magnitude and phase deviations of the small-signal diode bridge input current phasor, $\hat{\vec{i}}_d$, relative to the perturbations in the control input, $\hat{m}_i$ (as provided by (5.47) and (5.48)), with the small-signal deviations in the load current, $\hat{i}_{\text{load}}$, which directly depend on the magnitude deviation, $\hat{i}_{d\text{-mag}}$, and phase deviation, $\hat{\theta}_d$, in the diode bridge input current (as given by (5.51) and (5.52)), the plant transfer function can be calculated as

$$G_{\text{plant}} = \frac{\hat{i}_{\text{load}}}{\hat{m}_i} = \frac{\hat{i}_{\text{load}}}{\hat{i}_{d\text{-mag}}}\frac{\hat{i}_{d\text{-mag}}}{\hat{m}_i} + \frac{\hat{i}_{\text{load}}}{\hat{\theta}_d}\frac{\hat{\theta}_d}{\hat{m}_i}\,. \tag{5.70}$$

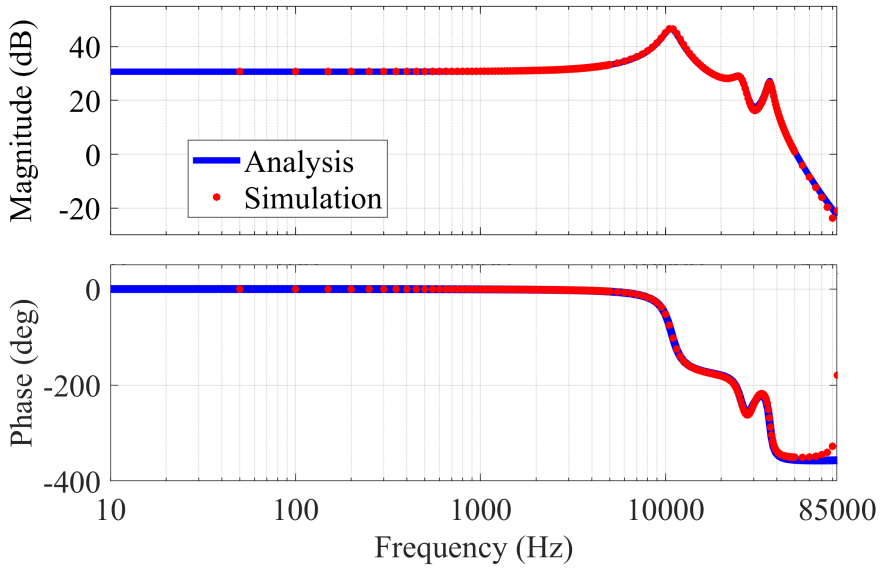


Fig. 5.8: Comparison of Bode plots of the plant $\left(G_{\text{plant}} = \dfrac{\hat{i}_{\text{load}}}{\hat{m}_i}\right)$ of the T-type bridge-based dc-dc converter with a double-sided LCC resonant tank, obtained from the phasor transformation-based small-signal modeling and PLECS simulation multitone analysis.

Table 5.1: Simulation parameters for the T-type bridge-based dc-dc conversion system with a double-sided LCC tank.

Parameter	**Value**	**Parameter**	**Value**
P_{out}	20 kW	C_{ps}, $r_{C_{ps}}$	9.9 nF, 10 kΩ
f_s	85 kHz	C_{ss}, $r_{C_{ss}}$	9.9 nF, 10 kΩ
$V_{g\text{-mag}}$	$480\sqrt{2}$ V	C_{sp}, $r_{C_{sp}}$	46.7 nF, 10 kΩ
v_{po}, v_{on}	379.4 V, 297.4 V	L_s, r_{L_s}	75.1 μH, 70 mΩ
V_{batt}	650 V	k_{coeff}	0.44
L_p, r_{L_p}	64.5 μH, 70 mΩ	L_{pri}, $r_{L_{\text{pri}}}$	419.2 μH, 150 mΩ
C_{pp}, $r_{C_{pp}}$	54.4 nF, 10 kΩ	L_{sec}, $r_{L_{\text{sec}}}$	427.9 μH, 150 mΩ

5.7 Simulation Results

A 20 kW T-type bridge-based dc-dc converter featuring a double-sided LCC resonant tank with isolation and a diode bridge connected to a battery load is simulated using PLECS multitone analysis. This analysis applies a multitone signal, composed of multiple

Table 5.2: Experimental parameters.

Parameter	**Value**
P_{out}, f_s	4 kW, 85 kHz
$V_{g\text{-mag}}$, V_{batt}	$208\sqrt{2}$ V, 316 V
v_{po}, v_{on}	208 V, 76 V
L_p, r_{L_p}	29.3 μH, 116.4 mΩ
C_{pp}, $r_{C_{pp}}$	119.9 nF, 14.9 kΩ
C_{ps}, $r_{C_{ps}}$	112.4 nF, 15.6 kΩ
L_l, r_{L_l}	37.1 μH, 31.5 mΩ
L_m	802.2 μH

sinusoidal signals, to encompass all investigated frequencies simultaneously. The simulation parameters are listed in Table 5.1. Parasitic resistances of inductors and capacitors are expressed in terms of series and parallel resistances, respectively. The Bode plots of the plant $G_{\text{plant}} = \dfrac{\hat{i}_{\text{load}}}{\hat{m}_i}$ obtained from small-signal modeling closely align with the simulation results in Fig. 5.8, thereby validating the accuracy of the modeling approach for the dc-dc converter with a double-sided LCC tank.

5.8 Experimental Validation

To validate the phasor transformation-based small-signal modeling in hardware, tests are conducted on the T-type bridge-based dc-dc conversion system illustrated in Fig. 5.9. This system comprises a single-sided LCC tank with isolation and a secondary-side diode-bridge rectifier connected to a battery load. Two dc-voltage sources, manufactured by REGATRON, are connected to the inputs of the T-type bridge, while a dc-voltage sink (NHR 9300) emulates a battery at the output. Experimental parameters are provided in Table 5.2. Parasitic resistances of inductors and capacitors are expressed in terms of series and parallel resistances, respectively. The modeling verification is carried out for the plant transfer function, $G_{\text{plant}} = \dfrac{\hat{i}_{\text{load}}}{\hat{m}_i}$, at an output power of 4 kW. In this verification, the

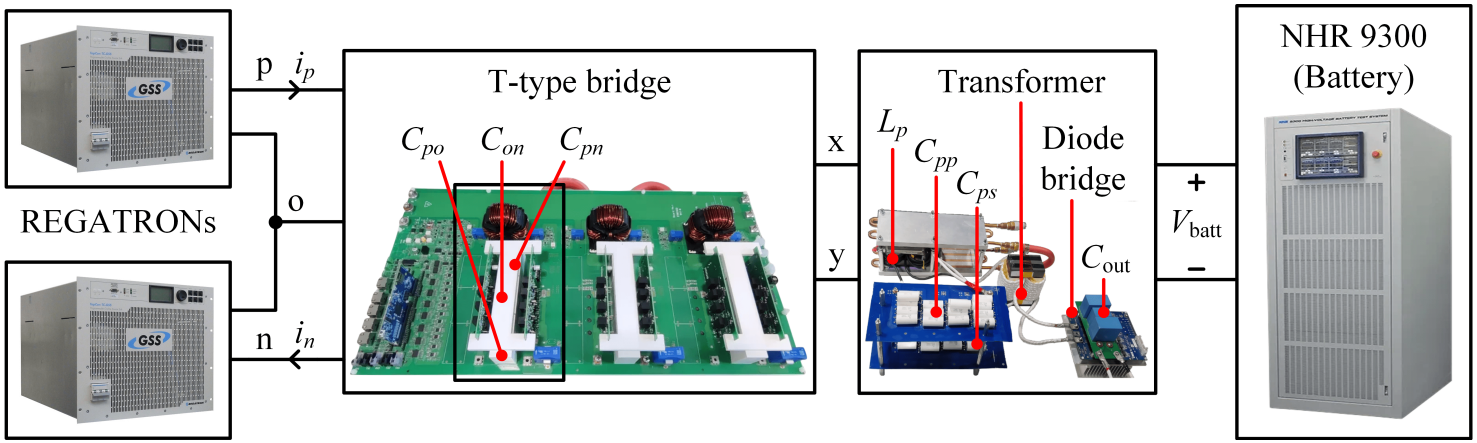


Fig. 5.9: A 4 kW hardware setup of a dc-dc conversion system featuring a T-type bridge, a single-sided *LCC* tank, and a diode bridge on the secondary side of the isolation. Two dc power supplies from REGATRON serve as dc input sources, while the NHR 9300 functions as a battery load. Small-signal perturbations are applied to the modulation index m_i using the TMS320F28379D microcontroller.

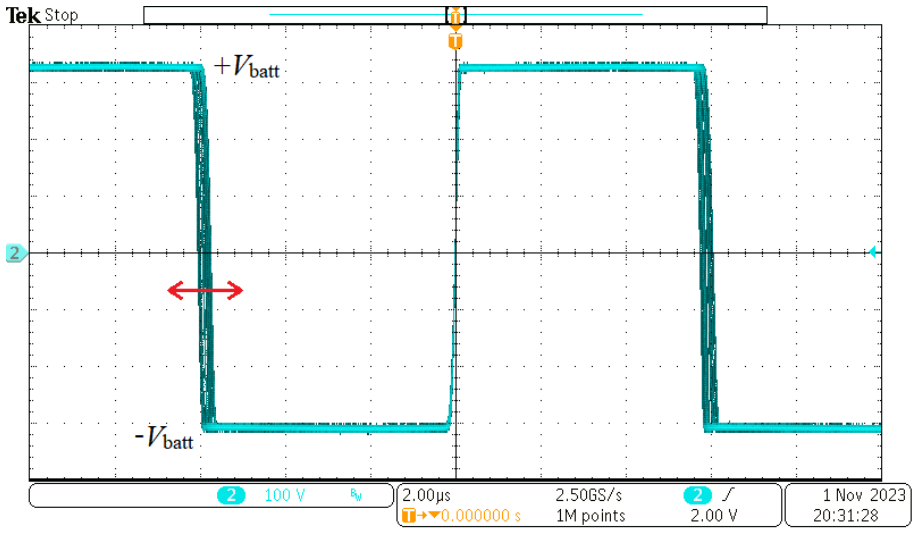


Fig. 5.10: Phase deviations ($\hat{\theta}_d$), as shown by the arrow, in the diode bridge input square-wave voltage due to perturbations introduced in the control input, $\hat{m}_i$, while the magnitude remains constant.

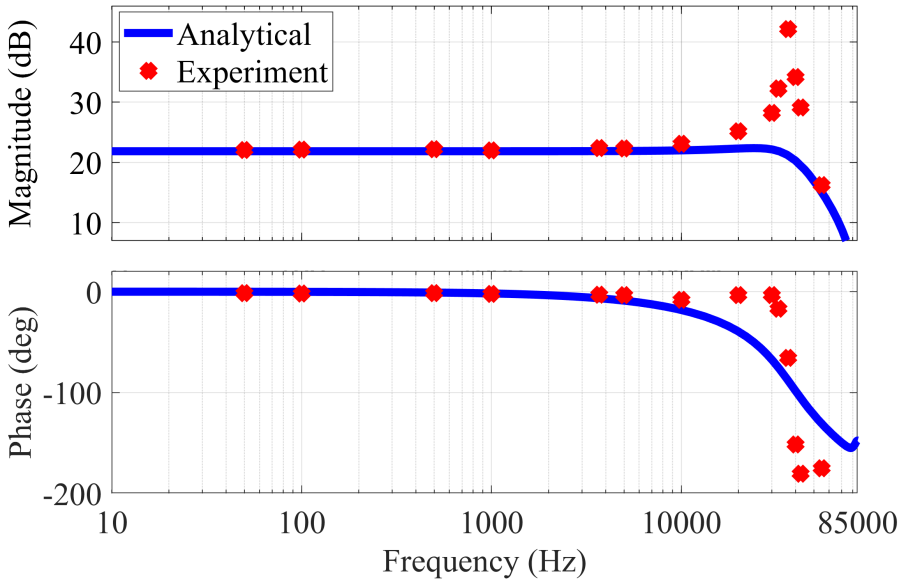


Fig. 5.11: Analytical Bode plots of G_{plant} compared with hardware results, where the diode bridge with a battery load is modeled as a resistor. The analysis results in excessive damping and fails to capture the high-frequency resonance.

modulation index, m_i, is sinusoidally perturbed by $\pm$ 0.05 around a steady-state value of 0.95. The perturbation is performed across a range of frequencies: 50 Hz, 100 Hz, 500 Hz, 1 kHz, 3.7 kHz, 5 kHz, 10 kHz, 20 kHz, 30 kHz, 32.5 kHz, 36.6 kHz, 40 kHz, 42.5 kHz, and

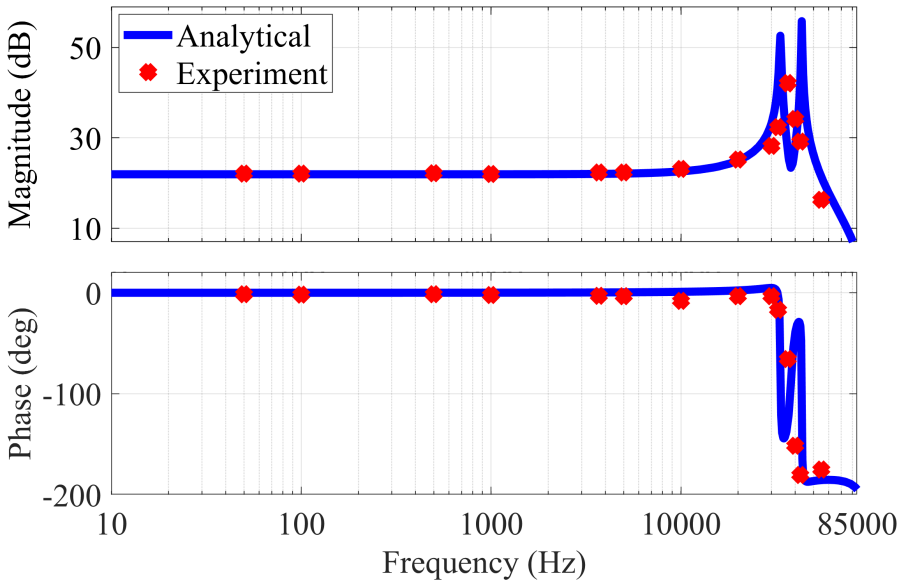


Fig. 5.12: Analytical Bode plots of G_{plant} compared with hardware results, where the diode bridge with a battery load is modeled as a constant independent voltage sink. The analysis results in excessive resonances.

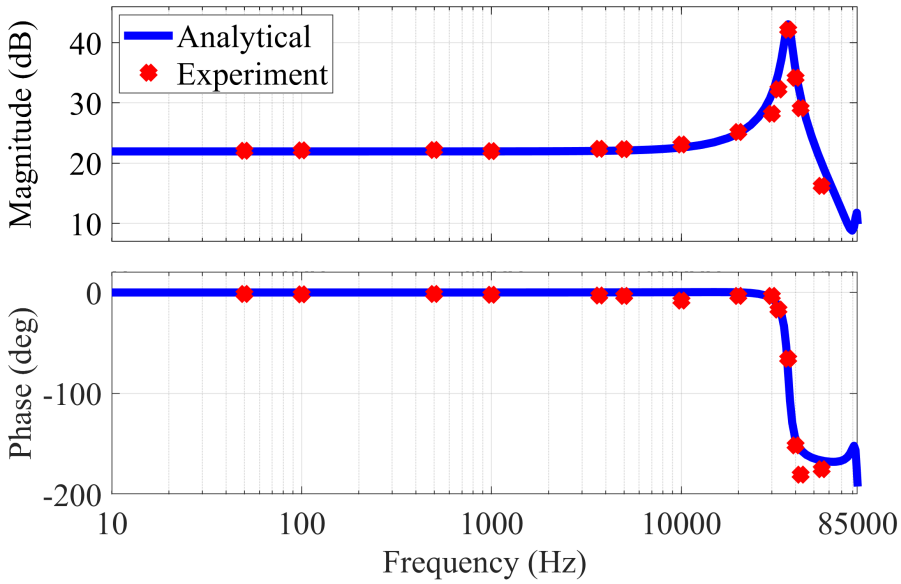


Fig. 5.13: Analytical Bode plots of G_{plant} compared with hardware results, where the diode bridge with a battery load is modeled as a dependent voltage sink with a constant magnitude and variable phase, as proposed in this chapter. The analysis accurately matches the hardware results.

55 kHz. The control input, m_i, is updated at twice the switching frequency (170 kHz) using an up-down carrier, implemented with the TMS320F28379D microcontroller. The resulting

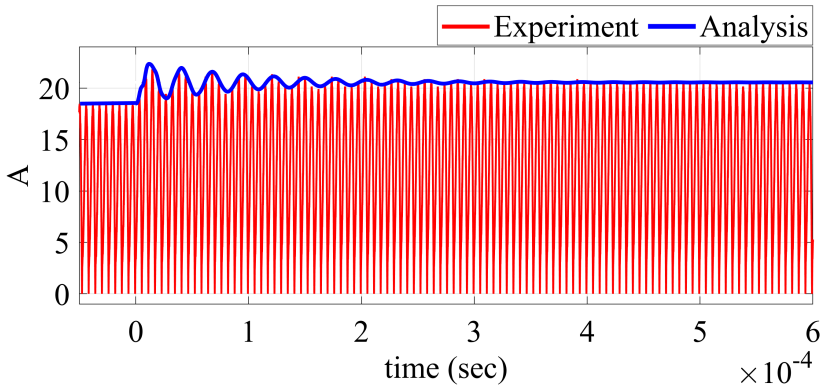


Fig. 5.14: Experimental waveform of the diode-bridge rectifier output current, i_{out}, for the T-type bridge-based dc-dc converter, superimposed on the envelope predicted by the small-signal model during a step change in the modulation index, m_i, from 0.9 to 1. The diode bridge with a battery load is modeled here as a dependent voltage sink with a constant magnitude and variable phase, as proposed in this chapter.

magnitude and phase of the perturbation-frequency component present in the load current, i_{load}, are measured to derive the Bode plots.

Fig. 5.10 illustrates the phase deviations in the diode bridge input square-wave voltage when m_i is perturbed, while its magnitude remains unchanged, as previously proven mathematically. Fig. 5.11, Fig. 5.12, and Fig. 5.13 provide a comparison of analytical Bode plots of G_{plant} with hardware results. In Fig. 5.11, modeling the diode bridge with a battery load as a resistor results in excessive damping of the higher-frequency resonance, leading to inaccurate analytical plots. In Fig. 5.12, treating the diode bridge with a battery load as an independent voltage sink with constant magnitude and phase while ignoring the phase deviations results in excessive resonances and inaccuracies. Modifications are made to Fig. 5.6 and (5.46) to model the diode bridge with a battery load as a resistor and as an independent voltage sink. Finally, Fig. 5.13 models the diode bridge with a battery load as a dependent voltage sink, incorporating small-signal phase deviations and constant magnitude, which produces accurate analytical Bode plots consistent with hardware results across all perturbation frequencies. Moreover, a step response of the diode bridge output current, i_{out}, has been measured during the hardware testing by introducing a step change in the modulation index from 0.9 to 1. The envelope observed during this step change in the hardware has been

compared with the step response obtained from the small-signal modeling with a dependent voltage sink, as presented in Fig. 5.14. The results demonstrate that the modeling precisely predicts the envelope of the diode bridge output current during this step change, thereby confirming the accuracy of the modeling. Accurate small-signal modeling that captures the high-frequency dynamics of the T-type bridge-based dc-dc resonant converter with a diode bridge connected to a battery load enhances the design and stability of closed-loop control, leading to more reliable and efficient power delivery.

The small-signal analysis presented in this chapter has also been applied to the T-type bridge-based dc-dc converter operated with leading-edge-aligned modulation, where the duty ratios are independently controlled, as detailed in Chapter 3. The corresponding results are presented below.

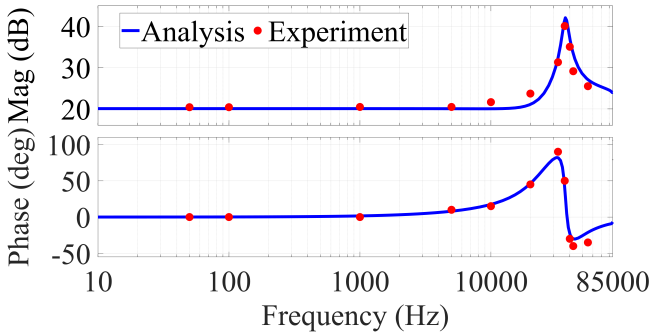


Fig. 5.15: Comparison of Bode plots of the transfer function $\frac{\hat{i}_p}{\hat{d}_p}$, obtained from the phasor transformation-based small-signal modeling and hardware testing.

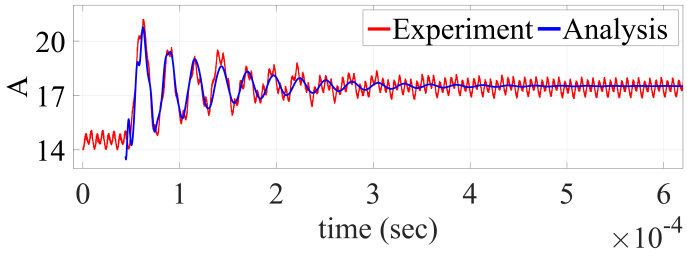


Fig. 5.16: Experimental waveform of the p-port current, i_p, superimposed upon the envelope predicted by the small-signal model under a step change in the duty d_p from 0.7068 to 0.9868.

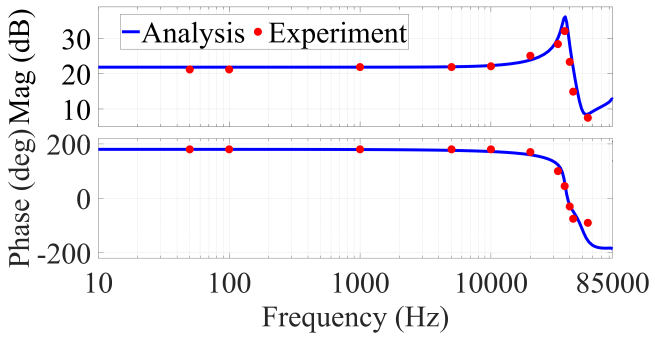


Fig. 5.17: Comparison of Bode plots of the transfer function $\frac{\hat{i}_n}{\hat{d}_p}$, obtained from the phasor transformation-based small-signal modeling and hardware testing.

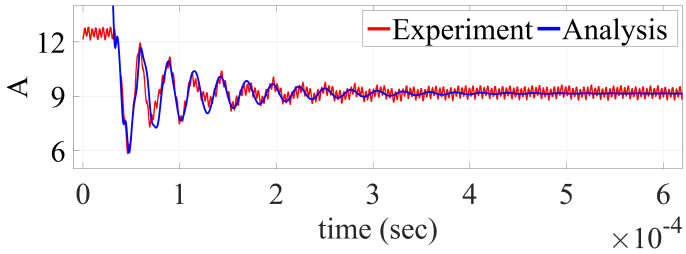


Fig. 5.18: Experimental waveform of the n-port current, i_n, superimposed upon the envelope predicted by the small-signal model under a step change in the duty d_p from 0.7068 to 0.9868.

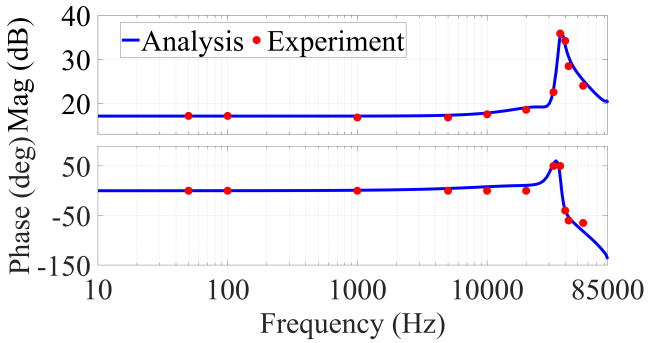


Fig. 5.19: Comparison of Bode plots of the transfer function $\frac{\hat{i}_{x\text{-mag}}}{\hat{d}_p}$, obtained from the phasor transformation-based small-signal modeling and hardware testing.

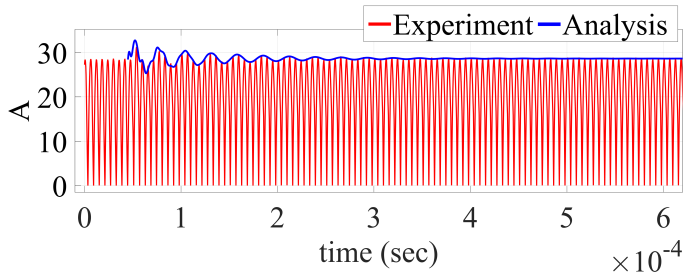


Fig. 5.20: Experimental waveform of the T-type bridge output current, i_x, superimposed upon the envelope predicted by the small-signal model under a step change in the duty d_p from 0.7068 to 0.9868.

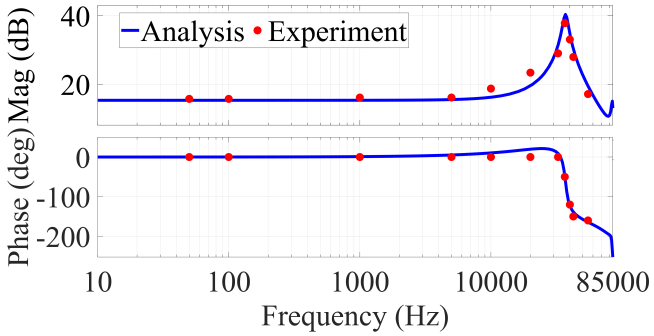


Fig. 5.21: Comparison of Bode plots of the transfer function $\frac{\hat{i}_{\text{out}}}{\hat{d}_p}$, obtained from the phasor transformation-based small-signal modeling and hardware testing.

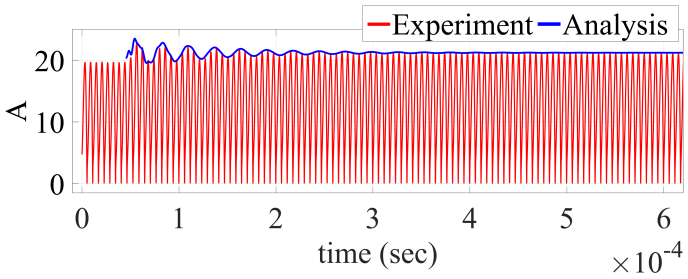


Fig. 5.22: Experimental waveform of the diode bridge output current, i_{out}, superimposed upon the envelope predicted by the small-signal model under a step change in the duty d_p from 0.7068 to 0.9868.

5.9 Conclusion

This chapter presents a comprehensive small-signal modeling that utilizes phasor transformation for a T-type bridge-based dc-dc converter. This system features both single-sided

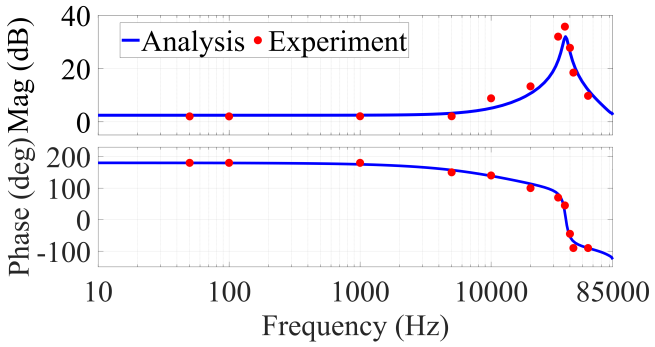


Fig. 5.23: Comparison of Bode plots of the transfer function $\frac{\hat{i}_p}{\hat{d}_n}$, obtained from the phasor transformation-based small-signal modeling and hardware testing.

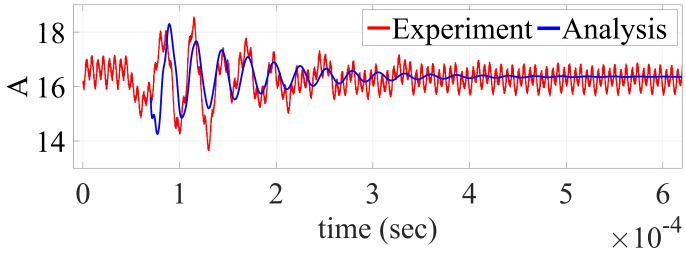


Fig. 5.24: Experimental waveform of the p-port current, i_p, superimposed upon the envelope predicted by the small-signal model under a step change in the duty d_n from 0.4825 to 0.7625.

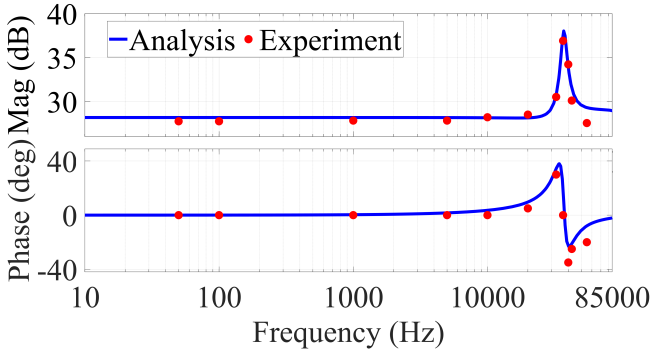


Fig. 5.25: Comparison of Bode plots of the transfer function $\frac{\hat{i}_n}{\hat{d}_n}$, obtained from the phasor transformation-based small-signal modeling and hardware testing.

and double-sided LCC resonant tanks, with a secondary side isolated diode bridge connected to a battery load, representing a typical configuration used in WPT applications. The mod-

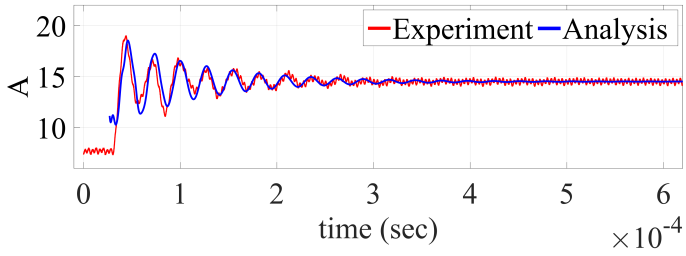


Fig. 5.26: Experimental waveform of the n-port current, i_n, superimposed upon the envelope predicted by the small-signal model under a step change in the duty d_n from 0.4825 to 0.7625.

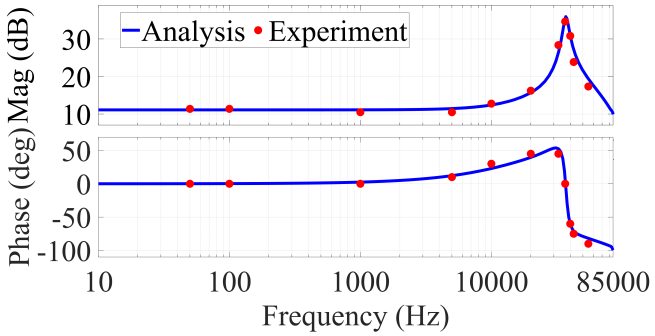


Fig. 5.27: Comparison of Bode plots of the transfer function $\frac{\hat{i}_{x\text{-mag}}}{\hat{d}_n}$, obtained from the phasor transformation-based small-signal modeling and hardware testing.

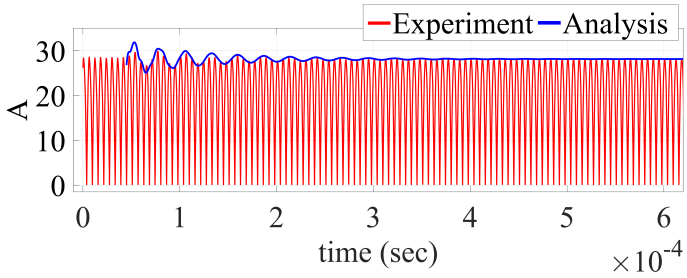


Fig. 5.28: Experimental waveform of the T-type bridge output current, i_x, superimposed upon the envelope predicted by the small-signal model under a step change in the duty d_n from 0.4825 to 0.7625.

eling procedure is divided into distinct steps, each of which is clarified to facilitate a clear and intuitive understanding of the methodology employed. The precise model presented here enhances the design and stability of closed-loop control, resulting in more reliable and

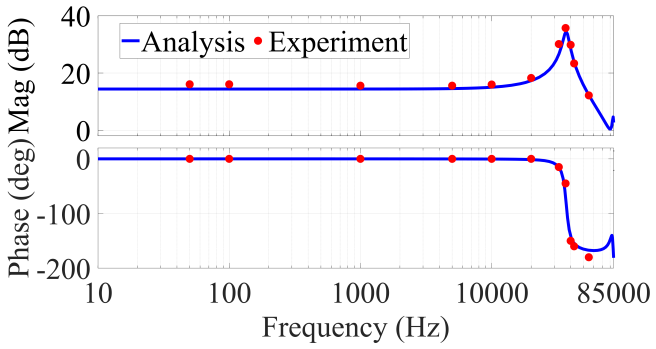


Fig. 5.29: Comparison of Bode plots of the transfer function $\frac{\hat{i}_{\text{out}}}{\hat{d}_n}$, obtained from the phasor transformation-based small-signal modeling and hardware testing.

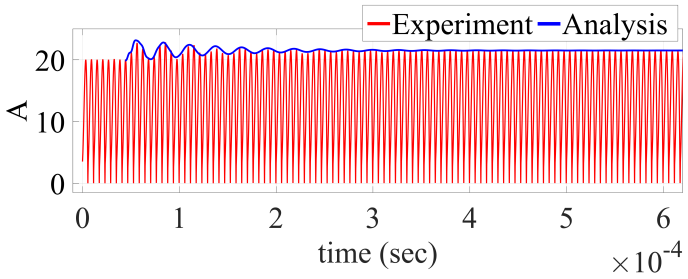


Fig. 5.30: Experimental waveform of the diode bridge output current, i_{out}, superimposed upon the envelope predicted by the small-signal model under a step change in the duty d_n from 0.4825 to 0.7625.

efficient power delivery. The proposed analytical model is validated through simulations of a 20 kW T-type bridge-based dc-dc converter with a double-sided LCC resonant tank. Furthermore, the small-signal modeling is also verified through hardware testing of a 4 kW, 85 kHz prototype consisting of a single-sided LCC tank, confirming its accuracy for perturbation frequencies up to 55 kHz. The small-signal modeling has been experimentally verified in hardware for both the center-aligned and leading-edge-aligned modulation strategies of the T-type bridge discussed in Chapter 2 and Chapter 3.

CHAPTER 6

DESIGN AND OPERATION OF UNFOLDING-BASED MULTIPORT SYSTEM WITH A TAB-BASED RESONANT CONVERTER

6.1 Introduction

The transportation sector remains one of the largest energy consumers worldwide, with internal combustion engine vehicles still dominating the landscape. For example, in 2023, the United States alone consumed approximately 137 billion gallons of gasoline and 46 billion gallons of diesel, resulting in a total energy usage of around 6.36 trillion kWh [34]. In comparison, the nation's total electricity generation was approximately 4.25 trillion kWh [35], illustrating the immense energy demand associated with fossil-fuel-based transportation. These figures highlight the significant challenge of transitioning to fully electric mobility systems, particularly when electricity infrastructure is not yet scaled to meet such demands. As countries worldwide pursue electrification of transport, it becomes essential to not only expand EV charging infrastructure but also strengthen the power grid. Integrating battery energy storage and renewable generation is emerging as a viable strategy to support this shift at scale [36].

In typical practice, the integration of battery storage or renewable energy sources with the grid for EV battery charging is achieved either through ac-coupling at the grid, as depicted in Fig. 6.1(a), or dc-coupling at the output of the grid-tied ac-dc converter, as shown in Fig. 6.1(b) [36, 96]. An example of an ac-coupled system is the supercharger station in Mountain View, California [96]. Both configurations are well-studied and offer good reliability and simplicity; however, they suffer from poor conversion efficiency due to multiple cascaded converters. Compared to the ac-coupled system, the dc-coupled configuration involves fewer conversion stages, which improves efficiency. Nonetheless, the number of conversion stages can be further reduced by eliminating multiple dc-ac converters after the

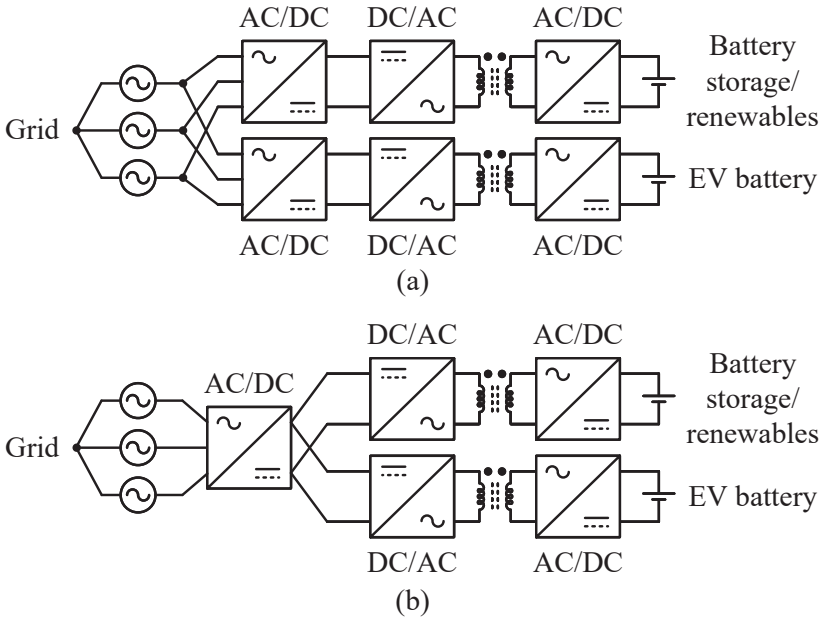


Fig. 6.1: Conventional multiport system architectures for integrating battery storage/renewables with the grid for EV charging: (a) ac-coupled architecture, where integration occurs at the grid side; and (b) dc-coupled architecture, where integration occurs at the output of the grid-tied converter.

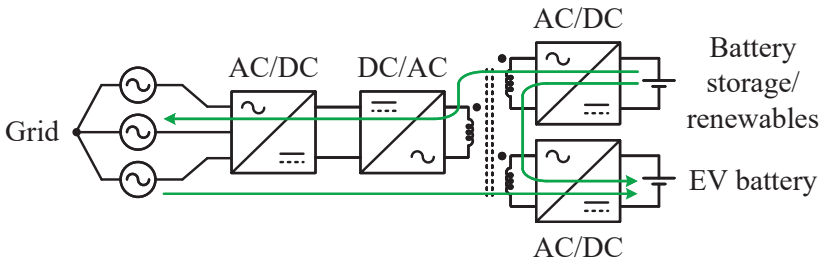


Fig. 6.2: Proposed multiport system to integrate battery storage/renewables with the grid for EV charging. The grid-tied ac-dc converter consists of an Unfolder and a current injection circuit. A TAB-based three-port dc-dc converter with a three-winding transformer is utilized to integrate the different ports. Different power flow directions explored in this study are indicated by green arrows.

grid-tied converter. This study proposes an architecture with a single dc-ac converter and a multi-winding HF transformer-based conversion system to integrate battery storage or renewable energy sources with the grid for EV battery charging. The resulting HF ac-coupled system, illustrated in Fig. 6.2, reduces the number of power conversion stages compared to conventional ac-coupled and dc-coupled architectures, thereby improving overall system

cost and efficiency. Such HF ac-coupled systems have been studied in prior literature, primarily to demonstrate dc-dc converter operation with multiple dc ports [46, 47, 97–104]. Various aspects of these systems have been explored, including steady-state power flow analysis [46, 47], decoupled power flow techniques [47, 99, 100, 104], multi-winding transformer design [100, 104], soft-switching analysis [46, 101, 102], and conduction loss minimization [103]. However, these studies are limited to dc-dc converter operation and do not address the implementation of a complete ac-dc architecture with grid integration, which is critical for the practical deployment of battery storage or renewable energy sources integrated with the grid to support EV charging infrastructure. In [105], a grid-tied multiport system is designed using an interleaved totem pole, a current-fed DAB, and an interleaved buck stage. In [106], a grid-tied multiport system is designed using 1-ϕ AFE converter and TAB. In [107], a 1-ϕ grid-tied multiport system is designed using a three-port integrated topology comprising an ac-dc full-bridge converter followed by individual dc-dc converters for the dc ports. In [108], a 1-ϕ grid-tied multiport system is designed using a current source converter with partial power processing control. However, these multiport systems rely on a 1-ϕ grid connection, which limits the maximum transferable power, leads to higher grid current stresses, and restricts scalability. As a result, such systems are not suitable for high-power EV charging infrastructure, where a 3-ϕ grid interface is typically required.

[37–43] propose multiport systems with 3-ϕ grid connection. In [37], a split-source inverter is employed for grid connection, and all dc ports are interfaced with a common dc link, either directly or through buck/boost converters. In [38], a matrix converter is employed for grid connection, while the dc ports are interfaced through interleaved parallel boost converters. In [39], an AFE is used for grid connection, while buck/boost converters interface the dc ports. In [40], an AFE is employed for grid connection, while an interleaved boost converter and a flyback converter are used for the dc ports. In [41], a matrix converter is used for ac-dc conversion. [42] employs current-source inverter bridges with HF transformer isolation. [43] utilizes an AFE for grid connection, while the dc-dc stages employ full-bridge and buck converters. However, these 3-ϕ grid-tied multiport systems have one or more of the

following limitations: (i) an AFE is utilized as the grid-side converter, which is operated at HF and undergoes hard switching [37,39,40,43]. The use of an AFE increases the required dc-link capacitance and grid-side filtering effort, as well as switching losses and EMI concerns. (ii) a matrix converter operated at HF requires extensive grid-side filtering and leads to complications in the control strategy [38,41]. (iii) dc-dc converters are hard-switched at HF, resulting in higher switching losses and EMI issues [37,39,40,43]. (iv) the EV dc port is non-isolated, which may raise safety concerns [37,39]. (v) the converter is designed for lower battery voltages and is unsuitable for present EV battery voltage levels [37–39,42,43]. (vi) converter operation over a wide EV battery voltage range (e.g., 200–800 V) is not demonstrated [37–39,41–43]. These limitations restrict the practical deployment of such multiport systems for high-power EV charging applications. The proposed 3-ϕ grid-tied multiport system in this work overcomes all the above limitations. A low-frequency operated (120 Hz in this work) grid-side converter is employed, which reduces the required dc-link capacitance. It also eliminates the need for external grid-side inductive filters since the grid inductance is sufficient for current shaping. Moreover, low-frequency operation leads to negligible grid-side converter switching losses. The dc-dc converter is carefully designed to achieve soft switching across a wide EV battery voltage range (200–800 V). The combination of low-frequency grid-side converter operation and soft switching of the dc-dc converter minimizes EMI concerns and improves system efficiency. The proposed converter also outperforms prior work in terms of efficiency and grid current THD. In addition, isolation is provided for the EV dc port, and the converter is designed to operate over a wide voltage range of 200–800 V, ensuring safe operation and practical suitability for EV charging infrastructure. A detailed comparison of the proposed multiport converter with prior converters is presented in the experimental validation section.

This chapter presents a complete ac-dc multiport system with 3-ϕ grid connection and introduces a grid interface through a low-frequency operated Unfolder, which operates at a maximum of twice the grid frequency [12,22,24–26,28,109,110]. The unfolding-based grid interface significantly reduces switching losses and improves overall system efficiency due

to its low-frequency operation. Moreover, the use of the Unfolder minimizes the required dc-link capacitance and eliminates the need for external grid-side inductive filters, facilitating a more compact and efficient design well-suited for high-power EV battery charging infrastructure. To interface with the Unfolder, which outputs two pulsating dc-link voltages, a dual-input dc-ac converter such as a T-type bridge or a pair of H-bridges is typically used to process power from both dc links [22, 26]. Additionally, integrating battery storage/renewables along with the EV battery requires two more ports, resulting in a four-port dc-dc converter. This increases design complexity and introduces challenges for closed-loop control. To simplify the circuit architecture, this study proposes a multiport system that incorporates a current injection circuit [45,111] and a TAB-based three-port dc-dc converter to effectively interface the grid port, the battery storage/renewables port, and the EV port. Since the Unfolder is operated at low frequency in open loop, it cannot handle control-related tasks such as sinusoidal shaping of the grid currents. This control task is instead carried out by the coordinated closed-loop control of the current injection circuit and the TAB-based dc-dc converter. The details of this coordinated closed-loop control, which must also handle multidirectional power flow in the proposed multiport system, together with the accurate small-signal modeling, are presented in this chapter.

In addition to the utilization of the Unfolder, the design of the TAB tank circuit plays a critical role in enabling efficient power transfer over wide operating conditions. While the commonly used series resonant tank can facilitate power transfer to the EV port due to its inherent ability to achieve ZVS and support HF operation with high conversion efficiency, it suffers from significant efficiency degradation when operated over a wide voltage gain range [112]. Alternatively, an LLC resonant tank, controlled through frequency modulation, can offer a wide voltage gain range while maintaining efficiency [113]; however, the use of frequency modulation in a TAB introduces complexity in power flow analysis and closed-loop control design. In this study, an LCL immittance network-based resonant tank [114–117] is employed for power transfer to the EV port. This configuration enables wide voltage gain at a fixed switching frequency and supports efficient operation with EV batteries at different

voltage levels, thereby improving adaptability. Unlike the simplified architectures in prior TAB converters [46, 47, 99–104] that employed inductive or series resonant tanks with stiff dc links, the utilization of a higher-order LCL tank integrated into an unfolding-based grid-tied multiport system introduces challenges in power flow analysis, closed-loop control, and system integration. These challenges are explicitly addressed in this chapter through detailed power flow analysis, design, and small-signal modeling. An optimized tank design is presented that minimizes conduction losses and ensures ZVS of the TAB MOSFETs across a wide EV battery voltage range, thereby enhancing efficiency. The design also accounts for the dc-link voltage variation due to the unfolding operation. In addition, accurate small-signal modeling of the TAB with an LCL tank is derived to achieve high closed-loop bandwidths to regulate power at the dc ports under pulsating dc-link voltage variation and to ensure stable operation during transients. Finally, a three-winding transformer design is proposed for the TAB that incorporates the required tank inductance into the transformer leakage inductance, and the transformer winding is optimized to minimize the kVAr/kW ratio of the LCL tank for a wide EV battery voltage range of 200–800 V, further improving system efficiency.

The proposed multiport system has been validated using a 5 kW, 480 V grid-tied hardware prototype. It achieves a peak ac-dc efficiency of 98.3% and maintains efficiency above 97% across various operating points, power flow directions, and a battery voltage range of 200–800 V. The prototype also demonstrates a low grid current THD of 2%. In addition, a modular architecture is proposed to achieve power scalability of the multiport topology, employing IPOP dc-dc converter modules that interface with a single grid-tied Unfolder. Scalability is demonstrated through simulations at 50 kW and further validated in hardware at the 10 kW level, achieving a peak efficiency of 98.1%.

6.2 Brief Overview of the Proposed Multiport System

The overall proposed ac-dc multiport system is illustrated in Fig. 6.3. As discussed earlier, to simplify the connection between the dc-dc converter and the Unfolder, which outputs two pulsating dc-link voltages, a current injection circuit is introduced after the

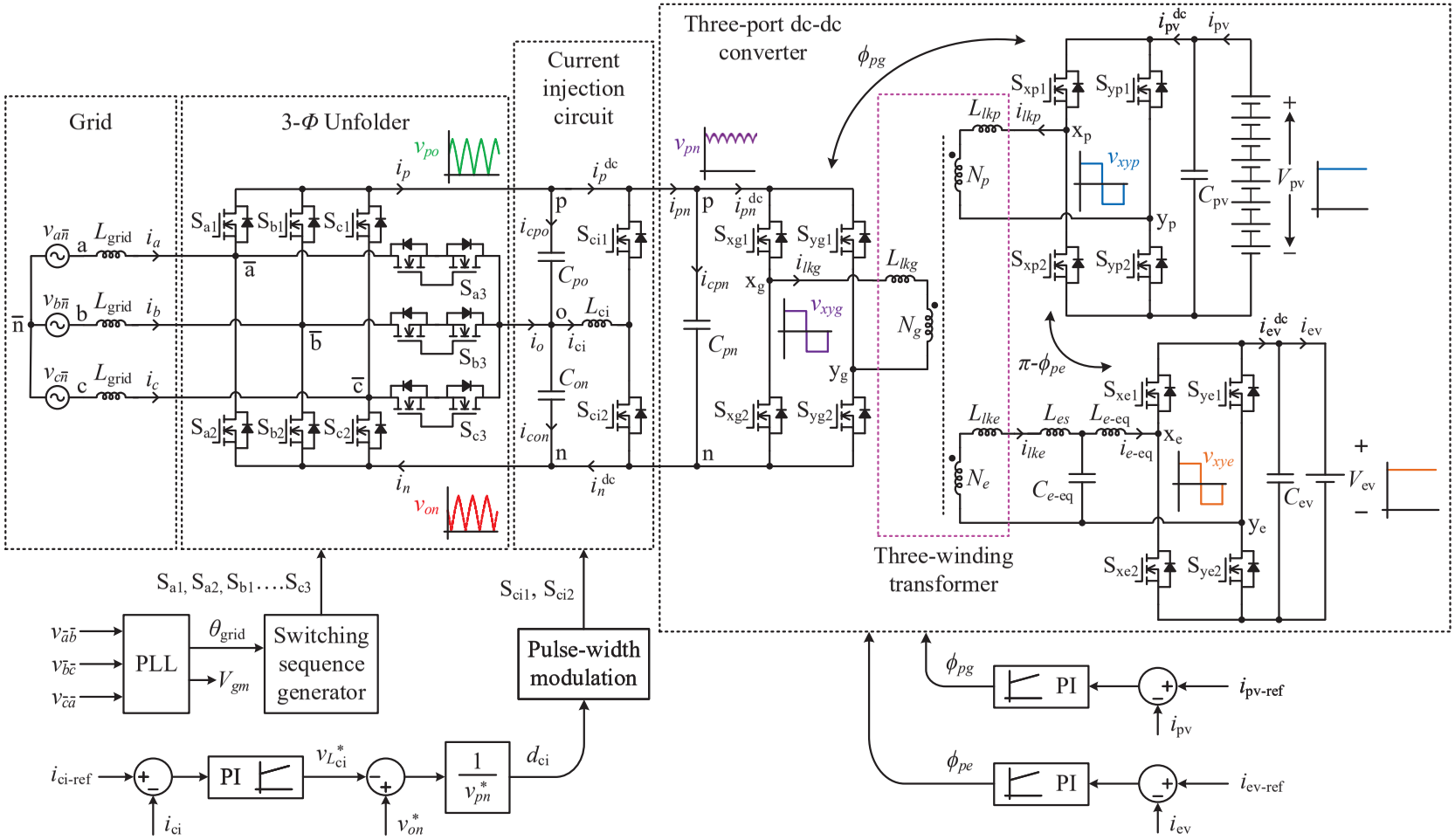


Fig. 6.3: Circuit schematic and control structure of the proposed multiport system, consisting of a grid-tied Unfolder, a current injection circuit, and a TAB-based three-port dc-dc converter. The system integrates battery storage/renewables with the grid for EV battery charging applications. These ports are coupled at the HF ac node using an HF three-winding transformer, which also integrates the tank components.

Unfolder to reduce the number of required dc ports on the grid side. This approach enables the use of an H-bridge connected to a single dc-link voltage. As a result, a TAB-based three-port dc-dc converter can be used to effectively interface the grid port, the battery storage/renewables port, and the EV port. For brevity, the battery storage/renewables port is referred to as the PV port in this chapter. As the dc voltage gain between the PV and grid ports remains close to unity, a DAB-based power architecture is implemented for dc-dc conversion between the PV and grid ports, with the required tank inductance between these ports integrated into the leakage inductance of the designed three-winding transformer. This integrated magnetics-based architecture enhances both the power density and efficiency of the system. To accommodate a wide voltage range for interfacing EV batteries with different voltage levels, an LCL immittance network-based resonant tank is employed for power transfer to the EV port, which effectively facilitates ZVS of MOSFETs and maintains consistently low conduction losses, thereby preserving high efficiency across the entire voltage range.

Fig. 6.3 also outlines the closed-loop control architecture of the proposed multiport system. The control loop for the current injection circuit regulates the third-harmonic injection current to ensure sinusoidal grid current shaping for PFC. The other two control loops are implemented within the dc-dc converter to regulate the current drawn from the PV port and the current delivered to the EV battery. Together, these control loops effectively manage power flow across all ports of the ac-dc multiport system.

6.3 Operation and Design of the Unfolder and Current Injection Circuit

6.3.1 Operation of the Unfolder and Current Injection Circuit

Unfolder

As depicted in Fig. 6.3, the grid-tied Unfolder utilized in the proposed multiport system consists of a 3-ϕ bidirectional rectifier and common-source switches ($\mathrm{S_{x3}},\ \mathrm{x} \in \{\mathrm{a}, \mathrm{b}, \mathrm{c}\}$) for carrying the third-harmonic current. The Unfolder connects to the grid through ac-side

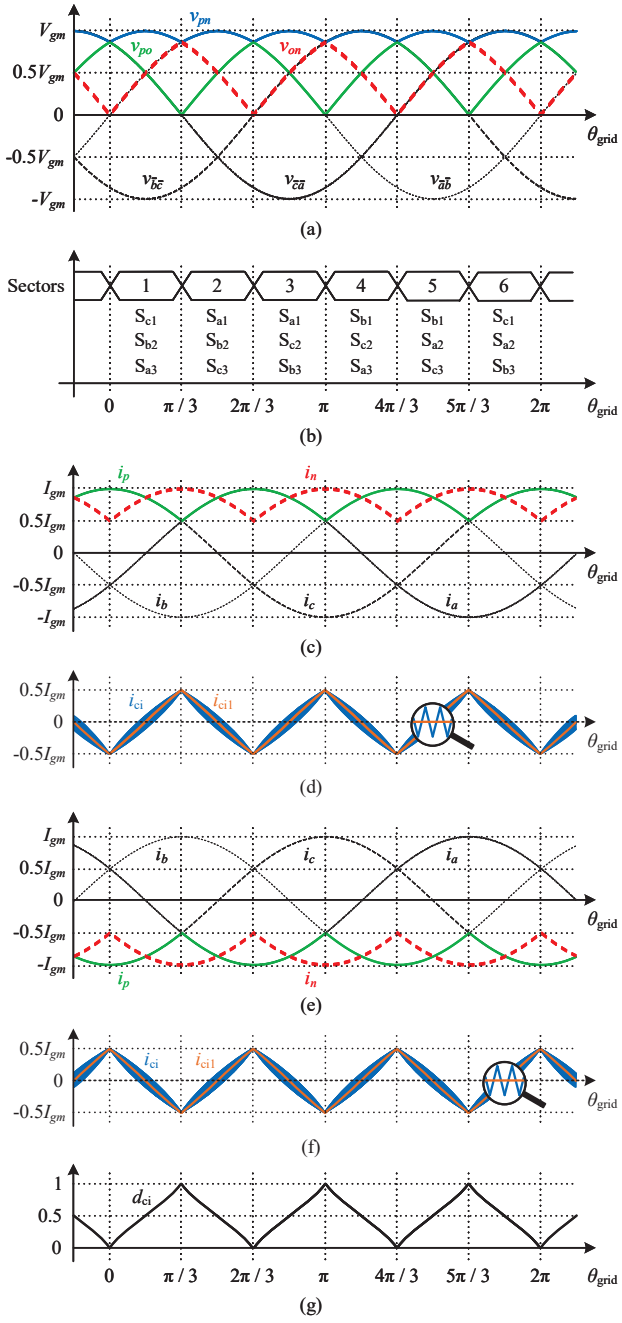


Fig. 6.4: (a) 3-ϕ ac input voltages are converted to pulsating dc-link voltages, v_{po}, v_{on}, and v_{pn}, by the Unfolder; (b) switching sequence of the Unfolder switches is determined based on the ac-voltage sectors; (c) sinusoidal 3-ϕ grid currents when the grid supplies rated power; (d) current through the filter inductor, L_{ci}, and its fundamental component, i_{ci1}, when the grid supplies power; (e) sinusoidal 3-ϕ grid currents when the grid receives rated power; (f) current through the inductor, L_{ci}, and its fundamental component, i_{ci1}, when the grid receives power; and (g) duty cycle used to modulate the current injection half-bridge leg.

grid inductances, L_{grid}, provided by the grid. In the Unfolder circuit, the input ac phases are connected to the positive, negative, or midpoint of the dc-link, based on the switching sequence shown in Fig. 6.4(b). Specifically, the phases with the highest and lowest instantaneous voltages are connected to the positive (p) and negative (n) terminals of the dc-link, respectively, while the remaining phase is linked to the midpoint (o). As a result, the common-source switches, S_{a3}, S_{b3}, and S_{c3}, operate at twice the grid frequency, whereas the 3-ϕ bidirectional rectifier switches, S_{a1}, S_{a2}, S_{b1}, S_{b2}, S_{c1}, and S_{c2}, operate at the grid frequency. This switching sequence results in time-varying Unfolder dc output voltages, v_{po} and v_{on}, as depicted in Fig. 6.4(a). As shown in this figure, the voltages v_{po} and v_{on} vary from 0 to $\frac{\sqrt{3}}{2}V_{gm}$, where V_{gm} denotes the peak value of the Unfolder's line-to-line ac input voltages. Furthermore, the addition of v_{po} and v_{on} results in the net dc-link voltage, v_{pn}, which is applied across the current injection circuit and the grid-side H-bridge of the TAB-based three-port dc-dc converter. The dc-link voltage, v_{pn}, exhibits a six-pulse waveform, as illustrated in Fig. 6.4(a), and varies within the range of $\frac{\sqrt{3}}{2}V_{gm}$ to V_{gm}. The pulsating nature of all the dc output voltages of the Unfolder eliminates the need for large dc-link capacitors. Instead, smaller capacitors, C_{po}, C_{on}, and C_{pn}, are specifically used to filter the HF switching current ripple generated by the HF-switched current injection circuit and dc-dc converter. Moreover, the low-frequency operation of the Unfolder eliminates the need for external grid-side inductive filters, as the grid inductance is sufficient to achieve PFC. The Unfolder is operated in open loop and cannot handle control tasks such as maintaining sinusoidal grid currents for PFC. This control task is instead carried out by the coordinated closed-loop control of the current injection circuit and the TAB-based dc-dc converter, as explained in the following.

Current Injection Circuit

The current injection circuit consists of a half-bridge leg, comprising S_{ci1} and S_{ci2}, which is switched at HF of $f_{\text{sw-ci}}$ and is modulated by the duty cycle, d_{ci}, as illustrated in Fig. 6.4(g). A filter inductor, L_{ci}, is employed, which, in conjunction with the capacitors C_{po}, C_{on}, and the grid inductances, L_{grid}, forms an LCL filter to ensure that the grid

currents do not contain significant switching frequency components. The current injection circuit regulates the current, i_{ci}, which includes both a switching frequency component and a fundamental component, i_{ci1}, at three times the grid frequency, using the closed-loop control shown in Fig. 6.3. The current reference, $i_{\text{ci-ref}}$, for this control is calculated as

$$i_{\text{ci-ref}} = \frac{\sqrt{3} I_{gm}}{V_{gm}} \left(-\max(v_{\bar{a}\bar{n}}, v_{\bar{b}\bar{n}}, v_{\bar{c}\bar{n}}) - \min(v_{\bar{a}\bar{n}}, v_{\bar{b}\bar{n}}, v_{\bar{c}\bar{n}}) \right) , \tag{6.1}$$

where I_{gm} denotes the peak grid current utilized in deriving the current reference and is determined as

$$I_{gm} = \frac{2}{\sqrt{3}} \frac{(-V_{\text{pv}} i_{\text{pv}} + V_{\text{ev}} i_{\text{ev}})}{V_{gm}} , \tag{6.2}$$

where V_{pv} and i_{pv} denote the voltage and current on the dc side of the H-bridge in the TAB-based dc-dc converter, which interfaces with the PV, while V_{ev} and i_{ev} represent the EV battery voltage and current supplied to the EV battery, respectively. The value of I_{gm} is positive when the grid supplies power and negative when the grid receives power. The closed-loop control ensures that the fundamental component, i_{ci1}, remains equal to the current reference, $i_{\text{ci-ref}}$, which results in sinusoidal grid currents, as shown in Figs. 6.4(c) and 6.4(d) when the grid supplies power, and in Figs. 6.4(e) and 6.4(f) when the grid receives power.

To examine how regulating the current, i_{ci}, ensures sinusoidal grid currents, the operation in Sector 3 $\left(\frac{2\pi}{3} \leq \theta_{\text{grid}} < \pi\right)$ is analyzed when the grid supplies power. Here, θ_{grid} denotes the angle of the line-to-line Unfolder input voltage $v_{\bar{a}\bar{b}}$, as determined by the PLL [118]. As shown in Figs. 6.4(c) and 6.4(d), the current i_b in Sector 3 is equal to the current i_{ci1}, which is maintained using the closed-loop as

$$i_b = i_{\text{ci1}} = I_{gm} \sin\left(\theta_{\text{grid}} - {}^{5\pi}/_{6}\right) . \tag{6.3}$$

Now, consider the Unfolder input phase voltages to be

$$v_{\bar{a}\bar{n}} = \left(V_{gm}/\sqrt{3}\right) \sin\left(\theta_{\text{grid}} - \pi/6\right) , \tag{6.4}$$

$$v_{\bar{b}\bar{n}} = \left(V_{gm}/\sqrt{3}\right) \sin\left(\theta_{\text{grid}} - 5\pi/6\right) , \tag{6.5}$$

$$v_{\bar{c}\bar{n}} = \left(V_{gm}/\sqrt{3}\right) \sin\left(\theta_{\text{grid}} - 3\pi/2\right) , \tag{6.6}$$

and the power supplied by the grid is maintained at $\frac{\sqrt{3}}{2} V_{gm} I_{gm}$ by the subsequent TAB-based dc-dc converter, which controls the system power by managing the power at the dc ports through the closed-loop control of the currents i_{pv} and i_{ev}. In the proposed three-port system, regulating the PV and EV port currents is sufficient to manage overall power flow, since the grid power is automatically determined by power balance. Consequently,

$$v_{\bar{a}\bar{n}} i_a + v_{\bar{b}\bar{n}} i_b + v_{\bar{c}\bar{n}} i_c = \frac{\sqrt{3}}{2} V_{gm} I_{gm} . \tag{6.7}$$

Moreover, since the Unfolder is a 3-ϕ, 3-wire system, the current i_c can be expressed as

$$i_c = -i_a - i_b . \tag{6.8}$$

Combining (6.3)-(6.8) gives

$$i_a = I_{gm} \sin\left(\theta_{\text{grid}} - \pi/6\right) , \text{ and} \tag{6.9}$$

$$i_c = I_{gm} \sin\left(\theta_{\text{grid}} - 3\pi/2\right) . \tag{6.10}$$

Therefore, by regulating the injection current i_{ci} and ensuring the correct grid power level through the closed-loop control of the TAB-based dc-dc converter, sinusoidal grid currents are maintained. Such coordinated closed-loop control of the current injection circuit and the TAB-based dc-dc converter ensures PFC.

6.3.2 Design of the Unfolder and Current Injection Circuit

Unfolder

As previously discussed, the Unfolder operates at a maximum of twice the grid frequency, leading to negligible switching losses. The power dissipation in the Unfolder is due to conduction losses, which are determined by the rms currents through the MOSFETs, given as

$$I_{\text{unf-rms-S}_{1/2}} = I_{gm}\sqrt{\frac{1}{6}+\frac{\sqrt{3}}{8\pi}}\,,\; I_{\text{unf-rms-S}_3} = I_{gm}\sqrt{\frac{1}{6}-\frac{\sqrt{3}}{4\pi}}\,, \tag{6.11}$$

where $I_{\text{unf-rms-S}_{1/2}}$ denotes the rms current of the top and bottom MOSFETs, and $I_{\text{unf-rms-S}_3}$ represents the rms current of the common-source MOSFETs in the Unfolder. Additionally, the MOSFET blocking voltages are given by

$$V_{\text{unf-block-S}_{1/2}} = V_{gm}\,,\; V_{\text{unf-block-S}_3} = \frac{\sqrt{3}}{4}V_{gm}\,, \tag{6.12}$$

for the top and bottom MOSFETs, and for the common-source MOSFETs, respectively. The conduction losses, derived using the rms currents, along with the blocking voltage calculations, provide essential parameters for selecting appropriate MOSFETs and designing the Unfolder effectively.

Current Injection Circuit

For the current injection circuit, the filter inductor L_{ci} and the half-bridge leg must be designed. The inductor value is determined based on the allowable switching frequency ripple in i_{ci}, which consists of both a switching frequency component and a fundamental component, i_{ci1}, at three times the grid frequency. The switching frequency ripple exhibits a triangular waveform, with its peak-to-peak value given by

$$\Delta i_{\text{ci}} = \frac{1}{L_{\text{ci}} f_{\text{sw-ci}} \left(\frac{1}{v_{po}}+\frac{1}{v_{on}}\right)}\,. \tag{6.13}$$

Since the dc voltages, v_{po} and v_{on}, are time-varying, the peak-to-peak ripple changes over the grid cycle. The maximum peak-to-peak ripple is given by

$$\Delta I_{\text{ci-max}} = \frac{V_{gm}}{4L_{\text{ci}}f_{\text{sw-ci}}}\,, \tag{6.14}$$

which occurs at $\theta_{\text{grid}} = \left(\frac{k\pi}{3} - \frac{\pi}{6}\right)$, where $k \in \{1,2,3,4,5,6\}$ represents the Unfolder sector, as seen in Figs. 6.4(d) and 6.4(f). The rms value of this maximum ripple is given by

$$\Delta I_{\text{ci-max-rms}} = \frac{V_{gm}}{8\sqrt{3}L_{\text{ci}}f_{\text{sw-ci}}}\,. \tag{6.15}$$

Moreover, the rms of the fundamental component, i_{ci1}, is

$$I_{\text{ci1-rms}} = I_{gm}\sqrt{\frac{1}{2} - \frac{3\sqrt{3}}{4\pi}}\,. \tag{6.16}$$

The inductor, L_{ci}, can now be selected such that the ratio $\Delta I_{\text{ci-max-rms}}/I_{\text{ci1-rms}}$ remains below 25%, ensuring minimal switching frequency components in the grid currents, as determined by

$$L_{\text{ci}} \geq \frac{V_{gm}}{f_{\text{sw-ci}}I_{gm}\sqrt{6 - \frac{9\sqrt{3}}{\pi}}}\,. \tag{6.17}$$

The half-bridge leg in the current injection circuit operates at a switching frequency of $f_{\text{sw-ci}}$, resulting in both conduction and switching losses. The conduction losses are determined by the rms currents through the MOSFETs, given by

$$I_{\text{ci-rms-S}_{\text{ci1/2}}} = I_{gm}\sqrt{\frac{1}{4} - \frac{3\sqrt{3}}{8\pi}}\,. \tag{6.18}$$

Additionally, the MOSFETs need to block the peak value of the dc-link voltage, v_{pn}, which is equal to V_{gm}. When calculating the switching losses of the half-bridge leg, it is essential to account for the fact that half of the MOSFET switching transitions exhibit soft-switching.

This is due to the triangular waveshape of the current, i_{ci}, which alternates in polarity, facilitating soft-switching for half of the transitions. The hard-switching losses for the remaining transitions can be determined using the turn-on and turn-off energy losses specified in the MOSFET datasheet. These energy values must be appropriately scaled based on the voltage and current levels at which switching occurs, as well as the selected gate resistance in the circuit. Additionally, losses associated with the output capacitance (C_{oss}) of the MOSFET must be considered. The switching loss analysis for a half-bridge configuration is provided in [119]. The conduction losses, determined from the rms current, along with the blocking voltage and switching loss calculations, serve as critical parameters for optimal MOSFET selection and effective half-bridge leg design in the current injection circuit.

6.4 Design of the TAB-Based Three-Port DC-DC Converter

6.4.1 Analysis of the Power Flow

As previously discussed, the proposed TAB-based three-port dc-dc converter incorporates a DAB-based power architecture for dc-dc conversion between the PV and grid ports, while an LCL resonant tank is utilized for power transfer to the EV port, enabling a wide voltage range for the EV battery load. The power transfer between the PV and grid ports can be evaluated using the exact power flow expression for a DAB converter. On the other hand, for the power transfer paths from the PV port to the EV port and from the grid port to the EV port, the FHA is applicable due to the higher-order nature of the LCL tank, which results in near-sinusoidal tank currents on the EV side. Under the FHA, the LCL tank can be modeled by an inductor, $L_{lke} + L_{es}$, in series with the fundamental sinusoidal component of v_{xye}, denoted as v_{xye1}, as depicted in Fig. 6.5(a), when analyzing steady-state power flow. Additionally, the three-port wye-connected system can be equivalently represented by a delta-connected configuration for the purpose of power flow analysis, as illustrated in Fig. 6.5(b). Furthermore, all quantities involved in the power flow analysis

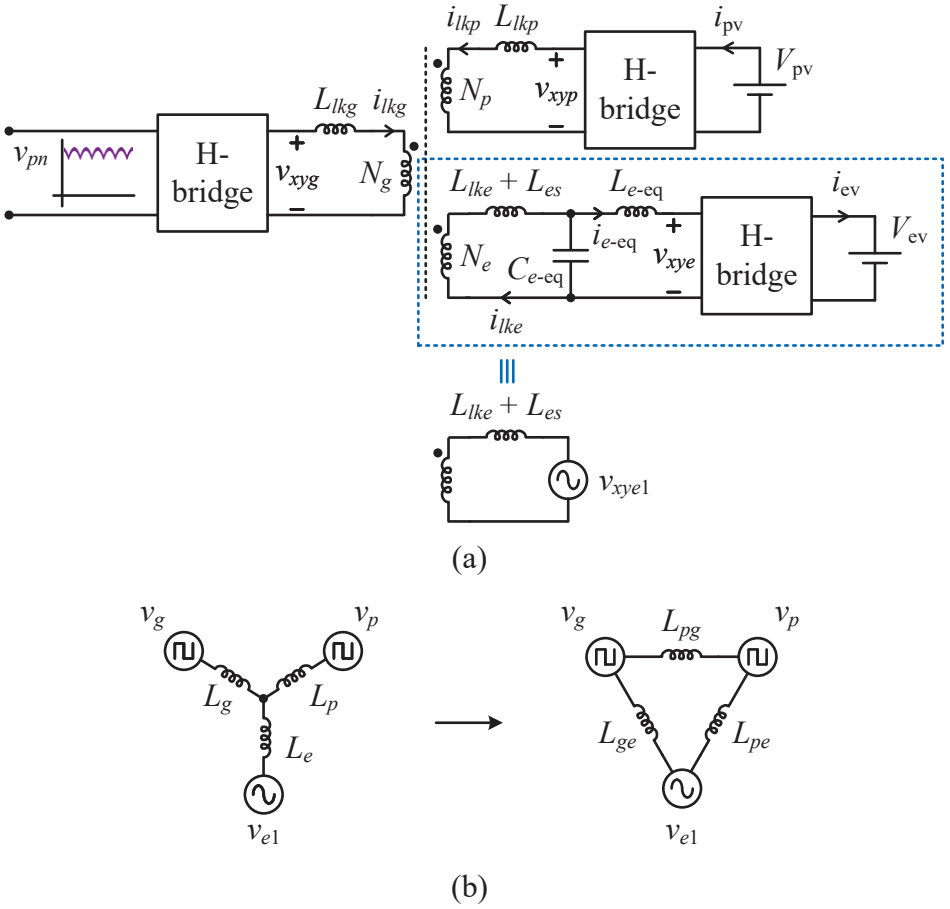


Fig. 6.5: (a) Using the FHA, the EV HF side with the LCL tank is modeled as an inductor, $L_{lke} + L_{es}$, in series with the fundamental sinusoidal component of v_{xye}, denoted as v_{xye1}, for steady-state power flow analysis; and (b) power flow analysis is performed by applying a wye-delta transformation to the tank and associated ports.

are referred to the PV side to maintain analytical consistency and are defined as

$$v_p = v_{xyp}\,, \tag{6.19}$$

$$v_g = v_{xyg}\left(\frac{N_p}{N_g}\right), \tag{6.20}$$

$$v_e = v_{xye}\left(\frac{N_p}{N_e}\right), \tag{6.21}$$

$$L_p = L_{lkp}\,, \tag{6.22}$$

$$L_g = L_{lkg}\left(\frac{N_p}{N_g}\right)^2, \tag{6.23}$$

$$L_e = (L_{lke} + L_{es})\left(\frac{N_p}{N_e}\right)^2, \tag{6.24}$$

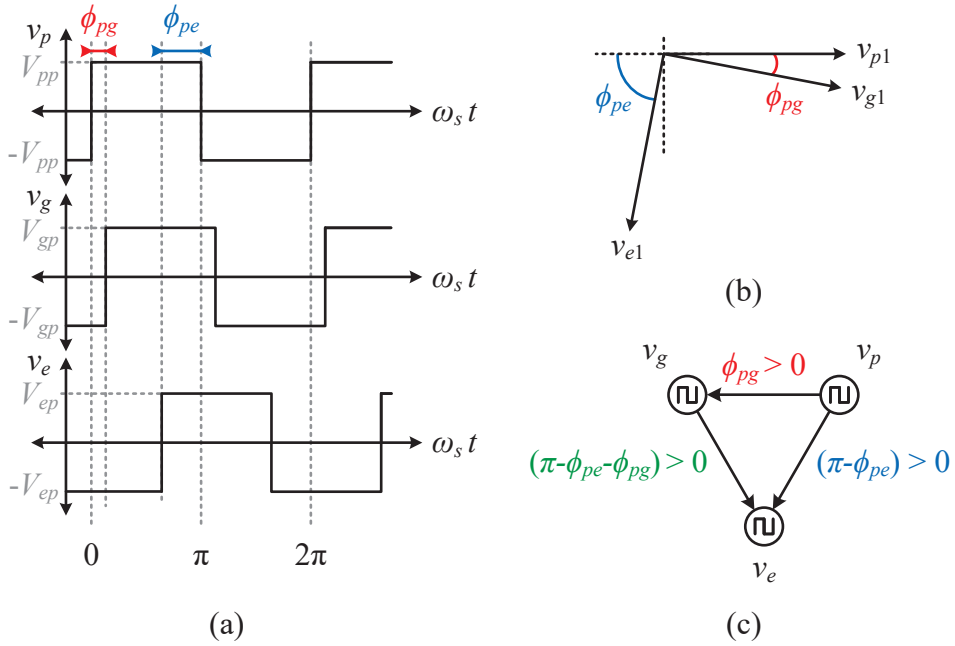


Fig. 6.6: The figure corresponds to the case where the HF ac voltage of the PV port leads that of the grid port, and both lead the EV port. In this operating condition, the PV port delivers positive power, while the EV port receives positive power. The net power supplied by the grid port may be either positive or negative, depending on the relative phase shifts. (a) Square-wave voltage waveforms at the HF sides of the respective ports, referenced to the PV side; (b) phasor diagram of the fundamental components of these voltages; and (c) corresponding power flow diagram among the three ports.

$$L_{pg} = L_p + L_g + \frac{L_p L_g}{L_e}\,, \tag{6.25}$$

$$L_{pe} = L_p + L_e + \frac{L_p L_e}{L_g}\,, \tag{6.26}$$

$$L_{ge} = L_g + L_e + \frac{L_g L_e}{L_p}\,. \tag{6.27}$$

Utilizing the delta-equivalent configuration depicted in Fig. 6.5(b), the power flow equations are derived as

$$P_{pg} = \frac{V_{pp} V_{gp}}{\omega_s L_{pg}}\,\phi_{pg}\left(1 - \frac{\phi_{pg}}{\pi}\right), \tag{6.28}$$

$$P_{pe} = \frac{8}{\pi^2}\frac{V_{pp} V_{ep}}{\omega_s L_{pe}}\sin(\phi_{pe})\,, \tag{6.29}$$

$$P_{ge} = \frac{8}{\pi^2}\frac{V_{gp} V_{ep}}{\omega_s L_{ge}}\sin(\phi_{pg} + \phi_{pe})\,, \tag{6.30}$$

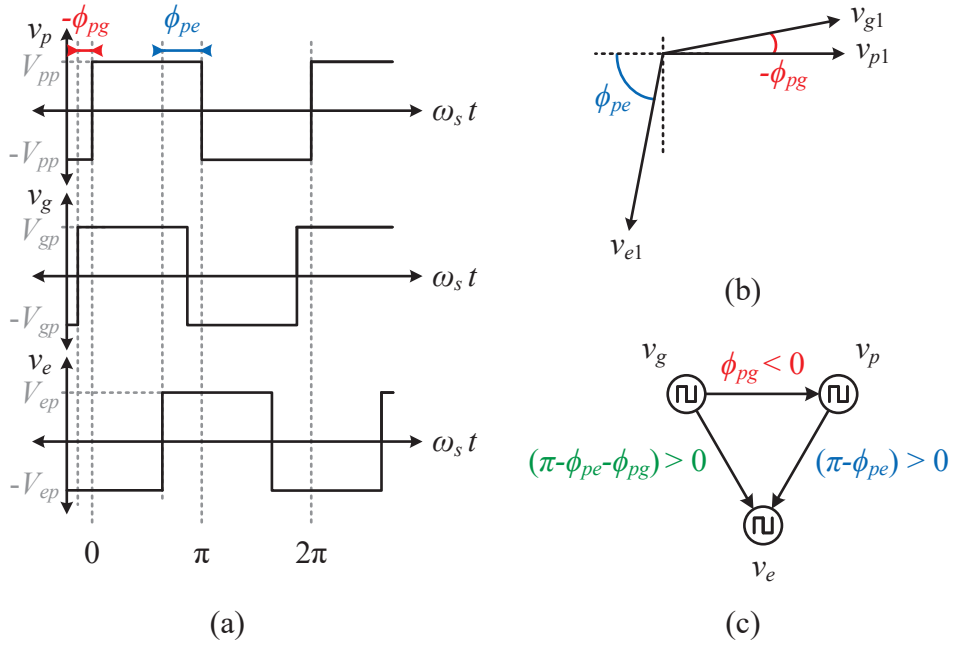


Fig. 6.7: The figure corresponds to the case where the HF ac voltage of the grid port leads that of the PV port, and both lead the EV port. Under this operating condition, the power demand at the EV port exceeds the available power from the PV port; therefore, the grid port supplies additional positive power, while the EV port continues to receive positive power. (a) Square-wave voltage waveforms at the HF sides of the respective ports, referenced to the PV side; (b) phasor diagram of the fundamental components of these voltages; and (c) corresponding power flow diagram among the three ports.

$$P_p = P_{pg} + P_{pe}\,, \tag{6.31}$$

$$P_g = -P_{pg} + P_{ge}\,, \tag{6.32}$$

$$P_e = -P_{pe} - P_{ge}\,, \tag{6.33}$$

where ω_s denotes the angular switching frequency of the dc-dc converter, P_{pg} represents the power transfer from the PV port to the grid port, P_{pe} corresponds to the power transfer from the PV port to the EV port, and P_{ge} denotes the power transfer from the grid port to the EV port. The parameters V_{pp}, V_{gp}, and V_{ep} denote the peak amplitudes of the HF ac square-wave voltages referred to the PV side, as illustrated in Figs. 6.6(a) and 6.7(a). The phase shifts between the square-wave voltages on the PV-to-grid and PV-to-EV sides are given by ϕ_{pg} and $(\pi - \phi_{pe})$, respectively, as shown in Figs. 6.6 and 6.7. L_{pg}, L_{pe}, and L_{ge}

are the tank inductances represented in the delta configuration, as depicted in Fig. 6.5(b). Finally, P_p, P_g, and P_e denote the net power flowing into or out of the PV, grid, and EV ports, respectively.

In this study, it is considered that the PV port supplies power within the range of 0 to P_{rated}, while the EV port receives power within the same range. If the PV port generates more power than required by the EV battery, the excess is received by the grid port. Conversely, if the PV port cannot supply sufficient power to the EV battery, the deficit is supplied by the grid port. Accordingly, all possible cases of square-wave voltage waveforms, phasor diagrams, and the corresponding power flow diagrams are illustrated in Figs. 6.6 and 6.7. From these figures, it can be observed that the EV-side square-wave voltage is kept at a phase lag of $(\pi - \phi_{pe})$ with respect to the PV-side voltage, which maintains a phase lag greater than $\frac{\pi}{2}$. This ensures the correct polarity and magnitude of the current flowing into the EV-side H-bridge, $i_{e\text{-eq}}$, in the LCL tank, thereby enabling ZVS of the H-bridge over a wide range of EV battery voltages. This phenomenon is explained below.

LCL Resonant Tank under Wide Load-Voltage Variation

In an LCL resonant tank, the inductances of L_1 and L_2, as shown in Fig. 6.8(a), are kept equal, and the capacitor C_1 is selected to resonate with these inductors at the switching frequency of operation [114–117], resulting in

$$C_1 = \frac{1}{\omega_s^2 L_1} = \frac{1}{\omega_s^2 L_2}\,. \tag{6.34}$$

By representing the circuit in Fig. 6.8(a) in Norton form, with the capacitor C_1 resonating with the inductor L_1 at the switching frequency, a current source at the switching frequency is generated that flows through the inductor L_2 and into the connected H-bridge (representing the EV-side H-bridge in this study). This current source, illustrated in Fig. 6.8(b), is calculated as

$$i_{L_2} = \frac{v_1}{j\omega_s L_1} = \frac{v_1}{\omega_s L_1} \angle \left(-\frac{\pi}{2}\right)\,. \tag{6.35}$$

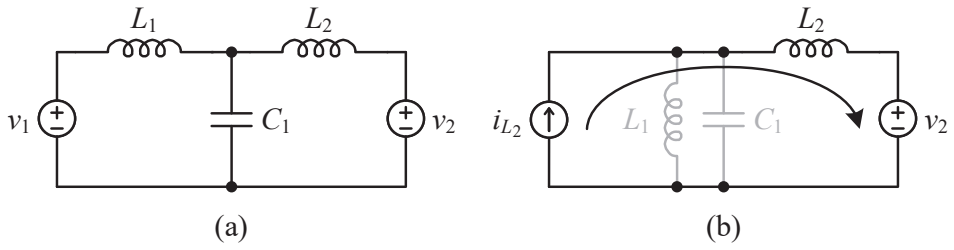


Fig. 6.8: (a) Circuit of an LCL tank, and (b) equivalent Norton form, where the capacitor C_1 resonates with the inductor L_1 at the switching frequency, generating a current source that flows through the inductor L_2.

Since the current flowing into the H-bridge has a phase lag of $\frac{\pi}{2}$, the H-bridge can be switched such that its input voltage, v_2, maintains a phase lag greater than $\frac{\pi}{2}$. This ensures that the polarity and magnitude of the current entering the load-side H-bridge are suitable to achieve ZVS of the MOSFETs [115, 117]. From (6.35), it is observed that the current i_{L_2} is independent of v_2, and hence the load-side dc voltage does not affect i_{L_2}. In other words, variations in the EV battery load voltage do not influence the current responsible for enabling ZVS in the H-bridge. Consequently, ZVS of the EV-side H-bridge can always be ensured over a wide range of battery voltages, provided the EV-side square-wave voltage is maintained with a phase lag greater than $\frac{\pi}{2}$ by appropriately switching the H-bridge MOSFETs. Furthermore, to achieve the above-mentioned current source, which is independent of the battery load voltage, the dc-dc converter must operate at a constant switching frequency equal to the resonant frequency of the capacitor C_1 and the inductor L_1.

6.4.2 Analytical Tank Currents Over the Switching Period

Analytical tank currents are essential for selecting tank components, as they enable the calculation of conduction losses and the optimization of the tank design. To calculate the analytical tank currents, a case is considered where the HF ac square-wave voltage of the PV port leads that of the grid port, and both lead the EV port, as shown in Fig. 6.6. The analysis can also be extended to the alternate case shown in Fig. 6.7. The analytical tank currents are derived piecewise by solving differential equations across three distinct time intervals: (i) $0 \leqslant t < t_{pg}$, (ii) $t_{pg} \leqslant t < (T_s/2)$, and (iii) $t_{pe} \leqslant t < (T_s/2) + t_{pe}$, as

Table 6.1: Analytical tank currents referenced to the PV side.

	Expression for $0 \leqslant t < t_{pg}$
$i_p(t)$	$-I_{p1} + \frac{V_{pp}\,(1+K_{lpe})\,t + V_{gp}t}{L_p\,(2+K_{lpe})} + \frac{V^p_{e\text{-eq-}p}\,(\cos(\omega_s t - \theta_{ce\text{-eq}}) - \cos(\theta_{ce\text{-eq}}))}{\omega_s L_e\,(2+K_{lpe})}$
$i_g(t)$	$-I_{g1} - \frac{(V_{pp}+V_{gp})\,t}{L_g} + \frac{V_{pp}\,(1+K_{lge})\,t + V_{gp}t}{L_g\,(2+K_{lge})} + \frac{V^p_{e\text{-eq-}p}\,(\cos(\omega_s t - \theta_{ce\text{-eq}}) - \cos(\theta_{ce\text{-eq}}))}{\omega_s L_e\,(2+K_{lge})}$
$i_e(t)$	$i_p(t) + i_g(t)$
I_{p1}	$\frac{(V_{pp}\,(1+K_{lpe}) - V_{gp})\,\pi}{2\,\omega_s L_p\,(2+K_{lpe})} + \frac{V_{gp}t_{pg}}{L_p\,(2+K_{lpe})} - \frac{V^p_{e\text{-eq-}p}\cos(\theta_{ce\text{-eq}})}{\omega_s L_e\,(2+K_{lpe})}$
I_{g1}	$\frac{(V_{gp}-V_{pp})\,\pi}{2\,\omega_s L_g} - \frac{V_{gp}t_{pg}}{L_g} + \frac{(V_{pp}\,(1+K_{lge}) - V_{gp})\,\pi}{2\,\omega_s L_g\,(2+K_{lge})} + \frac{V_{gp}t_{pg}}{L_g\,(2+K_{lge})} - \frac{V^p_{e\text{-eq-}p}\cos(\theta_{ce\text{-eq}})}{\omega_s L_e\,(2+K_{lge})}$
	Expression for $t_{pg} \leqslant t < (T_s/2)$
$i_p(t)$	$I_{p2} + \frac{V_{pp}\,(1+K_{lpe})\,t - V_{gp}t}{L_p\,(2+K_{lpe})} + \frac{V^p_{e\text{-eq-}p}\,(\cos(\omega_s(t+t_{pg}) - \theta_{ce\text{-eq}}) - \cos(\omega_s t_{pg} - \theta_{ce\text{-eq}}))}{\omega_s L_e\,(2+K_{lpe})}$
$i_g(t)$	$-I_{g2} - \frac{(V_{pp}-V_{gp})\,t}{L_g} + \frac{V_{pp}\,(1+K_{lge})\,t - V_{gp}t}{L_g\,(2+K_{lge})} + \frac{V^p_{e\text{-eq-}p}\,(\cos(\omega_s(t+t_{pg}) - \theta_{ce\text{-eq}}) - \cos(\omega_s t_{pg} - \theta_{ce\text{-eq}}))}{\omega_s L_e\,(2+K_{lge})}$
$i_e(t)$	$i_p(t) + i_g(t)$
I_{p2}	$-I_{p1} + \frac{V_{pp}\,(1+K_{lpe})\,t_{pg} + V_{gp}t_{pg}}{L_p\,(2+K_{lpe})} + \frac{V^p_{e\text{-eq-}p}\,(\cos(\omega_s t_{pg} - \theta_{ce\text{-eq}}) - \cos(\theta_{ce\text{-eq}}))}{\omega_s L_e\,(2+K_{lpe})}$
I_{g2}	$I_{g1} + \frac{(V_{pp}+V_{gp})\,t_{pg}}{L_g} - \frac{V_{pp}\,(1+K_{lge})\,t_{pg} + V_{gp}t_{pg}}{L_g\,(2+K_{lge})} - \frac{V^p_{e\text{-eq-}p}\,(\cos(\omega_s t_{pg} - \theta_{ce\text{-eq}}) - \cos(\theta_{ce\text{-eq}}))}{\omega_s L_e\,(2+K_{lge})}$
	Expression for $t_{pe} \leqslant t < (T_s/2) + t_{pe}$
$i^p_{e\text{-eq}}$	$I^p_{e\text{-eq}} - \frac{V^p_{e\text{-eq-}p}\,(\cos(\omega_s(t+t_{pe}) - \theta_{ce\text{-eq}}) - \cos(\omega_s t_{pe} - \theta_{ce\text{-eq}}))}{\omega_s L^p_{e\text{-eq}}} - \frac{V_{ep}t}{L^p_{e\text{-eq}}}$
$I^p_{e\text{-eq}}$	$\frac{V_{ep}\pi - 2\,V^p_{e\text{-eq-}p}\cos(\omega_s t_{pe} - \theta_{ce\text{-eq}})}{2\,\omega_s L^p_{e\text{-eq}}}$

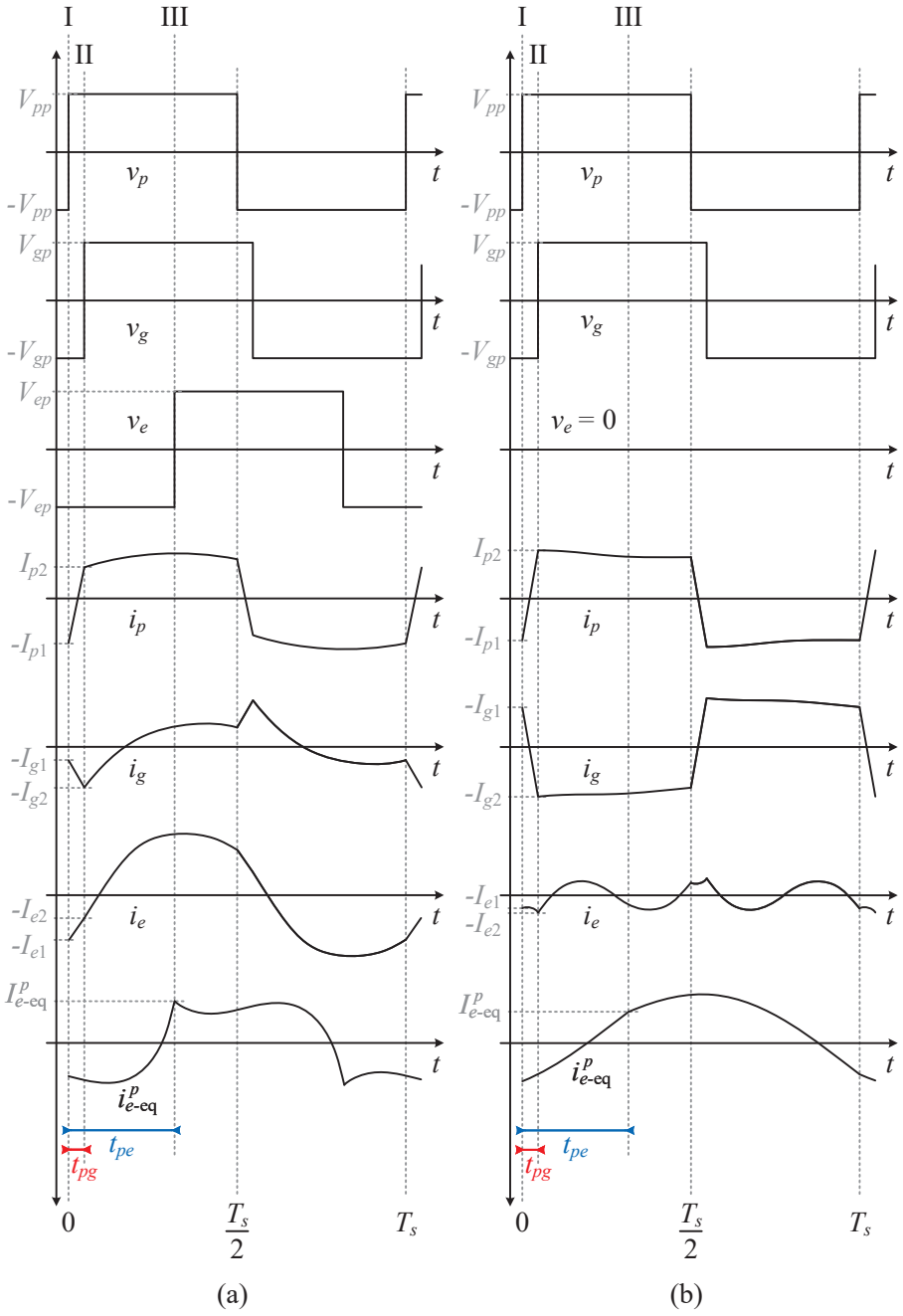


Fig. 6.9: Analytical tank currents referenced to the PV side for the following power flow conditions: (a) the PV port supplies full power to the EV battery, with no power delivered to the grid, and (b) the PV port supplies full power to the grid, while the EV battery is disconnected, resulting in zero power at the EV port by maintaining a zero ac square-wave voltage on the EV side. The shape of the tank currents varies throughout the grid cycle due to the pulsating dc-link voltage, v_{pn}. The waveforms in this figure correspond to the condition where v_{pn} is at its maximum.

illustrated in Fig. 6.9. The resulting tank current expressions, referenced to the PV side, are provided in Table 6.1. In these expressions, $V^{p}_{e\text{-eq-}p}\,(= V_{e\text{-eq-}p}(N_p/N_e))$ denotes the peak voltage across the tank capacitor $C_{e\text{-eq}}$, referenced to the PV side, while $\theta_{ce\text{-eq}}$ represents the phase lag of this voltage with respect to the square-wave voltage at the PV side, and

$$i_p = i_{lkp}\,, \tag{6.36}$$

$$i_g = i_{lkg}\left(\frac{N_g}{N_p}\right), \tag{6.37}$$

$$i_e = i_{lke}\left(\frac{N_e}{N_p}\right), \tag{6.38}$$

$$i^{p}_{e\text{-eq}} = i_{e\text{-eq}}\left(\frac{N_e}{N_p}\right), \tag{6.39}$$

$$L^{p}_{e\text{-eq}} = L_{e\text{-eq}}\left(\frac{N_p}{N_e}\right)^2, \tag{6.40}$$

$$K_{lpe} = \frac{L_p}{L_e}\,, \tag{6.41}$$

$$K_{lge} = \frac{L_g}{L_e}\,. \tag{6.42}$$

The analytical tank currents provided in Table 6.1 are plotted in Fig. 6.9. These expressions, referenced to the PV side, can be referred to the respective grid and EV sides using the transformer turn ratios. The rms values of these tank current waveforms can be computed using MATLAB, and based on these values, the conduction losses in the transformer, LCL tank network, and TAB MOSFETs can be accurately determined.

6.4.3 H-Bridge Voltages and Tank Currents During Switching Transitions

As the TAB-based three-port dc-dc converter operates at a high switching frequency of f_s, it is important to achieve ZVS for all three H-bridges to minimize switching losses. To ensure the ZVS of the MOSFETs, it is essential to observe the H-bridge voltages and corresponding tank currents during the switching transitions in the dead-time intervals. These voltages and currents are calculated for the three transitions identified in Figs. 6.9(a) and 6.9(b), referred to as transitions I, II, and III. During each transition, the H-bridge undergoing switching is modeled using a charge-equivalent capacitor [29,30,72] that accounts

for the nonlinear variation of the MOSFET output capacitance, C_{oss}, with respect to the drain-to-source voltage, as given by

$$C_{\text{eq},Q}\Big|_0^{v_c} = \frac{1}{v_c}\int_0^{v_c} C_{\text{oss}}|_v \, \mathrm{d}v, \tag{6.43}$$

where the charge stored in $C_{\text{eq},Q}$ at voltage v_c is the same as the charge stored when charging C_{oss} from 0 to v_c, where v_c can be any value from 0 to the rated operating voltage of the MOSFET.

The equivalent circuits corresponding to transitions I, II, and III are depicted in Figs. 6.10(a), 6.10(b), and 6.10(c), respectively. All circuits are referred to the PV side. Due to the relatively large inductance of L_e, the EV side can be approximated as a current source with a value equal to the current flowing through L_e, denoted as i_e, during the analysis of the PV and grid-side H-bridge transitions. During transition I, the differential equations corresponding to the equivalent circuit in Fig. 6.10(a) are solved to obtain the expressions for the voltage v_p and the current i_p during the switching transition, given by

$$v_p(t) = A_p \cos\left(\omega_p t + B_p\right) - V_{gp}\,, \tag{6.44}$$

$$i_p(t) = \frac{A_p}{R_p}\sin\left(\omega_p t + B_p\right)\,, \tag{6.45}$$

where

$$\omega_p = \frac{1}{\sqrt{(L_p + L_g)C_{\text{eq},Q\text{-}p}}}\,,\ R_p = \sqrt{\frac{L_p + L_g}{C_{\text{eq},Q\text{-}p}}}\,, \tag{6.46}$$

$$B_p = \tan^{-1}\left(\frac{-I_{p1}R_p}{-V_{pp} + V_{gp}}\right),\ A_p = \frac{-V_{pp} + V_{gp}}{\cos(B_p)}\,. \tag{6.47}$$

Using (6.44), the ZVS time required for the PV side H-bridge MOSFETs to complete the C_{oss} charging or discharging process, corresponding to the voltage v_p transitioning from $-V_{pp}$ to V_{pp}, can be calculated. The ZVS time is given by

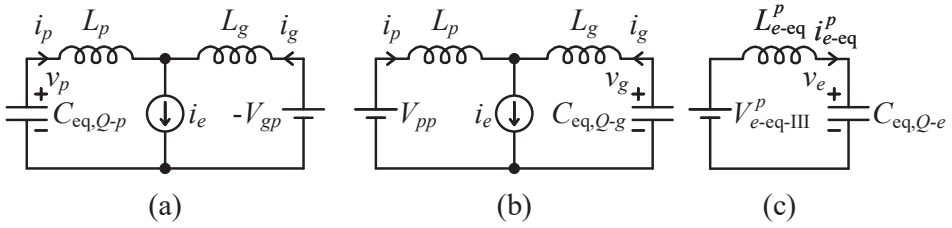


Fig. 6.10: Equivalent circuits, referred to the PV side, during switching transitions: (a) I, (b) II, and (c) III, where $V^p_{e\text{-eq-III}}$ denotes the voltage across the tank capacitor $C_{e\text{-eq}}$ during transition III, referred to the PV side.

$$t_{\text{zvs-pv}} = \frac{\sin^{-1}\left(\frac{V_{pp}+V_{gp}}{A_p}\right) - B_p - \frac{\pi}{2}}{\omega_p}\,. \tag{6.48}$$

Similarly, the analysis can be extended to derive the expressions for transition II as

$$v_g(t) = A_g \cos\left(\omega_g t + B_g\right) + V_{pp}\,, \tag{6.49}$$

$$i_g(t) = \frac{A_g}{R_g} \sin\left(\omega_g t + B_g\right)\,, \tag{6.50}$$

$$t_{\text{zvs-grid}} = \frac{\sin^{-1}\left(\frac{V_{gp}-V_{pp}}{A_g}\right) - B_g - \frac{\pi}{2}}{\omega_g}\,, \tag{6.51}$$

where

$$\omega_g = \frac{1}{\sqrt{(L_g + L_p)C_{\text{eq},Q\text{-}g}}}\,,\ R_g = \sqrt{\frac{L_g + L_p}{C_{\text{eq},Q\text{-}g}}}\,, \tag{6.52}$$

$$B_g = \tan^{-1}\left(\frac{-I_{g2}R_g}{-V_{gp} - V_{pp}}\right),\ A_g = \frac{-V_{gp} - V_{pp}}{\cos(B_g)}\,. \tag{6.53}$$

Finally, the analysis can be extended to derive the expressions for transition III as

$$v_e(t) = A_e \cos\left(\omega_e t + B_e\right) + V^p_{e\text{-eq-III}}\,, \tag{6.54}$$

$$i^p_{e\text{-eq}}(t) = \frac{-A_e}{R_e} \sin\left(\omega_e t + B_e\right)\,, \tag{6.55}$$

$$t_{\text{zvs-ev}} = \frac{\sin^{-1}\left(\frac{V_{ep}-V^p_{e\text{-eq-III}}}{A_e}\right) - B_e - \frac{\pi}{2}}{\omega_e}\,, \tag{6.56}$$

where

$$\omega_e = \frac{1}{\sqrt{L^p_{e\text{-eq}} C_{\text{eq},Q\text{-}e}}}\,,\ R_e = \sqrt{\frac{L^p_{e\text{-eq}}}{C_{\text{eq},Q\text{-}e}}}\,, \tag{6.57}$$

$$B_e = \tan^{-1}\left(\frac{-I^p_{e\text{-eq}} R_e}{-V_{ep} - V^p_{e\text{-eq-III}}}\right),\ A_e = \frac{-V_{ep} - V^p_{e\text{-eq-III}}}{\cos(B_e)}\,, \tag{6.58}$$

$$V^p_{e\text{-eq-III}} = V^p_{e\text{-eq-}p} \sin(\omega_s t_{pe} - \theta_{ce\text{-eq}})\,. \tag{6.59}$$

In the above equations, the charge-equivalent capacitors $C_{\text{eq},Q\text{-}p}$, $C_{\text{eq},Q\text{-}g}$, and $C_{\text{eq},Q\text{-}e}$ are all referred to the PV side.

6.4.4 Optimized Selection of the Tank Components

As the proposed multiport system involves multiple power flow scenarios, the tank component selection process for the TAB-based dc-dc converter is simplified by considering the case where the PV port supplies the full rated power, P_{rated}, and the EV port receives power ranging from 0 to P_{rated}. If the EV port requires less than P_{rated}, the remaining power is delivered to the grid port. The optimization is performed by determining the phase shifts, ϕ_{pg} and $(\pi - \phi_{pe})$, along with the corresponding tank components, to minimize the rms tank currents, as calculated using the expressions in Section 6.4.2, thereby reducing conduction losses. Moreover, sufficient tank current magnitude and appropriate polarity during the switching transitions are ensured to achieve ZVS for all three H-bridges, based on the analysis presented in Section 6.4.3.

For the power architecture between the PV and grid ports in the proposed multiport system, the operating point corresponding to the minimum phase shift, ϕ_{pg}, results in a lower tank current for ZVS on the grid side during switching transitions and therefore requires careful analysis to ensure ZVS of the grid-side H-bridge. Guaranteeing ZVS at this operating point inherently ensures ZVS across all other operating points. Furthermore, as discussed earlier in Section 6.4.1, the EV-side HF ac square-wave voltage is maintained at a phase lag of $(\pi - \phi_{pe})$ relative to the PV-side voltage, which maintains the phase lag greater than $\frac{\pi}{2}$. It must be ensured that this phase lag does not fall below $\frac{\pi}{2}$, as doing so could

compromise closed-loop control stability and also result in the EV-side H-bridge losing ZVS, as explained in Section 6.4.1. Considering these factors, it is evident that lower values of the phase shifts, ϕ_{pg} and $(\pi - \phi_{pe})$, must be carefully selected to avoid issues related to ZVS and control stability. Therefore, phase shift selection should be based on the power flow scenario that requires relatively smaller phase shift values, corresponding to the case where the EV port receives the full power from the PV port, while the grid port receives no power. Now, for this power flow scenario, the phase shifts are swept from 0 to $\frac{\pi}{2}$ and from $\frac{\pi}{2}$ to π, corresponding to $(\phi_{pg})_{\text{sweep}}$ and $(\pi - \phi_{pe})_{\text{sweep}}$, respectively. For each value in these phase shift sweeps, the corresponding tank component values are subsequently calculated. The tank inductors represented in a delta-connected configuration, L_{pg}, L_{pe}, and L_{ge}, are first calculated using the power flow equations given in (6.28)–(6.33). Using these, the individual tank components are then calculated as

$$L_{lkp} = L_p = \frac{L_{pg}L_{pe}}{L_{pg} + L_{pe} + L_{ge}}, \tag{6.60}$$

$$L_{lkg} = L_g \left(\frac{N_g}{N_p}\right)^2 = \frac{L_{pg}L_{ge}}{L_{pg} + L_{pe} + L_{ge}} \left(\frac{N_g}{N_p}\right)^2, \tag{6.61}$$

$$L_{lke} + L_{es} = L_e \left(\frac{N_e}{N_p}\right)^2 = \frac{L_{pe}L_{ge}}{L_{pg} + L_{pe} + L_{ge}} \left(\frac{N_e}{N_p}\right)^2. \tag{6.62}$$

Now, $L_{e\text{-eq}}$ is determined by calculating the equivalent inductance referred to the EV side, using the parallel combination of L_p and L_g in series with L_e, as

$$L_{e\text{-eq}} = \left(L_e + \frac{L_p L_g}{L_p + L_g}\right) \left(\frac{N_e}{N_p}\right)^2. \tag{6.63}$$

Finally, $C_{e\text{-eq}}$ is selected to resonate at the switching frequency with the equivalent inductance calculated above, as discussed in Section 6.4.1. The value of this capacitor is given as

$$C_{e\text{-eq}} = \frac{1}{\omega_s^2 L_{e\text{-eq}}}. \tag{6.64}$$

Following the calculation of multiple sets of tank component values corresponding to

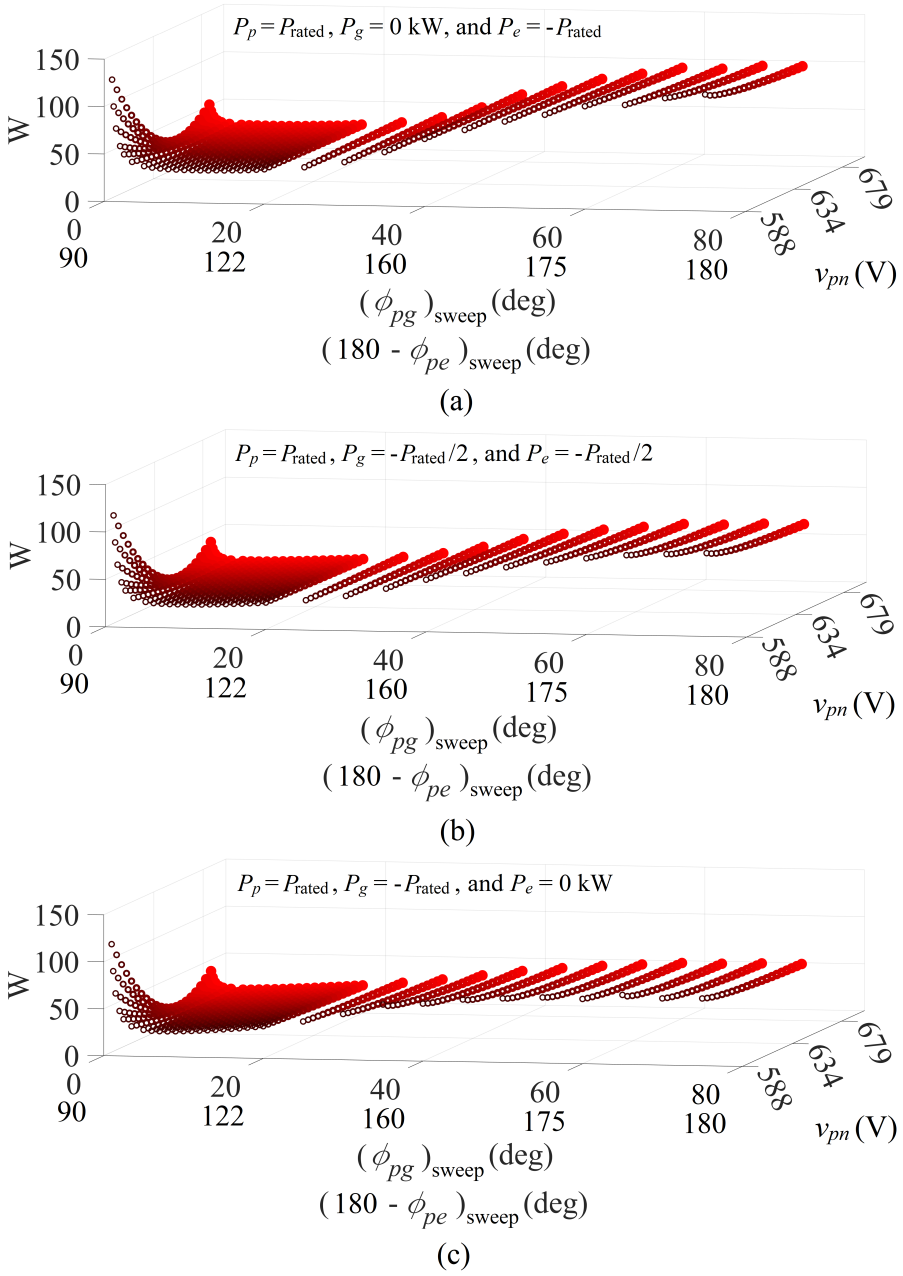


Fig. 6.11: Different values of phase-shift combinations, $(\phi_{pg})_{\text{sweep}}$ and $(\pi - \phi_{pe})_{\text{sweep}}$, are considered. Based on these values, tank components are calculated. The corresponding analytical tank currents and conduction losses are then evaluated across various operating scenarios: (a) the PV port supplies full power to the EV port, (b) the PV port supplies power to both the EV and grid ports, and (c) the PV port supplies all power to the grid port. The pulsating nature of the dc-link voltage, v_{pn}, is also taken into account.

various combinations of $(\phi_{pg})_{\text{sweep}}$ and $(\pi - \phi_{pe})_{\text{sweep}}$, the analytical tank currents and corresponding conduction losses can be evaluated for various operating scenarios: (i) the PV

port supplies the full power to the EV port, (ii) the PV port supplies power to both the EV and grid ports, and (iii) the PV port supplies all the power to the grid port. By evaluating the conduction losses for various power flow scenarios, the selection of optimized tank components can be done, which leads to an efficient dc-dc converter for various operating conditions. The evaluated conduction losses for these three power flow scenarios are illustrated in Figs. 6.11(a), 6.11(b), and 6.11(c), respectively. The x-axis in all these plots represents each value in the phase shift sweeps and the corresponding evaluated tank components. It should also be noted that the conduction loss calculations account for all MOSFETs in the H-bridges of the dc-dc converter. These figures reveal a plateau region of minimal conduction losses, indicating favorable phase-shift combinations for efficient dc-dc converter operation.

For the ZVS analysis, the H-bridge voltages and corresponding tank currents during the switching transitions are derived using (6.44), (6.45), (6.49), (6.50), (6.54), and (6.55). Based on these expressions, state-plane diagrams for switching transitions I, II, and III, corresponding to the PV-side, grid-side, and EV-side H-bridges, are plotted in Fig. 6.12. For ZVS of the MOSFETs, the polarity and magnitude of the tank currents must be appropriate to charge or discharge the C_{oss} of the MOSFETs. This ensures that the voltages v_p, v_g, and v_e, corresponding to the PV-side, grid-side, and EV-side H-bridges, respectively, transition completely from $-V_{pp}$ to V_{pp}, $-V_{gp}$ to V_{gp}, and $-V_{ep}$ to V_{ep} during transitions I, II, and III, within the dead time. Phase-shift combinations, along with their associated tank components and tank currents, that fail to fully transition these voltages within the dead time are excluded from consideration. Such failures, resulting from either incorrect polarity or insufficient magnitude of the tank currents, lead to incomplete or no ZVS.

Moreover, the ZVS durations are calculated using (6.48), (6.51), and (6.56). Phase-shift combinations that result in ZVS durations exceeding 150 ns are also excluded. This threshold is selected based on the hardware implementation, which uses a constant dead time of 150 ns, corresponding to 1.5% of the switching period. This value serves as a practical upper bound to avoid the effect of switching transitions during the dead time on

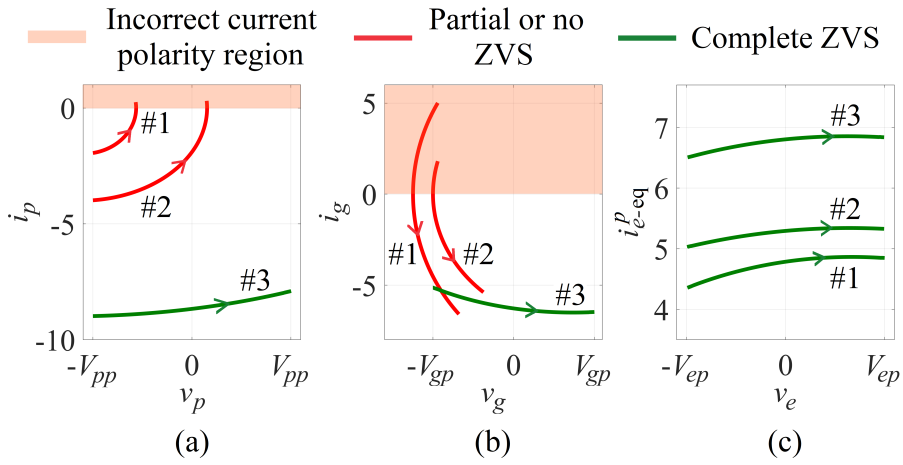


Fig. 6.12: State-plane diagrams for three phase-shift combinations (#1, #2, and #3) of $(\phi_{pg})_{\text{sweep}}$ and $(\pi - \phi_{pe})_{\text{sweep}}$, plotted using the expressions for H-bridge voltages and tank currents derived in (6.44), (6.45), (6.49), (6.50), (6.54), and (6.55), during the switching transitions of (a) PV-side H-bridge (transition I), (b) grid-side H-bridge (transition II), and (c) EV-side H-bridge (transition III). Phase-shift combinations #1 and #2 result in partial or no ZVS for the PV and grid-side H-bridge MOSFETs, whereas combination #3 achieves complete ZVS across all three H-bridges of the TAB. For phase-shift combination #3, the respective tank current polarities for all three transitions are correct and have sufficient magnitude to transition H-bridge voltages from $-V$ to $+V$ within the dead time.

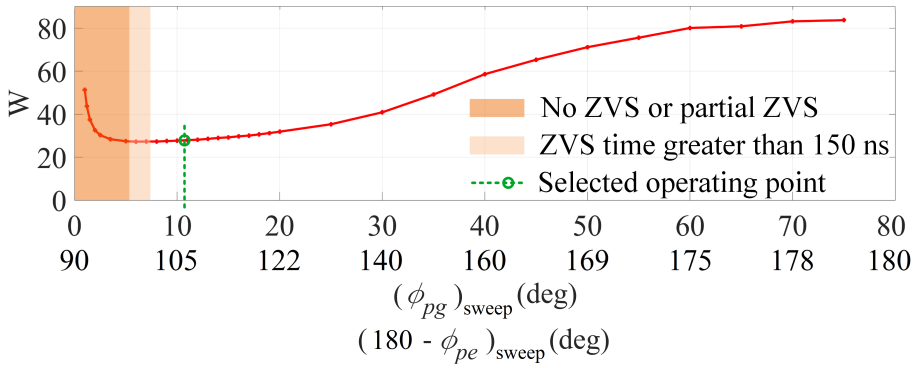


Fig. 6.13: Averaged conduction losses of the TAB-based three-port dc-dc converter for different combinations of phase shifts, $(\phi_{pg})_{\text{sweep}}$ and $(\pi - \phi_{pe})_{\text{sweep}}$, combining the operating cases shown in Fig. 6.11. The figure also highlights non-favorable operating regions where complete ZVS is not achieved or the ZVS duration exceeds the 150 ns limit. The selected operating point is chosen to minimize conduction losses and ensure complete ZVS.

the steady-state power flow.

Fig. 6.13 presents a consolidated analysis of the average conduction losses of the dc-dc converter, and it also highlights the non-favorable operating regions where complete ZVS is

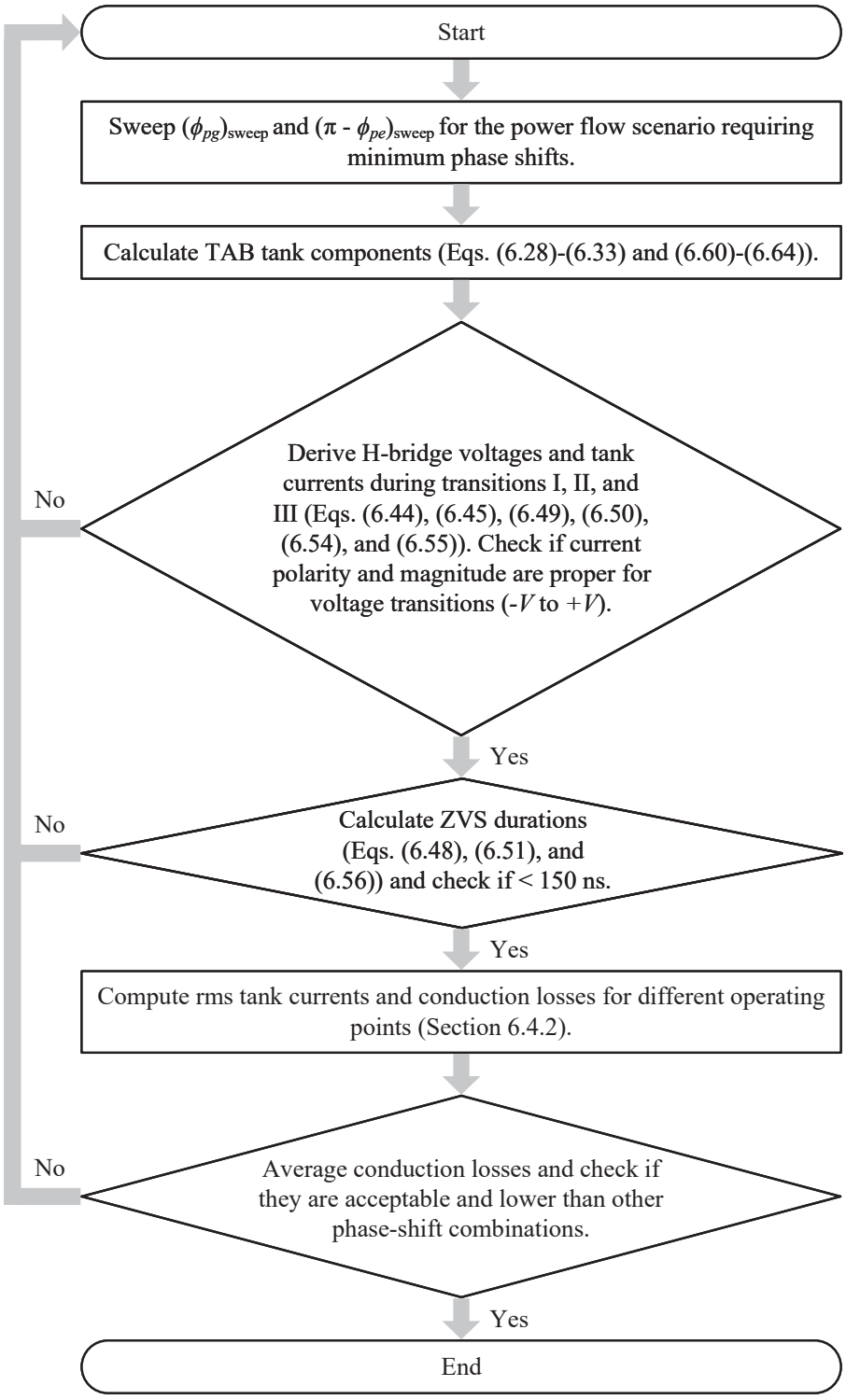


Fig. 6.14: Flowchart illustrating the process for determining optimized tank components to minimize conduction losses and ensure complete ZVS.

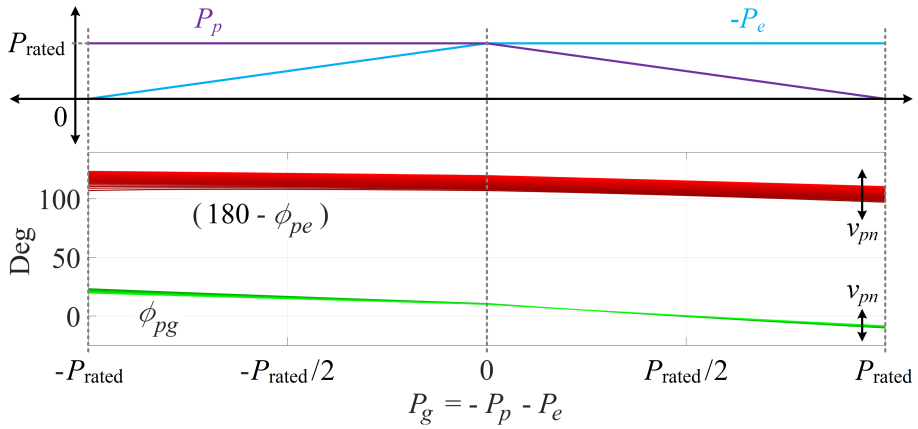


Fig. 6.15: Phase shifts ϕ_{pg} and $(\pi - \phi_{pe})$ corresponding to various power flow scenarios considered in this study are shown. The pulsating nature of the dc-link voltage, v_{pn}, is also taken into account for each power flow case.

not achieved or the ZVS duration exceeds the 150 ns limit. By excluding such non-favorable regions and minimizing conduction losses, the optimal phase-shift combination is identified, as illustrated in Fig. 6.13. The corresponding evaluated tank parameters are detailed in the experimental validation section. A flowchart is provided in Fig. 6.14, illustrating the process for determining optimized TAB-based dc-dc converter tank components to minimize conduction losses and ensure complete ZVS. Finally, for the selected tank components, the calculated phase shifts ϕ_{pg} and $(\pi - \phi_{pe})$, corresponding to all power flow scenarios discussed in Section 6.4.1, are presented in Fig. 6.15.

6.5 Control and Modeling of the Multiport System

The multiport system is designed to support multiple power flow scenarios, as discussed in Section 6.4.1. The proposed control architecture, illustrated in Fig. 6.3, autonomously manages all corresponding power flow directions. The phase shift between the ac square wave voltages at the PV and grid sides, ϕ_{pg}, regulates the PV current, i_{pv}, whereas the phase shift between the PV and EV sides, $(\pi - \phi_{pe})$, regulates the EV current, i_{ev}. The current references for these two control loops can be generated through supervisory control that incorporates the MPPT algorithm for PV-based renewable sources, along with the EV battery charging profile. Based on real-time evaluation of the power demand at the EV port

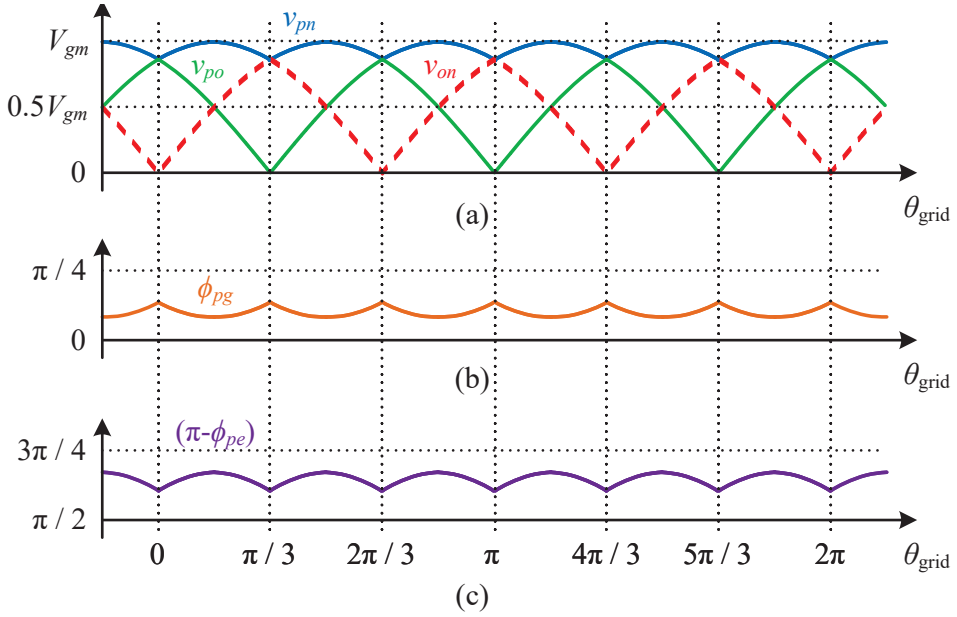


Fig. 6.16: (a) Pulsating dc-link voltages v_{po}, v_{on}, and v_{pn} on the grid side. Since the pulsating v_{pn} connects to the grid-side H-bridge, 360 Hz variations in the control angles are required to regulate PV and EV currents: (b) ϕ_{pg}, (c) $(\pi - \phi_{pe})$.

and the available power from the PV port, the system accordingly computes the current reference for grid-side current injection using (6.1) and (6.2), as detailed in Section 6.3. This ensures the generation of appropriate sinusoidal grid currents that either receive the excess power or supply the required deficit.

As discussed earlier, the dc-link voltage on the grid side, v_{pn}, exhibits a six-pulse waveform at six times the grid frequency, which corresponds to 360 Hz in this study. To regulate accurate power flow at all ports, the associated control loops must operate with closed-loop bandwidths exceeding 360 Hz. This enables appropriate variations in the control angles ϕ_{pg} and $(\pi - \phi_{pe})$, as shown in Fig. 6.16, to regulate the PV and EV currents over the grid cycle. Appropriate selection of bandwidths requires the derivation of the plant transfer functions for all control loops shown in Fig. 6.3. The plant for the grid side current injection control is modeled as $G_{\text{plant-ci}} = 1/(sL_{\text{ci}})$. The plant transfer functions for the PV and EV current control loops are derived using a phasor transformation-based small-signal modeling approach [60–63, 94]. This modeling process consists of three main steps: (i) steady-state analysis to establish the relationship between steady-state PV or EV

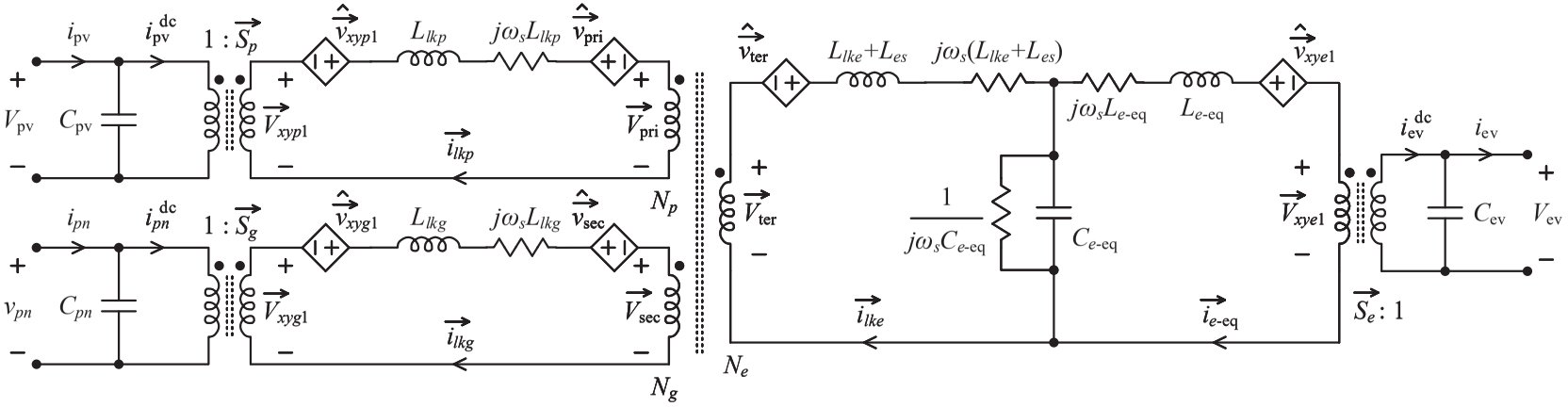


Fig. 6.17: Combined steady-state and small-signal phasor-transformed representation of the TAB-based three-port dc-dc converter with a three-winding transformer and an LCL tank on the EV side.

currents and their corresponding steady-state phase shift control variables; (ii) derivation of the phasor-transformed equivalent circuit for the TAB-based three-port dc-dc converter, as illustrated in Fig. 6.17; and (iii) small-signal derivation of the plant transfer functions based on the aforementioned phasor-transformed circuit. The resulting plant transfer functions for the PV and EV current control loops are

$$G_{\text{plant-pv}} = \frac{\hat{i}_{\text{pv}}}{\hat{\phi}_{pg}} = \frac{\hat{i}_{\text{pv}}^{\hat{i}_{lkp\text{-mag}}}}{\hat{i}_{lkp\text{-mag}}} \frac{\hat{i}_{lkp\text{-mag}}}{\hat{\phi}_{pg}} + \frac{\hat{i}_{\text{pv}}^{\hat{\theta}_{lkp}}}{\hat{\theta}_{lkp}} \frac{\hat{\theta}_{lkp}}{\hat{\phi}_{pg}}, \tag{6.65}$$

$$G_{\text{plant-ev}} = \frac{\hat{i}_{\text{ev}}}{\hat{\phi}_{pe}} = \frac{\hat{i}_{\text{ev}}^{\hat{i}_{e\text{-eq-mag}}}}{\hat{i}_{e\text{-eq-mag}}} \frac{\hat{i}_{e\text{-eq-mag}}}{\hat{\phi}_{pe}} + \frac{\hat{i}_{\text{ev}}^{\hat{\theta}_{le\text{-eq}}}}{\hat{\theta}_{le\text{-eq}}} \frac{\hat{\theta}_{le\text{-eq}}}{\hat{\phi}_{pe}} + \frac{\hat{i}_{\text{ev}}^{\hat{\phi}_{pe}}}{\hat{\phi}_{pe}}, \tag{6.66}$$

where

$$\frac{\hat{i}_{\text{pv}}^{\hat{i}_{lkp\text{-mag}}}}{\hat{i}_{lkp\text{-mag}}} = \frac{2}{\pi} \cos(\Theta_{lkp}), \tag{6.67}$$

$$\frac{\hat{i}_{\text{pv}}^{\hat{\theta}_{lkp}}}{\hat{\theta}_{lkp}} = \frac{2}{\pi} I_{lkp\text{-mag}} \sin(\Theta_{lkp}), \tag{6.68}$$

$$\frac{\hat{i}_{\text{ev}}^{\hat{i}_{e\text{-eq-mag}}}}{\hat{i}_{e\text{-eq-mag}}} = \frac{2}{\pi} \cos(\pi - \Phi_{pe} - \Theta_{le\text{-eq}}), \tag{6.69}$$

$$\frac{\hat{i}_{\text{ev}}^{\hat{\theta}_{le\text{-eq}}}}{\hat{\theta}_{le\text{-eq}}} = \frac{2}{\pi} I_{e\text{-eq-mag}} \sin(\pi - \Phi_{pe} - \Theta_{le\text{-eq}}), \tag{6.70}$$

$$\frac{\hat{i}_{\text{ev}}^{\hat{\phi}_{pe}}}{\hat{\phi}_{pe}} = \frac{2}{\pi} I_{e\text{-eq-mag}} \sin(\pi - \Phi_{pe} - \Theta_{le\text{-eq}}), \tag{6.71}$$

and $\frac{\hat{i}_{lkp\text{-mag}}}{\hat{\phi}_{pg}}$, $\frac{\hat{\theta}_{lkp}}{\hat{\phi}_{pg}}$, $\frac{\hat{i}_{e\text{-eq-mag}}}{\hat{\phi}_{pe}}$, and $\frac{\hat{\theta}_{le\text{-eq}}}{\hat{\phi}_{pe}}$ are calculated by splitting the equations $\frac{\hat{\overrightarrow{i_{lkp}}}}{\hat{\phi}_{pg}}$ and $\frac{\hat{\overrightarrow{i_{e\text{-eq}}}}}{\hat{\phi}_{pe}}$, derived using Fig. 6.17, into their linearized magnitude and phase components using a first-order Taylor series approximation, as detailed in Chapter 5.

In the above equations, $\hat{i}_{\text{pv}}^{\hat{i}_{lkp\text{-mag}}}$ and $\hat{i}_{\text{pv}}^{\hat{\theta}_{lkp}}$ represent perturbations in the PV current, i_{pv}, that depend upon the small-signal changes in the magnitude ($\hat{i}_{lkp\text{-mag}}$) and phase ($\hat{\theta}_{lkp}$) of the tank current phasor on the PV side ($\hat{\overrightarrow{i_{lkp}}}$), respectively. These perturbations arise due to small-signal deviations introduced in the control input ϕ_{pg}. Similarly, $\hat{i}_{\text{ev}}^{\hat{i}_{e\text{-eq-mag}}}$ and $\hat{i}_{\text{ev}}^{\hat{\theta}_{le\text{-eq}}}$ are perturbations in the EV battery current, i_{ev}, that depend upon the small-signal changes

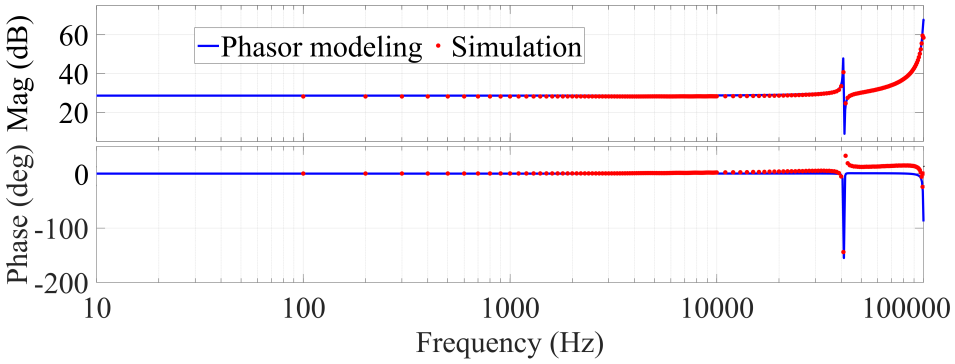


Fig. 6.18: Comparison of Bode plots of the plant ($G_{\text{plant-pv}} = \hat{i}_{\text{pv}}/\hat{\phi}_{pg}$) of the TAB-based three-port dc-dc converter, obtained from the phasor transformation-based small-signal modeling and PLECS multitone analysis-tool-based simulation.

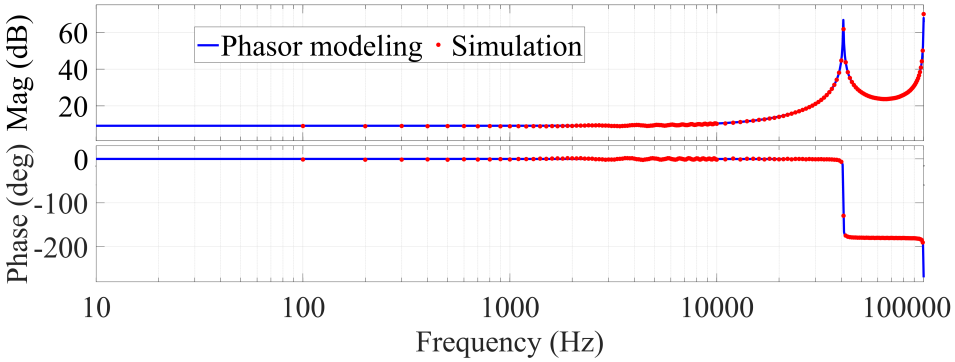


Fig. 6.19: Comparison of Bode plots of the plant ($G_{\text{plant-ev}} = \hat{i}_{\text{ev}}/\hat{\phi}_{pe}$) of the TAB-based three-port dc-dc converter, obtained from the phasor transformation-based small-signal modeling and PLECS multitone analysis-tool-based simulation.

in the magnitude ($\hat{I}_{e\text{-eq-mag}}$) and phase ($\hat{\theta}_{le\text{-eq}}$) of the EV side H-bridge input current phasor ($\overrightarrow{i_{e\text{-eq}}}$), respectively. These perturbations arise due to small-signal deviations introduced in the control input ϕ_{pe}. Moreover, $\hat{i}_{\text{ev}}^{\phi_{pe}}$ represents the direct effect of the small-signal change in ϕ_{pe} on the current i_{ev}. Finally, Θ_{lkp}, $I_{lkp\text{-mag}}$, Φ_{pe}, $\Theta_{le\text{-eq}}$, and $I_{e\text{-eq-mag}}$ denote the steady-state values of the corresponding system parameters.

The Bode plots of the plant transfer functions $G_{\text{plant-pv}}$ and $G_{\text{plant-ev}}$, derived from phasor transformation-based modeling, are validated through comparison with the Bode plots obtained via multitone analysis using the PLECS simulation tool, as shown in Figs. 6.18 and 6.19. The Bode plots are provided for the case where the grid-side dc-link voltage equals its average value. Additionally, the parameters of the PI controller employed in all three

Table 6.2: PI controller parameters for various closed-loop controls.

Plant Being Compensated	**Bandwidth (Hz)**	$\boldsymbol{K_p}$-PI	$\boldsymbol{K_i}$-PI
$G_{\text{plant-ci}}$	1800	8.28	23403.5
$G_{\text{plant-pv}}$	1080	0.01	252.4
$G_{\text{plant-ev}}$	720	0.1	1574.7

control loops, along with their respective closed-loop bandwidths, are provided in Table 6.2.

6.6 Three-Winding Transformer Design

As discussed earlier, a DAB-based power architecture is employed for the PV-to-grid side dc-dc conversion. The required tank inductance for power transfer is integrated into the three-winding transformer through its leakage inductance. This integration eliminates the need for additional discrete inductors on both the PV and grid HF ac sides, thereby reducing the number of magnetic components and enhancing overall system efficiency and power density. The equivalent leakage inductance between the PV and grid-side windings, referred to the PV side, is given as

$$L_{lk\text{-pv-grid}} = L_{lkp} + L_{lkg}\left(\frac{N_p}{N_g}\right)^2 = L_p + L_g\,. \tag{6.72}$$

Moreover, the equivalent leakage inductances between the EV and grid-side windings, and between the EV and PV-side windings, both referred to the PV side, are given as

$$L_{lk\text{-ev-grid}} = L_{lke}\left(\frac{N_p}{N_e}\right)^2 + L_{lkg}\left(\frac{N_p}{N_g}\right)^2 = L_{lke}\left(\frac{N_p}{N_e}\right)^2 + L_g\,, \tag{6.73}$$

$$L_{lk\text{-ev-pv}} = L_{lke}\left(\frac{N_p}{N_e}\right)^2 + L_{lkp} = L_{lke}\left(\frac{N_p}{N_e}\right)^2 + L_p\,. \tag{6.74}$$

In this study, the design choice of $L_p = L_g$ is considered to ensure that the LCL tank remains symmetric for power transfer from both the PV and grid ports to the EV port. From (6.73) and (6.74), it can be observed that, to maintain $L_p = L_g$, $L_{lk\text{-ev-pv}}$ should be equal to $L_{lk\text{-ev-grid}}$. This implies that the leakage inductance between the EV and PV-side windings,

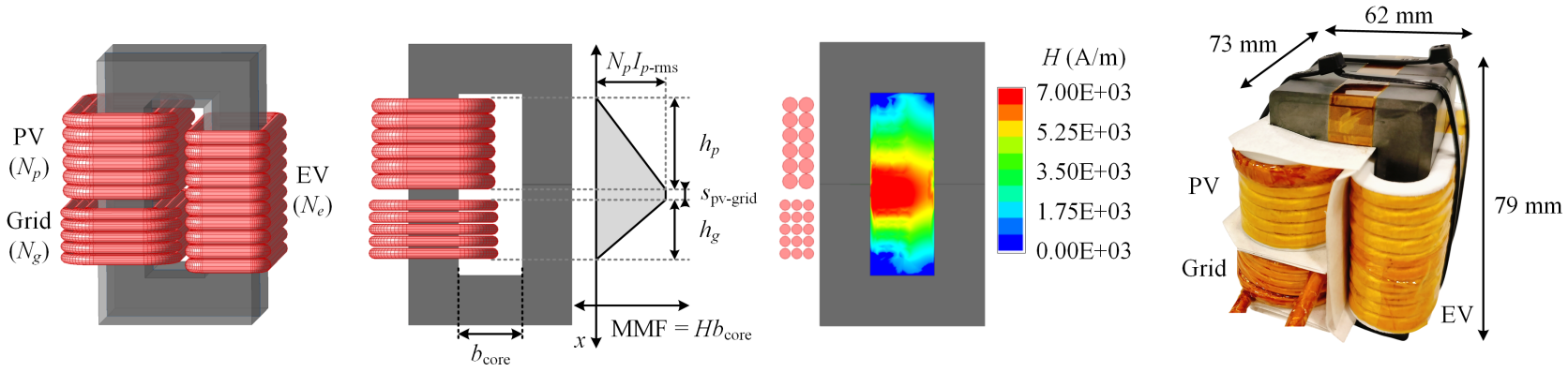


Fig. 6.20: (a) Three-winding transformer designed in ANSYS MAXWELL using four U46/40/28 ferrite cores, with the PV and grid-side windings placed on one limb and the EV-side winding on the other limb; (b) analytical field distribution for the PV and grid-side windings with the EV-side winding left unenergized; (c) 3D FEA simulation showing the H-field distribution when the PV and grid-side windings are energized; and (d) fabricated three-winding transformer for hardware implementation.

and between the EV and grid-side windings, must be equal to satisfy the design choice. As the leakage inductance in a transformer is a function of geometric parameters [104,120,121], the PV and grid-side windings should be placed symmetrically with respect to the EV-side winding. Given that, the PV and grid windings are placed on one limb of the UU core-shaped transformer and the EV winding is placed on the other limb, as shown in Fig. 6.20(a). Four U46/40/28 ferrite cores from Ferroxcube are used and the cores are paralleled to reduce the flux density and minimize hysteresis losses, which have been calculated using the iGSE [122].

As mentioned later in the experimental validation section, the PV port is connected to a 500 V dc supply, while the average value of the pulsating dc-link voltage on the grid side, $V_{pn\text{-avg}}$, is $\frac{3}{\pi}V_{gm}$, which evaluates to 648 V. Considering these voltage levels and to maintain the core flux density below 150 mT to keep hysteresis losses within acceptable limits, the PV-side winding is designed with 12 turns (N_p) and the grid-side winding with 15 turns (N_g). Finally, the number of turns in the EV-side winding, N_e, is determined by minimizing the kVAr/kW ratio of the LCL tank, thereby enhancing system efficiency by reducing reactive power. A wide EV battery voltage range of 200–800 V is considered. For each value of N_e, the kVAr/kW ratio of the LCL tank is computed over this battery voltage range using

$$(Q/P)_{L_{lke},\,L_{es}} = \frac{i^2_{lke\text{-rms}}\omega_s(L_{lke}+L_{es})}{P_e}\,, \tag{6.75}$$

$$(Q/P)_{C_{e\text{-eq}}} = \frac{(i_{lke}-i_{e\text{-eq}})^2_{\text{rms}}}{\omega_s C_{e\text{-eq}} P_e}\,, \tag{6.76}$$

$$(Q/P)_{L_{e\text{-eq}}} = \frac{i^2_{e\text{-eq-rms}}\omega_s L_{e\text{-eq}}}{P_e}\,, \tag{6.77}$$

$$(Q/P)_{LCL} = (Q/P)_{L_{lke},\,L_{es}} + (Q/P)_{C_{e\text{-eq}}} + (Q/P)_{L_{e\text{-eq}}}\,, \tag{6.78}$$

and averaged, as shown in Fig. 6.21. The figure indicates that the tank achieves its minimum kVAr/kW ratio when N_e is close to 10. Based on this observation, the EV-side winding is designed with 10 turns. All three windings are designed using Litz wire to minimize winding losses caused by skin and proximity effects.

In this work, the inductor required between the PV- and grid-side H-bridges is realized

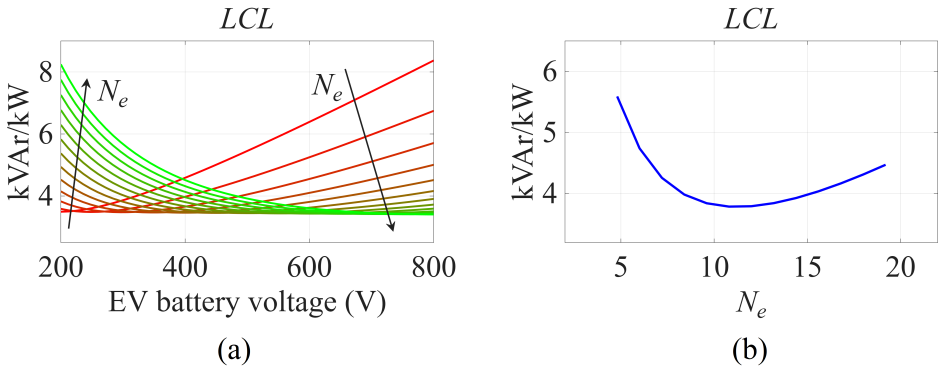


Fig. 6.21: kVAr/kW ratio of (a) the overall LCL tank for various EV battery voltages and turns on the EV-side winding (N_e), and (b) the averaged kVAr/kW ratio of the LCL tank with respect to N_e. To minimize the kVAr/kW ratio and improve efficiency, $N_e = 10$ is selected.

Table 6.3: Fabricated three-winding transformer parameters.

Parameter	**Value**
$N_p : N_g : N_e$	12 : 15 : 10
Cores	4×U46/40/28, 3C95 (Ferroxcube)
PV and EV-side windings Litz wire	1100 strands of AWG 40
Grid-side winding Litz wire	700 strands of AWG 40
$s_{\text{pv-grid}}$	2.762 mm
$L_{lk\text{-pv-grid}} = L_p + L_g$	24.86 μH
L_{lkp}, L_{lkg}, and L_{lke}	12.43 μH, 19.42 μH, and 18.25 μH
Magnetizing inductance referred to the PV side	1.54 mH

through the leakage inductance of the designed three-winding transformer. This integration eliminates the need for additional discrete inductors, reducing magnetic components and improving system efficiency and power density. The spacing between the PV and grid-side windings, $s_{\text{pv-grid}}$, is analytically determined to achieve the desired leakage inductance,

assuming a negligible H-field in the core and magnetic field lines orthogonal to the core surface due to its high permeability. The magnetic field distribution is shown in Figs. 6.20(b) and 6.20(c). The field distribution is illustrated only for the PV and grid-side windings, as the EV-side winding remains unenergized during the calculation of leakage inductance between the PV and grid-side windings. The resulting leakage inductance, referred to the PV side, can be expressed as a function of $s_{\text{pv-grid}}$ by solving $\frac{1}{2}(L_p + L_g)I_{p\text{-rms}}^2 = \frac{\mu_o}{2}\int H^2 dV_{\text{core}}$, which gives

$$\left.\begin{aligned} L_{lk\text{-pv-grid}} &= L_{lkp} + L_{lkg}\left(\frac{N_p}{N_g}\right)^2 = L_p + L_g \\ &= 4\pi\times10^{-4}\,\frac{N_p^2}{b_{\text{core}}}\left(\frac{h_p \text{MLT}_p}{3} + \frac{h_g \text{MLT}_g}{3} + s_{\text{pv-grid}}\text{MLT}_{\text{avg}}\right), \end{aligned}\right\} \tag{6.79}$$

where b_{core} is the spacing between the UU core limbs; h_p, MLT_p, h_g, and MLT_g are the heights and mean turn lengths of the PV and grid-side windings, respectively. The average mean turn length, MLT_{avg}, is the arithmetic mean of MLT_p and MLT_g. The inductance is in μH, and all dimensions are in mm. It should be noted that the expression provided in (6.79) to calculate leakage inductance is derived assuming that the H-field lines are orthogonal to the core surface. This approximation is typically valid when the ratio $\frac{b_{\text{core}}}{\lambda}$, where $\lambda = h_p + h_g + s_{\text{pv-grid}}$, is greater than 10, which is often the case for concentric windings [123]. However, in this study, since the PV and grid-side windings are placed side by side, the ratio is less than 1, making the expression in (6.79) inaccurate. To correct this, a correction factor proposed by Dr. Rogowski [123] is multiplied to improve the leakage inductance estimate. The correction factor is given as

$$\begin{aligned} K_r = 1 - \frac{1-e^{-2\pi b_{\text{core}}/\lambda}}{2\pi b_{\text{core}}/\lambda}\Bigg[1 - \frac{e^{-4\pi d/\lambda}}{2}\left(1-e^{-2\pi b_{\text{core}}/\lambda}\right) \\ \left\{\frac{\text{MLT}_{\text{avg}} - \text{MLT}_{\text{fe}}}{\text{MLT}_{\text{avg}}} + \frac{\text{MLT}_{\text{fe}}}{\text{MLT}_{\text{avg}}}\left(1+e^{-2\pi(d'-d)/\lambda}\right)\right\} - \frac{\text{MLT}_{\text{fe}}}{\text{MLT}_{\text{avg}}}e^{-2\pi(b_{\text{core}}+2d+2d')/\lambda}\Bigg], \end{aligned} \tag{6.80}$$

where MLT_{fe} refers to the portion of the MLT that is enclosed by ferrite on both sides (inside the UU core geometry), while d and d' denote the distances from the ferrite to the windings

on the two sides. The corrected leakage inductance is then given by $L_{lk\text{-pv-grid-corrected}} = K_r\, L_{lk\text{-pv-grid}}$. Using (6.79) and (6.80), the spacing between the PV and grid-side windings, $s_{\text{pv-grid}}$, required to achieve the desired leakage inductance can now be accurately calculated.

The three-winding transformer is initially modeled using ANSYS MAXWELL, as illustrated in Figs. 6.20(a), 6.20(b), and 6.20(c), and subsequently fabricated for hardware implementation, as shown in Fig. 6.20(d). Bobbin and Nomex sheets are used to adjust the spacing between the windings to achieve the desired leakage inductance. All parameters associated with the fabricated transformer are summarized in Table 6.3. The coupling coefficient and inductance matrices obtained from the 3D FEA simulations and experimental measurements exhibit close agreement, as presented below:

$$k_{\text{FEA}} = \left[\begin{array}{c|ccc} & \text{PV} & \text{Grid} & \text{EV} \\ \hline \text{PV} & 1 & 0.9920 & 0.9880 \\ \text{Grid} & 0.9920 & 1 & 0.9880 \\ \text{EV} & 0.9880 & 0.9880 & 1 \end{array}\right],$$

$$L_{\text{FEA}} = \left[\begin{array}{c|ccc} & \text{PV} & \text{Grid} & \text{EV} \\ \hline \text{PV} & 1.5518 & 1.9259 & 1.2760 \\ \text{Grid} & 1.9259 & 2.4288 & 1.5963 \\ \text{EV} & 1.2760 & 1.5963 & 1.0748 \end{array}\right] \text{(in mH)},$$

$$k_{\text{measured}} = \left[\begin{array}{c|ccc} & \text{PV} & \text{Grid} & \text{EV} \\ \hline \text{PV} & 1 & 0.9919 & 0.9874 \\ \text{Grid} & 0.9919 & 1 & 0.9874 \\ \text{EV} & 0.9874 & 0.9874 & 1 \end{array}\right],$$

$$L_{\text{measured}} = \left[\begin{array}{c|ccc} & \text{PV} & \text{Grid} & \text{EV} \\ \hline \text{PV} & 1.5476 & 1.9201 & 1.2721 \\ \text{Grid} & 1.9201 & 2.4211 & 1.5911 \\ \text{EV} & 1.2721 & 1.5911 & 1.0725 \end{array}\right] \text{(in mH)},$$

where k_{FEA} and L_{FEA} represent the coupling coefficient and inductance matrices derived

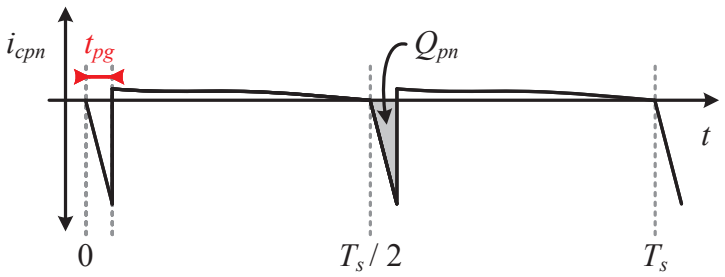


Fig. 6.22: Current waveform through the capacitor C_{pn} under the condition where the grid port receives the rated power P_{rated}. The grey-shaded area represents the value of Q_{pn}.

from FEA simulations, respectively, and k_{measured} and L_{measured} correspond to the coupling coefficient and inductance matrices obtained from experimental measurements of the fabricated three-winding transformer.

6.7 Selection of DC-link Capacitors

6.7.1 C_{po}, C_{on}, and C_{pn}

The dc-link capacitors on the grid-side are designed based on the allowable HF voltage ripple in the dc-link voltages. In the unfolding-based topology, the capacitors C_{po}, C_{on}, and C_{pn} are selected to be equal to form a balanced Δ-connected configuration [12]. Accordingly, C_{pn}, placed on the dc-link of the grid-side H-bridge, is first determined, and its value is then assigned to C_{po} and C_{on}. Now, to ensure that the peak-to-peak HF voltage ripple across C_{pn} remains within the maximum permissible limit of $\Delta V_{pn\text{-max}}$, the required capacitance can be derived using

$$C_{pn} = \frac{Q_{pn}}{\Delta V_{pn\text{-max}}}, \tag{6.81}$$

where Q_{pn} is obtained from the analytical current expressions derived in Section 6.4.2 and is illustrated in Fig. 6.22 as the grey-shaded area. This figure depicts the current waveform through the capacitor C_{pn} under the condition when the grid-port receives the rated power P_{rated}, resulting in the maximum HF voltage ripple in the dc-link voltage v_{pn}.

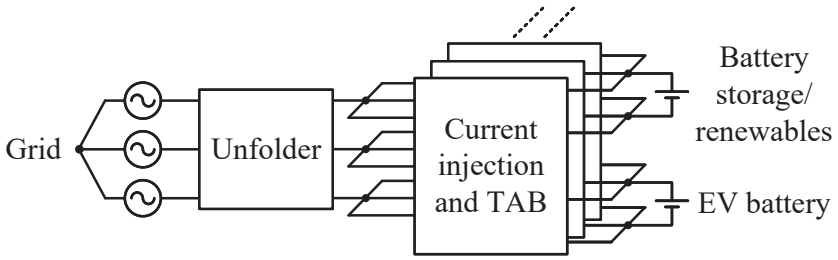


Fig. 6.23: Modular IPOP-based configuration of the proposed multiport topology, showing paralleled TAB-based dc-dc converter modules with individual current injection circuits connected to a single grid-tied Unfolder.

6.7.2 C_{pv} and C_{ev}

Similar to the grid-side dc-link capacitors, the dc-link capacitors on the PV and EV sides are also dimensioned based on the permissible HF voltage ripple in their respective dc-link voltages. Accordingly, the required capacitance values on the PV and EV sides can be determined as

$$C_{\text{pv}} = \frac{P_{\text{rated}}}{\omega_s V_{\text{pv}} \Delta V_{\text{pv-max}}}, \tag{6.82}$$

$$C_{\text{ev}} = \frac{P_{\text{rated}}}{\omega_s V_{\text{ev}} \Delta V_{\text{ev-max}}}, \tag{6.83}$$

where $\Delta V_{\text{pv-max}}$ and $\Delta V_{\text{ev-max}}$ denote the maximum allowable peak-to-peak HF voltage ripples across the dc-link capacitors C_{pv} and C_{ev}, respectively.

6.8 Scalability of the Proposed Topology

A modular approach has been proposed in this study to demonstrate the scalability of the multiport topology. In this approach, the inputs and outputs of the TAB-based dc-dc converter modules are paralleled to form an IPOP configuration. Each module includes its own current injection circuit, while the paralleled system connects to a single grid-tied Unfolder. The architecture of this scalable approach is shown in Fig. 6.23. As discussed in Section 6.3, the Unfolder mainly contributes to conduction losses with negligible switching losses. Leveraging this advantage, a single high-power Unfolder interfaced with multiple parallel-connected dc-dc modules is proposed to minimize the number of semiconductor de-

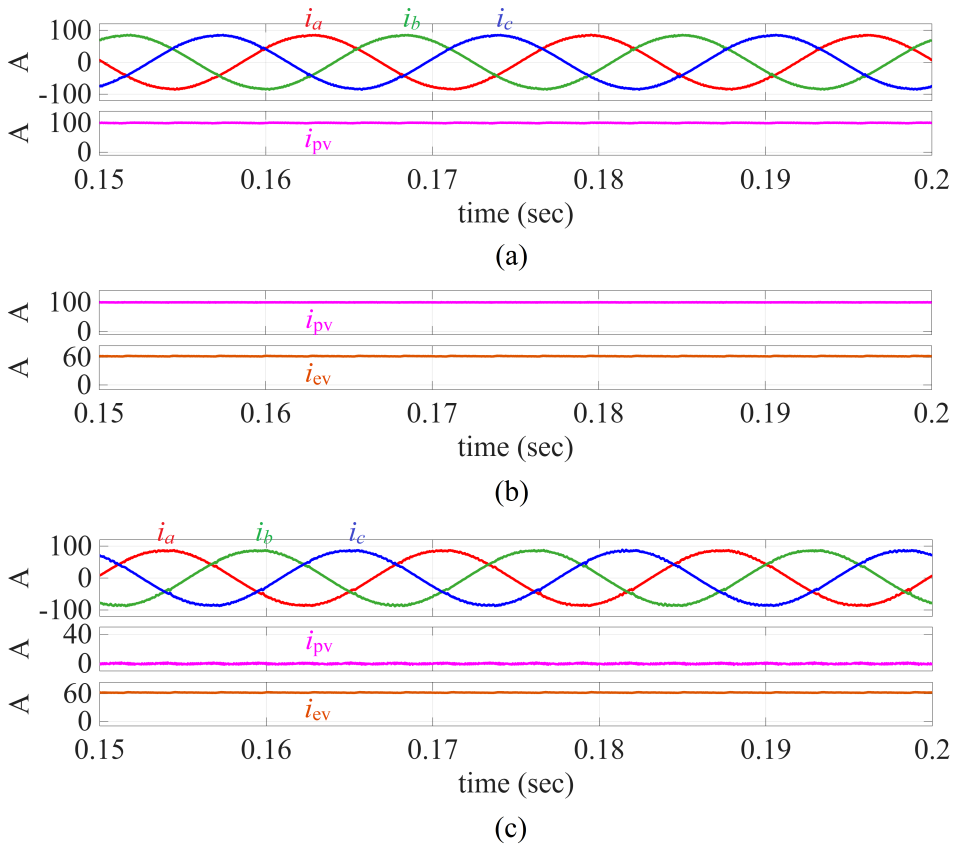


Fig. 6.24: To evaluate the scalability of the proposed multiport topology, simulations are carried out with ten paralleled dc-dc modules connected to a single grid-tied Unfolder, corresponding to a total power of 50 kW. The simulation results for the grid currents, PV bus current, and EV battery current are shown for: (a) the 500 V PV dc bus supplying 50 kW to the grid with no EV battery connected; (b) the PV dc bus delivering 50 kW to the 800 V EV battery load with no power supplied to the grid; and (c) the PV dc bus unavailable, with the grid supplying the entire 50 kW required by the 800 V EV battery load.

vices associated with the Unfolder and reduce conduction losses by employing high-current, low-resistance semiconductor devices.

Moreover, paralleling the dc-dc modules facilitates several key advantages. It allows for straightforward power scaling to meet higher load demands, enhances system reliability through redundancy, simplifies maintenance by enabling module-level replacement or upgrades, and provides flexibility to integrate additional energy sources or EV battery loads without significant redesign of the individual modules. This modular IPOP approach also enables incremental capacity expansion and supports the efficient distribution of power

among modules, making it particularly suitable for scalable EV charging infrastructure.

To evaluate the scalability of the proposed multiport topology, simulations are performed with ten paralleled dc-dc modules and a single grid-tied Unfolder, corresponding to a total power of 50 kW. Simulation results are shown in Figs. 6.24(a), 6.24(b), and 6.24(c) for the following cases: (i) the 500 V PV dc bus supplies a total of 50 kW to the grid, with no EV battery connected; (ii) the 50 kW output from the PV dc bus is delivered to the 800 V EV battery load, with no power supplied to the grid; and (iii) the PV dc bus cannot supply power, and the grid provides the entire 50 kW required by the 800 V EV battery load. The simulation results demonstrate stable system operation at high-power levels with high-quality grid currents when the grid receives or supplies power. The results also demonstrate stable multidirectional power flow and reliable power delivery to the high-power EV battery load. Moreover, a single dc-dc module can be designed for higher power ratings based on the design details provided in this chapter, reducing the number of modules required in parallel for scalability.

6.9 Experimental Validation

Experimental validation is carried out using a 5 kW ac-dc hardware prototype consisting of a grid-tied Unfolder, a current injection circuit, and a TAB-based dc-dc converter, as shown in Fig. 6.25. The corresponding hardware parameters are provided in Table 6.4. The California Instruments MX-30 emulates the grid, a Regatron dc power supply emulates the dc-link voltage at the PV port, and an NH Research 9300 system emulates the EV battery load. The Texas Instruments TMS320F28379D microcontroller is used to control the hardware. Moreover, the scalability of the proposed topology, discussed in Section 6.8, is validated in hardware at the 10 kW power level by paralleling the inputs and outputs (IPOP configuration) of two 5 kW TAB-based dc-dc converter modules, each equipped with its own current injection circuit. The paralleled system connects to a single 10 kW grid-tied Unfolder. The stacked PCBs for paralleling are shown in Fig. 6.26.

To begin with, the pulsating dc-link voltages v_{po}, v_{on}, and v_{pn} are observed at the output of the Unfolder, as shown in Fig. 6.27. The effect of the pulsating nature of v_{pn} is

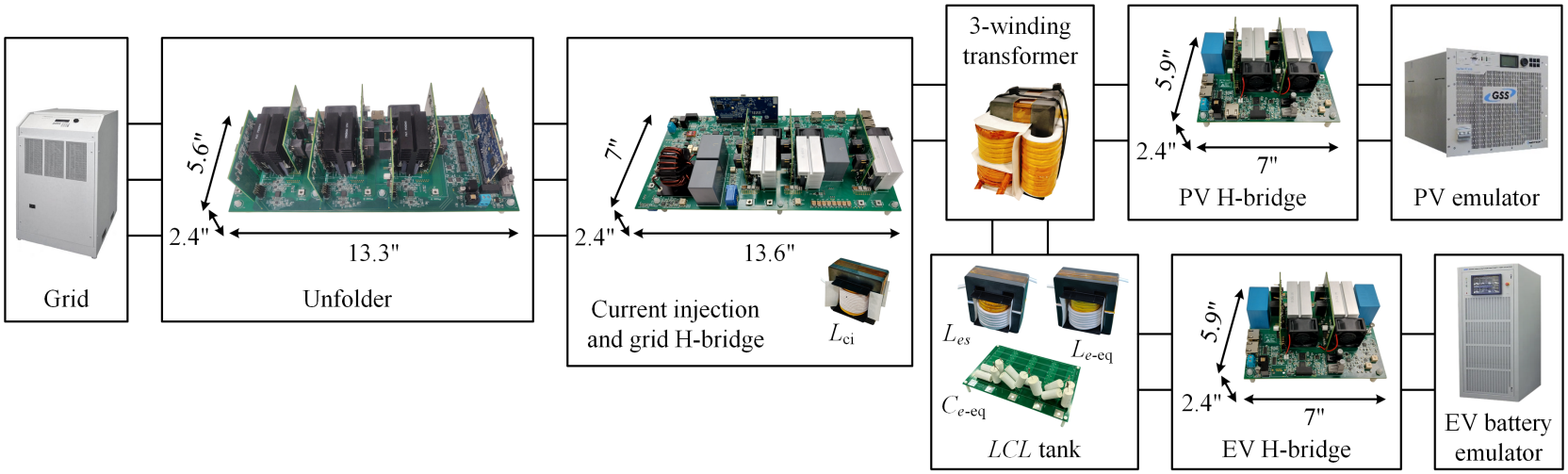
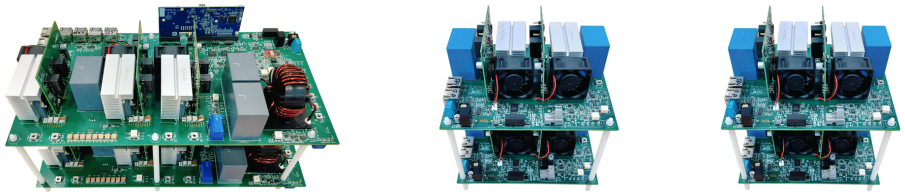


Fig. 6.25: A 5 kW hardware setup of the proposed multiport system, consisting of an Unfolder, a current injection circuit, a TAB, a three-winding transformer, and an LCL tank, for integrating battery storage/renewables with the grid for EV battery charging.



(a) (b) (c)

Fig. 6.26: To validate the scalability of the proposed multiport topology at 10 kW, two 5 kW TAB-based dc-dc converter modules are paralleled, each including an individual current injection circuit. The paralleled dc-dc system connects to a single grid-tied 10 kW Unfolder. The figure shows the stacked PCBs for paralleling: (a) individual current injection circuit and grid-side H-bridges, (b) PV-side H-bridges, and (c) EV-side H-bridges.

Table 6.4: Hardware parameters of the multiport system.

Parameter	**Value**
Grid voltage	480 V (l-l), 60 Hz ac 3-ϕ
PV-side dc-link voltage	500 V
EV-side dc-link voltage	200 V - 800 V (0 V when battery disconnected)
Unfolder MOSFETs	NTH4L014N120M3P (1200 V, 14 mΩ)
Current injection half-bridge and TAB MOSFETs	NTH4L022N120M3S (1200 V, 22 mΩ)
Unfolder switching frequency	60 Hz (top and bottom MOSFETs), 120 Hz (common-source MOSFETs)
Current injection half-bridge switching frequency	100 kHz
TAB switching frequency	100 kHz
L_{grid}	100 μH (MX-30)
C_{po}, C_{on}, and C_{pn}	1.8 μF
L_{ci}	750 μH
LCL tank: $(L_{lke} + L_{es})$, $L_{e\text{-eq}}$, and $C_{e\text{-eq}}$	75.67 μH, 79.61 μH, and 31.98 nF
C_{pv} and C_{ev}	24 μF

evident in the tank waveforms shown in Fig. 6.28, corresponding to the case when the grid receives all the power from the PV port and the EV battery is not connected. The voltage at the output of the grid-side H-bridge, v_{xyg}, exhibits a six-pulse waveform, as the H-bridge connects to the pulsating dc-link voltage v_{pn}. This pulsating nature of the tank voltage

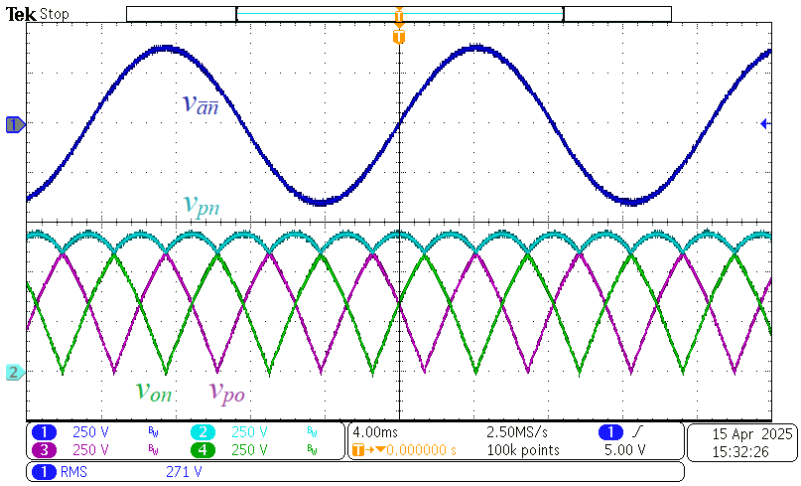


Fig. 6.27: Pulsating dc-link voltages v_{po}, v_{on}, and v_{pn} at the output of the Unfolder. The grid-side H-bridge connects to the dc-link voltage v_{pn}.

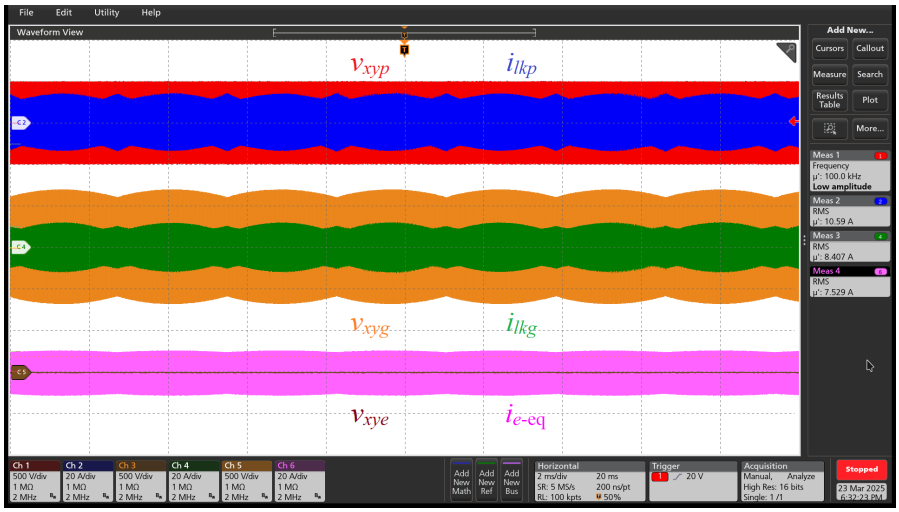


Fig. 6.28: Tank voltages and currents for the case when the grid receives all the power from the PV port and the EV battery is not connected. The pulsating dc-link voltage v_{pn} results in pulsating tank currents.

on the grid side leads to pulsating tank currents, as illustrated in the figure. To maintain power flow at different ports despite the pulsating nature of the grid-side dc-link voltage and the corresponding pulsating tank currents, the phase shifts ϕ_{pg} and $(\pi - \phi_{pe})$ are also varied throughout the grid cycle by the high-bandwidth closed-loop controls, as discussed earlier in Section 6.5.

Hardware verification is performed under two operating scenarios. In the first scenario,

the PV port delivers 5 kW of power. In the second, the PV port cannot supply sufficient power to the EV battery, so the grid provides the deficit. The efficiency and THD results are presented following the discussion of these two scenarios, with the subsequent transient responses validating the robustness of the designed closed-loop control architecture. Finally, the scalability of the proposed topology is demonstrated at the 10 kW power level.

6.9.1 Operation with PV Port Supplying 5 kW

In this experimental scenario, the PV port delivers 5 kW of power, while the EV port receives between 0 and 5 kW. If the EV port requires less than 5 kW, the remaining power is delivered to the grid. Figs. 6.29 and 6.30 show the experimental results, including the phase-a Unfolder input voltage, phase-a grid current, injection current, one of the pulsating dc-link voltages, PV and EV battery voltages and currents, and tank waveforms. Figs. 6.29(a), 6.29(b), and 6.29(c) correspond to the case where the PV port delivers the full 5 kW of power to the grid, with the EV battery disconnected. In the subsequent cases, an EV battery is connected at voltage levels of 200 V (Figs. 6.29(d)–6.29(f)), 400 V (Figs. 6.30(a)–6.30(c)), and 800 V (Figs. 6.30(d)–6.30(f)). Since the LCL tank on the EV HF side behaves as a current source, the power delivered to the EV port increases with the battery voltage: 1.25 kW at 200 V, 2.5 kW at 400 V, and 5 kW when an 800 V battery is connected. It should also be noted that the EV current, i_{ev}, can be adjusted by modifying the current reference, $i_{\text{ev-ref}}$, in the closed-loop control to achieve different current and corresponding power levels at a given battery voltage. As more power is supplied to the EV port, the grid current correspondingly decreases, indicating reduced power delivered to the grid, as shown in Figs. 6.29(a), 6.29(d), 6.30(a), and 6.30(d). The tank waveforms shown in Figs. 6.29(c), 6.29(f), 6.30(c), and 6.30(f) are captured using the envelope (persistent) mode of the Tektronix 4 Series oscilloscope [124], which accumulates waveform data over time to enable the observation of variations induced by the pulsating dc-link voltage, v_{pn}. The waveforms show that the tank currents maintain appropriate polarity and sufficient magnitude during the voltage transitions of all H-bridges in the TAB, thereby ensuring ZVS of the MOSFETs under all operating conditions.

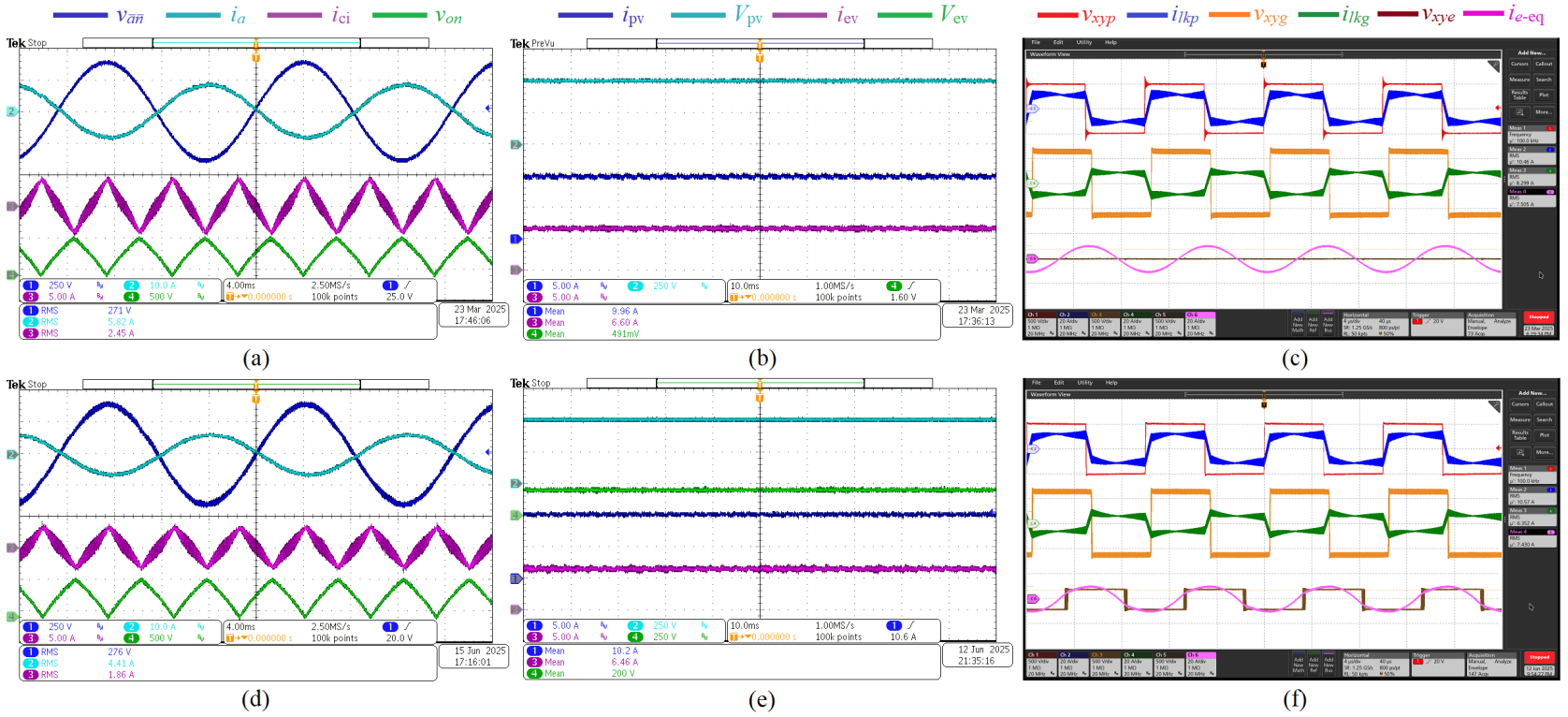


Fig. 6.29: Experimental results for the case where the PV port supplies 5 kW of power, and the EV port receives between 0 and 5 kW. If the EV port receives less than 5 kW, the remaining power is delivered to the grid. The PV port supplies 5 kW to the grid when the EV battery is not connected: (a) grid-side and Unfolder output waveforms, (b) dc-side waveforms, and (c) tank waveforms. When a 200 V EV battery is connected and the EV port receives 1.25 kW: (d) grid-side and Unfolder output waveforms, (e) dc-side waveforms, and (f) tank waveforms. Tank waveforms are captured using the envelope (persistence) mode of a Tektronix 4 Series oscilloscope to observe variations over the grid cycle.

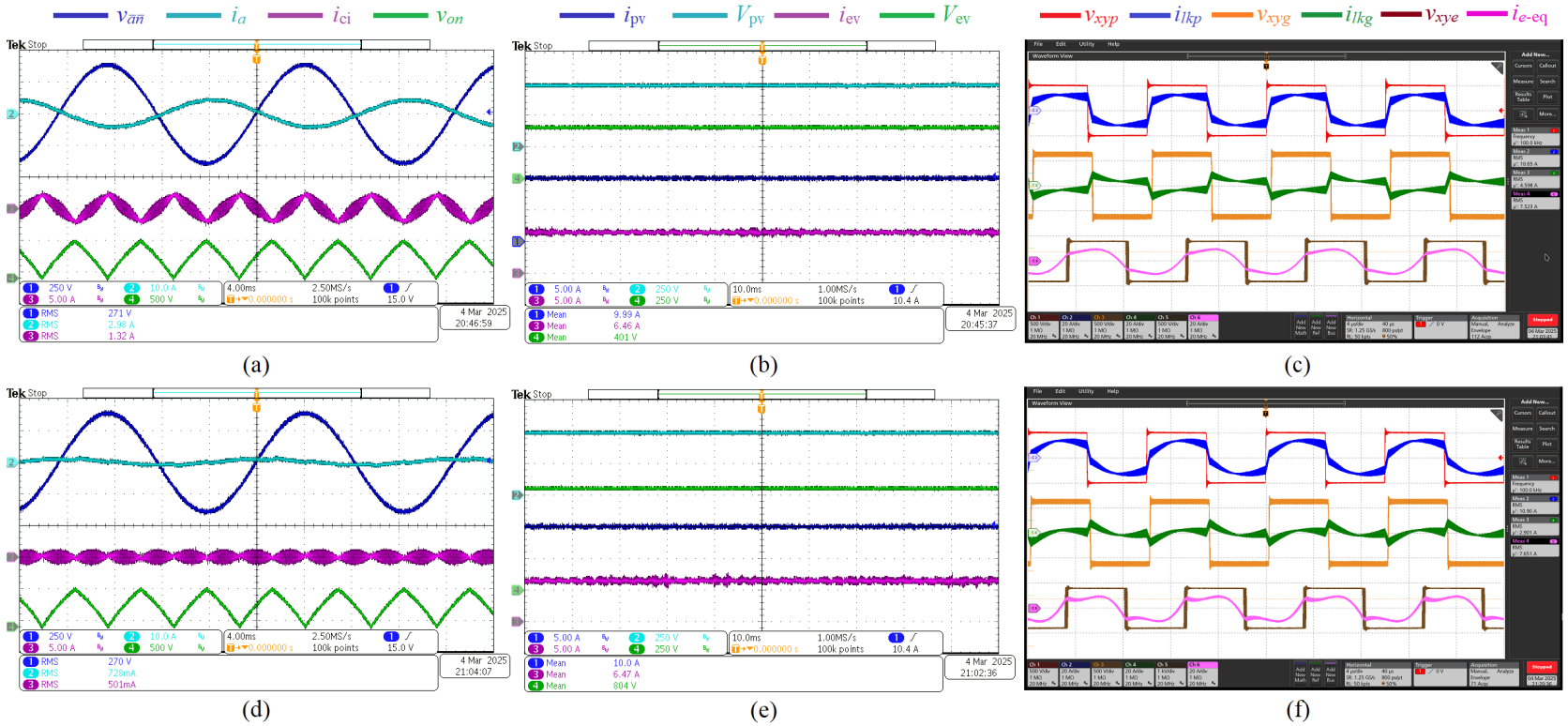


Fig. 6.30: Experimental results for the case where the PV port supplies 5 kW of power, and the EV port receives between 0 and 5 kW. If the EV port receives less than 5 kW, the remaining power is delivered to the grid. When a 400 V EV battery is connected and the EV port receives 2.5 kW: (a) grid-side and Unfolder output waveforms, (b) dc-side waveforms, and (c) tank waveforms. When an 800 V EV battery is connected and the EV port receives 5 kW: (d) grid-side and Unfolder output waveforms, (e) dc-side waveforms, and (f) tank waveforms. Tank waveforms are captured using the envelope (persistence) mode of a Tektronix 4 Series oscilloscope to observe variations over the grid cycle.

6.9.2 Operation with PV Port Supplying Less Than 5 kW

In this experimental scenario, the PV port cannot supply the full 5 kW required by the EV battery, so the grid provides the deficit. To implement this condition in hardware, the PV port current, i_{pv}, is reduced to 25% of its rated value and then to 0 A by adjusting the current reference, $i_{\text{pv-ref}}$. As the PV current decreases, the power delivered from the PV port is reduced, and the grid supplies the remaining power required by the EV battery. Fig. 6.31 shows the experimental results, including the phase-a Unfolder input voltage, phase-a grid current, injection current, one of the pulsating dc-link voltages, PV and EV battery voltages and currents, and tank waveforms. Figs. 6.31(a), 6.31(b), and 6.31(c) correspond to the case where the PV port supplies 1.25 kW of power, while the EV port requires 5 kW as it connects to an 800 V battery and i_{ev} is maintained at its full rated value. The deficit of 3.75 kW, along with system losses, is supplied by the grid. Figs. 6.31(d), 6.31(e), and 6.31(f) show the case where the PV port supplies no power and all the required power is provided by the grid. From the tank waveforms in Figs. 6.31(c) and 6.31(f), it can also be observed that the H-bridges of the TAB achieve ZVS due to the appropriate polarity and magnitude of the tank currents during switching transitions.

6.9.3 Efficiency and THD Measurements

Efficiency and THD measurements of the proposed multiport system are performed using the Yokogawa WT1806E power analyzer. The formula used to calculate efficiency is given as:

$$\text{Efficiency} = \frac{\Sigma P_{\text{received}}}{\Sigma P_{\text{supplied}}} \times 100\,, \tag{6.84}$$

where $\Sigma P_{\text{received}}$ denotes the total power received by the ports, and $\Sigma P_{\text{supplied}}$ denotes the total power supplied by the ports. When the PV port delivers the full rated power of 5 kW, $\Sigma P_{\text{supplied}}$ corresponds to the PV port power, while $\Sigma P_{\text{received}}$ is the sum of the power received by the EV port and the grid. Conversely, when the PV port cannot supply the full rated power and the grid compensates for the deficit, $\Sigma P_{\text{supplied}}$ is the sum of the powers

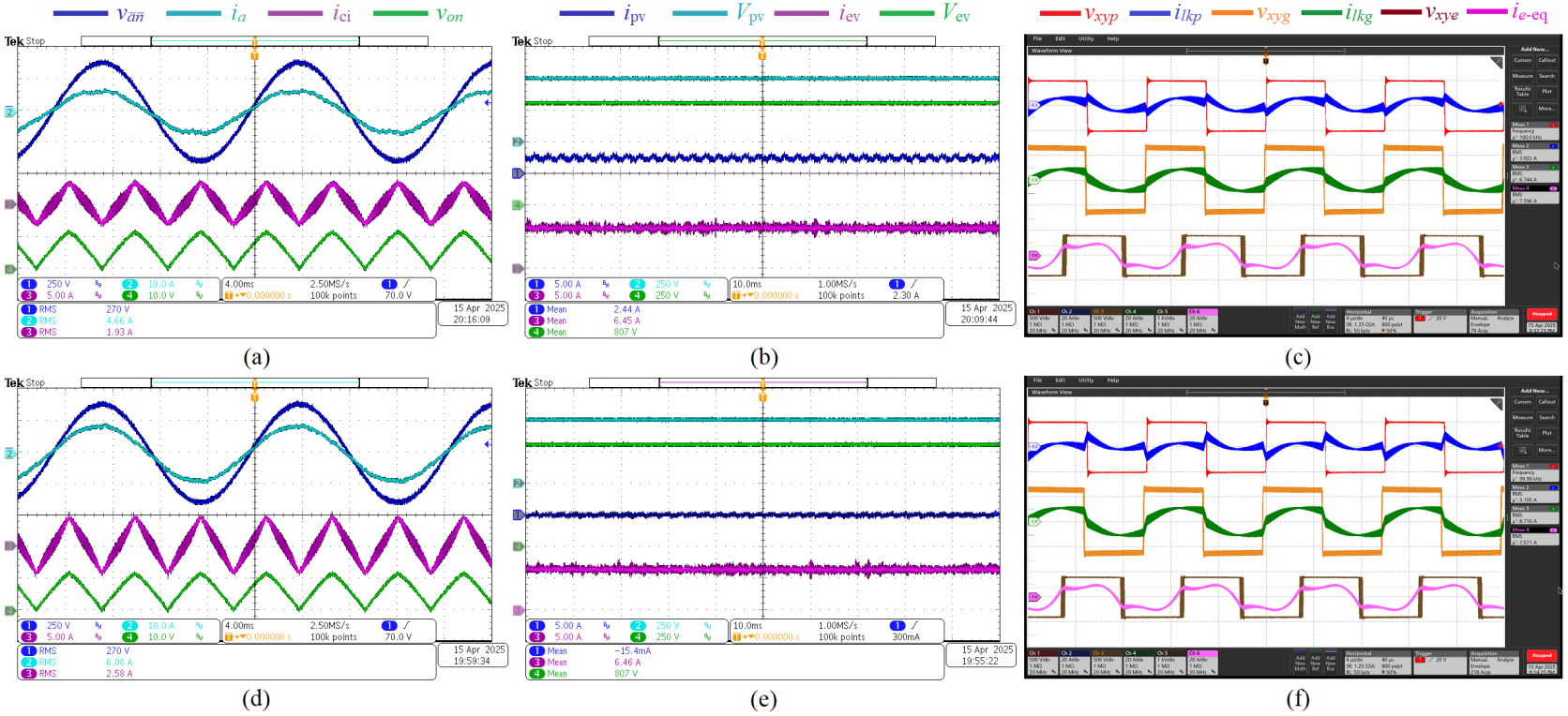


Fig. 6.31: Experimental results for the case where the PV port cannot supply the full 5 kW required by the EV battery, and the grid provides the deficit. The PV port supplies 1.25 kW, and the grid supplies the remaining power required by the EV battery: (a) grid-side and Unfolder output waveforms, (b) dc-side waveforms, and (c) tank waveforms. In the second case, the PV port supplies no power as the PV current drops to 0 A, and the grid supplies the full power to the EV battery: (d) grid-side and Unfolder output waveforms, (e) dc-side waveforms, and (f) tank waveforms.

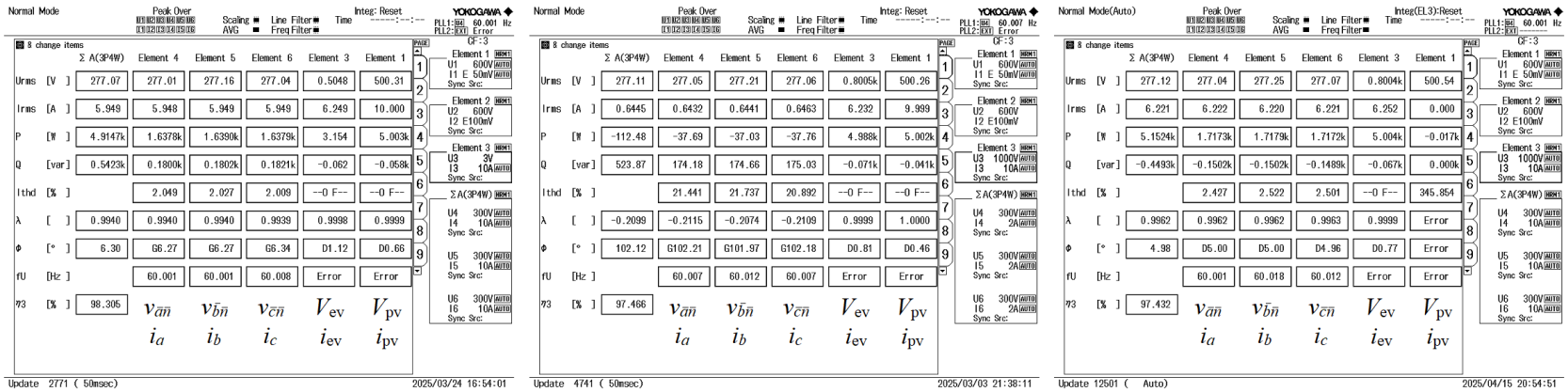


Fig. 6.32: Power analyzer data measured using the Yokogawa WT1806E for the following cases: (a) the PV port supplies all the power to the grid, achieving a peak system efficiency of 98.3% and a grid current THD of 2% at this operating point; (b) the PV port supplies all the power to the EV port with an 800 V battery; and (c) the PV port supplies no power, and the grid provides all the power to the EV port with an 800 V battery.

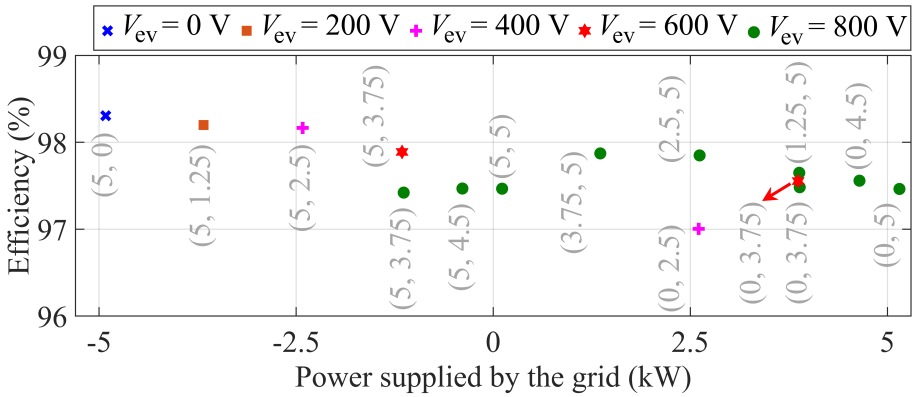


Fig. 6.33: Efficiency of the proposed multiport system for different values of grid-supplied power. Efficiency is also shown for the case when the battery is disconnected, resulting in 0 V across the EV-side H-bridge dc-link. The power supplied by the PV port and received by the EV port, represented as (X, Y) kW, is also provided. A peak ac-dc efficiency of 98.3% is achieved, with efficiency maintained above 97% across various operating conditions, power flow directions, and a battery voltage range of 200–800 V.

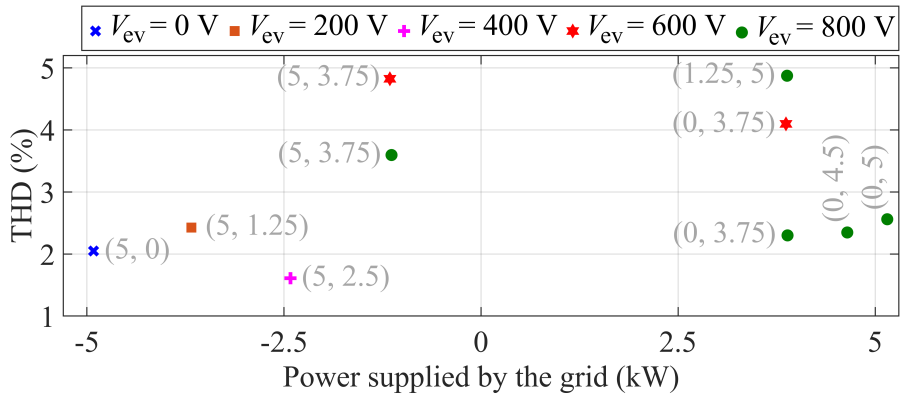


Fig. 6.34: THD of the grid current in the proposed multiport system for different values of grid-supplied power and various battery voltages. THD values for cases with low grid power are disregarded due to the negligible fundamental component of the grid current in these scenarios. The power supplied by the PV port and received by the EV port, represented as (X, Y) kW, is also provided.

from the PV port and the grid, and $\Sigma P_{\text{received}}$ is the power delivered to the EV port.

The measurements obtained from the power analyzer are presented in Fig. 6.32 for three operating points: (i) the PV port supplies all the power to the grid, achieving a peak system efficiency of 98.3% and a grid current THD of 2%; (ii) the PV port supplies all the power to the EV port with an 800 V battery, achieving an efficiency of 97.47%; and (iii) the PV port supplies no power, and the grid provides all the power to the EV port with an

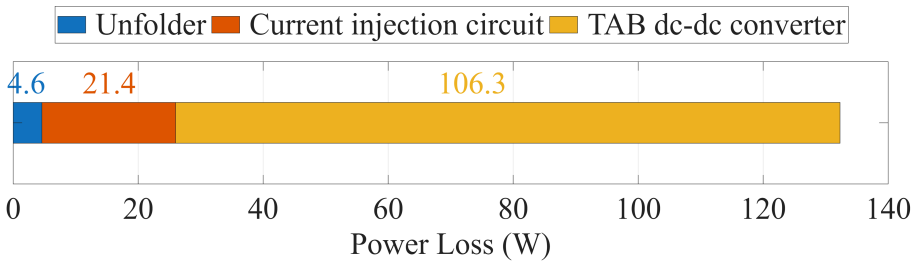


Fig. 6.35: Power loss distribution among the Unfolder, current injection circuit, and TAB-based dc-dc converter of the multiport system when supplying rated power from the grid to an 800 V EV battery load.

800 V battery, achieving an efficiency of 97.43%. The efficiency and THD measurements for all the operating points tested in hardware are presented in Figs. 6.33 and 6.34. Efficiency is maintained above 97% across various operating conditions, power flow directions, and a battery voltage range of 200–800 V. Finally, Fig. 6.35 shows the power loss distribution among the subsystems of the multiport topology when supplying rated power from the grid to an 800 V EV battery load.

6.9.4 Transient Responses

To demonstrate the robustness of the proposed closed-loop control architecture, transient hardware responses are presented for various scenarios. Fig. 6.36(a) shows the step response of the battery load current, i_{ev}, from 4.69 A to 6.25 A. With the 800 V battery load connected, the EV port power increases dynamically from 75% of the system rated power (3.75 kW) to 100% rated power (5 kW). In Fig. 6.36(b), the grid-side voltages are subjected to a 10% step change from 277 V to 250 V. During this grid voltage sag, the closed-loop control appropriately maintains the grid, PV, and EV currents. Fig. 6.37(a) shows the step response of the PV current, i_{pv}, from 10 A to 0 A. In this case, the PV port becomes unavailable and cannot supply power to the 800 V EV battery load. The power flow direction shifts, and the grid provides the required 5 kW power to the battery load. Finally, Fig. 6.37(b) shows the response to a PV bus voltage deviation from 500 V to 470 V. The closed-loop control maintains the PV and EV currents during this voltage change. These results demonstrate that the proposed multiport system and its closed-loop

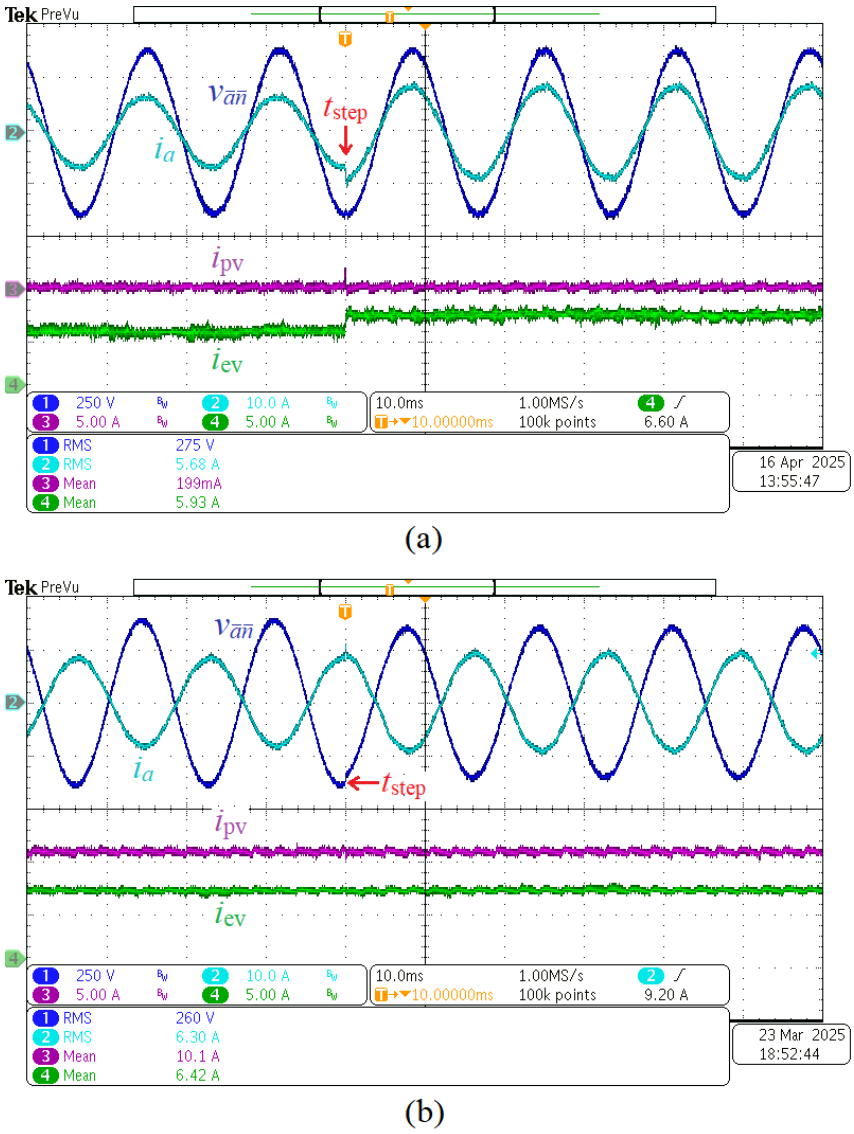


Fig. 6.36: (a) A step change is applied to the EV battery current, i_{ev}, from 4.69 A to 6.25 A. With the 800 V battery connected, the EV port power increases from 75% of the rated power (3.75 kW) to 100% rated power (5 kW). (b) A 10% step change is applied to the Unfolder input ac voltages, from 277 V to 250 V. The closed-loop control maintains the grid, PV, and EV currents during this grid voltage sag.

control respond effectively to transients and properly manage shifts in power flow direction.

6.9.5 TAB Validation

In addition to the ac-dc verification of the proposed multiport system, the design of the TAB-based dc-dc converter is further validated using a 5 kW hardware prototype. Hardware

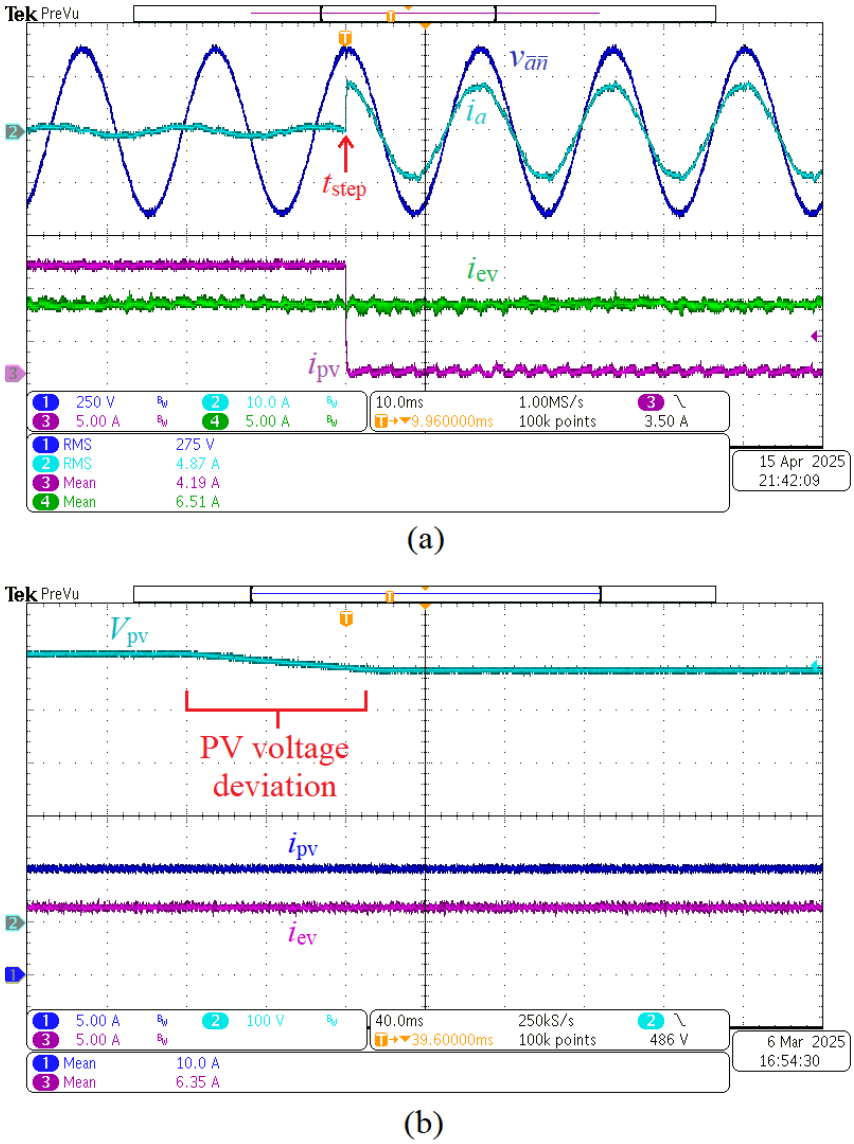


Fig. 6.37: (a) A step change in PV current, i_{pv}, from 10 A to 0 A shifts the power flow from the PV port supplying 5 kW to an 800 V EV battery, to the grid supplying 5 kW to the battery load. (b) A deviation in PV bus voltage, V_{pv}, from 500 V to 470 V is applied in hardware. The control maintains the PV and EV currents properly during this voltage change.

results are presented in Fig. 6.38 for two power flow scenarios. Figs. 6.38(a)–6.38(d) show the tank voltages, currents, and loss distribution of the dc-dc converter when an 800 V battery load is connected to the EV port. In this case, the full 5 kW is delivered from the PV port to the EV battery, with no power transferred to the grid port. A dc-dc converter

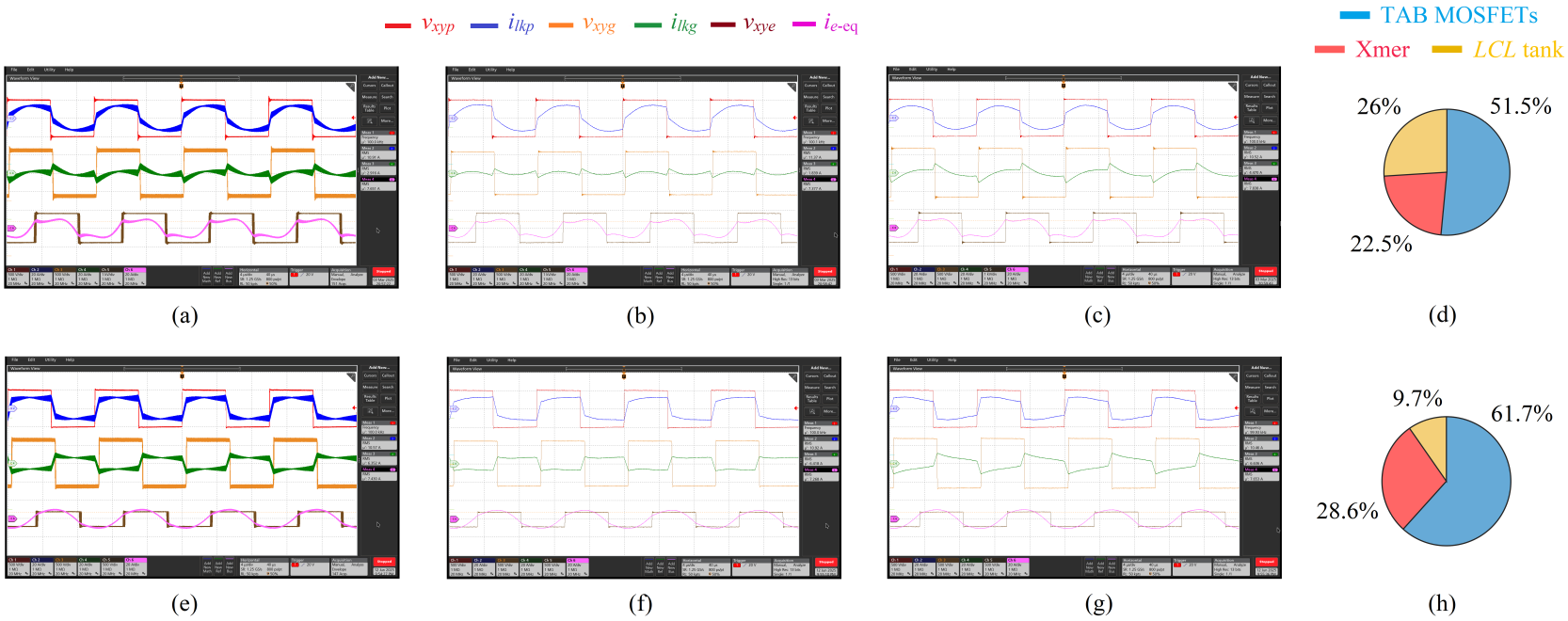


Fig. 6.38: Hardware results of the TAB-based dc-dc converter under two operating conditions: when an 800 V EV battery is connected and receives 5 kW from the PV port, with no power delivered to the grid port, (a) tank-voltage and tank-current waveforms, (b) waveforms measured at a 588 V grid-port dc-link voltage, (c) waveforms measured at a 679 V grid-port dc-link voltage, and (d) overall loss distribution of the dc-dc converter corresponding to a total loss of 97.5 W at an efficiency of 98.05%. When a 200 V EV battery is connected and receives 1.25 kW from the PV port while the remaining 3.75 kW is delivered to the grid port, (e) tank-voltage and tank-current waveforms, (f) waveforms measured at a 588 V grid-port dc-link voltage, (g) waveforms measured at a 679 V grid-port dc-link voltage, and (h) overall loss distribution of the dc-dc converter corresponding to a total loss of 74.5 W at an efficiency of 98.51%. Tank waveforms in (a) and (e) are captured using the envelope (persistence) mode of a Tektronix 4 Series oscilloscope to observe variations over the grid cycle due to the pulsating grid-port dc-link voltage.

efficiency of 98.05% (97.5 W power loss) is achieved in this scenario. Figs. 6.38(e)–6.38(h) show the tank waveforms and loss distribution when a 200 V EV battery is connected. Here, 1.25 kW is delivered to the EV battery, and the remaining 3.75 kW is supplied to the grid port. The dc-dc converter achieves an efficiency of 98.51% (74.5 W power loss) in this case. The waveforms in Figs. 6.38(a) and 6.38(e) are captured using the envelope (persistence) mode of a Tektronix 4 Series oscilloscope [124] to observe variations in tank waveforms over a grid cycle, caused by the pulsating dc-link voltage on the grid side. Figs. 6.38(b) and 6.38(f) show results when the grid-side dc-link voltage is 588 V, while Figs. 6.38(c) and 6.38(g) correspond to the dc-link voltage of 679 V.

Moreover, the validity of the analytical derivations presented in Section 6.4.3 of the chapter is verified using the state-plane plots shown in Fig. 6.39. Figs. 6.39(a)–6.39(c) correspond to the PV-side, grid-side, and EV-side H-bridges, representing transitions I, II, and III, respectively. The analytically obtained state-plane trajectories are compared with the experimental state-plane trajectories for the case where an 800 V EV battery is connected and the grid-port dc-link voltage is 679 V. The close agreement between the analytical and experimental state planes confirms the accuracy of the derived expressions in Section 6.4.3 [(6.44), (6.45), (6.49), (6.50), (6.54), and (6.55)], which are used to determine the H-bridge voltages and tank currents during the switching transitions.

Finally, the ZVS behavior of the TAB MOSFETs for 800 V and 200 V EV battery voltages is verified in hardware, as shown in Fig. 6.40. Figs. 6.40(a) and 6.40(b) correspond to the 800 V battery voltage with grid-port dc-link voltages of 588 V and 679 V, respectively, while Figs. 6.40(c) and 6.40(d) correspond to the 200 V battery voltage with 588 V and 679 V grid-port dc-link voltages, respectively. In all cases, the tank-current polarities and magnitudes during the switching transitions are appropriate such that the H-bridge voltages transition from $-V$ to $+V$ before the gate pulses turn on, implying that the corresponding MOSFET drain-source voltages also transition accordingly. This indicates that the output capacitances C_{oss} charge/discharge during the dead time, thereby confirming ZVS operation for all tested conditions.

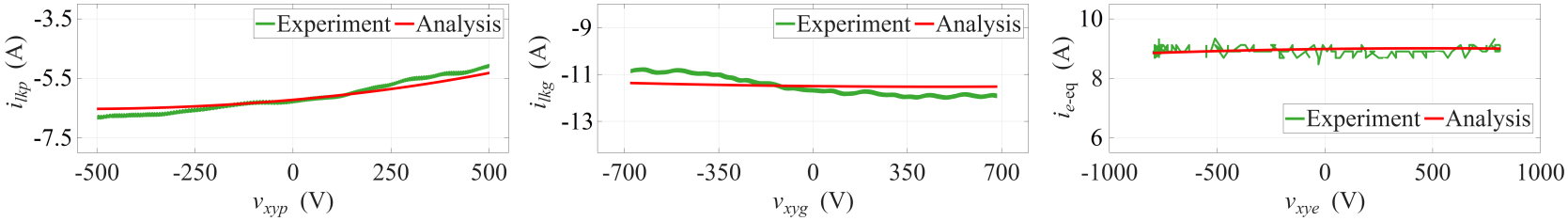


Fig. 6.39: State-plane diagrams for the three transitions discussed in Section 6.4.3 corresponding to (a) the PV-side H-bridge (transition I), (b) the grid-side H-bridge (transition II), and (c) the EV-side H-bridge (transition III). The analytically obtained state-plane diagrams are verified by comparison with experimental plots for the case where an 800 V EV battery is connected and the grid-port dc-link voltage is 679 V.

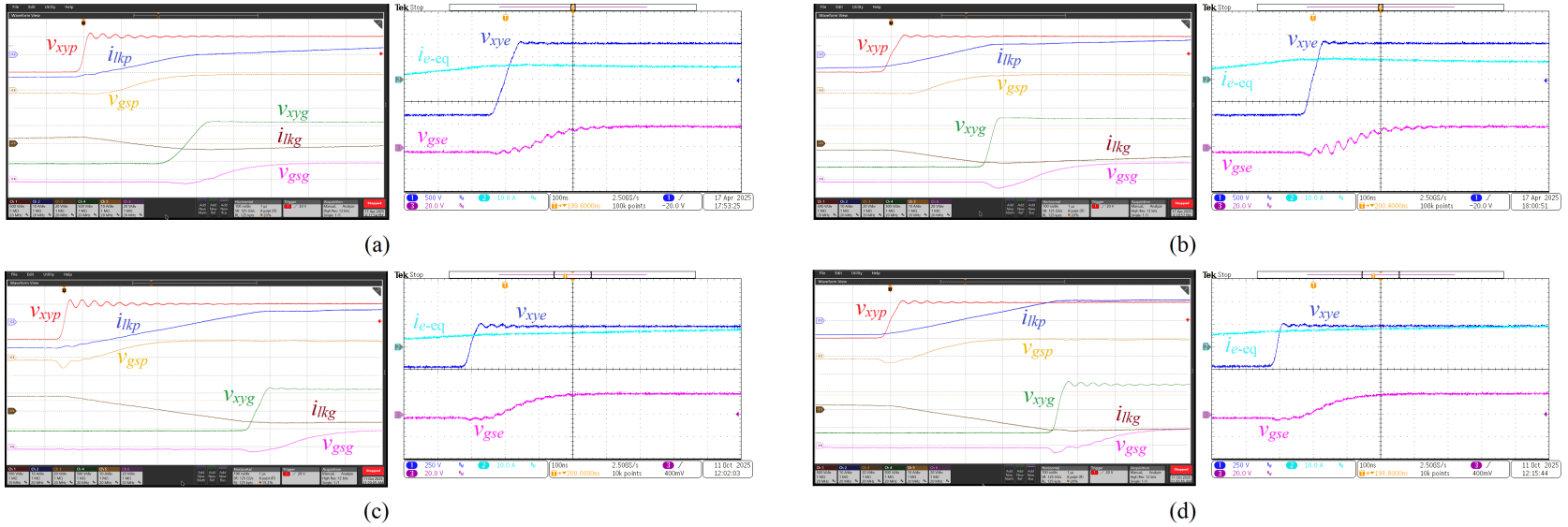


Fig. 6.40: ZVS verification of the TAB MOSFETs for 800 V and 200 V EV battery voltages. H-bridge voltages, tank currents, and gate-source voltages for (a) 800 V battery voltage and 588 V grid-port dc-link voltage, (b) 800 V battery voltage and 679 V grid-port dc-link voltage, (c) 200 V battery voltage and 588 V grid-port dc-link voltage, and (d) 200 V battery voltage and 679 V grid-port dc-link voltage. It can be observed in all cases that the tank-current polarities and magnitudes during the switching transitions are appropriate such that the H-bridge voltages transition from $-V$ to $+V$ before the gate pulses turn on, indicating that the MOSFET output capacitances C_{oss} charge/discharge during the dead time. This confirms ZVS operation for all tested conditions.

6.9.6 Scalability Verification at 10 kW

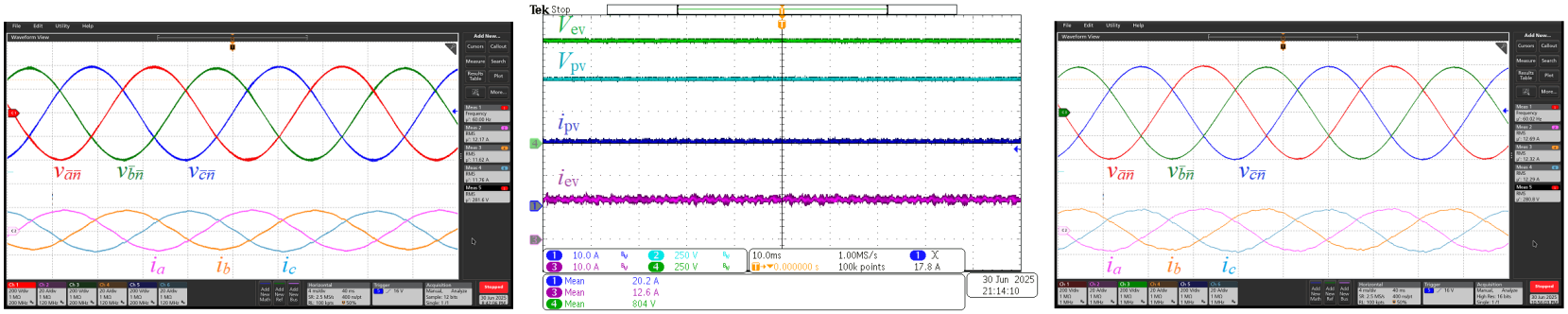
The scalability of the proposed multiport topology, discussed in Section 6.8, is validated in hardware at the 10 kW power level by paralleling the inputs and outputs (IPOP configuration) of two 5 kW TAB-based dc-dc converter modules, each equipped with its own current injection circuit. The paralleled system connects to a single 10 kW Unfolder, which either supplies power to or receives power from the grid. The hardware setup is illustrated in Figs. 6.25 and 6.26. In the first testing condition, Fig. 6.41(a) shows the grid-side voltages and currents when the 500 V PV dc bus supplies a total of 10 kW to the grid, with no EV battery connected. An overall conversion efficiency of 98.1% and a grid current THD of 2.2% are obtained, as shown in Fig. 6.42(a).

Following this, an 800 V battery load is connected to the paralleled EV dc ports. In this case, the 10 kW output from the PV dc bus is delivered to the battery load, as shown in Fig. 6.41(b), which presents the dc-side waveforms of the PV and EV ports. These waveforms show the PV dc bus supplying a total of 20 A and the EV battery load receiving 12.5 A. An overall efficiency of 97.4% is achieved, as shown in Fig. 6.42(b). In this scenario, the grid does not receive power, and all power is delivered to the EV battery load.

Finally, a scenario is tested in which the PV dc bus cannot supply power, and the grid provides the entire 10 kW required by the 800 V EV battery load. Fig. 6.41(c) shows the grid-side voltages and currents for this case. An efficiency of 97.1% and a grid current THD of 2.9% are achieved, as shown in Fig. 6.42(c). These hardware results demonstrate that the proposed multiport topology has the potential for scalability to support higher-power EV charging infrastructure, leveraging the IPOP modularity approach to distribute power efficiently, enhance system reliability through redundancy, improve thermal management by reducing stress on individual modules, and simplify maintenance. The modular design also facilitates seamless capacity expansion to meet future higher-power requirements.

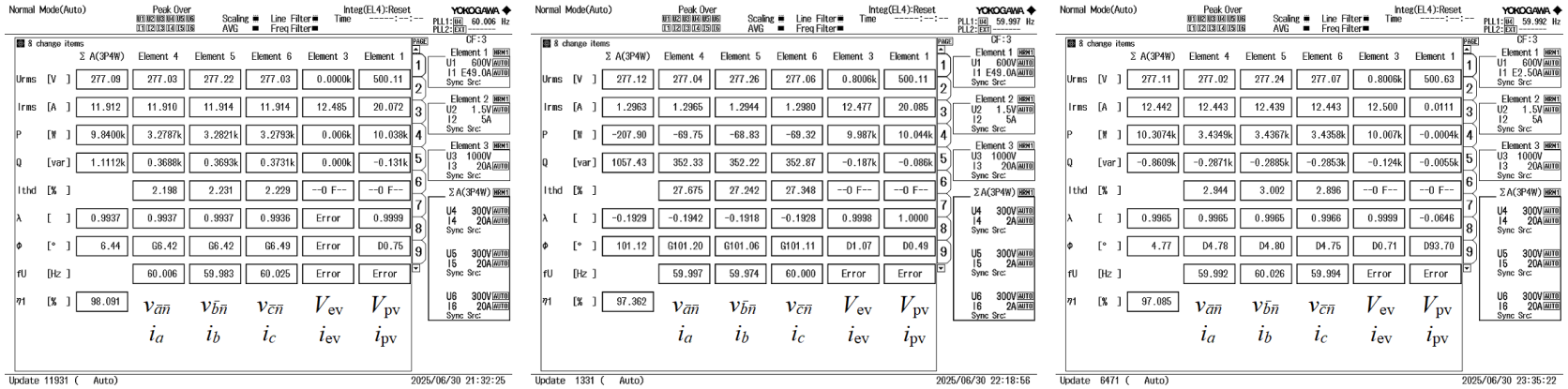
6.9.7 Summary of Experimental Results and Comparison with Prior Work

The summary of the experimental results of the proposed multiport system is provided in Table 6.5. Moreover, the performance of the proposed 3-ϕ grid-tied multiport converter



(a) (b) (c)

Fig. 6.41: Hardware verification of the scalability of the proposed multiport topology at 10 kW: (a) grid-side voltages and currents when the 500 V PV dc bus supplies a total of 10 kW to the grid, with no EV battery connected; (b) dc-side waveforms of the PV and EV ports when the 10 kW output from the PV dc bus is delivered to the 800 V EV battery load, with no power supplied to the grid; and (c) grid-side voltages and currents when the PV dc bus cannot supply power, and the grid provides the entire 10 kW required by the 800 V EV battery load.



(a) (b) (c)

Fig. 6.42: Power analyzer data measured using the Yokogawa WT1806E for the following cases: (a) the 500 V PV dc bus supplies a total of 10 kW to the grid, with no EV battery connected; (b) the 10 kW output from the PV dc bus is delivered to the 800 V EV battery load, with no power supplied to the grid; and (c) the PV dc bus cannot supply power, and the grid provides the entire 10 kW required by the 800 V EV battery load.

Table 6.5: Summary of experimental results: 5 kW ac-dc multiport hardware tests and 10 kW hardware scalability tests (grid voltages: 480 V (l-l); PV port voltage: 500 V).

EV battery voltage (V)	**Power supplied by PV port (kW)**	**Power supplied by grid (kW)**	**Power received by EV battery (kW)**	**Efficiency (%)**	**Grid current THD (%)**	**TAB ZVS**
5 kW ac-dc multiport hardware tests						
No EV battery	5.003	-4.915	-	98.305	2.049	Yes
200	5.014	-3.675	1.249	98.198	2.426	Yes
400	5.004	-2.417	2.495	98.165	1.611	Yes
800	5.002	0.112	4.988	97.466	-	Yes
800	1.242	3.882	5.004	97.649	4.873	Yes
800	0	5.152	5.004	97.432	2.427	Yes
10 kW hardware scalability tests						
No EV battery	10.038	-9.840	-	98.091	2.198	Yes
800	10.044	0.208	9.987	97.362	-	Yes
800	0	10.307	10.007	97.085	2.944	Yes

Table 6.6: Performance comparison of the proposed 3-ϕ grid-tied multiport converter with prior 3-ϕ grid-tied multiport converters.

Work	**Ports**	**Grid-side converter**	**No. of devices**	**No. of passives**	**Control complexity**	**Power**	**Efficiency (maximum)**	**Grid current THD**	**Battery voltage**
[37]	5 (1 ac and 4 dc, non isolated)	AFE (HF, hard-switched)	13	19	High	0.1 kW	96.83%	–	12 V
[38]	3 (1 ac and 2 dc, isolated)	Matrix (HF)	20	19	High	2 kW	93.5%	2.65%	200 V
[39]	3 (1 ac and 2 dc, non isolated)	AFE (HF, hard-switched)	16	22	High	3.7 kW	–	2.5%	240 V
[40]	3 (1 ac and 2 dc, isolated)	AFE (HF, hard-switched)	24	21	Moderate	10 kW	96.4%	2.95%	50–500 V
[41]	3 (1 ac and 2 dc, isolated)	Matrix (HF)	42	13	High	40 kW	92%	–	400 V
[42]	3 (1 ac and 2 dc, isolated)	Current source inverter (HF)	14	15	Moderate	3 kW	97% (theoretical)	–	125 V
[43]	4 (1 ac and 3 dc, partially isolated)	AFE (HF, hard-switched)	16	17	Moderate	2 kW	–	–	48 V
This work	**3 (1 ac and 2 dc, isolated)**	**Unfolder (low frequency, negligible switching losses)**	**26**	**13***	**Moderate**	**5 kW (scalability shown at 10 kW)**	**98.3%**	**2%**	**200–800 V**

– Data not reported in the respective work.

* Because of the low-frequency operation of the Unfolder, external grid-side inductors are not required, and the inherent grid inductance is sufficient to achieve PFC. The dc blocking capacitors used in the TAB-based dc-dc converter are included in the component count.

is compared with prior 3-ϕ grid-tied multiport converters in Table 6.6. It can be observed that the proposed system surpasses prior work in key parameters, achieving higher efficiency through a low-frequency-switched Unfolder and an optimized TAB tank, lower THD, and reliable operation over a wide EV battery voltage range of 200–800 V. In addition, the use of an Unfolder, which minimizes grid-side filtering requirements with grid inductance sufficient for PFC, together with the integrated three-winding transformer design, reduces the overall count of passive components in the system. The scalability of the proposed converter is also demonstrated through 50 kW simulation results and 10 kW hardware tests, supporting its potential for practical high-power EV charging infrastructure.

6.10 Conclusion

In conclusion, this chapter proposes a high-efficiency, 3-ϕ grid-tied ac-dc multiport system for integrating battery storage or renewable energy sources for EV battery charging. The utilization of a low-frequency grid-side converter and the optimized dc-dc converter design result in notable improvements in system efficiency compared to conventional approaches. The system employs an unfolding-based grid interface with a current injection circuit and an optimized TAB-based dc-dc converter to minimize conduction losses and ensure ZVS across a wide range of operating conditions. A three-winding transformer is used to integrate the H-bridges of the TAB, with the required tank inductance embedded into its leakage. An LCL resonant tank ensures compatibility with a wide range of EV battery voltages, with the transformer winding optimized to minimize the kVAr/kW ratio of the LCL tank across 200–800 V, thereby improving system efficiency. For the proposed tank circuit and dc-dc converter configuration, power flow analysis is presented along with the closed-loop control and corresponding small-signal model to enable effective power transfer between ports.

The proposed multiport system has been validated using a 5 kW, 480 V grid-tied hardware prototype. Experimental results demonstrate various power flow scenarios, including (i) the battery storage/renewables port supplying rated power to other ports, and (ii) the grid compensating when the battery storage/renewables port cannot meet the EV battery

load demand. The prototype achieves a peak ac-dc efficiency of 98.3%, maintains efficiency above 97% across various operating conditions, power flow directions, and a battery voltage range of 200–800 V, and exhibits a low grid current THD of 2%. In addition, a modular architecture is proposed to achieve power scalability of the multiport topology, employing IPOP dc-dc converter modules that interface with a single grid-tied Unfolder. Scalability is demonstrated through simulations at 50 kW and further validated in hardware at the 10 kW level, achieving a peak efficiency of 98.1%. The summary of the experimental results of the proposed 3-ϕ multiport system is provided in Table 6.5, and its performance is compared with prior 3-ϕ grid-tied multiport converters in Table 6.6.

Overall, the proposed system, as presented in this chapter and in the corresponding article [125], demonstrates higher efficiency, lower THD, reduced passive component count, and reliable wide-voltage operation compared to prior approaches. These results confirm the viability of the proposed architecture for future scalable, efficient, and compact EV charging infrastructure capable of integrating multiple energy sources.

CHAPTER 7

CONCLUSIONS

The global effort to reduce greenhouse gas emissions and dependence on fossil fuels identifies electric mobility as a central strategy for achieving a sustainable future. This transition increases the demand for advanced charging infrastructure and high-efficiency grid-tied ac-dc converters. Such converters are essential not only for reliable EV charging but also for the integration of renewable resources into the grid. To meet the large power levels required for widespread electrification, grid-connected converters must operate efficiently, reliably, and cost-effectively. Conventional EV charging systems typically use a two-stage architecture with an AFE PFC stage and an isolated dc-dc converter. While the stiff dc link in this approach simplifies control, the AFE incurs high switching and reverse-recovery losses, limiting switching frequency, increasing filter size, and reducing efficiency due to successive full-power processing stages. These drawbacks have driven increasing interest in single-stage ac-dc converters for both conductive and wireless charging.

The first part of this thesis focuses on the design, development, and optimization of a single-stage unfolding-based ac-dc topology for high-power EV battery charging. The proposed architecture employs a 3-ϕ 480 V Unfolder and a T-type bridge-based three-port dc-dc converter to deliver regulated power over a battery voltage range of 649–755 V while simultaneously achieving PFC. By integrating these functions into a single conversion stage, the system eliminates the need for large grid-side inductors and dc-link capacitors, resulting in a compact, power-dense, and efficient solution. This configuration is particularly well suited for WPT charging of heavy-duty EVs, where modular scalability is essential. Hardware validation using a 21 kW prototype with a single T-type module demonstrates an ac-dc efficiency of 95.94%. The modular nature of the system further supports scalability, as verified through the parallel operation of six T-type modules with a single grid-tied Unfolder. Overall, the results confirm that the proposed converter achieves high efficiency, high power

density, and reliable output power regulation, making it suitable for WPT applications and adaptable across a wide range of power levels.

Several refinements are introduced to further enhance the performance of the system. A leading-edge-aligned PWM strategy, combined with a robust closed-loop control architecture, is developed to achieve ZVS of the resonant T-type bridge in the unfolding-based ac-dc topology. In contrast to center-aligned modulation, the leading-edge-aligned approach maintains ZVS of the MOSFETs across the entire grid cycle by accurately aligning the quasi-square output voltages of the T-type bridge. A multi-loop control framework is developed, where the outer loop regulates output power and the inner loops maintain sinusoidal grid currents to achieve PFC. A detailed ZVS analysis is presented to examine critical switching transitions, incorporating the nonlinear behavior of the MOSFET output capacitance through energy- and charge-equivalent capacitors. ZVS times are calculated to determine appropriate timing parameters for hardware validation. The tank design is then guided by this accurate ZVS analysis, combined with conduction loss calculations, to ensure correct polarity and sufficient magnitude of the tank current during switching transitions, while also minimizing conduction losses. Experimental validation on a 20 kW, 480 V grid-tied prototype demonstrates complete ZVS throughout the grid cycle, with a peak ac-dc efficiency of 96.51%. Compared with center-aligned modulation, the proposed strategy achieves 0.76% higher efficiency and reduces radiated EMI by 6 dB (a factor of 2), confirming the effectiveness of the proposed leading-edge-aligned approach. Further refinements involve addressing two critical challenges of unfolding-based ac-dc converters: grid current distortions and the detrimental effects of LC resonance between the grid inductance and dc-link capacitors on closed-loop control. For the first challenge, a control-based technique is proposed that leverages the HF dc-dc converter to emulate current sources/sinks, thereby reducing current distortions without requiring additional hardware. The operation of the proposed technique is studied on a grid-tied unfolding-based EV-battery charger circuit, and its effectiveness is verified through simulations and hardware experiments, confirming a significant improvement in grid current quality and reduced THD. For the second, Middlebrook's EET

and phasor-transformation-based small-signal modeling are employed to characterize the effect of LC resonance on plant transfer functions and closed-loop control architecture. A control-based solution is then proposed to damp the resonance, utilizing current-emulation-based active damping through feedforward control of the HF T-type bridge-based dc-dc converter. In this technique, the converter emulates current sources/sinks that damp the LC resonance dynamics, effectively suppressing oscillations without the need for additional passive components. The validity of this approach is confirmed through simulations and hardware verification on the proposed unfolding-based ac-dc system. The hardware results demonstrate a tenfold increase in closed-loop bandwidth compared to undamped systems. Stable operation is achieved at bandwidth levels above the LC resonance while maintaining a low grid current THD across all operating conditions with active damping. By eliminating passive damping circuits, this refinement further enhances the stability, efficiency, and overall performance of the unfolding-based ac-dc converter.

A comprehensive small-signal modeling framework for the T-type bridge-based dc-dc converter, integrated within the unfolding-based ac-dc system, is developed using phasor transformation. The analysis incorporates both single-sided and double-sided LCC resonant tanks, with the secondary side employing an isolated diode bridge connected to a battery load, representing a typical wireless power transfer configuration. The modeling procedure is organized into distinct steps to provide a clear and intuitive understanding of the methodology. The resulting analytical model strengthens closed-loop control design and stability, ensuring more reliable and efficient operation of the EV battery charger system. Its accuracy is confirmed through simulations with double-sided LCC resonant tanks and validated experimentally using hardware prototypes with single-sided LCC tanks, demonstrating validity for perturbation frequencies up to 55 kHz. Furthermore, the modeling approach has been experimentally verified for both center-aligned and leading-edge-aligned modulation strategies of the T-type bridge.

The second part of this thesis addresses the broader system-level challenge of limited electricity generation capacity amidst the rapid expansion of EV charging infras-

tructure. The energy demand from electrifying transportation exceeds current electricity generation, underscoring the need for charging solutions that integrate seamlessly with renewable generation and battery storage. To address this, the work extends unfolding-based concepts to a multiport architecture that uses a low-frequency 3-ϕ Unfolder for grid interfacing together with a current injection circuit and a TAB-based dc-dc converter. The TAB employs a three-winding transformer whose leakage inductance provides the required tank inductance. An LCL resonant network and transformer winding are optimized to support battery voltages from 200–800 V with a reduced kVAr/kW ratio. Through this combination, the system coordinates power transfer among the grid, EV battery, and storage/renewable ports, effectively integrating these sources for EV charging. This architecture is distinct from the single-stage approach discussed earlier, yet it retains the advantages of the unfolding-based grid connection such as negligible switching losses, simplified grid interfacing, and compact filtering requirements. The proposed multiport system demonstrates how unfolding-based principles can be scaled to more complex system-level architectures that are essential for future EV charging infrastructure.

Experimental validation confirms the viability of the proposed multiport approach. A 5 kW, 480 V prototype demonstrates multiple power-flow scenarios and achieves a peak ac-dc efficiency of 98.3%. It maintains efficiency above 97% across various operating conditions and battery voltages from 200–800 V, with a grid current THD of 2%. Scalability is further demonstrated through 50 kW simulations and a 10 kW hardware prototype achieving 98.1% peak efficiency. Compared with prior multiport converters, the proposed architecture achieves higher efficiency, lower THD, reduced passive component count, and reliable wide-voltage operation. These results confirm that unfolding-based multiport converters provide a scalable, efficient, and compact foundation for future EV charging infrastructure that integrates multiple energy sources with the grid.

In summary, this thesis advances both circuit-level and system-level innovations in unfolding-based ac-dc converters with three-port dc-dc resonant topologies for EV battery charging. From high-efficiency converter designs with advanced control and modeling to

scalable multiport architectures that integrate battery storage/renewables with the grid, the contributions establish a foundation for compact, reliable, and sustainable charging infrastructure that is essential for the electrification of transportation.

Future work for the first part of this thesis involves scaling the proposed single-stage unfolding-based converter architecture to the 1 MW level, which is the final target of the project for charging heavy-duty EVs within one hour. This will require paralleling 48 T-type modules, each rated at 21 kW, connected to a single 1 MW Unfolder, while accommodating and extending the optimization techniques presented in this thesis, such as advanced modulation, active damping, high-bandwidth control, and accurate modeling, to ensure efficiency, stability, and reliability at megawatt-scale operation. The closed-loop control stability of parallel-connected T-type modules must also be analyzed in detail, particularly considering interactions among the modules. In addition, to follow the EV battery charging profile at varying power levels, a module-shedding approach is proposed so that the active T-type modules operate at full power without the need to derate individual modules, thereby preserving ZVS of the MOSFETs. This strategy requires isolating the T-type modules being shed using IGBT-based series switches in the tank circuit. A detailed analysis of the design and control implications of such module shedding remains an important direction for future investigation.

Future work for the second part of this thesis involves first increasing the power rating of the single dc-dc module to further improve the scalability of the proposed multiport topology. The three-winding transformer design can also be implemented using a planar transformer to enhance power density and compactness. In addition, advanced feed-forward-based control strategies should be developed to achieve effective decoupling between the EV-battery current loop and the PV current loop, ensuring that the dynamics of one loop do not influence the other. The feed-forward action can mitigate cross-coupling effects to maintain independent and well-regulated loop performance during transients. Moreover, since an active H-bridge is employed on the EV side of the multiport system, vehicle-to-grid operation can be explored, with particular emphasis on addressing the control and stability

challenges.

Finally, the efficiency evaluation in this thesis primarily focused on losses associated with the power electronics conversion process. However, for practical system deployment, losses introduced by the thermal management system should also be incorporated to provide a more comprehensive representation of the overall system performance. Integrating these additional loss components will enable a more realistic assessment of system-level efficiency and support informed design decisions for future implementations.

APPENDIX

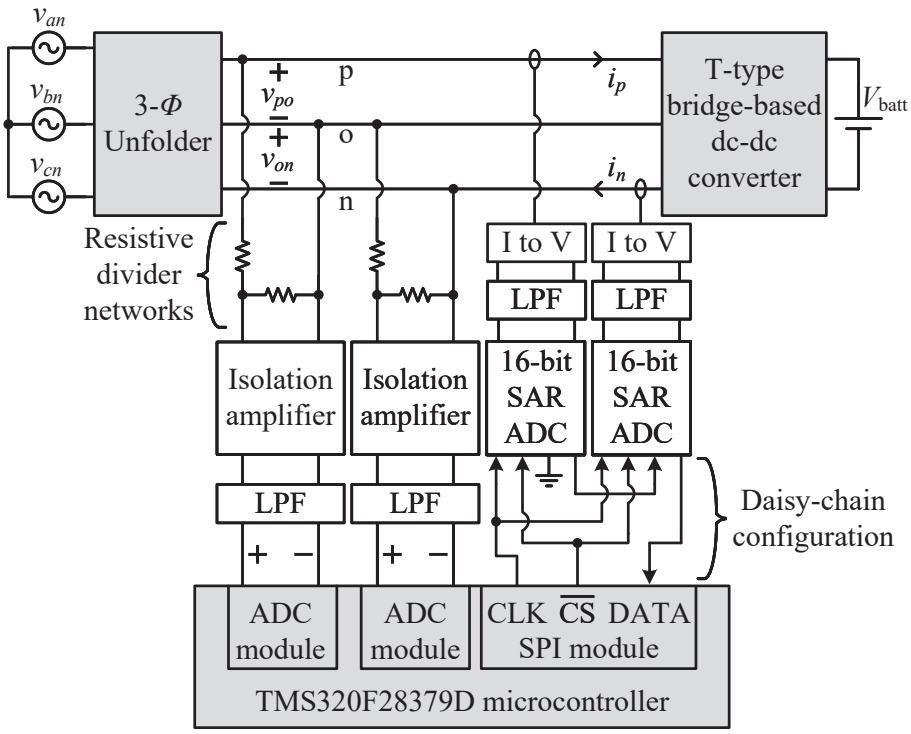


Fig. A.1: The structure of the voltage and current sensing circuits used for high-bandwidth control of the unfolding-based ac-dc system. The sensed voltages, v_{po} and v_{on}, and the sensed currents, i_p and i_n, are utilized for the feedforward and feedback controls shown in Fig. 4.31 of Chapter 4.

The voltages v_{po} and v_{on} are sensed for the feedforward control, as depicted in Fig. 4.31 of Chapter 4, using resistive divider networks. These sensed voltages are subsequently galvanically isolated using the isolation amplifier, ACPL-C870-500E from Broadcom Limited, and directed towards an LPF with a 20 kHz cutoff frequency. This cutoff frequency is set to be more than ten times greater than the LC resonant frequency and sufficiently below the switching frequency of the dc-dc converter. The filtered analog signals undergo digital conversion utilizing the 12-bit ADC module integrated within the Texas Instruments microcontroller TMS320F28379D [126]. The complete voltage sensing structure is illustrated

in Fig. A.1.

The currents i_p and i_n are sensed for the feedback control, as illustrated in Fig. 4.31 of Chapter 4, using CASR50-NP current sensors from LEM USA Inc., which provide equivalent analog voltage signals. These analog signals are passed through an LPF with a cutoff frequency of 30 kHz, which is ten times higher than the maximum closed-loop bandwidth and sufficiently below the dc-dc converter switching frequency. The filtered analog signals are then converted into digital signals through a 16-bit SAR-type ADC, specifically the ADS8318IDGST from Texas Instruments. Subsequently, these digital signals are interconnected in a daisy-chain configuration [127] and communicated to the microcontroller via the SPI protocol. The overall current sensing structure is presented in Fig. A.1.

CURRICULUM VITAE

Aditya Zade

Journal Articles

1. **A. Zade** et al., "A 21-kW Unfolding-Based Single-Stage AC–DC Converter for Wireless Charging Applications," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 12, no. 1, pp. 8-27, Feb. 2024, doi: 10.1109/JESTPE.2023.3309588.

2. **A. Zade**, S. Gurudiwan, D. Maksimović and R. Zane, "High-Bandwidth Control of a 20-kW Single-Stage Unfolding-Based AC–DC Converter Using the Extra Element Theorem and Current Emulation Technique," in IEEE Transactions on Power Electronics, vol. 39, no. 11, pp. 14411-14429, Nov. 2024, doi: 10.1109/TPEL.2024.3423705.

3. **A. Zade**, S. Gurudiwan and R. Zane, "98.3% Efficient Multiport System with Multi-Directional Power Flow to Integrate Battery Storage/Renewables with the Grid for EV Charging," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2025.3619441.

4. **A. Zade**, S. Gurudiwan and R. Zane, "Modulation, Control, and Tank Design for ZVS of a Resonant T-Type Bridge in a 20 kW Unfolding-Based Single-Stage AC-DC Converter," in IEEE Journal of Emerging and Selected Topics in Power Electronics (under review).

5. S. Gurudiwan, **A. Zade**, H. Wang and R. Zane, "Accurate ZVS Analysis of a Full-Bridge T-Type Resonant Converter for a 20-kW Unfolding-Based AC-DC Topology,"

in IEEE Open Journal of Power Electronics, vol. 5, pp. 692-708, 2024, doi: 10.1109/OJPEL.2024.3400256.

6. S. Gurudiwan, **A. Zade**, H. Wang and R. Zane, "Optimized Timing Control for Leading-Edge Aligned Modulation of a T-Type Bridge in Unfolding-Based AC–DC Converters," in IEEE Transactions on Power Electronics, vol. 40, no. 4, pp. 4716-4721, April 2025, doi: 10.1109/TPEL.2024.3514819.

Conference Papers

1. **A. Zade**, C. R. Teeneti, S. Gurudiwan, S. Poddar, M. Mansour and R. Zane, "Analysis and Mitigation of Sector Transition Distortions for Unfolding-based Grid-tied AC-DC Converters," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1945-1952, doi: 10.1109/APEC43580.2023.10131393.

2. **A. Zade**, S. Gurudiwan, M. Mansour, B. Hesterman, D. Maksimović and R. Zane, "High-Bandwidth Control of a 21 kW Unfolding-Based AC-DC Converter Using Extra Element Theorem and Current Emulation Technique," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 698-705, doi: 10.1109/APEC48139.2024.10509068.

3. **A. Zade**, S. Gurudiwan and R. Zane, "Small-Signal Phasor Modeling of T-Type Bridge-Based Single-Sided and Double-Sided LCC Resonant Converters for WPT Applications," 2025 IEEE Applied Power Electronics Conference and Exposition (APEC), Atlanta, GA, USA, 2025, pp. 2194-2201, doi: 10.1109/APEC48143.2025.10977075.

4. **A. Zade** and R. Zane, "Accurate Small-Signal Phasor Transformation-Based Modeling of Secondary-Side Diode-Bridge Rectifiers for Battery Charging Applications," 2025 IEEE Applied Power Electronics Conference and Exposition (APEC), Atlanta, GA, USA, 2025, pp. 1004-1011, doi: 10.1109/APEC48143.2025.10977532.

5. **A. Zade**, S. Gurudiwan and R. Zane, "Optimized Design of a TAB-Based Three-Port DC-DC Converter for an Unfolding-Based Multiport System," 2026 IEEE Applied Power Electronics Conference and Exposition (APEC).

6. **A. Zade**, B. Hesterman and R. Zane, "Three-Winding Transformer Design for a Multiport System Integrating Battery Storage/Renewables with the Grid for EV Battery Charging," 2026 IEEE Applied Power Electronics Conference and Exposition (APEC).

7. **A. Zade**, D. Venkatramanan and V. John, "Power Converter Based Impedance Emulation of Passive Loads for Anti-Islanding Tests," 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Chennai, India, 2018, pp. 1-6, doi: 10.1109/PEDES.2018.8707594.

8. S. Gurudiwan, **A. Zade**, R. Hatch, H. Wang and R. Zane, "ZVS Boundary Assessment for T-type-based Dual Active Bridge Series Resonant Converters using State-Plane Analysis," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 2098-2105, doi: 10.1109/APEC48139.2024.10509450.

9. S. Gurudiwan, **A. Zade**, H. Wang and R. Zane, "Nonlinear Capacitance-Based Accurate ZVS Analysis for Full-Bridge T-Type Resonant Converters," 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 2024, pp. 3288-3295, doi: 10.1109/ECCE55643.2024.10860915.

10. D. Goodrich, **A. Zade**, S. Gurudiwan, M. Mansour, R. Zane and H. Wang, "Small-Signal Modeling and Damping Design of Unfolding-Based Single Stage AC-DC Converter Using the Extra Element Theorem," 2025 IEEE Applied Power Electronics Conference and Exposition (APEC), Atlanta, GA, USA, 2025, pp. 719-726, doi: 10.1109/APEC48143.2025.10977164.

11. P. Bradford, **A. Zade**, S. Gurudiwan and H. Wang, "A Novel Thermal Modeling Analysis for Liquid-Cooled High-Power EV Chargers," 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 2024, pp. 6593-6599, doi: 10.1109/ECCE55643.2024.10861307.

12. M. Chawla, **A. Zade**, T. Newbolt, P. Mandal, A. Kamineni, H. Wang and R. Zane, "Modeling and Comparative Analysis of Power Distribution Architectures for Large-scale Electric Vehicle In-motion Wireless Charging Infrastructures," 2022 Wireless Power Week (WPW), Bordeaux, France, 2022, pp. 887-892, doi: 10.1109/WPW54272.2022.9901363.

13. S. Poddar, M. Mansour, **A. Zade** and R. Zane, "Investigation of Input Current Distortion at Sector Transitions in Unfolding-based Grid-tied AC-DC converters," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 2238-2244, doi: 10.1109/ECCE53617.2023.10362008.

14. T. Skinner, D. Goodrich, C. Sabin, M. Waite, **A. Zade** and H. Wang, "Design and Control of Three-phase Smart Inverter Using Gate-drive Integrated Gallium Nitride (GaN) Devices for Solar Energy Integration," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1463-1468, doi: 10.1109/APEC43580.2023.10131198.

15. M. Waite, C. Sabin, D. Goodrich, T. Skinner, **A. Zade**, S. Poddar and H. Wang, "GaN-based MHz-LLC Resonant Converter with High Voltage Gain for Solar Energy Integration," 2023 IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Shanghai, China, 2023, pp. 35-42, doi: 10.1109/PEDG56097.2023.102152 26.

Pending Patents

1. **A. Zade**, S. Gurudiwan, B. Hesterman and R. Zane, "High-Bandwidth Control of Unfolding-Based AC-DC Converters" (patent pending).

2. **A. Zade**, S. Gurudiwan and R. Zane, "Unfolding-Based Multiport System for Integrating Battery Storage or Renewables with the Grid for EV Battery Charging" (patent pending).

REFERENCES

[1] UN Environment Programme. (n.d.) Global transition from fossil fuels to electric mobility. [Online; accessed Sep. 2025]. [Online]. Available: https://www.unep.org/topics/air/global-transition-fossil-fuels-electric-mobility

[2] Charged: Electric Vehicles Magazine, "How to make heavy-duty electric trucks work in practice," *Charged EVs Magazine*, no. 62, Oct.-Dec. 2022, [Online; accessed Sep. 2025]. [Online]. Available: https://chargedevs.com/

[3] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, "Grid-interface bidirectional converter for residential dc distribution systems—part one: High-density two-stage topology," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1655–1666, Apr. 2013.

[4] L. Schrittwieser, M. Leibl, M. Haider, F. Thöny, J. W. Kolar, and T. B. Soeiro, "99.3% efficient three-phase buck-type all-sic swiss rectifier for dc distribution systems," in *Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC)*, 2017, pp. 2173–2178.

[5] A. Khaligh and S. Dusmez, "Comprehensive topological analysis of conductive and inductive charging solutions for plug-in electric vehicles," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 8, pp. 3475–3489, Oct. 2012.

[6] D. Aggeler, F. Canales, H. Zelaya-De La Parra, A. Coccia, N. Butcher, and O. Apeldoorn, "Ultra-fast dc-charge infrastructures for ev-mobility and future smart grids," in *Proc. IEEE PES Innovative Smart Grid Technologies Conf. Europe (ISGT Europe)*, 2010, pp. 1–8.

[7] M. Antivachis, J. A. Anderson, D. Bortis, and J. W. Kolar, "Analysis of a synergetically controlled two-stage three-phase dc/ac buck-boost converter," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 1, pp. 34–53, Mar. 2020.

[8] C.-C. Hou and P.-T. Cheng, "Experimental verification of the active front-end converters dynamic model and control designs," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1112–1118, 2011.

[9] T. Skinner, D. Goodrich, C. Sabin, M. Waite, A. Zade, and H. Wang, "Design and control of three-phase smart inverter using gate-drive integrated gallium nitride (gan) devices for solar energy integration," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1463–1468.

[10] Y. Guan, C. Cecati, J. M. Alonso, and Z. Zhang, "Review of high-frequency high-voltage-conversion-ratio dc–dc converters," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 2, no. 4, pp. 374–389, 2021.

[11] M. Waite *et al.*, "Gan-based mhz-llc resonant converter with high voltage gain for solar energy integration," in *2023 IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Shanghai, China, 2023, pp. 35–42.

[12] A. Zade, C. R. Teeneti, M. Mansour, S. Gurudiwan, B. Hesterman, H. Wang, and R. Zane, "A 21-kw unfolding-based single-stage ac–dc converter for wireless charging applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 1, pp. 8–27, 2024.

[13] D. Das, N. Weise, K. Basu, R. Baranwal, and N. Mohan, "A bidirectional soft-switched dab-based single-stage three-phase ac–dc converter for v2g application," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 1, pp. 186–199, 2019.

[14] N. Xuan Bac, D. M. Vilathgamuwa, and U. K. Madawala, "A sic-based matrix converter topology for inductive power transfer system," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4029–4038, Aug. 2014.

[15] S. Weerasinghe, U. K. Madawala, and D. J. Thrimawithana, "A matrix converter-based bidirectional contactless grid interface," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1755–1766, Mar. 2017.

[16] H. L. Li, A. P. Hu, and G. A. Covic, "A direct ac–ac converter for inductive power-transfer systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 661–668, Feb. 2012.

[17] M. Moghaddami, A. Anzalchi, and A. I. Sarwat, "Single-stage three-phase ac–ac matrix converter for inductive power transfer systems," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 10, pp. 6613–6622, Oct. 2016.

[18] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Swiss rectifier — a novel three-phase buck-type pfc topology for electric vehicle battery charging," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2617–2624.

[19] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, "Novel swiss rectifier modulation scheme preventing input current distortions at sector boundaries," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5771–5785, 2017.

[20] J. W. Kolar and T. Friedli, "The essence of three-phase pfc rectifier systems—part i," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, 2013.

[21] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase ac–dc power conversion using series-resonant converter modules and a three-phase unfolder," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9001–9012, 2017.

[22] B. Zhang, S. Xie, X. Wang, and J. Xu, "Modulation method and control strategy for full-bridge-based swiss rectifier to achieve zvs operation and suppress low-order harmonics of injected current," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6512–6522, 2020.

[23] C. R. Teeneti, R. Hatch, D. B. Yelaverthi, A. Kamineni, H. Wang, and R. Zane, "Unfolder-based single-stage ac-ac conversion system for wireless charging applications," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 5193–5198.

[24] C. S. Wong, J. Liu, L. Cao, and K. H. Loo, "A swiss-rectifier-based single-stage three-phase bidirectional ac–dc inductive-power-transfer converter for vehicle-to-grid applications," *IEEE Transactions on Power Electronics*, vol. 38, no. 3, pp. 4152–4166, 2023.

[25] A. Zade, S. Gurudiwan, D. Maksimović, and R. Zane, "High-bandwidth control of a 20-kw single-stage unfolding-based ac–dc converter using the extra element theorem and current emulation technique," *IEEE Transactions on Power Electronics*, vol. 39, no. 11, pp. 14 411–14 429, 2024.

[26] B. Zhang, S. Xie, Z. Li, P. Zhao, and J. Xu, "An optimized single-stage isolated swiss-type ac/dc converter based on single full-bridge with midpoint-clamper," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 288–11 297, 2021.

[27] B. Zeng, Z. Yang, S. Yan, L. Tan, and S. Xie, "A novel high power factor and soft switching sab-swiss rectifier with high-low-high-low modulation and hybrid frequency control," *IEEE Access*, vol. 12, pp. 185 187–185 199, 2024.

[28] S. Gurudiwan, R. Hatch, M. Mansour, H. Wang, and R. Zane, "An 18 kw battery charger module for extreme fast charging applications using an unfolding-based ac-dc topology," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1715–1722.

[29] S. GURUDIWAN, A. Zade, H. Wang, and R. Zane, "Accurate zvs analysis of a full-bridge t-type resonant converter for a 20-kw unfolding-based ac-dc topology," *IEEE Open Journal of Power Electronics*, vol. 5, pp. 692–708, 2024.

[30] S. Gurudiwan, A. Zade, H. Wang, and R. Zane, "Optimized timing control for leading-edge aligned modulation of a t-type bridge in unfolding-based ac–dc converters," *IEEE Transactions on Power Electronics*, vol. 40, no. 4, pp. 4716–4721, 2025.

[31] S. Gurudiwan, A. Zade, R. Hatch, H. Wang, and R. Zane, "Zvs boundary assessment for t-type-based dual active bridge series resonant converters using state-plane analysis," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 2098–2105.

[32] P. Grzejszczak, K. Wolski, M. Szymczak, M. Koszel, K. Bzura, and M. Jasiński, "Design and evaluation of robust 20-kw sic-based three-phase bidirectional ac–dc converter," in *2022 Progress in Applied Electrical Engineering (PAEE)*, Koscielisko, Poland, 2022, pp. 1–7.

[33] Dynex Semiconductor Ltd, *AN6156 Calculating Power Losses in an IGBT Module*, an6156-2 ed., Feb. 2021, lN40671. [Online; accessed Sep. 2025]. [Online]. Available: https://www.dynexsemi.com/Portals/0/assets/downloads/DNX_AN6156.pdf

[34] U.S. Energy Information Administration, "Petroleum and other liquids," https://www.eia.gov/petroleum/, [Online; accessed 22-September-2025].

[35] ——, "Electric power monthly," https://www.eia.gov/electricity/monthly/, [Online; accessed 22-September-2025].

[36] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 861–878, Dec. 2019.

[37] I. Roditis, M. Dakanalis, E. Koutroulis, and F. D. Kanellos, "Three-phase multiport dc–ac inverter for interfacing photovoltaic and energy storage systems to the electric grid," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 4, no. 3, pp. 982–994, Jul. 2023.

[38] K. Wang, F. Wu, J. Su, and G. Wang, "Three-phase single-stage three-port high-frequency isolated dc–ac converter," *IEEE Transactions on Power Electronics*, vol. 38, no. 9, pp. 11 113–11 124, Sep. 2023.

[39] A. Verma and B. Singh, "Multi-objective reconfigurable three-phase off-board charger for ev," *IEEE Transactions on Industry Applications*, vol. 55, no. 4, pp. 4192–4203, Jul. 2019.

[40] G. R. C. Mouli, J. Schijffelen, M. van den Heuvel, M. Kardolus, and P. Bauer, "A 10 kw solar-powered bidirectional ev charger compatible with chademo and combo," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1082–1098, Feb. 2019.

[41] G. Waltrich, J. L. Duarte, and M. A. M. Hendrix, "Multiport converter for fast charging of electrical vehicle battery," *IEEE Transactions on Industry Applications*, vol. 48, no. 6, pp. 2129–2139, Dec. 2012.

[42] N. Bilakanti, L. Zheng, P. Kandula, K. Kandasamy, and D. Divan, "Single stage soft-switching tri-port converter for integrating renewable source and storage with grid through galvanic isolation," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, Poland, 2017, pp. P.1–P.10.

[43] A. Hameed and G. Moschopoulos, "Three-phase single-stage multiport ac-dc converter with integrated dc-dc conversion stages," in *2025 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Atlanta, GA, USA, 2025, pp. 1972–1976.

[44] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Design and implementation of a three-phase buck-type third harmonic current injection pfc rectifier sr," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1608–1621, 2013.

[45] M. S. Khan, S. S. Nag, and A. Das, "A high efficiency non-isolated three-phase unfolding based electric vehicle powertrain," *IEEE Transactions on Industry Applications*, vol. 60, no. 4, pp. 6612–6621, Jul. 2024.

[46] H. Krishnaswami and N. Mohan, "Three-port series-resonant dc–dc converter to interface renewable energy sources with bidirectional load and energy storage ports," *IEEE Transactions on Power Electronics*, vol. 24, no. 10, pp. 2289–2297, Oct. 2009.

[47] C. Zhao, S. D. Round, and J. W. Kolar, "An isolated three-port bidirectional dc-dc converter with decoupled power flow management," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2443–2453, Sep. 2008.

[48] R. Tavakoli and Z. Pantic, "Analysis, design, and demonstration of a 25-kw dynamic wireless charging system for roadway electric vehicles," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1378–1393, 2018.

[49] A. Mahesh, B. Chokkalingam, and L. Mihet-Popa, "Inductive wireless power transfer charging for electric vehicles–a review," *IEEE Access*, vol. 9, pp. 137 667–137 713, 2021.

[50] S. Inoue, D. Goodrich, S. Saha, R. Nimri, A. Kamineni, N. S. Flann, and R. A. Zane, "Fast design optimization method utilizing a combination of artificial neural networks and genetic algorithms for dynamic inductive power transfer systems," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 915–929, 2022.

[51] M. Chawla, A. Zade, T. Newbolt, P. Mandal, A. Kamineni, H. Wang, and R. Zane, "Modeling and comparative analysis of power distribution architectures for large-scale electric vehicle in-motion wireless charging infrastructures," in *2022 Wireless Power Week (WPW)*, 2022, pp. 887–892.

[52] *Wireless Power Transfer for Light-Duty Plug-In Electric Vehicles and Alignment Methodology*, Society of Automotive Engineers Standard SAE J2954, 2019, [Online; accessed 14-Aug-2025]. [Online]. Available: https://www.sae.org/standards/content/j2954_201904/

[53] D. B. Yelaverthi, M. Mansour, H. Wang, and R. Zane, "Triple active bridge series resonant converter for three-phase unfolding based isolated converters," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 4924–4930.

[54] M. Mansour, D. B. Yelaverthi, and R. Zane, "Voltage balancing control for input-series-output-parallel three-port series resonant converter modules," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 01–08.

[55] N. H. Pham, T. Mannen, and K. Wada, "Power factor operation of a boost integrated three-phase solar inverter using current unfolding and active damping methods," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 2896–2903.

[56] R. Chen, Y. Yao, L. Zhao, and M. Xu, "Inhibiting mains current distortion for swiss rectifier - a three-phase buck-type harmonic current injection pfc converter," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1850–1854.

[57] C. R. Teeneti, U. Pratik, G. R. Philips, A. Azad, M. Greig, R. Zane, C. Bodine, C. Coopmans, and Z. Pantic, "System-level approach to designing a smart wireless charging system for power wheelchairs," *IEEE Transactions on Industry Applications*, vol. 57, no. 5, pp. 5128–5144, 2021.

[58] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. New York, NY, USA: Springer, 2001.

[59] A. P. Hu, "Modeling a contactless power supply using gssa method," in *2009 IEEE International Conference on Industrial Technology*, 2009, pp. 1–6.

[60] A. Zade, S. Gurudiwan, and R. Zane, "Small-signal phasor modeling of t-type bridge-based single-sided and double-sided lcc resonant converters for wpt applications," in *2025 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2025, pp. 2194–2201.

[61] C. Rim and G. Cho, "Phasor transformation and its application to the dc/ac analyses of frequency phase-controlled series resonant converters (src)," *IEEE Transactions on Power Electronics*, vol. 5, no. 2, pp. 201–211, 1990.

[62] D. Seltzer, L. Corradini, D. Bloomquist, R. Zane, and D. Maksimović, "Small signal phasor modeling of dual active bridge series resonant dc/dc converters with multi-angle phase shift modulation," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 2757–2764.

[63] A. Zade and R. Zane, "Accurate small-signal phasor transformation-based modeling of secondary-side diode-bridge rectifiers for battery charging applications," in *2025 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2025, pp. 1004–1011.

[64] V. Z. Barsari, D. J. Thrimawithana, and G. A. Covic, "An inductive coupler array for in-motion wireless charging of electric vehicles," *IEEE Transactions on Power Electronics*, vol. 36, no. 9, pp. 9854–9863, 2021.

[65] D. Cittanti, C. Gammeter, J. Huber, R. Bojoi, and J. W. Kolar, "A simplified hard-switching loss model for fast-switching three-level t-type SiC bridge-legs," *Electronics*, vol. 11, no. 11, p. 1686, 2022.

[66] B. Liu, R. Ren, E. A. Jones, H. Gui, Z. Zhang, R. Chen, F. Wang, and D. Costinett, "Effects of junction capacitances and commutation loops associated with line-frequency devices in three-level ac/dc converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6155–6170, 2019.

[67] P. Bradford, A. Zade, S. Gurudiwan, and H. Wang, "A novel thermal modeling analysis for liquid-cooled high-power ev chargers," in *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2024, pp. 6593–6599.

[68] A. Zade, C. R. Teeneti, S. Gurudiwan, S. Poddar, M. Mansour, and R. Zane, "Analysis and mitigation of sector transition distortions for unfolding-based grid-tied ac-dc converters," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1945–1952.

[69] S. S. Ahmad and G. Narayanan, "Double pulse test based switching characterization of sic mosfet," in *2017 National Power Electronics Conference (NPEC)*, 2017, pp. 319–324.

[70] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level t-type converter for low-voltage applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899–907, 2013.

[71] Texas Instruments, *TMS320F2837xD Dual-Core Microcontrollers Technical Reference Manual*, rev. i ed., Sep. 2019, [Online]. [Online]. Available: https://www.ti.com/tool/TMDSCNCD28379D#tech-docs

[72] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 985–995, 2015.

[73] S. Gurudiwan, A. Zade, H. Wang, and R. Zane, "Nonlinear capacitance-based accurate zvs analysis for full-bridge t-type resonant converters," in *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2024, pp. 3288–3295.

[74] H. Pham N., T. Mannen, and K. Wada, "A three-phase isolated rectifier using current unfolding and active damping methods," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 4587–4593.

[75] R. Erickson, "Optimal single resistors damping of input filters," in *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, vol. 2, 1999, pp. 1073–1079 vol.2.

[76] S. V. Dhople, B. B. Johnson, F. Dörfler, and A. O. Hamadeh, "Synchronization of nonlinear circuits in dynamic electrical networks with general topologies," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 9, pp. 2677–2690, 2014.

[77] A. Zade, D. Venkatramanan, and V. John, "Power converter based impedance emulation of passive loads for anti-islanding tests," in *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2018, pp. 1–6.

[78] S. Poddar, M. Mansour, A. Zade, and R. Zane, "Investigation of input current distortion at sector transitions in unfolding-based grid-tied ac-dc converters," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 2238–2244.

[79] R. Middlebrook, "Null double injection and the extra element theorem," *IEEE Transactions on Education*, vol. 32, no. 3, pp. 167–180, 1989.

[80] ——, "The two extra element theorem," in *Proceedings Frontiers in Education Twenty-First Annual Conference. Engineering Education in a New World Order*, 1991, pp. 702–708.

[81] R. Middlebrook, V. Vorperian, and J. Lindal, "The n extra element theorem," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 45, no. 9, pp. 919–935, 1998.

[82] D. Kim, B. Choi, D. Lee, and J. Sun, "Analysis of input filter interactions in switching power converters," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, vol. 1, 2005, pp. 191–198 Vol. 1.

[83] H. Yu, Y. Wang, H. Zhang, and Z. Chen, "Impedance modeling and stability analysis of triple-active-bridge-converter-based renewable-electricity-hydrogen-integrated metro dc traction power system," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 12, pp. 12 340–12 353, 2023.

[84] J. J. Cooley, P. Lindahl, C. L. Zimmerman, M. Cornachione, G. Jordan, S. R. Shaw, and S. B. Leeb, "Multiconverter system design for fuel cell buffering and diagnostics under uav load profiles," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 3232–3244, 2014.

[85] S.-Y. Chiu and K. A. Kim, "System analysis and design for multiconverter electrical power systems in nanosatellites," *IEEE Journal on Miniaturization for Air and Space Systems*, vol. 4, no. 1, pp. 41–53, 2023.

[86] C. T. Rim, "Unified general phasor transformation for ac converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 9, pp. 2465–2475, 2011.

[87] Y. Yin, R. Zane, J. Glaser, and R. Erickson, "Small-signal analysis of frequency-controlled electronic ballasts," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 8, pp. 1103–1110, 2003.

[88] A. Zade, S. Gurudiwan, M. Mansour, B. Hesterman, D. Maksimović, and R. Zane, "High-bandwidth control of a 21 kw unfolding-based ac-dc converter using extra element theorem and current emulation technique," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 698–705.

[89] W.-J. Lee and S.-K. Sul, "Dc-link voltage stabilization for reduced dc-link capacitor inverter," in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 1740–1744.

[90] E. Matijevic, R. Sharma, F. Zare, and D. Kumar, "A unified active damping for grid and converter current feedback in active front end converters," *IEEE Access*, vol. 10, pp. 30 913–30 924, 2022.

[91] S. Li and C. C. Mi, "Wireless power transfer for electric vehicle applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 1, pp. 4–17, 2015.

[92] Y. Yin, R. Zane, R. Erickson, and J. Glaser, "Direct modeling of envelope dynamics in resonant inverters," in *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03.*, vol. 3, 2003, pp. 1313–1318 vol.3.

[93] A. C. Bagchi, H. Wang, T. Saha, and R. Zane, "Small-signal phasor modeling of an underwater ipt system in constant current distribution," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 876–883.

[94] W. Han and L. Corradini, "Analytical small-signal transfer functions for phase shift modulated dual active bridge converters using phasor transformation," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1442–1448.

[95] M. Cacciato, G. Nobile, G. Scarcella, and G. Scelba, "Real-time model-based estimation of soc and soh for energy storage systems," in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2015, pp. 1–8.

[96] S. Srdic and S. Lukic, "Toward extreme fast charging: Challenges and opportunities in directly connecting to medium-voltage line," *IEEE Electrification Magazine*, vol. 7, no. 1, pp. 22–31, Mar. 2019.

[97] J. Suvvala, S. Kumar, C. Dhananjayulu, H. Kotb, and A. Elrashidi, "Integration of renewable energy sources using multiport converters for ultra-fast charging stations for electric vehicles: An overview," *Heliyon*, vol. 10, no. 15, p. e35782, 2024.

[98] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii, and I. Batarseh, "A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications," *IEEE Access*, vol. 10, pp. 40 753–40 793, 2022.

[99] Y. Wang, F. Han, L. Yang, R. Xu, and R. Liu, "A three-port bidirectional multi-element resonant converter with decoupled power flow management for hybrid energy storage systems," *IEEE Access*, vol. 6, pp. 61 331–61 341, 2018.

[100] M. Rashidi, N. N. Altin, S. S. Ozdemir, A. Bani-Ahmed, and A. Nasiri, "Design and development of a high-frequency multiport solid-state transformer with decoupled control scheme," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7515–7526, 2019.

[101] I. Kougioulis, A. Pal, P. Wheeler, and M. R. Ahmed, "An isolated multiport dc–dc converter for integrated electric vehicle on-board charger," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 4, pp. 4178–4198, Aug. 2023.

[102] L. Gong *et al.*, "A simplified all-zvs strategy for high-frequency triple active bridge converters with designed magnetizing inductance," *IEEE Transactions on Power Electronics*, vol. 38, no. 11, pp. 13 781–13 797, 2023.

[103] S. Dey and A. Mallik, "Multivariable-modulation-based conduction loss minimization in a triple-active-bridge converter," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6599–6612, Jun. 2022.

[104] S. S. Chakraborty, S. Dey, and K. Hatua, "Design of a three-winding transformer for power decoupling of a three-port series resonant converter for an integrated on-board ev charger," *IEEE Transactions on Power Electronics*, vol. 38, no. 11, pp. 14 262–14 273, Nov. 2023.

[105] S. Ghosh and B. Singh, "A multiport charger for light electric vehicles with function of powering domestic appliances," *IEEE Transactions on Consumer Electronics*, vol. 70, no. 1, pp. 308–317, Feb. 2024.

[106] S. A. Khan, M. R. Islam, Y. Guo, and J. Zhu, "A new isolated multi-port converter with multi-directional power flow capabilities for smart electric vehicle charging stations," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 2, pp. 1–4, Mar. 2019.

[107] V. Monteiro, J. G. Pinto, and J. L. Afonso, "Experimental validation of a three-port integrated topology to interface electric vehicles and renewables with the electrical grid," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 6, pp. 2364–2374, Jun. 2018.

[108] L. Zheng, R. P. Kandula, and D. Divan, "Multiport control with partial power processing in solid-state transformer for pv, storage, and fast-charging electric vehicle integration," *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 2606–2616, Feb. 2023.

[109] Y. Li *et al.*, "Optimal synergetic operation and experimental evaluation of an ultra-compact gan-based three-phase 10-kw ev charger," *IEEE Transactions on Transportation Electrification*, vol. 10, no. 2, pp. 2377–2396, Jun. 2024.

[110] D. Goodrich, A. Zade, S. Gurudiwan, M. Mansour, R. Zane, and H. Wang, "Small-signal modeling and damping design of unfolding-based single stage ac-dc converter using the extra element theorem," in *2025 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Atlanta, GA, USA, 2025, pp. 719–726.

[111] T. B. Soeiro, F. Vancu, and J. W. Kolar, "Hybrid active third-harmonic current injection mains interface concept for dc distribution systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 7–13, Jan. 2013.

[112] M. M. Jovanović and B. T. Irving, "On-the-fly topology-morphing control—efficiency optimization method for llc resonant converters operating in wide input- and/or output-voltage range," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2596–2608, Mar. 2016.

[113] Z. Fang, T. Cai, S. Duan, and C. Chen, "Optimal design methodology for llc resonant converter in battery charging applications based on time-weighted average efficiency," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5469–5483, Oct. 2015.

[114] D. Huang, F. C. Lee, and D. Fu, "Classification and selection methodology for multi-element resonant converters," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011, pp. 558–565.

[115] S. Mukherjee, J. M. Ruiz, and P. Barbosa, "A high power density wide range dc–dc converter for universal electric vehicle charging," *IEEE Transactions on Power Electronics*, vol. 38, no. 2, pp. 1998–2012, Feb. 2023.

[116] T. Saha, A. C. Bagchi, and R. A. Zane, "Analysis and design of an lcl–t resonant dc–dc converter for underwater power supply," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6725–6737, Jun. 2021.

[117] M. Khatua, "Wide operating range resonant converters," Ph.D. dissertation, Cornell University, Dept. of Electrical and Computer Engineering, May 2022.

[118] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase plls: A review of recent advances," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017.

[119] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for mosfets in a half-bridge," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019.

[120] E. C. Snelling, "Properties of windings," in *Soft Ferrites: Properties and Applications*, 2nd ed. Oxford, U.K.: Butterworth-Heinemann, 1988, pp. 337–358.

[121] D. Aggeler, J. Biela, and J. W. Kolar, "A compact, high voltage 25 kw, 50 khz dc-dc converter based on sic jfets," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Austin, TX, USA, 2008, pp. 801–807.

[122] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings.*, Mayaguez, PR, USA, 2002, pp. 36–41.

[123] L. F. Blume, A. Boyajian, G. Camilli, T. C. Lennox, S. Minneci, and V. M. Montsinger, *Transformer Engineering: A Treatise on the Theory, Operation, and Application of Transformers*, 2nd ed. New York: Wiley, 1951.

[124] Tektronix, "4 series mso mixed signal oscilloscope datasheet," https://download.tek.com/datasheet/MSO4-Datasheet-EN-US-48W-61558-18.pdf, september 2024, [Online; accessed 22-September-2025].

[125] A. Zade, S. Gurudiwan, and R. Zane, "98.3% efficient multiport system with multi-directional power flow to integrate battery storage/renewables with the grid for ev charging," *IEEE Transactions on Power Electronics*, pp. 1–25, 2025.

[126] Texas Instruments, *TMS320F2837xD Dual-Core Microcontrollers Technical Reference Manual*, May 2024, rev. K. [Online]. Available: https://www.ti.com/tool/TMDSCNCD28379D#tech-docs

[127] Texas Instruments Application Report, "Daisy chain implementation for serial peripheral interface," Tech. Rep., Apr. 2021, rev. A. [Online]. Available: https://www.ti.com/lit/pdf/slvae25