ENHANCING GRID INTEGRATION OF HIGH-POWER LOADS THROUGH MODULAR UNFOLDING-BASED POWER CONVERSION WITH DECENTRALIZED CONTROL

by

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ABSTRACT

Enhancing Grid Integration of High-Power Loads through Modular Unfolding-Based Power Conversion with Decentralized Control

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Transportation electrification across all vehicle classes is essential for mitigating climate change and advancing a sustainable energy future. However, limited driving range and inadequate charging infrastructure continue to impede widespread electric vehicle (EV) adoption. DC Fast Charging (DCFC) technology plays a crucial role by significantly reducing charging times, thereby enabling long-distance travel and supporting the electrification of Medium- and Heavy-Duty (MDHD) vehicles.

Despite these benefits, implementing DCFC infrastructure presents challenges due to high power processing requirements, leading to substantial construction, operational, and maintenance costs. Integration with the electrical grid adds further complexity. This research aims to advance power conversion technologies central to DCFC systems, with the broader goal of reducing system and operational costs.

This work introduces a novel unfolding-based modular power converter architecture that connects directly with the medium-voltage (4.16-34.5 kV) grid. The proposed architecture supports both AC and DC output ports to maximize hardware utilization and

facilitate battery integration, minimizing the impact on the grid. It also incorporates isolated DC-DC modules functioning as DC transformers (DCXs), which enable decentralized power-sharing control, enhancing system flexibility, reliability, and maintainability.

The research addresses and overcomes key technical challenges related to the proposed architecture, including system implementation, DCX stage design and topology selection, dynamic and steady-state modeling of the DCX converters, and mitigation of sector distortion in the unfolding stage.

Overall, this dissertation presents an innovative approach to medium-voltage (MV) converter architecture that supports the development of cost-effective and reliable DC Fast Charging (DCFC) systems. It also contributes to the broader field of power electronics by addressing fundamental design, modeling, and control challenges. In addition, the proposed solutions are applicable to other high-power applications, such as data centers, supporting the development of more efficient and resilient energy infrastructure.

(114 pages)

PUBLIC ABSTRACT

Enhancing Grid Integration of High-Power Loads through Modular Unfolding-Based Power Conversion with Decentralized Control

Sanat R. Poddar

The transition to electric vehicles (EVs) is a critical step toward reducing greenhouse gas emissions and creating a cleaner, more sustainable transportation sector. However, many drivers — particularly those operating larger vehicles such as trucks and buses — face significant challenges, including limited driving range and lengthy charging times. High-power, fast-charging stations, which can rapidly replenish EV batteries, are therefore essential for mitigating these barriers and making electric transportation practical across all vehicle classes.

Despite the promise of electric vehicles, deploying high-power fast-charging stations presents significant challenges. They require large amounts of electricity, making them expensive to install, operate, and connect to the power grid. This research focuses on improving the core technology inside these charging stations: the systems that convert electricity from the grid into a form EVs can use.

This work introduces a new power converter design that can connect directly to the medium-voltage power grid. The design is more efficient and flexible, reducing both cost and complexity. The research also addresses key technical challenges to unlock the full potential of this system.

While the technology directly supports EV fast charging, its impact extends further. It can benefit other high-power applications, such as data centers, and the research contributes to the broader field of power electronics by addressing fundamental design and control challenges. These advances support the development of a more resilient, efficient, and intelligent electric infrastructure for a clean energy future.

To all those who have been a part of this journey...

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my advisor and mentor, Dr. Regan Zane, for his invaluable contributions to this work. His technical guidance, sharp insight, and steady support have been instrumental in shaping the direction of my research. I am especially grateful for the way he consistently challenged me to push beyond my limit. I consider his conduct to have had a lasting personal impact on me, both academically and beyond.

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CONTENTS

LIST OF FIGURES

ACRONYMS

AC	Alternating Current
DAB	Dual Active Bridge
DAB-SRC	Dual Active Bridge-Series Resonant Converter
DC	Direct Current
DCFC	DC Fast Charging
DCX	DC Transformer
EV	Electric Vehicle
ISOP	Input Series Output Parallel
LF	Line-Frequency
LV	Low-Voltage
LTI	Linear Time-Invariant
MDHD	Medium-Duty Heavy-Duty
MF	Medium-Frequency
MV	Medium-Voltage
SB-DCX	Series-Bridge DC Transformer
SST	Solid State Transformer
TCO	Total Cost of Ownership
THD	Total Harmonic Distortion
ToU	Time of Use

CHAPTER 1

Introduction

Transportation electrification is essential to decarbonize the transportation sector. Energy transition away from fossil-based sources is critical to alleviate climate change. The transportation sector consumes 28% of the total energy needs in the US [1] and is powered through fossil fuels. Cleaner transportation is essential to reduce greenhouse emissions. In combination with a greener generation mix, EVs are a solution to reduce emissions due to transportation.

EV adoption (across vehicle classes) at scale is enabled by a ubiquitous and seamless charging experience [2]. High battery costs, battery degradation, and limited driving range are the major barriers to EV adoption [3]. The presence of charging infrastructure helps mitigate these challenges by reducing the need for large onboard battery capacity (thus reducing upfront costs) and alleviating range anxiety among consumers. As a result, investment in charging infrastructure is crucial to accelerating the transition to electric mobility and achieving sustainable transportation solutions.

DC fast charging stations (DCFCs) are an integral part of the charging ecosystem. A DCFC station consists of multiple DCFC units. The DCFC unit has a high-power conversion system that delivers DC power to the battery from the 3-ϕ AC grid. It allows for charging at higher C-rates, thereby decreasing the vehicle charge time. This is necessary to improve consumer experience, alleviate range anxiety, and facilitate long-distance travel [4]. Further, commercially operated medium-duty and heavy-duty (MDHD) vehicles require DCFC to ensure minimum downtime, and thereby maximize revenue [5].

Widespread EV adoption, which is essential for reducing greenhouse gas emissions from the transportation sector, may ultimately depend on the establishment of a comprehensive fast-charging network. Charging infrastructure plays a critical role in addressing both perceived and actual driving range limitations, thereby encouraging consumer accep-

tance of electric vehicles. However, current power conversion technologies must be improved to reduce the initial capital investment and ongoing operational costs of DC fast-charging stations. This dissertation addresses these challenges by proposing a new direct medium-voltage (MV) power conversion architecture designed to facilitate easier grid interconnection, enhance performance, increase reliability, improve hardware utilization, and thereby lower overall system costs.

1.1 Challenges to Building DC Fast Charging Stations

The deployment of DCFCs necessitates a substantial capital investment. However, the process of investment recovery and the associated economic models are not always clear. The power conversion system is central to a DC fast charging (DCFC) unit and significantly impacts the cost of DCFCs.

For each DCFC unit, the power conversion hardware and equipment constitute a significant portion of the cost. The power rating for each DCFC unit ranges from 50 kW to 350 kW (or even higher to enable MDHD fast charging). Such high-power conversion requires sophisticated power conversion systems, charging connectors, communication and control systems, protection, and grid connection infrastructure. The higher the power requirement and efficiency, the higher the cost.

The power conversion system serves as the core of the DCFCs, where improvements in performance, reliability, and utilization have a significant impact on both initial investment and ongoing operational costs. Typically, high-power loads are connected to the three-phase AC grid (480 V AC). Within the DCFC unit, the power conversion system performs the essential conversion and control processes needed to charge EV batteries, which require DC voltages ranging from 200 V to 900 V. As power conversion requirements increase, so do the volume and weight of the converter, which in turn raise equipment, installation, and labor costs. Additionally, the efficiency of the power conversion system directly affects operating expenses, while the limited lifespan of power hardware leads to recurring maintenance costs. Therefore, to reduce the total cost of ownership and improve system performance, there is a clear need for high-performance, reliable, modular, and flexible power conversion systems

that are easier to maintain and upgrade.

DCFCs contain multiple DCFC units, which are interconnected with the feeder at medium voltage (4.16-34.5 kV) and require a line frequency transformer. This addition significantly increases both cost and system volume. Further grid upgrades may be needed to service the DCFCs. Therefore, high infrastructure costs remain a bottleneck for the construction of DCFCs. Low hardware utilization exacerbates the problem [6]. An operational model that increases hardware utilization could encourage investments in building DCFCs.

Additionally, due to the high instantaneous power requirement of DCFCs, they could pose a significant burden on the electricity grid [7, 8]. DCFCs can be considered variable high-power loads for the grid, making power balancing challenging for grid operators. Demand charges and time-of-utilization energy costs increase operational expenses, resulting in higher overall costs. This raises questions about the economics of DCFCs. Energy storage integration with the DCFCs helps resolve these challenges [9, 10].

In summary, the power conversion system significantly influences both the initial investment and ongoing operational costs of DCFCs, making its optimization crucial for cost-effectiveness.

1.2 Objectives and Contributions

This work aims to advance the technology of high-power conversion systems central to DC fast-charging stations, with a focus on power converter architecture, design, modeling, and control. The overarching goal is to reduce both the initial system cost and ongoing operational expenses.

We introduce a novel direct medium-voltage (MV) connected power converter architecture designed to enhance performance, improve system reliability, and maximize the utilization of power conversion hardware. The key innovation lies in the use of a naturally stackable DC-DC structure that supports medium-voltage grid input combined with a three-phase unfolder, while reducing the number of required power-processing stages to get to the desired output.

By eliminating the need for a bulky line-frequency transformer, the proposed direct MV-connected power converter significantly reduces both cost and system size. Its modular structure and decentralized power-sharing control improve fault tolerance and scalability, while a multi-port output capable of supplying both DC and $3-\phi$ AC power increases hardware utilization across diverse load types.

The objective of this work is to address the technical challenges associated with the proposed architecture and to validate its feasibility and performance through design, and experimental hardware testing.

The proposed architecture consists of multiple DC-DC modules that operate as DC transformers (DCXs), and the performance of these modules is crucial to the overall system. Accordingly, this dissertation additionally explores the design of the DC-DC modules and the system-level controls. The specific contributions are as follows:

1. Novel MV Converter Architecture to Improve Performance, Reliability, Utilization, and Grid Integration: We propose a three-phase unfolding-based MV converter architecture with both low-voltage (LV) $3-\phi$ AC and DC outputs. The architecture features fully decentralized power-sharing control for the modular structure that improves system reliability. A lab-scale prototype validates its feasibility and performance. Experimental results confirm key benefits, including natural voltage sharing among modules, hybrid distribution, single-stage AC to AC power conversion, and reactive power control, demonstrating this architecture as a practical and advantageous solution.

2. DCX Topology and Design for Operation with Unfolder: The proposed architecture adopts an input-series-output-parallel (ISOP) configuration of DC-DC modules, each functioning as an ideal DCX. DCX operation enables natural input-voltage sharing among modules, enhancing system reliability. Since topology selection for DCX operation with an unfolder is non-trivial, we examine multiple full-bridge DC-DC topologies that can achieve resonance, including Series Bridge-DCX (SB-DCX) and Dual Active Bridge-Series Resonant Converter (DAB-SRC). Hardware validation of the SB-DCX design for 10 kW power level, achieving efficiencies greater than 97%, confirms its practical feasibility and supports the

proposed architecture. Further, suitable mechanisms to counteract resonance mistuning are also investigated in DAB-SRC.

3. Relevant Steady-State and Dynamic Models: A scalable and tractable linear time-invariant (LTI) dynamic model is developed for the SB-DCX using half-cycle averaging. This model enables accurate system-level design and stability analysis. Additionally, to support DAB-SRC operation as a DCX, we derive steady-state models to predict the required minimum dead time as a function of resonance mistuning and power conversion parameters needed for the topology to operate as DCX. This analysis enables the practical implementation of DAB-SRC with an unfolder.

4. Control Techniques to Minimize Sector Distortions: Unfolding-based architectures can suffer from grid-current distortions known as sector distortions. These distortions increase total harmonic distortion (THD) and degrade system performance. We model the underlying causes of sector distortions and design control schemes to mitigate their impact. Experimental hardware results show a significant (about 50%) reduction in grid-current THD, demonstrating the effectiveness of the proposed methods.

1.3 Dissertation Structure

This dissertation adopts a multi-paper format, with Chapters 3 through 7 presenting individual research contributions. Chapter 2 provides a brief overview of the current state of technology in power architectures for DCFCs, 3-ϕ AC-DC converters, and power-sharing controls for modular converters, establishing the necessary background and context for understanding the advantages of the proposed architecture.

Chapter 3 presents the implementation of the complete MV converter architecture, including detailed simulation studies and experimental hardware validation. Chapter 4 explores the topology selection for DCX operation with an unfolder, detailing the design and hardware validation of a 10 kW SB-DCX module integrated with the unfolder. Chapter 5 develops predictive models for determining the minimum required dead time, enabling the practical use of the DAB-SRC topology for DCX operation. Chapter 6 introduces dynamic models for the SB-DCX topology, supporting accurate system-level design and stability

analysis. Finally, Chapter 7 documents the various causes of sector distortion in unfolding-based architectures and proposes control strategies to mitigate their impact on system performance.

CHAPTER 2

Technology Overview: High-Power AC-DC Converters & Power Sharing Controls

The power conversion system is central to the operation of DC fast-charging stations (DCFCs). High-power loads such as DCFCs are powered through the three-phase AC (3-ϕ) grid. In a DCFC station, multiple charging units are typically connected to the 3-ϕ AC grid. The conventional power distribution architectures for a DCFC station and their associated trade-offs are discussed in this chapter.

The power conversion system is responsible for converting 3-ϕ AC grid power into DC power suitable for charging EV batteries, while simultaneously meeting grid compliance requirements. These power converters are generally referred to as 3-ϕ AC-DC converters.

This chapter establishes the fundamental requirements for 3-ϕ AC-DC converters and provides an overview of current technologies, with a particular focus on applications in DCFCs. Direct medium-voltage-connected (MV-connected) power converters offer both cost and performance advantages over low-voltage (LV) interface converters by eliminating the need for bulky line-frequency transformers typically required for MV interconnection. Furthermore, unfolding-based converters can enhance performance by reducing the number of power conversion stages. However, the full potential of direct MV-connected converters has yet to be realized, and concerns persist regarding the long-term reliability of MV power electronic components.

Incorporating modularity into the system architecture can improve both reliability and performance. Effective power sharing among modules is essential to fully realize these benefits, although additional control strategies may be necessary to achieve optimal power balancing. A comprehensive review of power-sharing control techniques is presented in this chapter.

Opportunities for improvement in modular unfolding-based MV-connected power converters and power-sharing control methods are identified, and these advancements are incorporated into the proposed direct MV-connected unfolding-based converter architecture.

2.1 DC Fast Charging Stations: Power Distribution Architecture Review

High-power loads such as DCFCs are powered through the 3-ϕ AC grid. Unlike a 1-ϕ AC grid, a 3-ϕ AC grid provides a constant power draw, which eliminates the need for line-frequency energy buffering when supplying DC loads. Thus, for high-power loads supplied by a 3-ϕ AC grid, energy buffering is not a fundamental requirement.

A DCFC station typically includes multiple chargers that require power from the 3-ϕ grid. These chargers are commonly serviced through a line-frequency (LF) transformer connected to the primary distribution at medium voltage (4.16-34.5 kV). Deploying multiple chargers instead of a single-port charger allows the cost of MV interconnection to be distributed across several units, resulting in a combined power architecture that is more cost-effective [11, 12]. Furthermore, this approach facilitates the integration of energy storage and renewable energy sources, helping to mitigate negative impacts on the grid from the extreme power fluctuations associated with high-power, variable loads like EV fast chargers. Two commonly used power distribution architectures differ in how power is shared among individual chargers. In one approach, power is distributed via an AC bus; in the other, via a DC bus [12, 13].

In an AC distribution architecture (shown in Fig. 2.1), an LF transformer is used to step down the voltage from the MV grid, and power is then distributed as this stepped-down AC voltage. Each port—including chargers, energy storage systems, and renewable energy sources—has its own LV 3-ϕ AC-to-DC converter. While this approach is the most straightforward to implement, it results in a significantly higher total power conversion requirement. However, due to well-established protection schemes and standardized metrics, most commercial DCFCs currently deployed rely on AC distribution architectures, which benefit from a substantial body of research and mature standards [14].

In contrast, in a DC distribution architecture (shown in Fig. 2.2), a front-end AC-DC

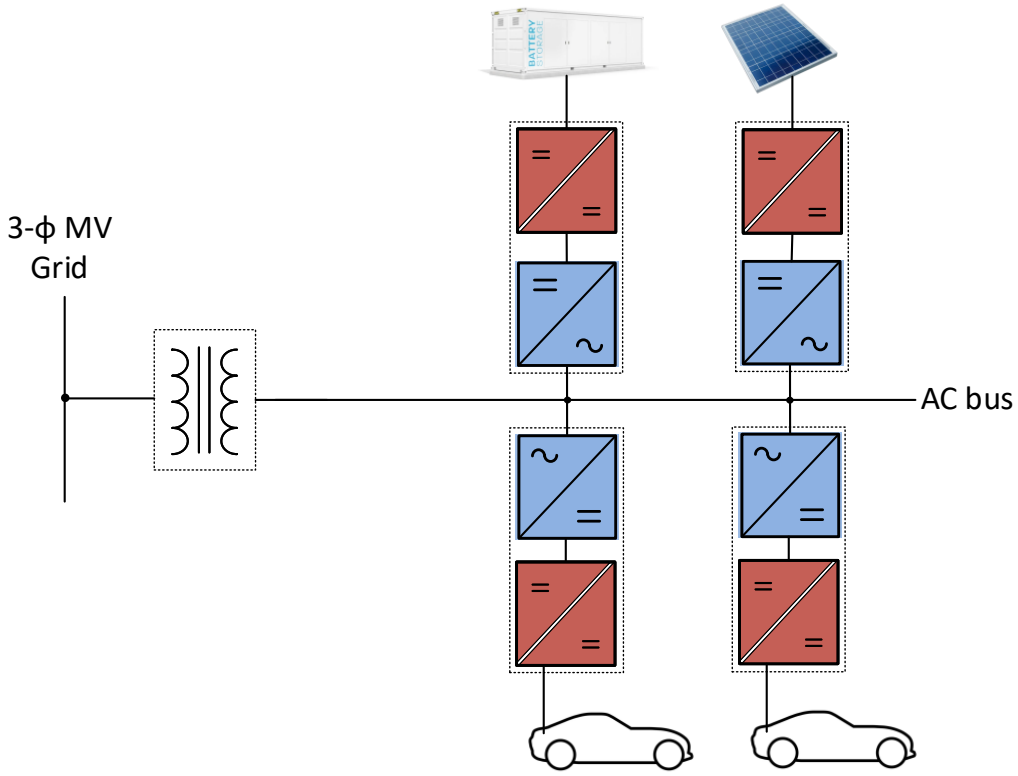


Fig. 2.1: DCFCs power architecture with AC distribution and MV-grid interconnection through line frequency transformer

converter generates a common DC bus (after the LF transformer), and power is distributed to each port via this DC bus. An isolated DC-DC converter is required to interface each port with the DC bus, as current standards mandate electrical isolation between individual ports [15]. This architecture provides a more straightforward method for integrating DC renewable energy sources and battery storage systems. Additionally, the overall power conversion effort is reduced compared to the AC distribution architecture.

The DC distribution architecture can be further improved by integrating the functionalities of the LF transformer with the front-end AC-DC converter into a direct MV-connected AC-DC power converter with isolation provided by high-frequency power electronics (shown

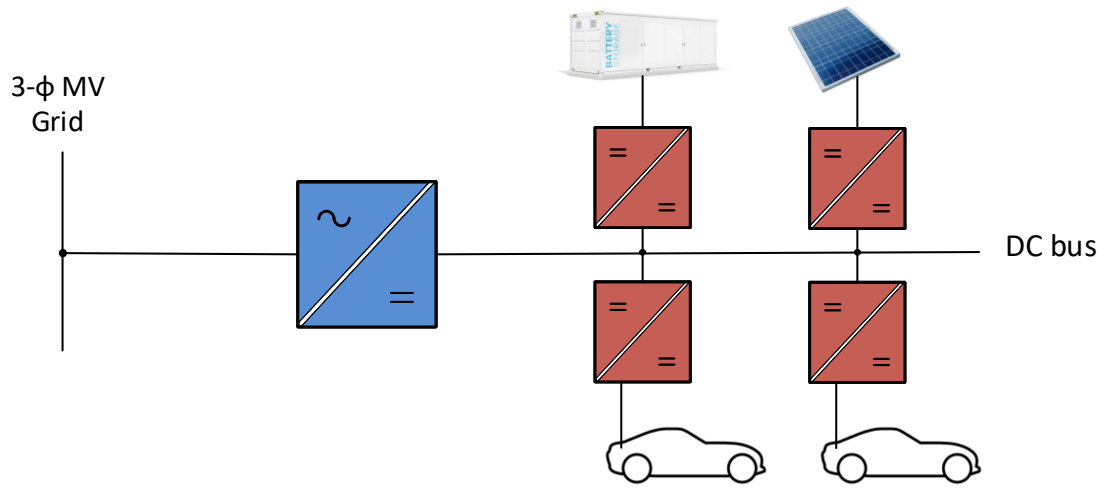


Fig. 2.2: DCFCs power architecture with DC distribution and MV-grid interconnection through line frequency transformer

in Fig. 2.3)—a configuration commonly referred to as a solid-state transformer (SST) [8]. This integration can enhance performance and reduce the overall cost of the power conversion system. MV-based power conversion architectures connect directly to primary distribution voltages, thereby bypassing the cost and size disadvantages associated with bulky grid-frequency transformers [16]. Medium-frequency (MF) transformers provide the necessary galvanic isolation while potentially decreasing the overall system footprint. MV architectures can offer higher power conversion efficiencies and lower system costs compared to conventional low-voltage solutions. Furthermore, in the context of DCFCs, MV converter architectures provide additional advantages, including significant reductions in cabling costs for power distribution [8].

Moreover, to improve the utilization of MV infrastructure and enable additional functionalities, *hybrid distribution* (Fig. 2.4)—comprising both AC and DC networks—has been actively explored [17, 18]. The coexistence of AC and DC distribution facilitates seamless integration of a wide range of load types and generation sources, while enhancing the flexibility, scalability, and efficiency of MV hardware deployment.

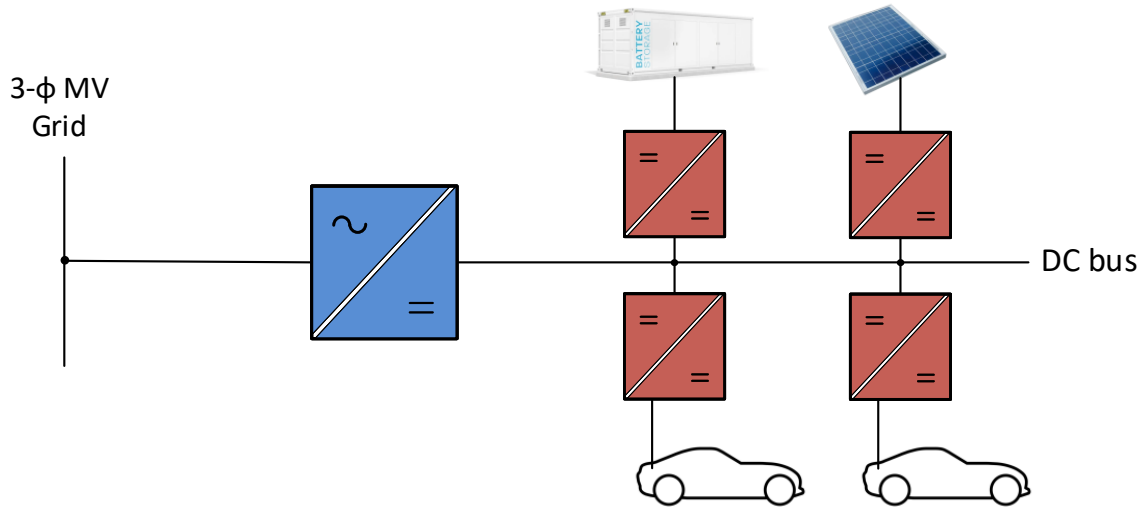


Fig. 2.3: DCFCs power architecture with DC distribution and MV-grid interconnection through a solid state transformer

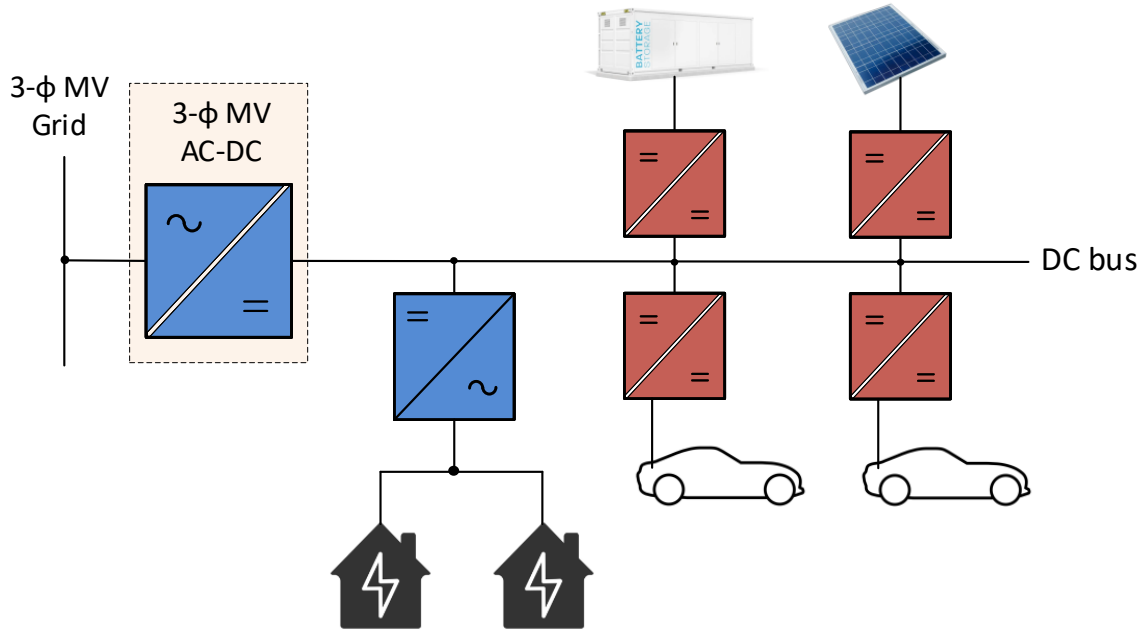


Fig. 2.4: DCFC power architecture with both AC and DC distribution enabled via a solid-state transformer

To enable simultaneous AC and DC distribution, the SST-based power conversion architecture typically follows a cascaded topology. It consists of an MV AC–DC converter to generate a low-voltage DC bus, followed by a DC–AC inverter to provide a 3-ϕ low-voltage AC output. The DC–AC inverter is conventionally implemented as a three-leg inverter, which can be controlled to operate either as a voltage source or a current source, depending on system requirements [19]. Multiple different topologies can be employed for the MV AC–DC converter, and a detailed review of these options is necessary to understand the fundamental requirements, trade-offs, and identify opportunities for further advancement.

2.2 MV Three-phase AC-DC Converters: Review

The core functional requirements of MV-connected 3-ϕ AC-DC converters include MV blocking capacity at the input, establishing an ideal unity input power factor (PF) with low current total harmonic distortion (THD) in compliance with grid requirements, providing controlled power at the required DC output voltage, and maintaining galvanic isolation. These requirements can be represented by the equivalent circuit shown in Fig. 2.5. Furthermore, converters that provide at least two independently controlled current sources at the input are sufficient, since the input of the converter can be modeled as a star-connected load that requires exactly two independent current sources for complete control.

Multiple converter topologies have been explored to achieve these requirements [12, 16, 20, 21]. It is important to categorize these topologies to understand their respective trade-offs and to identify the most suitable solutions and areas of improvement for high-performance EV charging systems. The categorization of different converter topologies is summarized in Fig. 2.6.

The 3-ϕ AC grid can be viewed as consisting of three 1-ϕ AC voltages. One approach to achieving 3-ϕ AC-DC power conversion is to use three independent 1-ϕ AC-DC converters as shown in Fig. 2.7, referred to as phase-modular systems (terminology borrowed from [20]). These converter architectures enable existing knowledge of single-phase converters to be extended to three-phase systems, albeit with increased implementation effort [22]. In contrast, direct 3-ϕ systems interface with all three phases simultaneously. They require

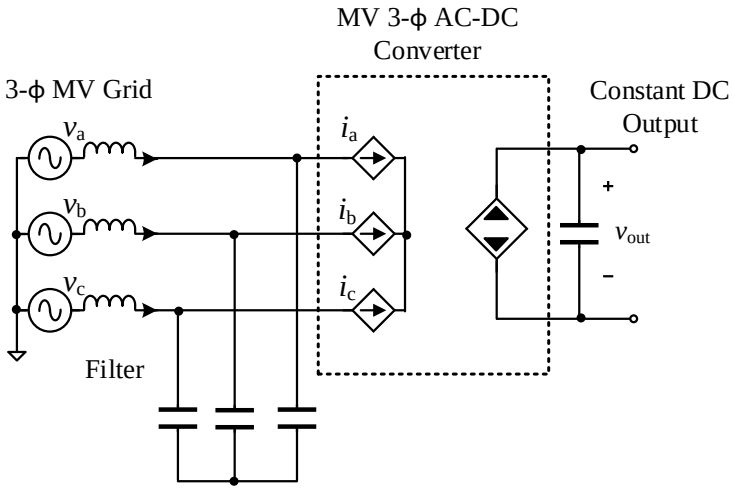


Fig. 2.5: Equivalent circuit representing the fundamental requirements of a 3-ϕ AC-to-DC power converter. The 3-ϕ grid input is modeled as ideal, independently controlled current sources to enable PFC. The converter output is represented as a constant power source with appropriate electrical isolation from the input side.

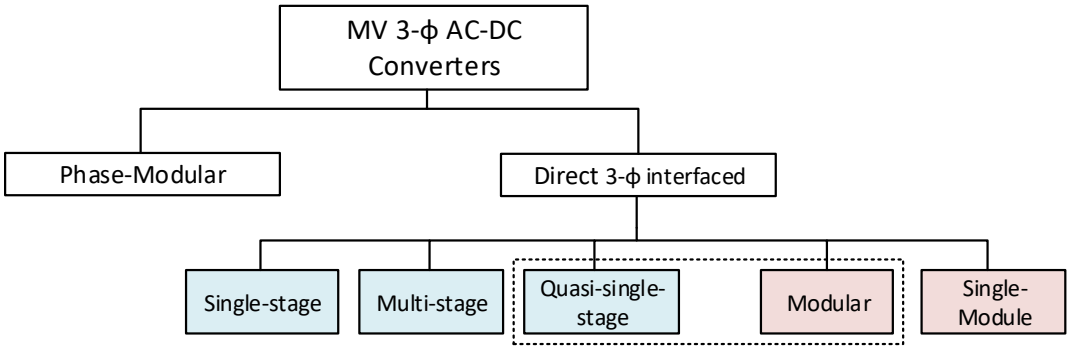


Fig. 2.6: Categorization of fully active MV 3-ϕ AC-DC converter topologies. The proposed architecture expands on quasi-single-stage modular power converter topologies.

fewer switches and impose lower sensing and signal processing demands. Therefore, only direct three-phase systems are considered in this work.

Direct 3-ϕ AC-DC converters can be further categorized based on the number of high-frequency power conversion stages. These converters typically employ a multi-stage architecture [20] to simplify implementation and meet the core requirements described earlier. A typical two-stage architecture (see Fig. 2.8) consists of two cascade-connected converters:

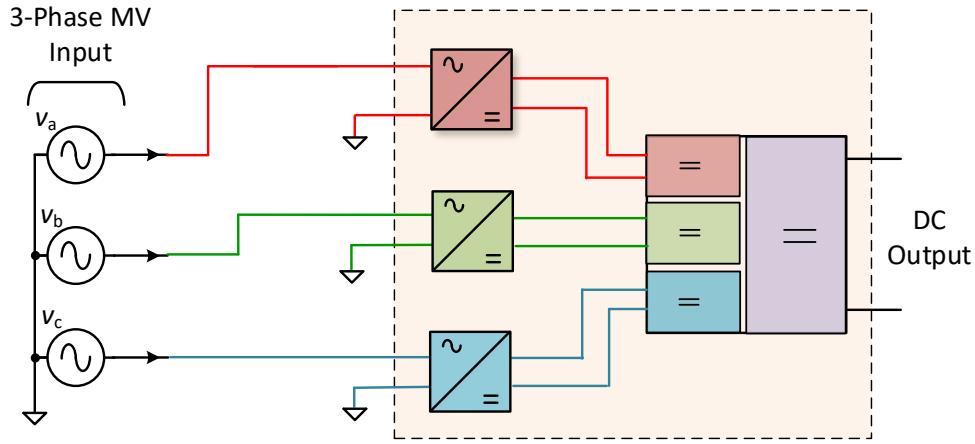


Fig. 2.7: Block diagram of a phase-modular implementation of a MV 3-ϕ AC-DC converter. Each phase consists of a similar structure with a 1-ϕ front-end AC-DC converter. The back-end DC-DC stage can be implemented separately or combined, depending on system requirements.

an active front-end (AFE) rectifier followed by a DC-DC converter [20]. The AFE rectifier performs power factor correction (PFC), while the DC-DC converter provides isolation and tight output voltage regulation. A two-stage architecture often includes a large decoupling capacitor to separate the dynamics of the two power conversion stages, which simplifies hardware and controller design but can limit overall performance.

In contrast, single-stage architectures (see Fig. 2.9) eliminate one power-processing stage, potentially offering higher performance [23]. In this configuration, all converter requirements—DC output power conversion, PFC, and isolation—are handled by a single stage. This approach can improve system efficiency and eliminate the need for bulky decoupling capacitors, thereby enhancing performance. However, implementing a single-stage architecture requires four-quadrant (4-Q) operation of the switches and introduces significant control complexity, making both design and achieving reliable performance challenging.

Quasi-single-stage architectures that integrate an unfolding stage offer a promising balance, achieving improved performance characterized by higher efficiency and power den-

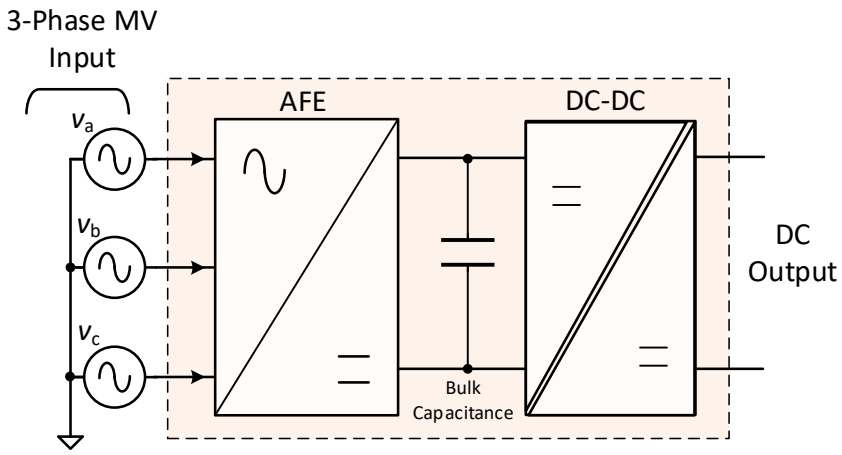


Fig. 2.8: Block diagram of the conventional two-stage implementation of a direct 3-ϕ AC-DC converter. An AFE stage is used for power factor correction, followed by an isolated DC-DC stage. Bulk capacitance is required to decouple the two stages, which can reduce overall system performance and reliability.

sity [24, 25]. These architectures consist of a line-switched unfolder (also referred to as an input voltage selector) followed by a DC-DC converter as shown in Fig. 2.10. Since the unfolder switches at line frequency without needing energy buffering, it is not counted as a power processing stage. The DC-DC converter is then responsible for fulfilling the three primary objectives of an AC-DC converter: voltage regulation, PFC, and isolation. Because there is only a single high-frequency power-processing stage, unfolding-based AC-DC architectures have the potential to achieve higher efficiency and power density compared to conventional multi-stage systems. Furthermore, they avoid the need for 4-Q switches in the high-frequency power conversion stage, which provides a significant advantage over single-stage topologies. This work explores unfolding-based converter architectures due to their potential for higher performance compared to multi-stage implementations, without the need for 4-Q switches.

MV-connected 3-ϕ AC-DC converters can also be categorized based on modular versus single-module implementations. Recent advancements in high-voltage silicon carbide (SiC) MOSFETs, with blocking capabilities of up to 10-15 kV, have enabled the development of single-module converter designs [26, 27], which can reduce overall system complexity.

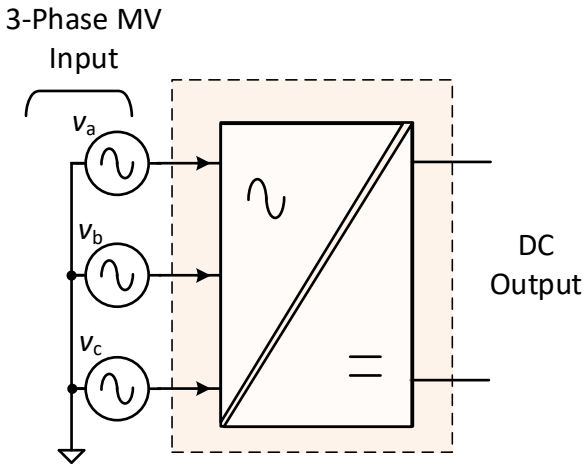


Fig. 2.9: In a single-stage implementation, all converter requirements must be managed within a single conversion stage. This necessitates the use of 4-Q switches to handle the input voltage, making the operation more challenging.

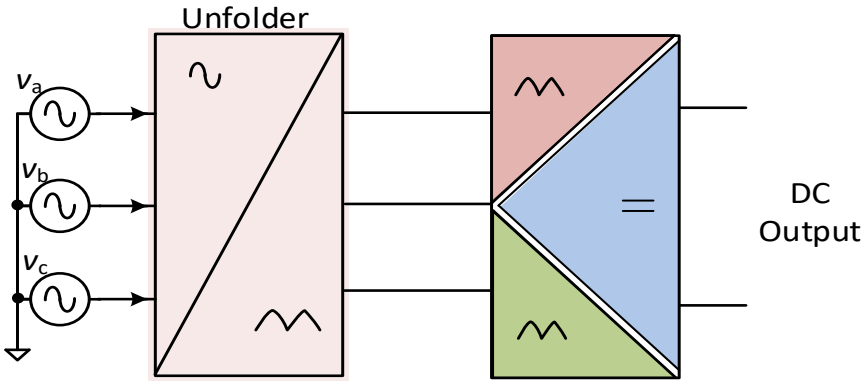


Fig. 2.10: The quasi-single-stage implementation employs line-side unfolder switches to eliminate the need for four-quadrant (4-Q) switches, enabling a single high-frequency power processing stage.

However, this technology remains in its early stages and requires further refinement for widespread adoption.

Conversely, modular implementations can deliver improved performance and higher reliability, as highlighted in recent reviews [28]. Modular systems can continue operating

even in the event of partial module failure and offer additional advantages such as flexibility, scalability, and ease of maintenance. Therefore, modular architectures are preferred for MV-connected power converters in this work. Nevertheless, modular converters require additional control strategies to ensure effective power sharing among modules.

2.3 Power Sharing Controls: Review

Commonly, MV converter architectures consist of an ISOP configuration of multiple converter modules. Modularity helps realize the required input voltage blocking capacity, voltage step-down, and high power conversion capacity. Modularity enables direct MV connection and provides an opportunity to improve the reliability of power conversion systems.

However, the input MV voltage (or power) doesn't naturally share among the series-connected modules [29]. This is fundamental because, for natural voltage sharing in closed-loop operation, the individual module's power control loop needs to be perfectly tuned and synchronized with each other. However, component tolerances and timing mismatches don't allow these ideal conditions, resulting in unequal voltage (and power) sharing. Therefore, additional voltage-sharing controls are required to avoid catastrophic failure.

Voltage sharing control structure can be categorized based on the extent of communication required - centralized, distributed, and decentralized [30]. Centralized controls require a master controller that communicates with all the other modules to ensure voltage sharing. The central controller is a single point of vulnerability that can result in global failure [29]. Distributed controls consist of a single communication line between all modules. Distributed controls need less communication infrastructure but the single communication line remains a vulnerability. Decentralized controls ensure voltage sharing without the need for communications. Hence, promising maximum reliability and opportunities for expandability and interoperability. Therefore, MV converter architectures that have decentralized controls are more reliable and scalable.

Droop controls have been predominantly utilized as decentralized controls [31, 32]. However, the inherent droop control logic entails a trade-off between voltage regulation and power sharing. An ideal decentralized control approach is proposed in [33], where

power-sharing information is encoded in the frequency of the output voltage. However, this method requires additional decoding circuitry for all modules, making its implementation cumbersome. Another approach in [29] suggests operating with novel non-linear controls. Although effective at low power, its performance under high power or time-varying input voltages remains unverified. An interesting approach is presented in [34]. Each module in the ISOP configuration operates as a DCX. Since the output of each module is in parallel and the module operates at a fixed voltage conversion ratio, it imposes a constraint on the input voltage, ensuring voltage sharing. This fully decentralized control approach will be extended to an unfolding-based architecture.

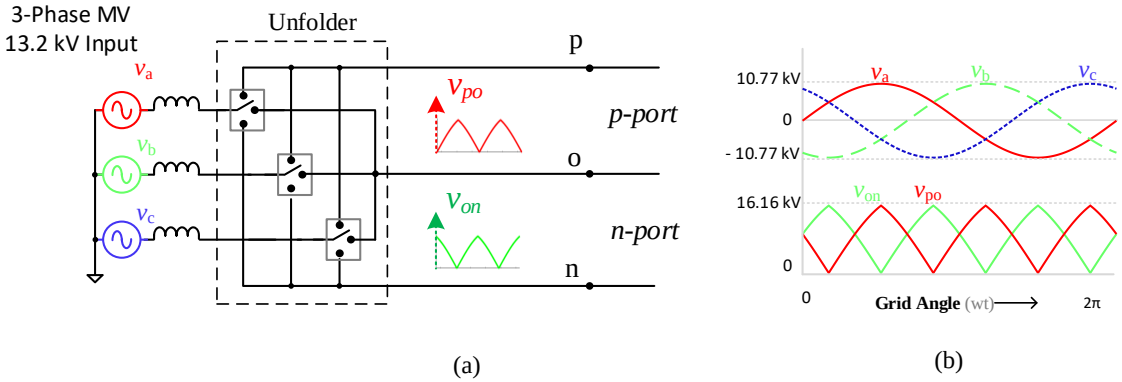
2.4 Improvement in Unfolding-based MV Converter Architecture & Power Sharing Controls

Power distribution architectures with hybrid power distribution—comprising both AC and DC distribution buses—enable better utilization of high-power conversion infrastructure, particularly in systems employing direct medium-voltage (MV)-connected power electronics. The hybrid distribution allows seamless interfacing with a diverse range of loads, thereby enhancing system utilization. Moreover, it combines the respective advantages of both AC and DC distribution systems.

As discussed earlier, the unfolding-based quasi-single-stage architecture offers performance benefits compared to conventional multi-stage solutions [35]. With fewer cascaded power-processing stages, unfolding-based converters can achieve higher efficiency. Therefore, a modular MV-connected unfolding architecture combined with hybrid distribution presents a compelling solution for the power conversion needs of DCFCs.

Each unfolder output has two terminals—referred to as the *p-port* and *n-port* (Fig. 2.11(a)), with the corresponding voltage waveforms shown in Fig. 2.11(b). The unfolder is implemented using a single-pole triple-throw (SPTT) switch, and its practical realization is illustrated in Fig. 2.12. This circuit converts the 3-ϕ AC voltage into two time-varying DC voltages without requiring high-frequency switching or energy buffering. The unfolder operates by switching six times per grid cycle, dividing the full 2π period into six equal

sectors.



(a) (b)

Fig. 2.11: (a) Ideal unfolder implementation using a single-pole triple-throw switch, which connects each phase input voltage (13.2 kV) to node p, o, or n as required. (b) Input phase voltages and the resulting v_{po} and v_{on} port voltages.

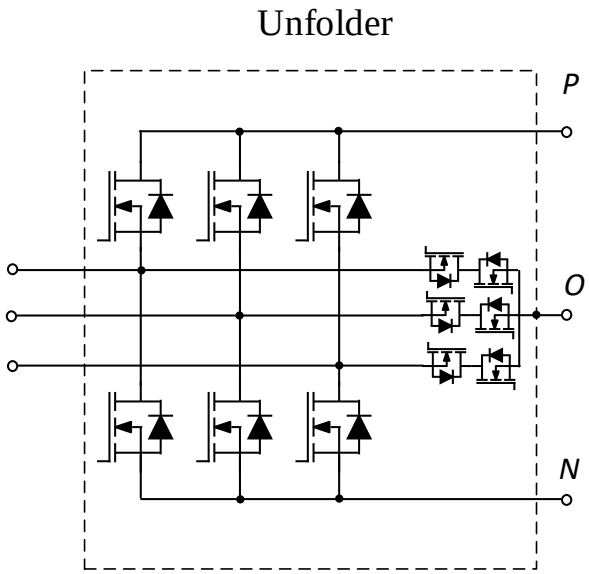


Fig. 2.12: Practical implementation of the unfolder using MOSFET switches. The o-node switches must support bidirectional voltage blocking and therefore require two MOSFETs in a cascode configuration.

The current state-of-the-art system employing a modular unfolding-based architecture for MV-connected power conversion features a hybrid distribution, as illustrated in Fig. 2.4. The complete block structure, with each power conversion stage highlighted, is shown in Fig. 2.13.

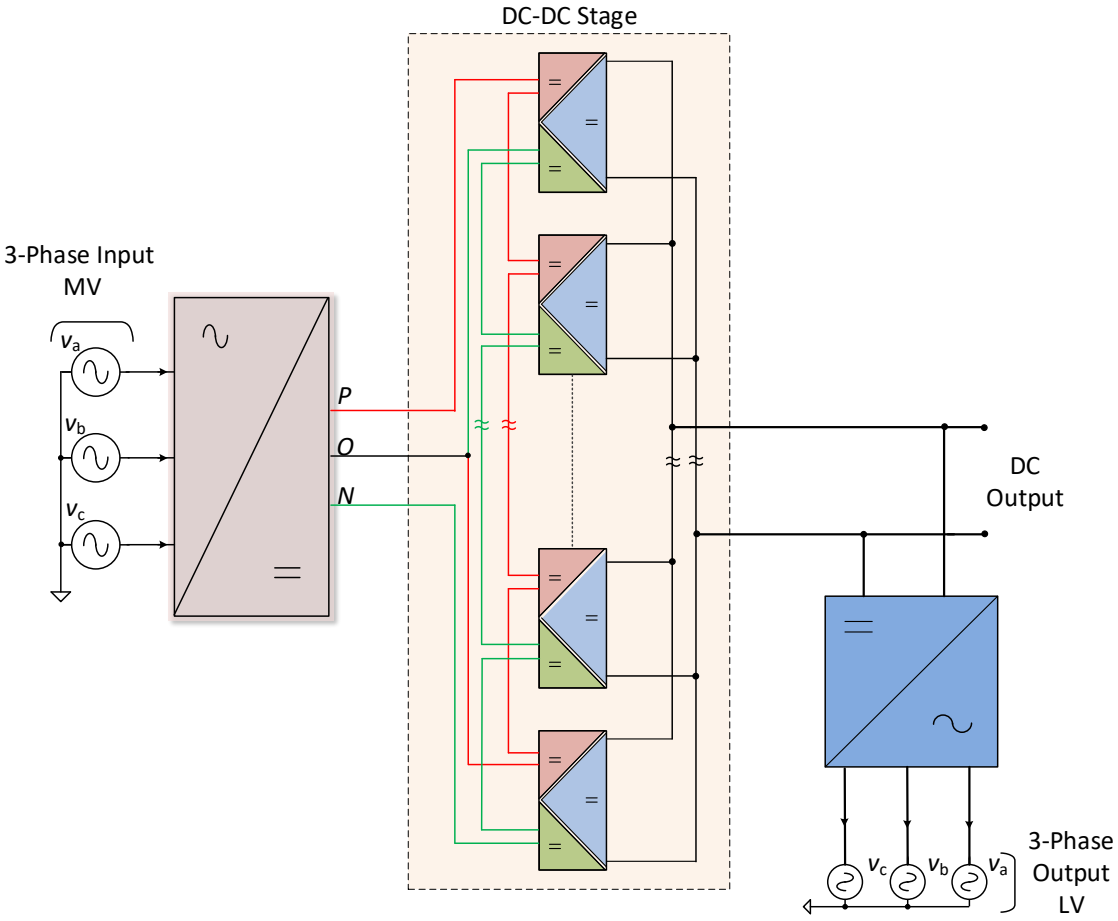


Fig. 2.13: Current state-of-the-art MV-connected unfolding-based power converter with hybrid distribution. A modular DC-DC stage using three-port converters interfaces the input from the unfolder output to the DC output bus. An additional DC–AC stage is included to generate the 3-ϕ low-voltage (LV) AC output.

The input unfolder converts the 3-ϕ AC input into two time-varying voltages: v_{po} and v_{on}. A modular configuration of three-port converters is required to interface with these unfolder outputs and maintain a regulated DC output bus. Each three-port converter

must perform power factor correction (PFC) at the input, regulate the output voltage, and provide galvanic isolation [36]. A comprehensive summary of the various converter topologies that can be used in conjunction with an unfolder to achieve these objectives and enable effective AC-DC conversion is provided in [37]. Additionally, a secondary stage is required to generate an AC output from the DC bus.

Furthermore, the modular DC-DC stage requires additional power-sharing controls to ensure voltage balancing across the unfolder ports. Decentralized control strategies, such as droop control, are difficult to implement in this context due to the complexity of managing voltage balance in a three-port converter topology. As a result, centralized control schemes are typically employed [38]; however, they introduce a single point of failure and may compromise system reliability. The need for additional control mechanisms within an already complex power conversion stage further increases implementation challenges.

Scope for Improvements:

- Development of decentralized control strategies for modular power sharing in unfolding-based architectures
- Simplification of control schemes and reduction of operational complexity in the DC-DC stage
- Minimization of power-processing stages in MV AC to LV AC conversion paths to improve system efficiency

This work introduces a novel architecture that enables natural voltage sharing among the modules in the DC-DC stage, thereby establishing fully decentralized voltage balancing control. Furthermore, the DC-DC stage operates as a passive DC transformer (DCX), eliminating the need for active control and significantly simplifying the implementation of the modular structure. The DC-DC stage is henceforth referred to as the *DCX stage*. Finally, the DCX stage facilitates a single high-frequency power conversion path from MV

3-ϕ AC to LV 3-ϕ AC, resulting in substantial improvements in both performance and overall system efficiency.

2.5 Proposed Direct MV-connected Unfolding-based Architecture with Hybrid Distribution and Natural Voltage Sharing

We propose a novel unfolding-based power converter architecture to directly connect high-power loads, such as DCFCs, to the MV grid. The architecture, illustrated in Fig. 2.14, supports both AC and DC distribution, providing flexibility and opportunities to leverage the advantages of each approach. Having both AC and DC outputs enables better utilization of MV hardware by allowing the system to interface with a wider variety of loads. MV integration is achieved through the DCX stage, which consists of an ISOP configuration of DC-DC modules, each functioning as a DCX to enable fully decentralized power-sharing controls. These modules provide the necessary isolation and voltage step-down, facilitating the provision of both LV 3-ϕ AC and DC output ports.

This architecture includes both an input (MV) unfolder and an output (LV) unfolder. The MV unfolder converts the MV 3-ϕ AC input into soft DC-link voltages, which are supported by multiple DC-DC modules arranged in an ISOP configuration. Each module functions as a DCX. A DCX, or "DC transformer," is a class of converter designed or controlled to operate at a fixed voltage conversion ratio [39, 40]. DCX-based DC-DC modules enable natural input voltage sharing without requiring inter-module communication, thereby realizing fully decentralized voltage-sharing controls and enhancing system reliability. Since the outputs of the modules are paralleled and each operates at a fixed voltage conversion ratio, the input voltages are inherently constrained to be shared among the modules, ensuring natural voltage balancing.

Furthermore, the output of the paralleled DC-DC modules is used to generate a DC output for charging EV loads through an additional DC-DC converter. Additionally, the output is employed to obtain a 480 V 3-ϕ AC output via the LV unfolder, facilitating the connection of both DC and conventional AC loads and thereby enhancing overall hardware utilization.

The complete hardware implementation and experimental validation of the proposed architecture are presented in Chapter 3. Particular attention is given to the implementation of the DCX stage, which poses significant design and integration challenges. A detailed discussion of its implementation and corresponding hardware validation is provided in Chapter 4.

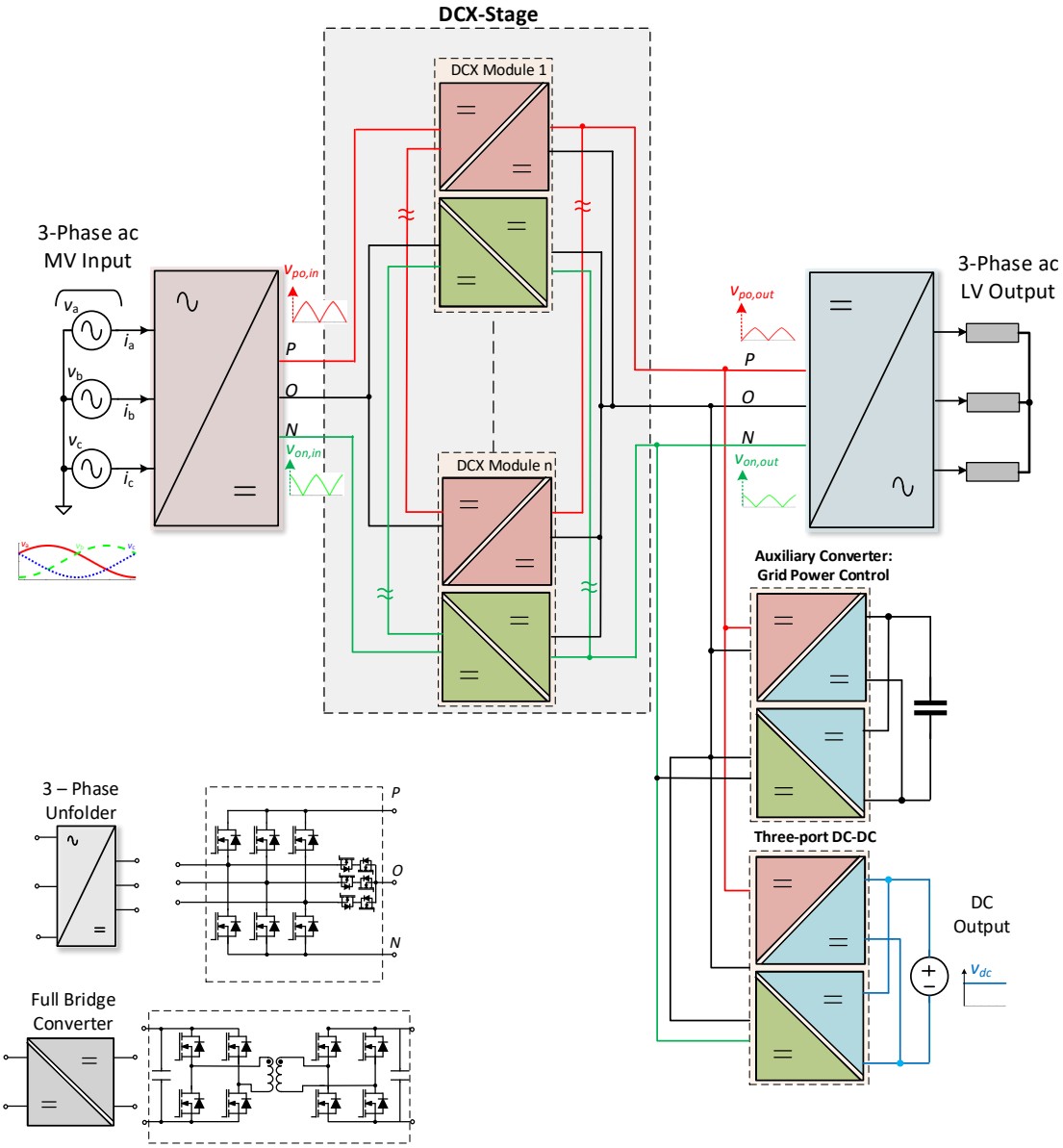


Fig. 2.14: DCX-based MV converter architecture. The DCX modules are connected in an ISOP configuration to step down the MV input to 480 V AC. Additionally, the output of the DCX modules can charge a vehicle battery via a DC-DC converter.

CHAPTER 3

Novel SST Architecture with Hybrid Power Distribution and Natural Voltage Sharing in a Modular Structure

The detailed implementation and validation of the proposed architecture are presented. Apart from the unfolder, the proposed architecture consists of a DCX stage, a three-port converter for DC output, and an auxiliary converter for reactive power control. The implementation of each of the stages is discussed, including topology selection and operational principles. While the DCX stage implementation is introduced here, detailed modeling and design are covered in Chapter 4.

Furthermore, simulation validation is provided for the complete system processing up to 1 MW of power with a 13.2 kV MV AC input. The simulations confirm ideal voltage sharing among the series-connected modules and demonstrate the feasibility of a single high-frequency power conversion stage from 13.2 kV AC to 480 V AC without the need for switches with bidirectional voltage-blocking capability. Hardware results are presented for the complete architecture, validating natural voltage sharing in the modular DCX stage, dual DC and AC outputs, and reactive power control via the auxiliary converter.

Three-Phase Unfolding-based Modular Solid State Transformer with Multi-port Output

Sanat Poddar, *Student Member, IEEE,* Regan Zane, *Fellow, IEEE*

***Abstract*—Unfolding-based three-phase (3-ϕ) grid-tied converter architectures offer a more efficient and power-dense alternative to conventional multi-stage designs by reducing the number of high-frequency power conversion stages. This paper presents a 3-ϕ unfolding-based solid-state transformer (SST) architecture with multi-port capability, enabling simultaneous delivery of 3-ϕ ac and regulated dc outputs. This enhances hardware utilization and provides greater flexibility for serving diverse load types. The 3-ϕ ac-ac conversion is realized using a single high-frequency stage, greatly improving performance. The modular design supports medium-voltage (MV) ac grid integration and includes a step-down dc transformer (DCX) stage that enables natural voltage sharing across input series-connected modules, improving system reliability and scalability without centralized control. An auxiliary converter is integrated to enable independent reactive power control, ensuring grid compliance while processing only reactive power. Key implementation challenges addressed include the non-trivial topology selection for the DCX stage and the design of converter stages capable of operating with the time-varying voltages inherent to unfolding-based systems. The proposed architecture is validated through comprehensive simulations of a 13.2 kV/1 MW-rated system and experimental results from a 480 V/1 kW laboratory prototype, demonstrating effective hybrid ac and dc operation, reliable voltage sharing, and reactive power control. The 3-ϕ ac–ac power conversion stage achieves an efficiency of 96.5%.**

***Index Terms*—Solid-state transformer, SST, three-phase, ac-ac, unfolding, multi-port, medium-voltage, MV, DCX, dc transformer, decentralized, modular, input-series, ISOP, resonance, series-bridge, SB**

I. Introduction

THE growing demand for electric energy necessitates continuous advancements in grid-tied power conversion systems [1]. The electrification of transportation through electric vehicles (EVs) and the expansion of energy-intensive data centers are among the key drivers of rising electricity consumption. Three-phase (3-ϕ) grid-tied power converters are essential for interfacing these high-power loads with the grid. Additionally, they are a critical enabling technology for integrating renewable energy sources [2]. Consequently, improvements in the performance, reliability, and cost efficiency of these converters are increasingly essential.

Solid-state transformers (SSTs) have emerged as a promising technology to enhance energy conversion performance, reduce costs and system size, and enable advanced control of grid-connected systems [3], [4]. SSTs replace bulky line-frequency transformers with power electronic converters, allowing the use of high-frequency transformers that offer significant advantages. This is particularly beneficial for eliminating conventional medium-voltage to low-voltage (MV-to-LV) line-frequency service transformers in secondary distribution networks, enabling direct integration of MV-rated power electronics for applications such as multi-megawatt fast-charging stations and data centers [5], [6]. Direct MV connection reduces installation time, minimizes system footprint, and can lower both capital costs and material usage [7].

To support MV grid integration, SSTs are typically implemented in a modular fashion to scale in voltage and power [8], [9]. A common approach is the Input-Series Output-Parallel (ISOP) configuration, where multiple converter modules are connected in series on the input to handle MV levels, and in parallel on the output to meet current demands. Alternatives include the series connection of discrete semiconductor devices or the use of high-voltage (HV) devices [10], [11], though these approaches face challenges such as limited performance and the immaturity of HV switch technology. Modular or multilevel converter topologies are generally preferred for MV SST applications due to their scalability and enhanced reliability.

SSTs often employ multistage architectures [12], [13]. Their primary functional requirements include grid current shaping, galvanic isolation, and generation of regulated dc and ac outputs. These are typically achieved using two or more power conversion stages to simplify control demands while avoiding the use of four-quadrant switches. A typical state-of-the-art ac-ac SST consists of an ac-dc stage for grid current shaping, a dc-dc stage for isolation and regulated bus generation, and a dc-ac stage for output generation [14], [15]. Intermediate bulk dc-link capacitance is often required to decouple stage dynamics and facilitate reactive power control. However, these multistage architectures may suffer from reduced efficiency due to cumulative losses and the need for bulky energy storage components.

Unfolding-based architectures allow for quasi-single-stage power conversion and have emerged as competitive alternatives for 3-ϕ ac-dc grid-tied converters [16]–[20]. These systems use a line-switched unfolder operating at twice the line frequency to convert 3-ϕ ac voltages into two time-varying soft dc-link voltages (or vice versa). By reducing the number of high-frequency switching stages, these architectures offer improved efficiency and power density compared to traditional designs [17].

Most prior work on unfolding-based SSTs has primarily focused on ac–dc or dc–ac conversion at either MV or LV

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levels. Reference [21] does explore ac–ac conversion, but the output ac frequency differs from the input. Moreover, existing modular approaches for MV applications typically require active control to maintain voltage balance, which complicates scalability. This work extends the benefits of unfolder-based designs to 3-ϕ ac–ac SST architectures by proposing a modular implementation that supports the same input and output frequency and achieves natural voltage sharing without the need for active balancing control.

This article proposes a 3-ϕ unfolding-based SST capable of multi-port output with hybrid 3-ϕ ac and dc distribution (see Fig. 1), using a single high-frequency power conversion stage for ac–ac conversion. The proposed ISOP modular implementation supports MV ac input and enables natural voltage sharing. Furthermore, it supports reactive power control through an auxiliary converter.

The system operates from a 3-ϕ MV ac input and delivers both 3-ϕ ac and regulated dc outputs. The MV unfolder converts the 3-ϕ ac input into two time-varying dc voltages ranging from 0 to 0.866 of the line-to-line peak ac voltage. A DCX stage, acting as an ideal dc transformer, provides galvanic isolation and voltage step-down, producing time-varying dc voltages at its outputs. These are then unfolded to generate a 3-ϕ LV output, achieving quasi-single-stage conversion from MV ac to LV ac.

Simultaneously, a constant dc output bus can be derived from the DCX stage using a dc-dc conversion stage. The resulting hybrid ac/dc distribution architecture enhances flexibility and allows efficient utilization of the MV–LV power conversion stage (the DCX stage), which is often the cost driver in direct-MV-connected converters [22].

The ISOP DCX stage facilitates natural voltage sharing, enabling a fully decentralized control strategy that improves reliability and reduces cost [23], [24]. An auxiliary converter is added to shape grid currents and support reactive power control. Importantly, this converter only circulates reactive power and does not handle full load power, ensuring efficient and compliant grid interfacing.

Overall, the proposed SST architecture offers significant advantages over conventional three-stage designs for applications requiring both ac and regulated dc outputs [25], [26]. By using an unfolder, the architecture reduces high-frequency conversion stages from three to one for ac–ac conversion. The modular MV–LV DCX stage enables natural input voltage sharing and can interface with multiple dc-dc converters to provide multiple regulated dc outputs. Additionally, the architecture allows for reactive power control and eliminates the need for intermediate energy storage. The proposed SST architecture provides a scalable, efficient solution for hybrid ac/dc distribution systems, with potential applications in high-power EV charging, data centers, and renewable integration.

In summary, the key contributions of this work are:

1) Introduction and validation of a 3-ϕ unfolding-based SST architecture that enables quasi-single-stage MV ac to LV ac conversion, providing both 3-ϕ ac and regulated dc outputs while improving efficiency and reducing stage count.
2) Realization of a modular ISOP DCX stage compatible with time-varying dc voltages, enabling natural voltage sharing across series-connected modules and improving scalability without centralized control.
3) Development of an auxiliary converter that operates from time-varying dc voltages, offering independent reactive power control and grid current shaping, without processing full load power.

The remainder of this article is organized as follows: Section II provides an overview of the architecture and introduces the system's key components, including the unfolder, DCX stage, three-port dc-dc converter, and auxiliary converter. Section III discusses the selection and design of DCX module topologies and their scalability for high-power applications. Section IV details the implementation of the three-port dc-dc and auxiliary converters. Section V presents simulation results for a 1 MW system, and Section VI describes experimental results from a 1 kW prototype, demonstrating ac/dc outputs, voltage sharing, and reactive power control.

II. Architecture Overview

The proposed architecture is centered on the use of 3-ϕ unfolders in combination with an ISOP modular configuration of DCX-operated dc-dc converters (the DCX stage). This achieves a quasi-single-stage MV-to-LV ac power conversion with natural voltage sharing among the input series-connected converters. Additionally, further converter stages can be interfaced with the low-voltage output of the DCX stage to provide a regulated dc port and to enable grid harmonic compensation and reactive power control as needed.

The input MV unfolder converts the 3-ϕ MV ac input into two time-varying dc voltages ranging from 0 to 0.866 of the line-to-line peak voltage. These two time-varying soft dc-link voltages, denoted as v_{po} and v_{on}—referred to as the p-port and n-port voltages, respectively—are illustrated in Fig. 2. The unfolder operates at a frequency on the order of the line frequency to produce these two time-varying voltages from the 3-ϕ ac input. A detailed explanation of the unfolder's switching operation is provided in [17], [18]. Since the unfolder does not require high-frequency switching or associated energy storage, its losses are negligible, and it is not classified as a power-processing stage.

The time-varying voltages are stepped down by the DCX stage, which comprises an ISOP modular configuration of full-bridge dc-dc converters, each operating as a DCX (see Fig. 1). This stage provides galvanic isolation and steps down the voltage at each port (p and n). Each port features an input series connection of full-bridge dc-dc converters that enable MV operation and provide the required voltage step-down. The voltage step-down ratio is determined by both the number of series-connected dc-dc converters and the transformer turns ratio. The stepped-down output voltage of the DCX stage is

$$v_{\text{out,port}} = \frac{v_{\text{in,port}}}{n \times N}, \tag{1}$$

where n is the number of modules in the ISOP configuration for the respective port, and N is the transformer turns ratio (P:S).

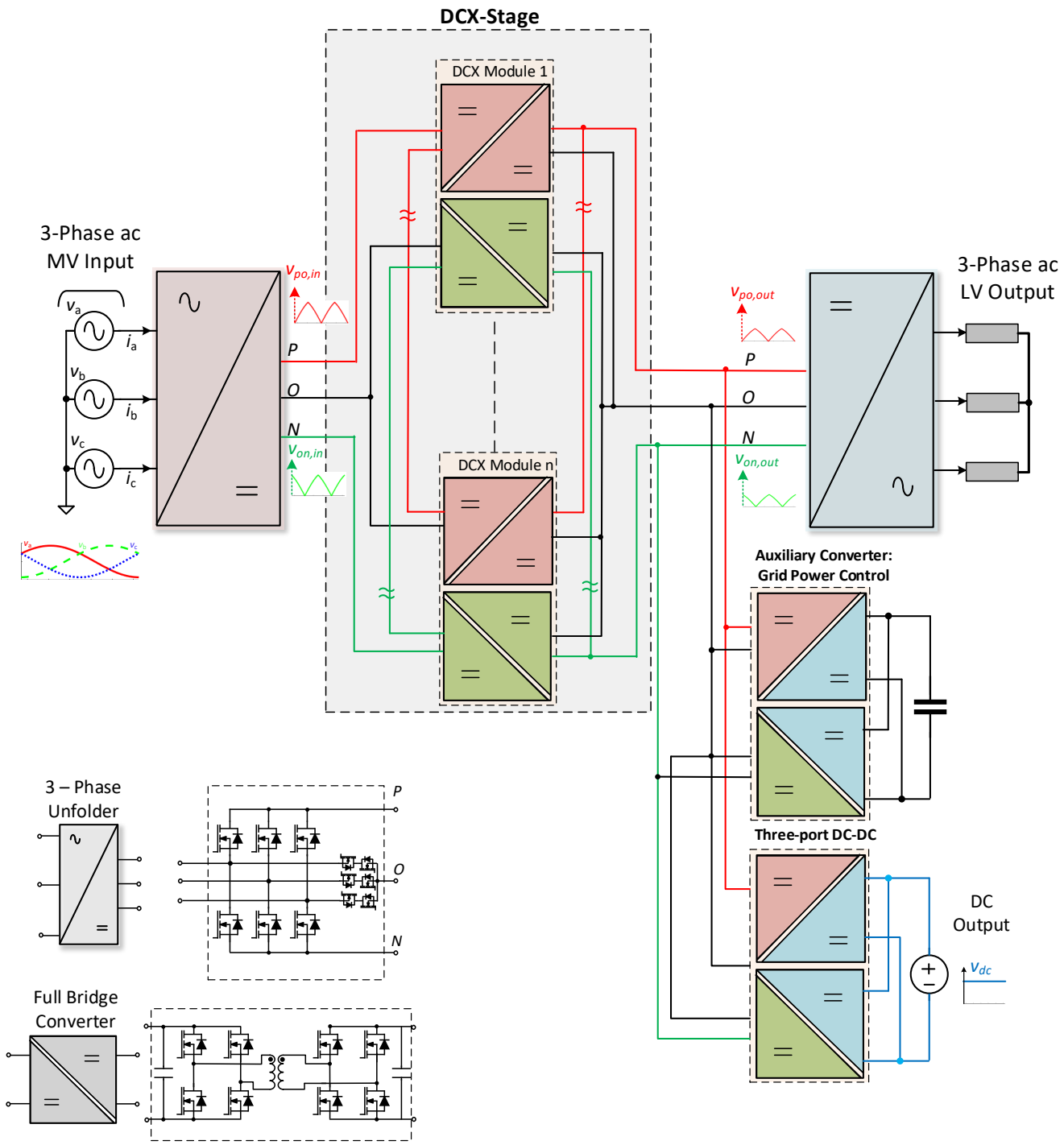


Fig. 1. Block diagram of the proposed unfolding-based solid-state transformer with multi-port output. The architecture includes a DCX stage that provides voltage step-down and galvanic isolation between the MV input and the 3-ϕ LV outputs. An additional converter shapes the MV input currents, functioning as an active filter to ensure compliance with grid power quality requirements and reactive power control. Furthermore, a dc-dc converter generates a regulated dc bus from the DCX stage output.

Operating each dc–dc converter in DCX mode enables natural input voltage sharing within the ISOP configuration, facilitating fully decentralized control—a critical feature for modular MV 3-ϕ ac grid-tied converters [27]. In steady-state DCX operation, the output voltage of each dc-dc converter depends solely on its input voltage and transformer turns ratio. With DCX operation and identical transformer turns ratios, all output parallel-connected modules share the same differential input voltage. This ensures natural input voltage sharing, resulting in robust performance with minimal control complexity and cost [27], [28].

The stepped-down output voltages of the DCX stage can be unfolded using an LV (higher current rated) unfolder to generate a 3-ϕ LV ac output, achieving quasi-single-stage

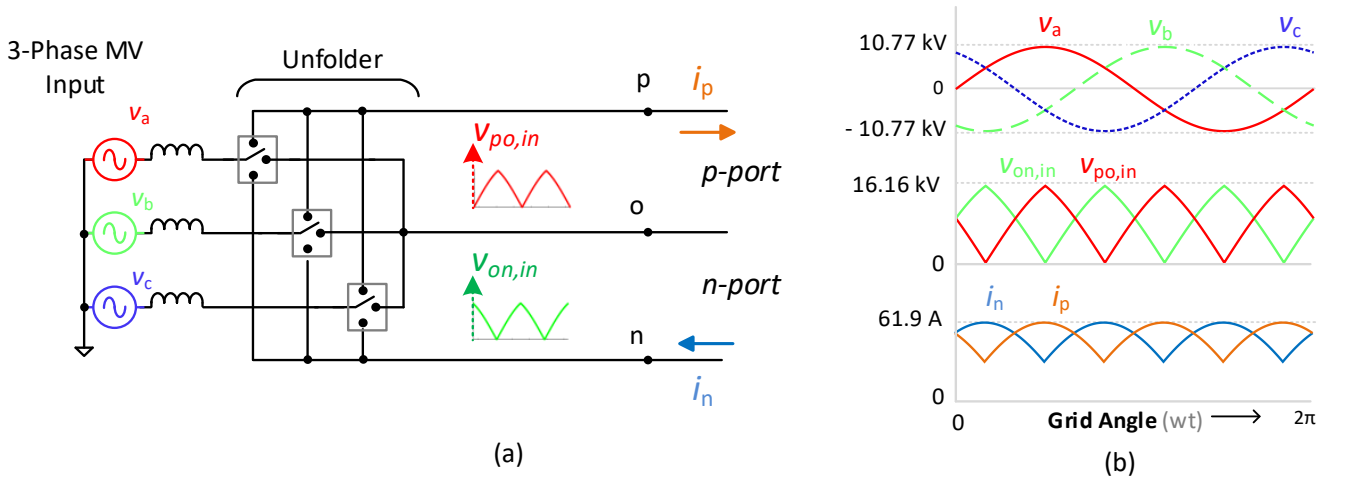


Fig. 2. (a) The line-switched MV unfolder, represented as a combination of single-pole triple-throw switches, is switched once every sector to obtain two time-varying dc voltages from 3-ϕ ac. (b) Ideal waveforms for a 480 V, 10 kW system: balanced 3-ϕ ac grid voltages, soft dc-link voltages over a line cycle, and ideal port currents emulating balanced 1 MW resistive loading of the 13.2 kV line-to-line input.

conversion from MV ac to LV ac. The combined number of series-connected modules and the transformer turns ratio determine the overall voltage step-down, as given by (1). An additional power conversion stage is required to convert the output of the DCX stage to a regulated dc bus, implementation discussed in detail in Section IV.

The time-varying nature of the port voltages by the unfolder introduces unique challenges for DCX operation of individual dc-dc converters. In particular, the selection of a suitable dc-dc topology requires further investigation.

III. Implementation of the DCX Stage

The primary challenge in implementing the DCX stage lies in selecting a suitable topology that can operate as a DCX while interfacing with the time-varying voltages produced by the unfolder. These time-varying inputs necessitate a topology that operates precisely at resonance to ensure consistent energy transfer. The Series-Bridge DCX (SB-DCX) topology provides a practical solution, as it inherently operates at resonance and functions as a DCX without requiring closed-loop control. This makes the SB-DCX highly robust to component tolerances, which is advantageous for practical implementation. In this section, the steady-state operation of the SB-DCX is analyzed, and key design adaptations are presented to enable high-power operation with unfolding architectures.

A. Challenges in Topology Selection for DCX Operation in Unfolding Architectures

The input voltages at the two ports (the *p*-port and *n*-port) vary from 0 to $V_{\text{in,max}}$ ($0.866 \times V_{ll,\text{peak}}$). This wide voltage variation complicates the task of maintaining a finite output current when the input voltage approaches zero—particularly for conventional full-bridge topologies.

Traditional full-bridge topologies, such as the phase-shift-controlled dual active bridge (DAB) or resonant converters like LLC [29]–[33], are commonly used in DCX applications. However, they are not well suited for operation with an unfolder. Under time-varying input voltages and balanced resistive loading (required for unity power factor at the grid interface), the topology must be capable of sourcing a finite input current even when the voltage is near zero. This requirement is illustrated in the ideal waveforms of Fig. 2(b). Although DABs and resonant converters are preferred in many DCX applications [28], [34], maintaining DCX functionality under low input voltage with finite output current is particularly challenging in their operating regimes.

B. SB-DCX as the DC–DC Topology

A key obstacle in realizing DCX functionality in practical systems is the impact of finite transformer leakage inductance, which limits current delivery to the output at low input voltages. To overcome this, a series capacitor is introduced to form a resonant tank, and the system is operated at its resonant frequency. At resonance, the energy needed to sustain current through the leakage inductance is stored and recycled within the tank, removing the dependency on the input voltage. This results in a zero net reactive impedance in the tank, allowing finite current to be delivered even at near-zero input voltages—an essential feature for operation with unfolder-based systems.

Achieving perfect resonance, however, is nontrivial. The series capacitor must be precisely tuned to match the leakage inductance. Even minor deviations can cause performance degradation. In uncontrolled DCX operation—whether using diode rectifiers [35] or synchronous rectifiers [36]—such detuning leads to load-dependent output voltages, which compromises DCX performance. Similarly, the approach of applying symmetric gate signals to both bridges with a resonant tank, as shown in Fig. 3, achieves ideal DCX behavior only under perfect tuning [37]–[39]. Small variations due to temperature drift

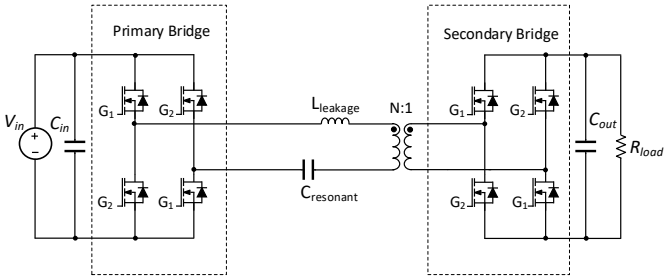


Fig. 3. A series resonant converter with symmetric gating signals for the primary and secondary H-bridges operates as an ideal bidirectional DCX if the series capacitor is tuned to resonate perfectly with the transformer's leakage inductance.

or component mismatch can result in excessive recirculating currents and reduced efficiency.

Frequency-tracking control strategies have been proposed to maintain resonance under such mismatches [40]–[42], but these add complexity and reduce system robustness.

An elegant solution is to augment the resonant tank with a series bridge (SB), which effectively emulates a variable capacitor [43]–[45]. This enables automatic and precise compensation for leakage inductance, maintaining resonance despite component tolerances. The resulting topology—referred to as the Series-Bridge DCX (SB-DCX)—functions as an ideal DCX without active control. Each DCX module consists of two SB-DCX converters, one interfacing each port as shown in Fig. 4.

The SB-DCX is adopted here to support DCX operation with the time-varying inputs of the unfolder. Details on SB gating, capacitor sizing, and steady-state behavior are discussed.

C. Steady-State Operation of the SB-DCX

The SB-DCX is inherently designed to operate as a DCX in steady-state without the need for active control and exhibits robustness to component variations. Neglecting losses, the output voltage is directly proportional to the input voltage, scaled by the transformer turns ratio given as

$$V_{\text{out}} = \frac{V_{\text{in}}}{N}. \tag{2}$$

This relation holds for slowly varying input voltages, such as v_{po} and v_{on}, which follow grid-frequency variations. As long as the SB capacitance C_{sb} is not excessively large, the system's dynamic response is fast enough to treat these voltages as quasi-static.

The SB-DCX achieves ideal DCX operation by operating at perfect resonance, resulting in zero tank reactance. Assuming a constant output voltage (i.e., neglecting capacitor ripple), the tank's input and output can be modeled as shown in Fig. 5. Series resistance R_s, representing conduction losses, is neglected in the steady-state analysis. With symmetric gating applied to both full bridges, steady-state operation is maintained only when the output voltage equals the input voltage—satisfying Kirchhoff's Voltage Law in the circuit of Fig. 5 for a transformer turns ratio of $N = 1$. This results in natural steady-state DCX behavior.

Perfect resonance is achieved through the combined effect of the SB and symmetric gating. Symmetric gating allows a constant output voltage only if the tank reactance is zero; otherwise, power transfer is disrupted (assuming minimal resistance). The SB automatically tunes the tank to resonance by emulating a variable capacitor. It adjusts the energy stored in its capacitor C_{sb}, which creates a dc voltage offset ($v_{\text{c,min}}$). This offset changes the effective SB capacitance, compensating for variations in leakage inductance or switching frequency, and maintains precise resonance.

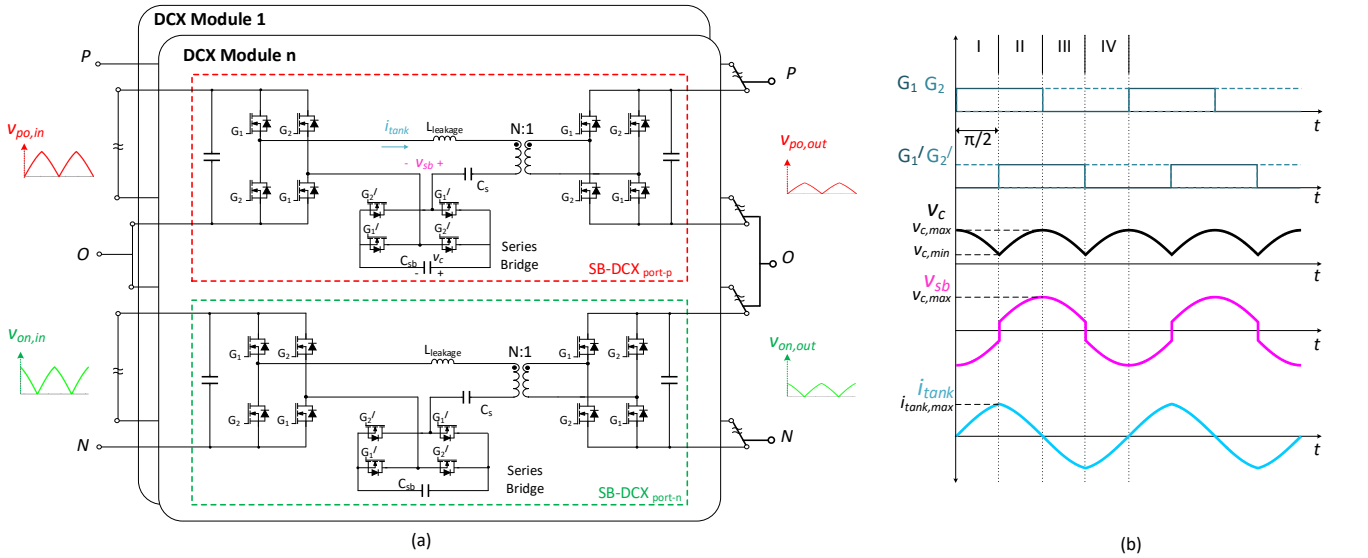


Fig. 4. (a) ISOP arrangement of the DCX stage using SB-DCX modules. Each module includes two SB-DCX converters for the p- and n-ports. The series bridge emulates a variable capacitance, enabling resonance and tolerance to tank parameter variation. (b) Ideal gating signals and steady-state tank waveforms. The SB is phase-shifted by 90° to produce resistive tank currents.

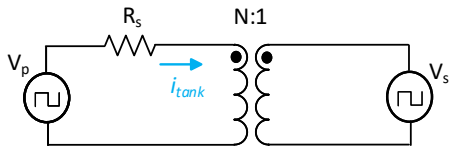


Fig. 5. Steady-state equivalent circuit of the SB-DCX, assuming ideal switching and perfect resonance. The primary and secondary bridges are modeled as in-phase square-wave voltage sources. The tank's net reactance is zero.

The SB is driven at the same frequency and duty cycle as the full bridges but with a 90° phase lag. This ensures resistive tank currents. A 100% duty cycle minimizes peak SB capacitor voltage, improves transient response, and produces near-sinusoidal tank current. Fig. 4(b) illustrates typical gate signals and tank waveforms for the SB-DCX converter (at a specific operating point). The effect of dead-time transitions is minimal and thus neglected in the derivation of the steady-state model.

D. Scaling SB-DCX for High Power

In high-power systems, an additional capacitor C_{s} is added to the resonant tank to reduce the reactive power circulating through the SB. This lowers the peak voltage stress across the SB switches, enabling the use of lower-voltage, lower-$R_{\mathrm{DS(on)}}$ devices, thereby improving efficiency. The peak voltage across the SB capacitor (in the absence of C_{s}) is given by

$$V_{\mathrm{c,max}} = \frac{I_{\mathrm{out}}}{4 f_{\mathrm{sw}} C_{\mathrm{sb}} \cdot \left(1 - \cos\left(\frac{1}{\sqrt{L_{\mathrm{lkg}} C_{\mathrm{sb}}} \cdot 4 f_{\mathrm{sw}}}\right)\right)}. \tag{3}$$

The reduction in voltage, ΔV, achieved by introducing C_{s}, is expressed as

$$\Delta V = \frac{I_{\mathrm{out}}}{8 C_{\mathrm{sb}} f_{\mathrm{sw}}} + \frac{I_{\mathrm{out}} \sin^2(\alpha)}{8 C_{\mathrm{sb}} f_{\mathrm{sw}} \left(\cos(\alpha) - 1\right)^2} + \frac{I_{\mathrm{out}} \left(C_{\mathrm{s}} + C_{\mathrm{sb}} \cos(\beta)\right)}{4 C_{\mathrm{s}} C_{\mathrm{sb}} f_{\mathrm{sw}} \left(\cos(\beta) - 1\right)}, \tag{4}$$

where

$$\alpha = \frac{1}{4\sqrt{C_{\mathrm{sb}}}\sqrt{L_{\mathrm{lkg}}} f_{\mathrm{sw}}}, \tag{5}$$

$$\beta = \frac{1}{4\sqrt{C}\sqrt{L_{\mathrm{lkg}}} f_{\mathrm{sw}}}, \tag{6}$$

$$C = \frac{C_{\mathrm{s}} C_{\mathrm{sb}}}{C_{\mathrm{s}} + C_{\mathrm{sb}}}. \tag{7}$$

A detailed derivation is provided in Appendix A. Based on this analysis, the capacitances C_{sb} and C_{s} must be selected based on the peak output power, transformer leakage inductance, and the maximum allowable voltage across the C_{sb} switches, while accounting for component tolerances. The tank parameter tolerances T_c and T_L represent the percentage deviations in C_{s} and L_{lkg}, respectively.

To ensure reliable operation under worst-case conditions, the peak voltage across C_{sb}—evaluated at full load and with a maximum leakage inductance of $L_{\mathrm{lkg}}(1 + T_L/100)$—must remain below the SB switch voltage rating. The addition of C_{s} serves to reduce this peak voltage, as quantified in (4).

Moreover, the SB voltage must remain strictly positive at all times to avoid conduction through the body diodes of the SB switches. This requirement imposes a lower bound on the permissible value of C_{s}, given by

$$C_{\mathrm{s,min}} = \frac{C_{\mathrm{res}}}{(1 - T_c/100)(1 - T_L/100)},$$

where C_{res} is the nominal value of the resonant capacitance. This condition ensures that resonance is maintained even under worst-case deviations in tank parameters.

IV. Converter for DC Output and Auxiliary Converter for Reactive Power Control

To obtain a regulated dc bus, an additional converter stage is required to interface with the output of the DCX stage and convert its time-varying voltage into a stable dc output. This section discusses various converter topologies and their associated trade-offs for achieving this functionality. In addition, an auxiliary converter stage can be incorporated to control grid reactive power. This auxiliary stage interfaces directly with the output of the DCX stage and does not need to process the full power. The converter topologies and their operational principles for achieving these objectives are detailed below.

A. Three-Port Converters for DC Output

A regulated dc voltage can be obtained from the output of the DCX stage using a three-port converter that transforms the time-varying voltages into a stable dc bus. The converter topology must also enable input current shaping to support power factor correction (PFC). Furthermore, multiple such converters can be connected in parallel to generate multiple isolated and regulated dc buses, depending on application requirements.

Several converter topologies have been proposed to interface with the two output ports of an unfolder (p-port and n-port) and convert the time-varying voltages into a regulated dc output [17]–[20], [46]. Fundamentally, the role of the dc–dc converter is to achieve output voltage regulation with PFC, while optionally providing galvanic isolation. To enable PFC behavior, the input of such converters should ideally emulate a pair of independent voltage-controlled current sources. Different current source configurations can be employed to meet various PFC objectives, with appropriate converter topologies selected accordingly.

A comprehensive overview of such configurations—albeit in the context of MV ac–dc conversion—is provided in [16], which outlines current-source arrangements and their associated isolated dc–dc converter implementations suitable for unfolder interfaces. In this work, we focus on a subset of those implementations that align with the proposed architecture.

Fig. 6 shows ideal input behaviors and practical non-isolated and isolated implementations. These converters must

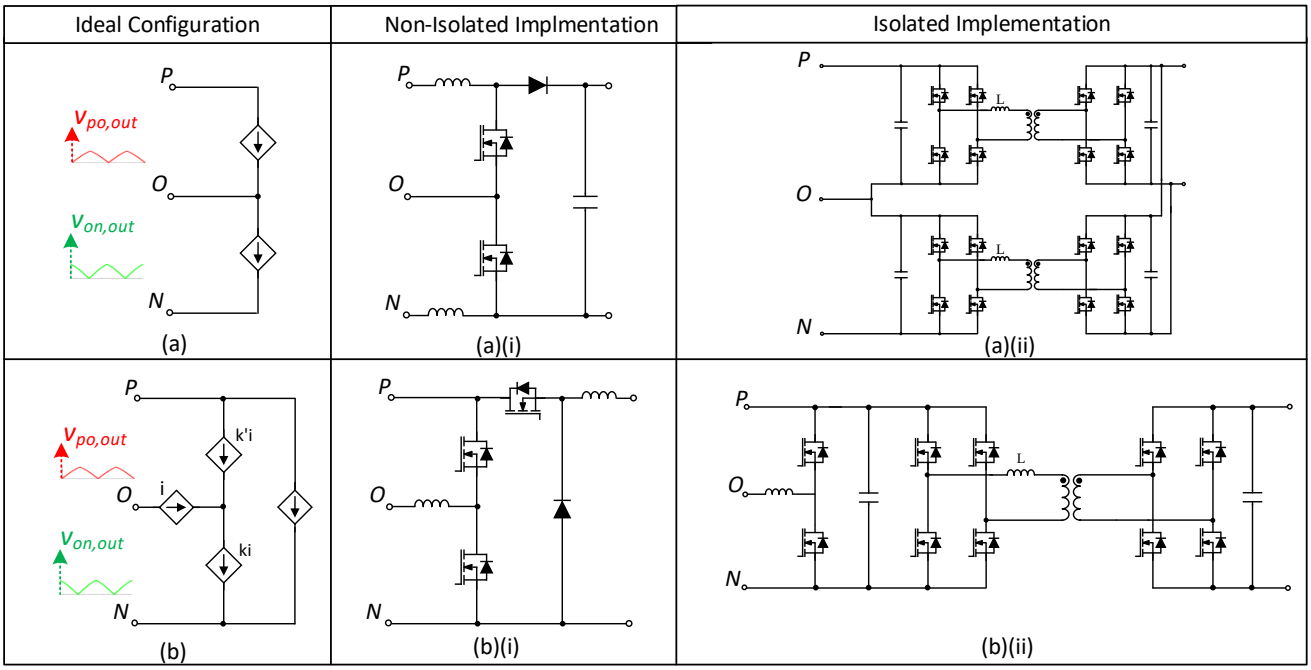


Fig. 6. Input modeling of dc–dc converters as various combinations of two independent current sources, along with examples of practical non-isolated and isolated implementations.

function as at least two independent current sources, arranged in configurations as illustrated. The implementations shown represent one class of feasible designs (each for isolated and non-isolated), although other topologies may be used if they meet the same functional objectives.

The simplest configuration uses one current source at each port—p and n as shown in Fig. 6(a). This requires the dc–dc converter to operate across a wide range of input voltages, which poses challenges, particularly for maintaining soft-switching across all operating points and under-utilization of hardware.

Reference [46] explores non-isolated implementations for this case, with one example shown in Fig. 6(a)(i). In this topology, the shapes of the average currents in the two inductors are controlled to achieve PFC, while their magnitudes are regulated to control the output voltage. For isolated operation, two independent full-bridge dc–dc converters—one for each port—with parallel outputs can be employed, as illustrated in Fig. 6(a)(ii) [18]. The control strategy for both full-bridge converters is the same as that used in the non-isolated implementation.

However, when independent current sources are implemented at each port, ports p and n experience large voltage variations, which can degrade efficiency. To mitigate this, T-type and triple active bridge (TAB) three-port converters have been proposed. These topologies combine the input voltages through high-frequency switching and have demonstrated favorable performance when interfaced with unfolder-based systems [19], [20].

An alternative configuration introduces a current source at the O node to circulate power, while another current source processes the full power between V_{pn} and the output as shown in Fig. 6(b). Known as the *harmonic injection leg*, this approach allows the main converter to operate across a reduced input voltage swing, simplifying its design. The trade-off is increased total processed power due to internal recirculation, which may limit scalability at higher power levels.

The harmonic injection leg can be implemented using a buck converter connected between the p and n nodes, with its output tied to the O node. This configuration supports both isolated and non-isolated implementations. The full-power converter—handling v_{pn} to output transfer—can be a conventional non-isolated converter (e.g., buck - Fig. 6(b)(i)) or an isolated topology with a transformer controlled to maintain constant power at the output (Fig. 6(b)(ii)). Reference [47] provides in-depth discussion of the control and implementation of harmonic injection legs.

This work demonstrates the hardware implementation of a DAB-SRC converter topology for interfacing the output of the DCX stage and producing a regulated dc bus [20].

B. Auxiliary Converter for Reactive Power Control

An auxiliary converter can be interfaced with the output of the DCX stage to provide reactive power control without processing full load power. While such converters are conventionally connected at the low-voltage 3-ϕ ac side [48], the proposed approach interfaces directly with the time-varying dc voltages v_{po} and v_{on}, reducing implementation complexity. However, the topology and control requirements are non-trivial and introduce unique design challenges.

The auxiliary converter operates as a three-port dc–dc converter with input ports connected to $v_{\text{po,out}}$ and v_{out}, and an

output connected to an energy storage element (e.g., capacitor or battery) to buffer exchanged energy, as illustrated in Fig. 1. Under steady-state conditions, it processes no real power (neglecting losses). The behavior of port voltages, currents, and power under purely inductive grid loading is shown in Fig. 7.

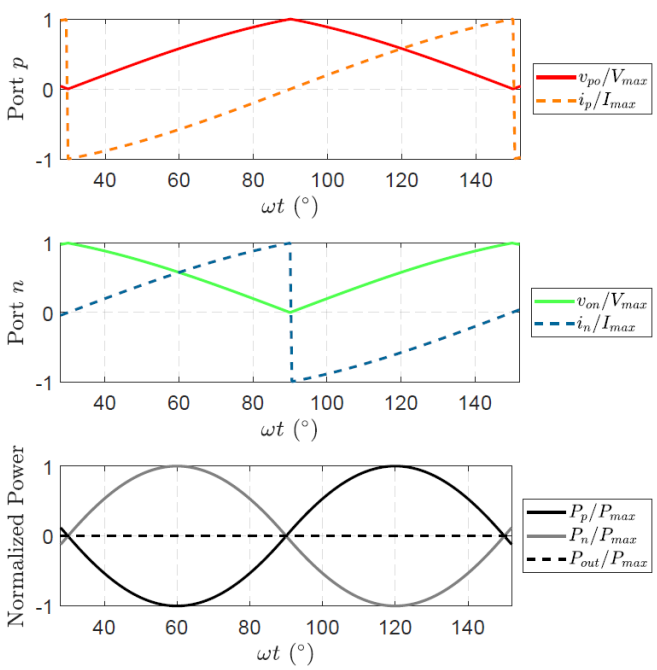


Fig. 7. Power parameters at the auxiliary converter input ports corresponding to purely inductive grid loading.

The converter must support wide voltage gain variations, abrupt current transitions near zero voltage, independent control of the two input currents, and bidirectional power flow at each port. Synchronous rotating reference frame (SRF) control is used to achieve fast current response and manage transitions based on the grid angle.

Two dual active bridge–series resonant converters (DAB-SRCs), arranged as in Fig. 8, are used to implement the auxiliary converter. These integrate well with SRF control, as demonstrated for ac–dc unfolder applications [49], and are adapted here for reactive power control.

The complete auxiliary converter system, including DAB-SRC implementation and control variables, is shown in Fig. 8. The converter is connected between the p-port and n-port outputs of the DCX stage. Its objective is to regulate currents auxiliary converter currents i_{p} and i_{n} based on measured grid currents $(i_{\mathrm{a}}, i_{\mathrm{b}}, i_{\mathrm{c}})$ to enable reactive power control. Control variables ϕ_{ADp} and ϕ_{ADn} used to control p-port power and n-port power respectively are derived from desired i_{p} and i_{n}, which in turn are functions of the real and reactive grid current components $i_{\mathrm{d,ref}}$ and $i_{\mathrm{q,ref}}$ in the dq-frame.

The i_{d} and i_{q} components are computed from the 3-ϕ grid currents using an abc $\rightarrow$ dq transformation, which requires the grid angle θ obtained from a phase-locked loop (PLL). These components can be regulated in closed-loop to generate reference currents for the auxiliary converter, denoted as $i_{\mathrm{d,ref}}$ and $i_{\mathrm{q,ref}}$. Alternatively, open-loop references for $i_{\mathrm{d,ref}}$ and $i_{\mathrm{q,ref}}$ may be applied to specify the desired real and reactive power exchange. The reference values are then normalized with respect to the converter's maximum current limit, $I_{\max}$, and the resulting normalized currents are transformed into port current commands using

$$\begin{bmatrix} i_{p,\mathrm{norm}} \\ i_{n,\mathrm{norm}} \end{bmatrix}_{S\ \mathrm{odd}} = \begin{bmatrix} \cos(\sigma) & -\sin(\sigma) \\ \sin\left(\sigma+\frac{\pi}{6}\right) & \cos\left(\sigma+\frac{\pi}{6}\right) \end{bmatrix} \begin{bmatrix} i_{d,\mathrm{norm}} \\ i_{q,\mathrm{norm}} \end{bmatrix},$$

$$\begin{bmatrix} i_{p,\mathrm{norm}} \\ i_{n,\mathrm{norm}} \end{bmatrix}_{S\ \mathrm{even}} = \begin{bmatrix} \sin\left(\sigma+\frac{\pi}{6}\right) & \cos\left(\sigma+\frac{\pi}{6}\right) \\ \cos(\sigma) & -\sin(\sigma) \end{bmatrix} \begin{bmatrix} i_{d,\mathrm{norm}} \\ i_{q,\mathrm{norm}} \end{bmatrix},$$

where the sector index S and internal angle σ are

$$S = \left\lceil \frac{\theta}{\pi/3} \right\rceil, \qquad \sigma = \theta - (S-1)\frac{\pi}{3}.$$

The control variables are finally computed using

$$\phi_{\mathrm{ADp}} = \sin^{-1}(i_{p,\mathrm{norm}}), \tag{8}$$

$$\phi_{\mathrm{ADn}} = \sin^{-1}(i_{n,\mathrm{norm}}). \tag{9}$$

This reactive power control method is implemented in open-loop form. However, it can be readily extended to closed-loop operation, where the $i_{\mathrm{d,ref}}$ component regulates output voltage and $i_{\mathrm{q,ref}}$ is tuned for precise grid reactive power control. The proposed topology and its control are experimentally validated in Section VI.

V. MV Simulation Validation & Practical Implementation

To validate the feasibility of the proposed architecture, simulation results are presented for a complete system delivering 1 MW from a 13.2 kV medium-voltage (MV) grid. The DCX stage achieves ideal voltage sharing among series-connected modules, even with up to 15% variation in tank parameters. A DAB-SRC topology is employed to interface the output of the DCX stage and generate a regulated dc output. Finally, key practical challenges in the hardware implementation of the 1 MW system are discussed.

A. Simulation Validation

The system parameters are listed in Table I, and the circuit parameters for each SB-DCX (rated for 37 kW peak power) are provided in Table II. Ideally, the transformer leakage inductance should be minimized to reduce recirculating energy within the series bridge (SB). For simulation purposes, a leakage inductance of 5 µH is selected, with up to 15% variation among modules. This value is significantly higher than the practical benchmark of 1.67 µH reported for MV-insulated systems [50]. The capacitors C_s and C_{sb} are chosen to ensure that the peak SB voltage remains below 150 V. enabling the use of GaN-based switches with high figures of merit [51], in accordance with (4).

The simulated waveforms are shown in Figs. 9 and 10. The 13.2 kV 3-ϕ input is converted into time-varying voltages $v_{po,in}$ and $v_{on,in}$, which swing from 0 to 16.6 kV, as shown

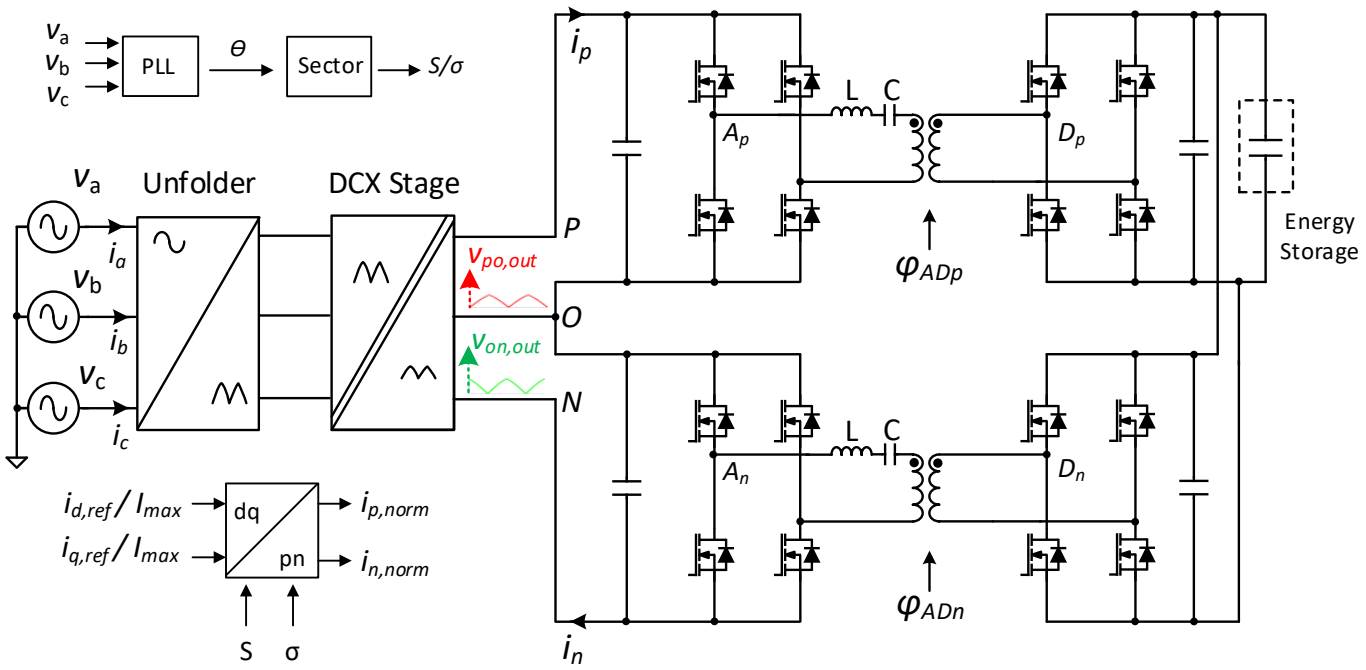


Fig. 8. Auxiliary converter for reactive power control implemented using DAB-SRC topology, controlled in the rotating reference frame to simplify current tracking.

TABLE I
SYSTEM SPECIFICATIONS FOR MV SYSTEM

Specification	Value
Input Voltage (3-ϕ ac)	13.2 kV
Input Power, P_{in}	1 MW
DCX Stage Voltage Step-Down	28:1
Number of DCX Modules	28
Output Voltage (3-ϕ ac), $V_{out,ac}$	480 V
Output Power (3-ϕ ac), $P_{out,ac}$	1 MW

TABLE II
COMPONENT VALUES FOR SB-DCX IN 37 KW MODULE

f_{sw}	C_{in}=C_{out}	C_s	C_{sb}	L_{tank}	N
100 kHz	4 µF	0.63 µF (±5%)	5 µF	5 µH (±15%)	1

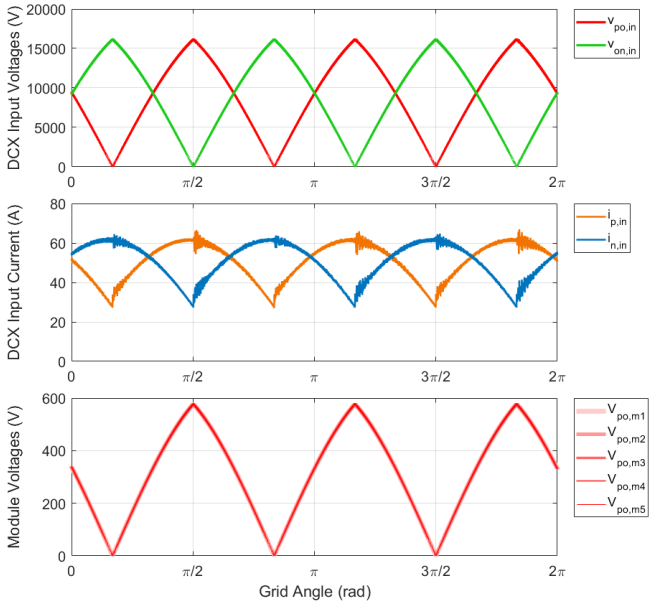


Fig. 9. Simulated input waveforms for the DCX stage. Subplot 1: The 13.2 kV ac input is converted by the unfolder into time-varying voltages peaking at 16.6 kV. Subplot 2: Input currents $i_{p,in}$ and $i_{n,in}$ to the DCX stage for a 1 MW load. Subplot 3: Ideal voltage sharing among ISOP modules despite 15% component variation.

in Fig. 9. These voltages feed the DCX stage, which uses an ISOP configuration of 28 modules to process 1 MW of power. The waveforms demonstrate ideal voltage sharing among the modules despite 15% variation in tank inductance, and without active control. The DCX operates with a voltage step-down ratio of 28:1, and the output, shown in Fig. 10, feeds an output unfolder that generates a 3-ϕ ac waveform, confirming the advantages of using an unfolder and the DCX stage to get quasi-single-stage ac-ac power conversion.

A regulated dc bus draws 80 kW at 300 V, while the remaining power is delivered to balanced resistive loads connected to a 480 V, 3-phase ac output. A DAB-SRC converter is used to generate the constant dc bus from the output of the DCX stage. The circuit parameters for the TAB-SRC stage are listed in Table III. This demonstrates that the proposed converter architecture enables simultaneous generation of both a single-stage 3-ϕ ac output and a regulated dc output. The overall architecture is validated through prototype hardware implementation.

TABLE III
COMPONENT VALUES FOR DAB-SRC FOR DC OUTPUT (80 KW)

f_{sw}	C_{in}=C_{out}	C_s	L_s	N
100 kHz	20 µF	0.381 µF	8.78 µH	1

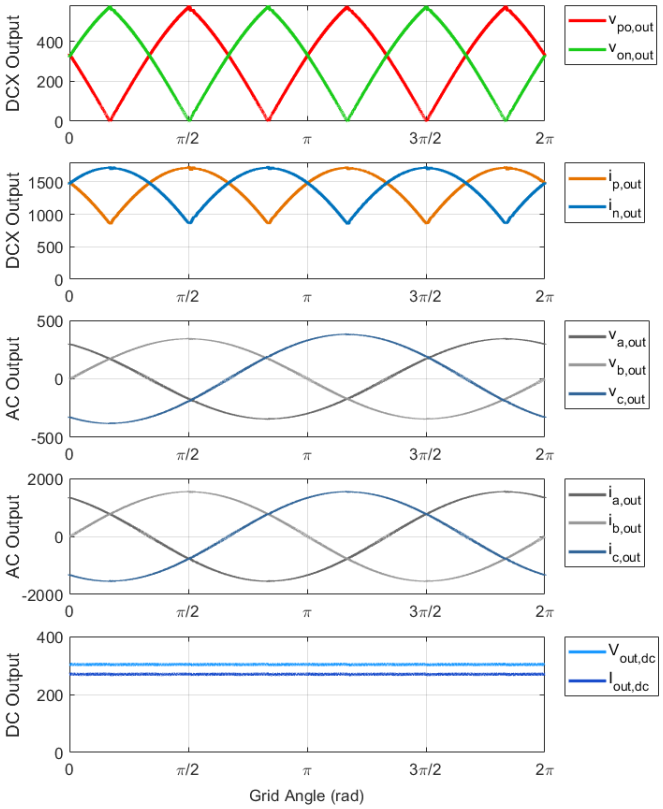


Fig. 10. Simulated output waveforms. The DCX stage output shows a 28:1 voltage step-down while providing galvanic isolation. The output unfolder generates a 480 V 3-ϕ ac waveform, completing the MV-to-LV ac conversion. The dc output port is obtained using a three-port converter.

B. Challenges to Hardware Implementation

This subsection highlights key practical challenges in the hardware implementation of the proposed architecture, with particular emphasis on interfacing with the MV grid. These include switch selection for the MV-rated unfolder and deployment considerations for the SB-DCX topology within a modular structure.

High-power unfolders have been developed [52]. However, managing high-voltage requirements remains a challenge. The primary unfolder is connected to the MV ac grid and must use switches capable of blocking the peak line-to-line voltage with adequate safety margin. A practical unfolder consists of 12 switches, as illustrated in Fig. 1. The back-to-back switches (required for bidirectional blocking capability) must be controlled devices rated for $0.866 \times V_{ll,\text{peak}}$ and can be implemented using IGBTs. The remaining unidirectional switches can be implemented using diodes rated for $V_{ll,\text{peak}}$, enabling a simpler realization.

For a 13.2 kV system, no single switch meets the required blocking voltage with sufficient margin. Therefore, multiple devices must be connected in series to meet this requirement. An example implementation at 4.16 kV ac input is presented in [53], using series-connected QIC6508001 IGBTs and QRD6516001 diodes. A similar approach can be extended for 13.2 kV systems. Significant research is ongoing to develop higher breakdown voltage semiconductor devices suitable for such applications.

While the SB-DCX topology has been validated for high power [44], it has not yet been demonstrated in a series-stacked configuration with MV isolation. This introduces additional challenges. The SB-DCX must be operated using symmetric gating (i.e., identical gate signals applied to both the primary and secondary bridges) to preserve its natural DCX characteristics and tolerance to tank mistuning, as described in Section III. However, in practice, achieving this symmetry is non-trivial due to differences in gate-driver circuitry between the MV-side (primary bridge) and the LV-side (secondary bridge). These differences may introduce small but non-negligible timing mismatches caused by propagation delays or clock skew across isolation boundaries.

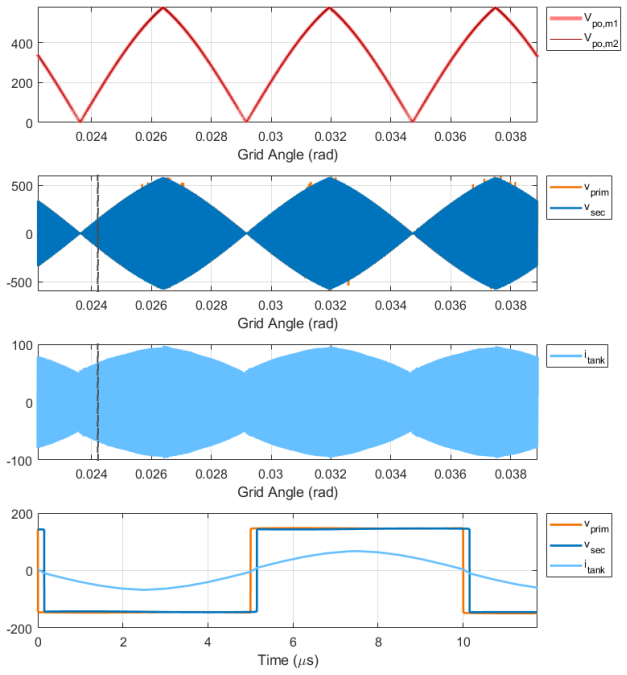


Fig. 11. Simulated waveforms under gate-timing mismatch. Subplot 1: Ideal input voltage sharing is maintained even when the two modules have different gate-timing mismatches. Subplots 2 and 3: Primary and secondary switch-node voltages and corresponding tank currents for the module with the largest mismatch (300 ns). Subplot 4: Zoomed-in view highlighting the mismatch and the resulting distortion in tank current waveform.

To evaluate this issue, simulations were performed with gate-timing mismatches up to 300 ns—a conservative worst-case estimate supported by propagation delays typical in isolated gate drivers [54]. Simulation results (see Fig. 11) show that the SB-DCX remains tolerant to these mismatches and continues to function as an ideal DCX, with balanced input voltage sharing among series-connected modules. This

confirms the robustness of the topology under practical implementation constraints.

Finally, the implementation and control of high-power three-port dc-dc converters for generating regulated dc output from unfolder-derived time-varying voltages has already been validated in hardware [52].

VI. Experimental Validation and Comparison

A 1 kW prototype of the complete system (setup shown in Fig. 12) has been implemented to validate the proposed architecture. The system is powered from a balanced 480 V three-phase ac source. The input unfolder converts this input into the time-varying dc voltages v_{po} and v_{on}, which are then stepped down by the DCX stage. The DCX stage consists of two modules configured in an ISOP arrangement, each implemented using SB-DCX converters with a transformer turns ratio of 1:1. This results in an overall DCX stage voltage step-down of 2:1 with galvanic isolation. Experimental results confirm natural voltage sharing among the series-connected DCX modules without requiring active balancing control.

The output of the DCX stage is connected to an output unfolder that produces a 240 V line-to-line ac output. In addition, two DAB-SRC converters are used to generate a regulated dc bus. These outputs are shown in the hardware waveforms of Fig. 13(b). The ac input and the corresponding DCX stage output are shown in Fig. 13(a). As illustrated, the DCX stage produces time-varying dc outputs with an effective 2:1 step-down ratio, achieved using two ISOP-connected modules. The complete system specifications are given in Table IV, and the DAB-SRC prototype parameters are listed in Table VI.

TABLE IV
System Specifications

Specification	Value
Input Voltage (3-ϕ ac)	480 V
Input Power, P_{in}	1 kW
DCX Stage Voltage Step-down	2:1
Output Voltage (3-ϕ ac), $V_{out,ac}$	240 V
Output Power (3-ϕ ac), $P_{out,ac}$	600 W
Output Voltage (dc), $V_{out,dc}$	135 V
Output Power (dc), $P_{out,dc}$	300 W
Auxiliary Converter Circulating Power	80 W

TABLE V
Component Values for the DCX Modules

f_{sw}	C_{in}	C_{sb}	L_{leak}	N	C_{out}
100 kHz	1.5 μF	1.2 μF	4.5–9.5 μH	1	1.5 μF

The voltage sharing performance of the ISOP DCX modules is shown in Fig. 14. The waveforms depict the input voltages at the p-port and n-port for both SB-DCX modules. As observed, the input voltage is evenly shared between the two modules at each port, without any active control. The system maintains

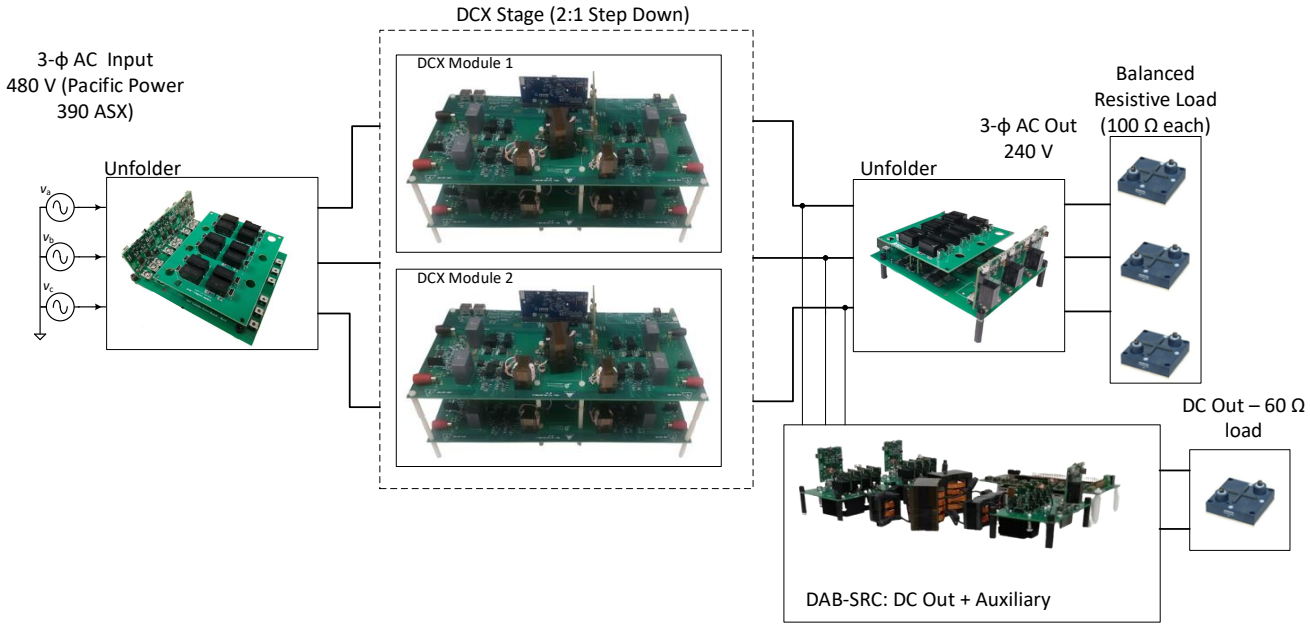
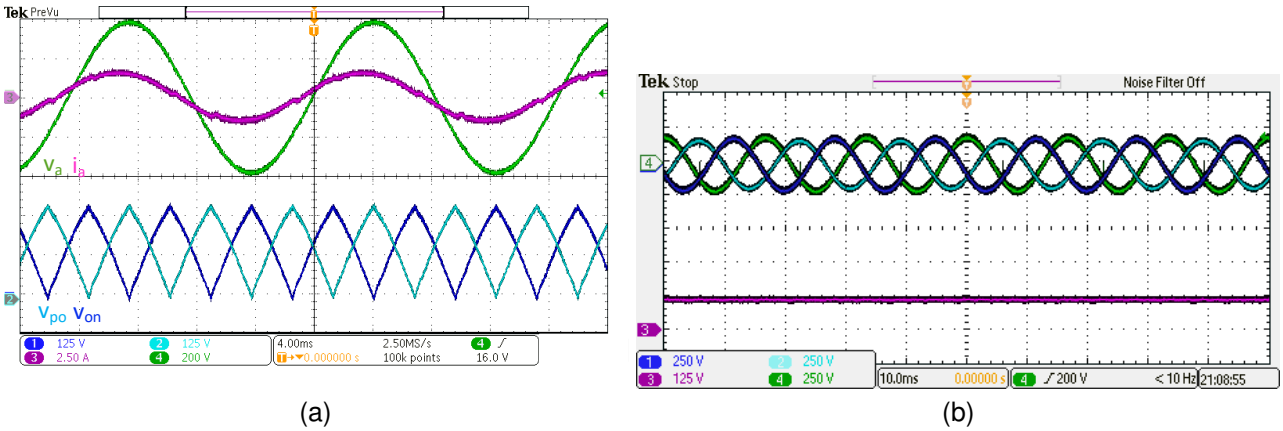


Fig. 12. Hardware test setup for the complete architecture: The input unfolder generates time-varying voltages from a 3-ϕ 480 V ac input; the DCX stage (using SB-DCX topology) provides isolation and step-down. The DCX stage output is interfaced with the output unfolder to supply an ac output feeding resistive loads. Two DAB-SRC converters are interfaced with the DCX output to obtain a regulated dc bus. The same converter is also used as an auxiliary converter to enable reactive power control.



(a) (b)

Fig. 13. Complete system results: (a) Phase a voltage and current of the 480 V three-phase ac input, along with the stepped-down (2:1) soft DC-link voltage from the DCX stage. (b) Three-phase ac output (240 V) and regulated dc output.

TABLE VI
COMPONENT VALUES FOR THE DAB-SRC FOR DC OUTPUT AND FOR REACTIVE POWER CONTROL

f_{sw}	C_{in}	C	L	N	C_{out}
100 kHz	1 μF	0.015 μF	185 μH	1	1 μF

this sharing even under large variations in leakage inductance, with tests performed for deviations up to 100%. The SB-DCX module parameters are summarized in Table V.

The auxiliary converter, implemented using the same DAB-SRC topology and operated as described in Section IV, effectively circulates power to compensate for reactive current drawn by the filter capacitors. As shown in Fig. 15, this results in nearly resistive input currents. The auxiliary converter only consumes power necessary to offset circulating losses.

The power conversion efficiency was measured using a Yokogawa WT1806E power analyzer. For the 480 V 3-ϕ ac to 240 V 3-ϕ ac path, the measured efficiency is 96.5% at 600 W output power. This high efficiency is achieved due to the single high-frequency power conversion stage in the DCX, which directly interfaces the ac input and output. For the 480 V 3-ϕ ac to 135 V dc path, the measured efficiency is 93% at 300 W output power, slightly lower due to the additional power stage for dc regulation.

A. Comparison with Other SST Architectures

The proposed unfolding-based SST architecture is compared against recent SST architectures in Table VII, considering supported ports, number of conversion stages, switching device requirements, bulk energy storage needs, reactive power control, voltage-sharing control, and control complexity.

The MUSE-SST [55] follows a conventional three-stage configuration to derive both LV ac and dc outputs from an MV ac input. However, this cascaded approach reduces efficiency and requires bulky energy storage for stable control. Voltage-sharing control is unnecessary since it uses a single module with HV-rated devices.

TABLE VII
COMPARISON OF PROPOSED SST WITH OTHER SSTS

Parameter	**[55]** *Single Module*	**[56]** *M-S4T*	**[16], [53]** *Unfolder*	**This Work** *Unfolder*
MVAC port	✓	✓	✓	✓
LVDC port	✓	✗	✓	✓
LVAC port	✓	✓	✗	✓
AC→DC stages	2	—	1	2
AC→AC stages	3	1	—	1
4Q switch	—	Req.	—	—
Bulk E-cap	Req.	—	—	—
Q-control	✓	—	✗	✓
V-share ctrl.	Not Req.	Req.	Req.	Not Req.
Ctrl. complexity	Simple	Diff.	Diff.	Simple

The M-S4T SST [56] enables single-stage MV–LV conversion but requires 4-quadrant switches. It can provide either ac or dc output at a time, not both simultaneously, and requires active voltage-sharing control for ISOP configurations. Reactive power control is not possible.

The unfolding-based SST in [16], [53] eliminates the need for 4Q switches and uses a single high-frequency stage but supports only dc output and requires voltage-sharing control. It also lacks reactive power control capability.

The proposed work combines these advantages, enabling ac–ac conversion with a single high-frequency stage, avoiding 4Q switches, requiring no voltage-sharing control, supporting both LV ac and dc outputs, and allowing reactive power control for enhanced flexibility and efficiency in MV SST applications.

VII. CONCLUSION

This article presents an unfolding-based multi-port SST architecture that enables three-phase ac–ac conversion using a single high-frequency power conversion stage, offering a simplified alternative to conventional three-stage systems. For MV ac to LV ac applications, the architecture incorporates a modular DCX stage that naturally shares voltage among series-connected modules, enhancing system reliability and

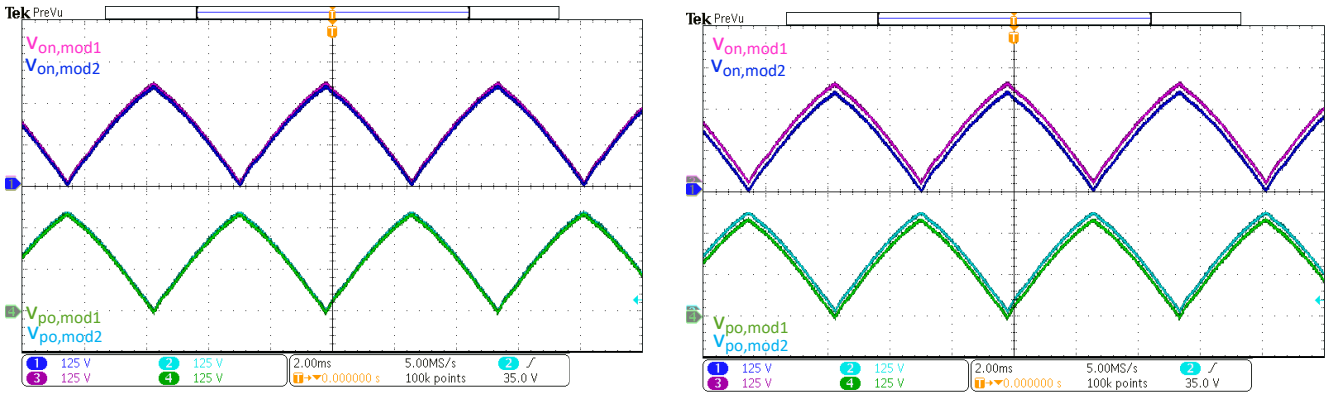


Fig. 14. Voltage sharing among ISOP DCX modules: (a) Ideal input voltage sharing between the series-connected modules (scale: 125 V/div). (b) Split-view of the voltage waveforms (scale: 125 V/div).

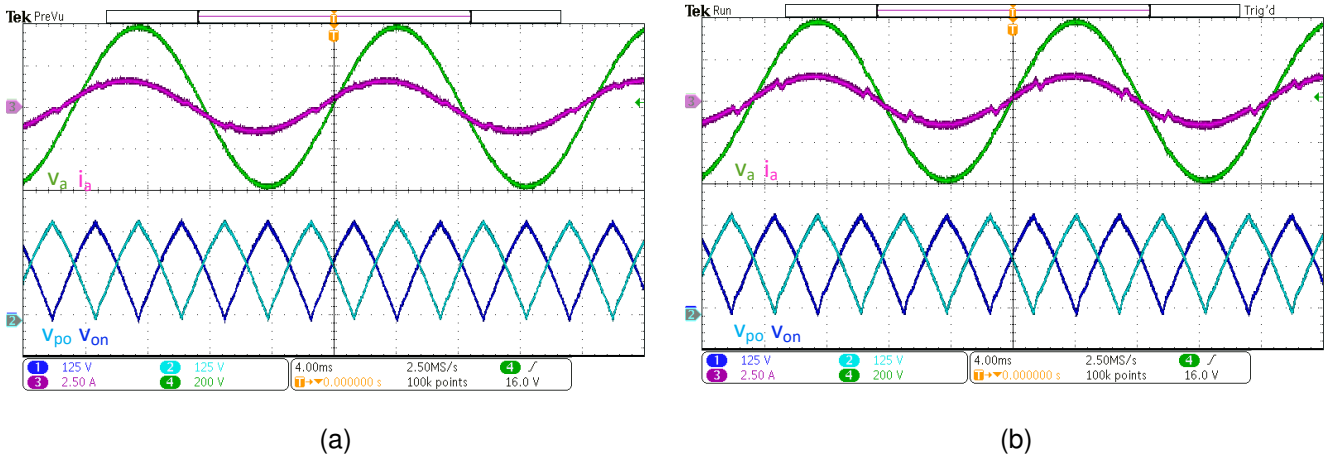


Fig. 15. Auxiliary converter for reactive power control: (a) Operation without auxiliary converter. (b) Operation with auxiliary converter, showing regulated grid currents and near-zero reactive power draw.

scalability without the need for centralized control. The natural voltage sharing is validated through both simulation (at 1 MW scale) and hardware experiments (at 1 kW). Additionally, the architecture supports integration of a three-port dc-dc converter to generate a regulated dc bus, allowing simultaneous support for ac and dc loads directly from the MV grid—thus improving overall hardware utilization.

A key challenge in implementing the DCX stage is the time-varying voltages from the unfolding stage, which complicate the use of conventional DCX topologies. To address this, the SB-DCX converter is proposed for its ability to operate precisely at resonance and its tolerance to component mismatches. Key design elements for scaling to high power and for robust operation with the unfolder are discussed. Furthermore, an auxiliary converter is introduced to enable reactive power control; a DAB-SRC topology with control in the rotating DQ reference frame satisfies all necessary requirements to interface with the time-varying unfolder voltages while achieving full grid current control. The complete system demonstrates scalable performance, natural voltage sharing, ac and dc outputs, and reactive power compensation—all validated through simulations and hardware measurements. The overall 480 V 3-ϕ ac to 240 V 3-ϕ ac power conversion efficiency is 96.5%, higher compared to the conventional 3-stage architecture, further highlighting the advantage of the proposed system architecture.

Appendix A
C_{SB} Voltage Decrease with Additional Series Capacitance

The addition of C_{s} in series with the LV series bridge (SB) reduces the peak voltage (ΔV) across the SB capacitance C_{sb}. The value of ΔV can be determined using (4).

ΔV is the difference in peak voltage across C_{sb} without and with C_{s}. The peak voltage without C_{s} is given by (3). To find the peak voltage with C_{s}, the constraints imposed on capacitive energy requirement and the capacitor charge conservation are used. These constraints are represented as

$$C_{\text{sb}}\left(V_{\text{c,max-new}}^2 - V_{\text{c,min-new}}^2\right) + C_s V_{\text{c,s}}^2 = L_{\text{lkg}} I_{\text{max,new}}^2, \quad (10)$$

$$C_{\text{sb}}\left(V_{\text{c,max-new}} - V_{\text{c,min-new}}\right) = \frac{I_{\text{out}}}{4f_{\text{sw}}}, \tag{11}$$

$$C_s V_{\text{c,s}} = \frac{I_{\text{out}}}{4f_{\text{sw}}}, \tag{12}$$

where

$$I_{\text{max,new}} = \frac{I_{\text{out}} \sin\left(\frac{1}{\sqrt{L_{\text{lkg}}C}\cdot 4f_{\text{sw}}}\right)}{\left(4f_{\text{sw}}\sqrt{L_{\text{lkg}}C}\right)\cdot\left(1-\cos\left(\frac{1}{\sqrt{L_{\text{lkg}}C}\cdot 4f_{\text{sw}}}\right)\right)}. \tag{13}$$

Solving (10) – (13) to get an expression for $V_{\text{c,max-new}}$. The voltage difference is obtained using

$$\Delta V = V_{\text{c,max}} - V_{\text{c,max-new}}. \tag{14}$$

REFERENCES

[1] J. Huber, L. Imperiali, D. Menzi, F. Musil, and J. W. Kolar, "Energy efficiency is not enough!" *IEEE Power Electronics Magazine*, vol. 11, no. 1, pp. 18–31, 2024.

[2] R. Singh, P. Paniyil, and Z. Zhang, "Transformative role of power electronics: In solving climate emergency," *IEEE Power Electronics Magazine*, vol. 9, no. 2, pp. 39–47, 2022.

[3] X. She and A. Huang, "Solid state transformer in the future smart electrical system," in *2013 IEEE Power Energy Society General Meeting*, 2013, pp. 1–5.

[4] J. E. Huber and J. W. Kolar, "Solid-state transformers: On the origins and evolution of key concepts," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 19–28, 2016.

[5] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 861–878, 2019.

[6] J. Huber, P. Wallmeier, R. Pieper, F. Schafmeister, and J. W. Kolar, "Comparative evaluation of mvac-lvdc sst and hybrid transformer concepts for future datacenters," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, 2022, pp. 2027–2034.

[7] J. E. Huber and J. W. Kolar, "Volume/weight/cost comparison of a 1mva 10 kv/400 v solid-state against a conventional low-frequency distribution transformer," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 4545–4552.

[8] M. Liserre, L. Costa, Z. Guo, D. D'Amato, S. S. Queiroz, and A. Huang, "Last developments and new technologies in solid-state transformer," in *2024 IEEE 15th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2024, pp. 1–8.

[9] D.-M. Predescu and -G. Roșu, "Solid-state transformers: A review—part ii: Modularity and applications," *Technologies*, vol. 13, no. 2, 2025. [Online]. Available: https://www.mdpi.com/2227-7080/13/2/50

[10] F. Wang, G. Wang, A. Huang, W. Yu, and X. Ni, "Design and operation of a 3.6kv high performance solid state transformer based on 13kv sic mosfet and jbs diode," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 4553–4560.

[11] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1% efficient 10 kv sic-based medium-voltage zvs bidirectional single-phase pfc ac/dc stage," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 779–797, 2019.

[12] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, 2013.

[13] M. A. Hannan, P. J. Ker, M. S. H. Lipu, Z. H. Choi, M. S. A. Rahman, K. M. Muttaqi, and F. Blaabjerg, "State of the art of solid-state transformers: Advanced topologies, implementation issues, recent progress and improvements," *IEEE Access*, vol. 8, pp. 19 113–19 132, 2020.

[14] X. She, X. Yu, F. Wang, and A. Q. Huang, "Design and demonstration of a 3.6-kv–120-v/10-kva solid-state transformer for smart grid application," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3982–3996, 2014.

[15] X. Yu, X. She, X. Zhou, and A. Q. Huang, "Power management for dc microgrid enabled by solid-state transformer," *IEEE Transactions on Smart Grid*, vol. 5, no. 2, pp. 954–965, 2014.

[16] J. Huber, U. Drofenik, F. Canales, and J. W. Kolar, "Comparative evaluation of three-phase-unfolder-based mvac-lvdc solid-state transformers," in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2024, pp. 254–263.

[17] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Swiss rectifier — a novel three-phase buck-type pfc topology for electric vehicle battery charging," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2617–2624.

[18] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase ac–dc power conversion using series-resonant converter modules and a three-phase unfolder," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9001–9012, 2017.

[19] D. B. Yelaverthi, M. Mansour, H. Wang, and R. Zane, "Triple active bridge series resonant converter for three-phase unfolding based isolated converters," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 4924–4930.

[20] D. B. Yelaverthi, R. Hatch, M. Mansour, H. Wang, and R. Zane, "3-level asymmetric full-bridge soft-switched pwm converter for 3-phase unfolding based battery charger topology," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2737–2743.

[21] H. P. N., T. Mannen, and K. Wada, "A current source three-phase ac-ac converter using current unfolding and active damping principles," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 6239–6245.

[22] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today's and future distribution grids," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 317–326, 2019.

[23] S. Roy, M. Joisher, and A. J. Hanson, "A decentralized nonlinear control scheme for modular power sharing in dc-dc converters," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 2798–2805.

[24] F. Gao, R. Kang, J. Cao, and T. Yang, "Primary and secondary control in dc microgrids: a review," *Journal of Modern Power Systems and Clean Energy*, vol. 7, no. 2, pp. 227–242, 2019.

[25] X. Yu, X. She, X. Zhou, and A. Q. Huang, "Power management for dc microgrid enabled by solid-state transformer," *IEEE Transactions on Smart Grid*, vol. 5, no. 2, pp. 954–965, 2014.

[26] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa, and Z.-X. Zou, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Industrial Electronics Magazine*, vol. 10, no. 2, pp. 46–58, 2016.

[27] B. Majmunović, S. Mukherjee, T. Martin, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson, and D. Maksimović, "1 kv, 10-kw sic-based quadruple active bridge dcx stage in a dc to three-phase ac module for medium-voltage grid integration," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14 631–14 646, 2022.

[28] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimović, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 5774–5781.

[29] S. Mukherjee, A. Kumar, and S. Chakraborty, "Comparison of dab and llc dc–dc converters in high-step-down fixed-conversion-ratio (dcx) applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4383–4398, 2021.

[30] W. Qin, X. Wu, and J. Zhang, "A family of dc transformer (dcx) topologies based on new zvzcs cells with dc resonant capacitance," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2822–2834, 2017.

[31] J. Kucka and D. Dujic, "Smooth power direction transition of a bidirectional llc resonant converter for dc transformer applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6265–6275, 2021.

[32] B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "Modular multilevel high-frequency-link dc transformer based on dual active phase-shift principle for medium-voltage dc power distribution application," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1779–1791, 2017.

[33] X. Wang, Y. Peng, J. Chai, Y. Xia, W. Wei, and M. Yu, "An ideal dc transformer for active dc distribution networks based on constant-transformation-ratio dabc," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 2170–2183, 2020.

[34] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3931–3940, 2013.

[35] R. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 174–182, 1988.

[36] Y. Ren, M. Xu, J. Sun, and F. Lee, "A family of high power density unregulated bus converters," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1045–1054, 2005.

[37] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kv sic-based 7 kv/400 v dc transformer for future data centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, 2019.

[38] A. Esser and H.-C. Skudelny, "A new approach to power supplies for robots," *IEEE Transactions on Industry Applications*, vol. 27, no. 5, pp. 872–875, 1991.

[39] S. Lim, A. J. Hanson, J. A. Santiago-González, and D. J. Perreault, "Bus converter using isolation capacitance for zvs and invariant operation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 1971–1982, 2020.

[40] Y. Yin, M. Shirazi, and R. Zane, "Electronic ballast control ic with digital phase control and lamp current regulation," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 11–18, 2008.

[41] S. Jiang, W. Zhang, B. Liu, and F. Wang, "Automatic resonant frequency tracking in unregulated llc resonant converters based on total resonant current harmonic calculation," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 4193–4198.

[42] W. Feng, P. Mattavelli, and F. C. Lee, "Pulsewidth locked loop (pwll) for automatic resonant frequency tracking in llc dc–dc transformer (llc -dcx)," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1862–1869, 2013.

[43] R. Raju, "Series resonant converters with the resonant capacitor replaced by a bridge," in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, 2017, pp. 999–1,002.

[44] Y. Cao and D. Dong, "Design and implementation of a 12 kw scalable electronic-embedded transformer (eet)-based dc transformer (dcx) with trapezoidal current," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 2340–2347.

[45] S. Poddar and R. Zane, "Dynamic modeling of the resonant series-bridge dcx converter," in *2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2025.

[46] J. W. Kolar and T. Friedli, "The essence of three-phase pfc rectifier systems—part i," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, 2013.

[47] H. Yoo and S.-K. Sul, "A new circuit design and control to reduce input harmonic current for a three-phase ac machine drive system having a very small dc-link capacitor," 03 2010, pp. 611 – 618.

[48] H. Akagi, A. Nabae, and S. Atoh, "Control strategy of active power filters using multiple voltage-source pwm converters," *IEEE Transactions on Industry Applications*, vol. IA-22, no. 3, pp. 460–465, 1986.

[49] W. W. Chen and R. Zane, "Active rectifier system using three-phase unfolder and series resonant converters controlled in synchronous rotating frame," in *2016 IEEE International Telecommunications Energy Conference (INTELEC)*, 2016, pp. 1–7.

[50] Z. Guo, S. Rajendran, J. Tangudu, Y. Khakpour, S. Taylor, L. Xing, Y. Xu, X. Feng, and A. Q. Huang, "A novel high insulation 100 kw medium frequency transformer," *IEEE Transactions on Power Electronics*, vol. 38, no. 1, pp. 112–117, 2023.

[51] J. Rivas, R. Wahby, J. Shafran, and D. Perreault, "New architectures for radio-frequency dc–dc power conversion," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 380–393, 2006.

[52] A. Zade, C. R. Teeneti, M. Mansour, S. Gurudiwan, B. Hesterman, H. Wang, and R. Zane, "A 21-kw unfolding-based single-stage ac–dc converter for wireless charging applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 1, pp. 8–27, 2024.

[53] D. B. Yelaverthi, "Three-phase unfolding based soft DC-link converter topologies for AC to DC applications," Ph.D. Dissertation, Utah State University, Logan, Utah, USA, May 2021, all Graduate Theses and Dissertations, Paper 8015. [Online]. Available: https://digitalcommons.usu.edu/etd/8015

[54] S. Poddar and R. Zane, "Estimation of minimum dead time to counter resonance mistuning in dab-src for dcx operation," in *2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2025.

[55] A. Anurag, S. Acharya, N. Kolli, S. Bhattacharya, T. R. Weatherford, and A. A. Parker, "A three-phase active-front-end converter system enabled by 10-kv sic mosfets aimed at a solid-state transformer application," *IEEE Transactions on Power Electronics*, vol. 37, no. 5, pp. 5606–5624, 2022.

[56] L. Zheng, X. Han, Z. An, R. P. Kandula, K. Kandasamy, M. Saeedifard, and D. Divan, "Sic-based 5-kv universal modular soft-switching solid-state transformer (m-s4t) for medium-voltage dc microgrids and distribution grids," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 326–11 343, 2021.

CHAPTER 4

Series-Bridge DCX as the DC-DC Topology for the DCX Stage

The implementation of the DCX stage is critical to realizing the perceived advantages of the proposed unfolding-based architecture. However, topology selection for the DCX stage are non-trivial. This chapter comprehensively details these challenges and proposes the SB-DCX topology as a practically viable solution. Furthermore, the design and hardware validation of a complete DCX module are presented, demonstrating its ideal DCX behavior when paired with the unfolder.

The DCX stage provides the necessary voltage step-down and electrical isolation, consisting of multiple input-series-output-parallel (ISOP) connected DCX modules, which enable natural voltage sharing among the series-connected modules at the input.

Each DCX module serves as the fundamental building block of the DCX stage. It comprises two DCX cells: one for port-p and one for port-n. Each DCX cell is a DC-DC converter operating as a DC transformer (DCX). However, selecting and designing the appropriate converter topology for DCX operation in conjunction with the unfolder is challenging, as the time-varying nature of the unfolder voltages complicates both topology selection and the design process.

Due to near-zero voltages occurring during certain portions of the grid cycle at the unfolder output, topologies that operate precisely at resonance are required to maintain proper DCX operation. As detailed in this chapter, none of the conventionally used topologies are suitable for this application.

The SB-DCX topology is proposed as a practically relevant solution, capable of operating at resonance in open-loop conditions, even in the presence of mismatches. Steady-state models are developed to enable the design of the SB-DCX to function effectively as a DCX when paired with time-varying voltages from the unfolder. Hardware results provided in this chapter validate the DCX operation of a complete 10 kW DCX module in combination

with the unfolder, achieving a total efficiency of approximately 97%, thereby demonstrating the validity and performance of the proposed topology.

DCX Module in a Three-Phase Unfolding-based Solid State Transformer with Multi-port Output

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***Abstract*—Unfolding-based 3-ϕ grid-tied converter architectures offer a more efficient and power-dense alternative to conventional multi-stage designs. This work proposes a 3-ϕ unfolding-based dual output solid-state transformer (SST) supporting both 3-ϕ ac and dc loads, facilitating higher hardware utilization. The modular architecture features natural voltage sharing among series-connected modules and allows for reactive power control. The architecture includes a dc-dc power conversion stage operating as a step-down DCX (dc transformer). The DCX stage is critical to the advantages of the proposed architecture, as it allows for natural input voltage sharing among series-input parallel-output (ISOP) connected dc-dc modules. The time-varying soft dc-link voltages, characteristic of unfolding architectures, pose challenges for conventional DCX topologies. This article examines these challenges and proposes series bridge-DCX (SB-DCX) converter topology suitable for DCX operation. Furthermore, design elements of the SB-DCX are examined using developed analytical models specific to the unfolding architecture. Hardware results are provided to validate the DCX operation using a 600 V, 5 kW dc-dc prototype converter that achieves a peak efficiency of 98.5%. DCX operation of the complete 10 kW DCX module is validated under time-varying soft dc-link voltages.**

***Index Terms*—Solid-state transformer, SST, three-phase, ac, unfolding, multi-port, medium-voltage, MV, DCX, dc transformer, resonance, series-bridge, SB**

I. Introduction

THE growing demand for energy from the electric grid necessitates continuous advancements in grid-tied power conversion systems [1]. Electrification of transportation through Electric Vehicles (EVs) and the growth of energy-intensive data centers are among the key drivers of rising electricity demand. 3-ϕ grid-tied power converters are essential for interfacing these high-power loads with the power grid. Additionally, they serve as a key enabling technology for the integration of renewable energy sources into the grid [2]. Consequently, it is imperative to focus on advancing the performance, reliability, and cost-efficiency of these systems.

Solid-state transformers (SSTs) have emerged as a promising technology to enhance energy conversion efficiency, reduce costs, and provide advanced control and protections for grid-connected systems. SSTs replace traditional bulky line-frequency transformers with advanced power electronics that enable the use of high-frequency transformers with potential advantages. This is particularly advantageous for eliminating the conventional medium voltage to low voltage (MV-to-LV) line-frequency transformer used in secondary distribution networks, allowing the direct integration of MV-rated power electronics for various applications such as multi-megaWatt fast charging stations and data centers [3], [4]. Direct MV-connected power electronics enable fast installations, size reduction, potential cost savings, and reduced material usage [5].

Typically, SSTs employ multistage architectures. The primary functional requirements for these systems include grid current shaping, isolation, and output voltage control. Two or more power conversion stages facilitate the fulfillment of these objectives with relatively low hardware and control complexity. A state-of-the-art ac-ac SST may consist of a cascade of power converters that convert from ac to dc and back to ac, with appropriate control to obtain the desired 3-ϕ ac output [6]. An intermediate bulk DC-link capacitance would also be required to decouple the dynamics of the individual stages and enable reactive power control. Despite their design and control simplicity, multi-stage architectures limit SST performance due to the cascade of multiple power conversion stages and bulk energy storage.

In contrast, unfolding-based architectures have emerged as a competitive solution for 3-ϕ ac grid-tied converters [7]–[11]. These architectures feature a line-switched unfolder, which operates at twice the line frequency to convert 3-ϕ ac voltages into two time-varying soft dc-link voltages or vice versa. This method of voltage conversion eliminates a high-frequency switched power conversion stage, offering the potential for higher efficiency and power density compared to conventional converter architecture designs [8].

The authors propose a 3-ϕ unfolding-based solid-state transformer (SST) capable of reactive power control and multi-port output configuration with hybrid 3-ϕ ac and dc distribution (see Fig. 1). The system operates from a 3-ϕ MV ac grid input and delivers both 3-ϕ ac and dc outputs. The input MV unfolder converts the 3-ϕ MV ac input into two time-varying dc voltages, ranging from 0 to 0.866 of the line-to-line peak voltage. A DCX stage, functioning as an ideal dc transformer, ensures galvanic isolation and performs voltage step-down to produce time-varying dc voltages at the outputs. These voltages are unfolded to generate a 3-ϕ LV output, achieving a single high-frequency power conversion from MV ac to LV ac. In tandem, a constant dc output bus can be derived from the DCX output using an auxiliary power conversion stage. The multi-port output facilitates a more efficient hardware utilization of the MV-LV power conversion stage (the DCX stage), which is the major cost driver in direct-MV-connected power converters [12].

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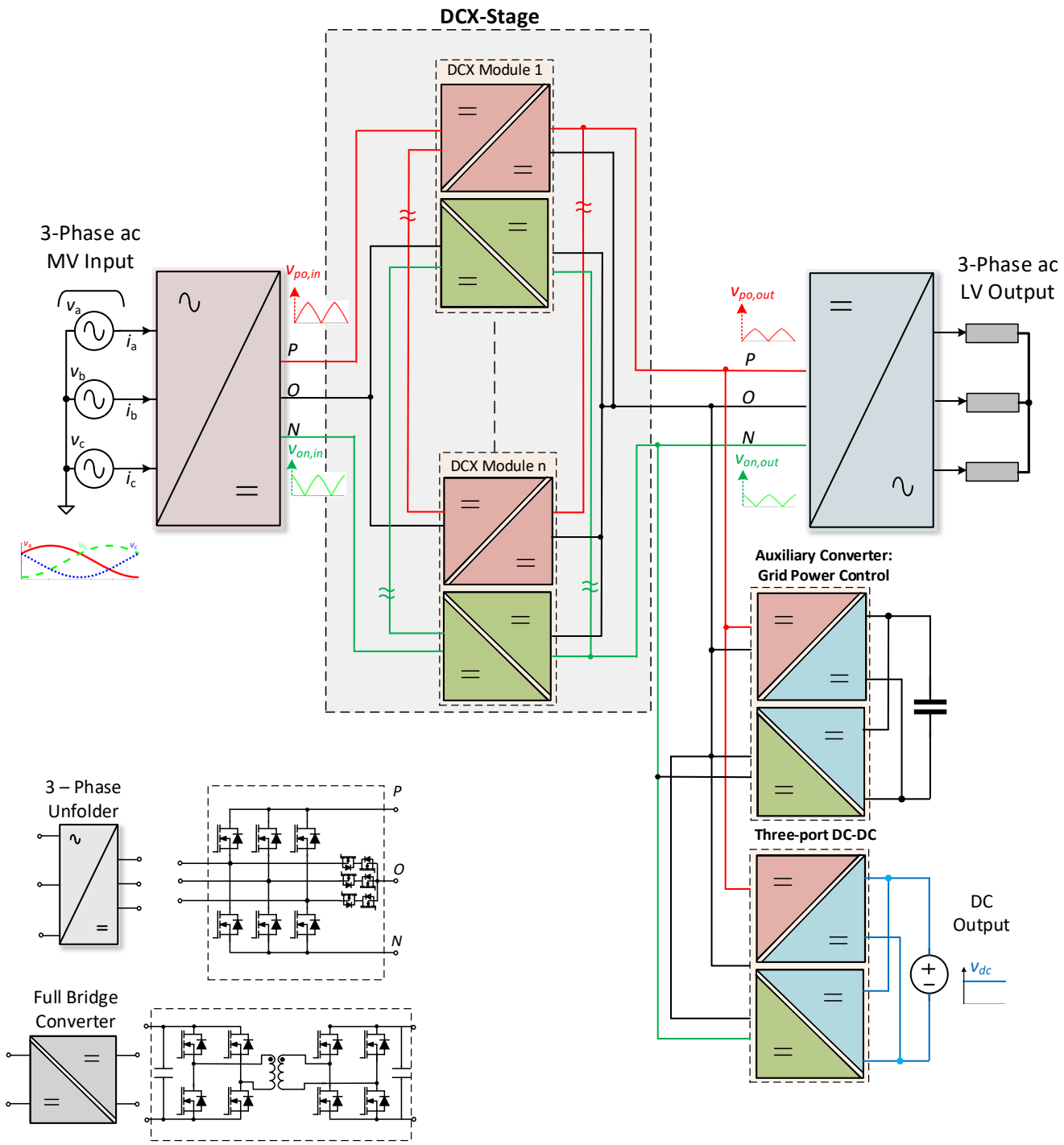


Fig. 1. Block diagram of the proposed unfolding-based solid-state transformer with multi-port output. The architecture includes a DCX stage that provides voltage step-down and galvanic isolation between the MV input and the 3-ϕ LV outputs. An additional converter shapes the MV input currents, functioning as an active filter to ensure compliance with grid power quality requirements and reactive power control. Furthermore, an additional dc-dc is employed to convert the output of the DCX stage into a regulated dc-bus.

The DCX stage facilitates natural input voltage sharing in an ISOP modular structure, enabling a fully decentralized voltage-sharing control architecture that enhances system reliability and reduces costs [13], [14]. An additional converter is incorporated to regulate and shape the grid current and support reactive power control. Notably, the auxiliary converter doesn't process the full load power. Rather, it circulates reactive power as needed, ensuring robust grid interaction and compliance with grid requirements.

This article focuses on the design and validation of the DCX module in the overall topology, which is connected in ISOP configuration to form the DCX stage in the proposed 3-ϕ unfolding SST. The implementation of the DCX stage is crucial to realizing the benefits of the proposed architecture.

The time-varying nature of the soft dc-link voltages, V_{po} and V_{on} (refer to Fig. 2 (b)), presents unique challenges for the dc-dc converter within the module to function as a DCX. The fundamental challenge is ensuring a finite output current at near-zero input voltages. As detailed in Section II (a), actively controlled full-bridge topologies, such as phase-shift-controlled DAB or LLC converters [15]–[20], are not suitable for this application. Instead, series resonance-based topologies that operate precisely at resonance are required [21], [22]. However, achieving perfect resonance in practice is challenging due to component tolerances and variations during operation. Additional control mechanisms to control frequency to tune it to resonance can be implemented [23]–[25]. However, the additional complexity and stability challenges can be avoided.

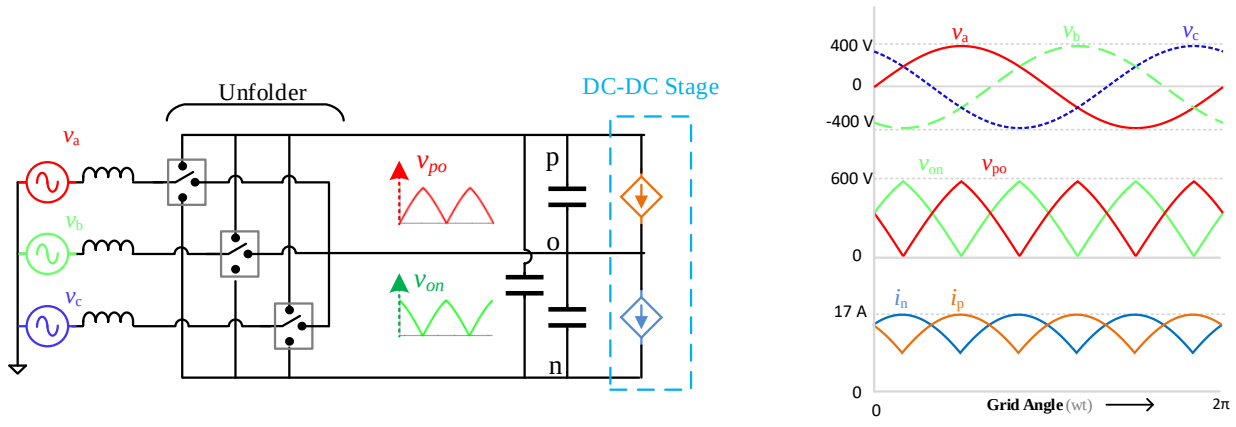
This work uses a topology similar to that proposed in [26], referred to here as the series-bridge DCX (SB-DCX). It naturally functions as a DCX by operating at resonance and inherently compensates for component tolerances. A similar topology has recently been explored for enabling transformer-level paralleling [27]. However, its design and SB gate modulation techniques cannot be directly applied to operation with unfolder. Furthermore, to the author's knowledge, none of the previous work related to SB-DCX or DCX topologies, in general, has addressed the unique operational and design requirements when operating with unfolder.

To summarize, the key contribution of this article is the systematic analysis and design of a dc-dc topology for DCX operation with time-varying soft dc-link voltages in the proposed unfolding SST architecture. Specifically, this work addresses the challenges in topology selection, steady-state modeling, and design for reliable DCX operation. Section II examines the fundamental challenges associated with topology selection and establishes the necessity of the SB-DCX topology for achieving effective DCX operation. Section III presents the working principles and steady-state modeling of the SB-DCX topology, leveraging state-plane analysis to develop analytical insights. These models serve as a foundation for the design of the SB-DCX when interfacing with time-varying dc voltages, as discussed in Section IV. Finally, Section V details the hardware prototype and experimental validation of a 10 kW DCX module (with two SB-DCX converters), demonstrating the feasibility and practical performance of the proposed approach.

II. Design of DCX Module

The inputs to the DCX stage are two time-varying soft dc-link voltages, V_{po} and V_{on}, referred to as the p-port and n-port voltage, respectively (see Fig. 2). These voltages are generated by the unfolder, which operates on the order of the line frequency to convert the 3-ϕ ac input into the two time-varying voltages. A detailed explanation of the unfolder's switching operation is available in [8]. Since the unfolder does not require high-frequency switching or associated energy storage, its losses are negligible, and it is not classified as a power-processing stage.

The DCX stage comprises an ISOP modular configuration of full-bridge dc-dc converters, each functioning as a DCX (see Fig. 1). This stage provides galvanic isolation and steps down the voltage at each port (p and n). Each port has an input series configuration of full-bridge dc-dc converters that support MV operation and provide the necessary voltage step-down. The voltage step-down ratio is determined by the number of dc-dc converters in series and the transformer turns ratio. Two dc-dc converters interfacing the p-port and n-port independently combine to form a modular block referred to as a DCX module.



(a) (b)

Fig. 2. (a) A grid-tied unfolder followed by a dc-dc converter stage. Grid/filter inductors are modeled for completeness. The line switched unfolder, a combination of single pole triple throw switch, is switched once every "sector" to obtain two time-varying dc voltages from 3ϕ ac. The input ports of the dc-dc converters are modeled as two controlled current sources to highlight the requirement of unity power factor. (b) Ideal waveforms for a 480 V, 10 kW system: Balanced 3ϕ ac grid voltages, soft-dc link voltages (in a complete line cycle), and ideal dc-dc currents to emulate balanced resistive loading to the grid.

Operating each dc-dc converter in a module in DCX mode enables natural input voltage sharing in the ISOP configuration with decentralized controls, a crucial feature for modular systems in MV 3-ϕ ac grid-tied converters [15]. In steady-state DCX operation, the output voltage of each dc-dc is a function of its input voltage and transformer turns ratio only. With DCX operation and identical transformer turns ratio for all, the parallel output connected modules will have the same differential input voltage. This results in the total input voltage being evenly distributed among the dc-dc modules at both p and n input ports. This ensures natural input voltage sharing leading to robust performance with minimal control complexity and cost [15], [16].

However, the time-varying nature of the port voltages in the proposed unfolding architecture presents unique challenges for DCX operation. In particular, the selection of a suitable dc-dc topology requires further investigation.

A. Challenges to topology selection for DCX operation of dc-dc converters in unfolding architecture

The input voltages to the two ports (p-port and n-port) vary from 0 to $V_{in,max}$ ($0.866 \times V_{ll,\text{peak}}$). This wide voltage variation it difficult to maintain finite input current when the input voltage approaches zero, as required for DCX operation, especially with conventional full-bridge circuits.

Conventional full-bridge topologies used for DCX, such as the phase shift-controlled dual active bridge (DAB) or LLC converter [17]–[20], [28], fail to meet the requirements needed to operate the dc-dc as DCX in combination with unfolder. With time-varying input voltages and assumed balanced resistive loading (to maintain unity power factor at the grid input), the topology must be capable of conducting finite currents at near-zero input voltages. This concept is illustrated in ideal waveforms shown in Fig. 2(b). While they are often the preferred topologies for DCX operation [16], [29], achieving DCX operation with near-zero input voltage and finite input current proves challenging within a DAB or conventional resonant converter framework.

To understand the fundamental challenge, the DCX operation of the DAB is examined in detail. Physically, a DAB comprises a tank inductor, often the transformer leakage inductance, which serves as the energy transfer element and governs energy flow. The problem arises from the absence of an energy source to build current in the leakage inductance of the transformer under near-zero input voltage conditions. To sustain the required output current, sufficient input voltage is necessary to build current (or energy) in this inductor. This is mathematically modeled by the expression for output current in a DAB as

$$I_{out} = \phi \times (1 - \phi) \times \frac{V_{in}}{f_{sw} \times L}, \tag{1}$$

where ϕ is the phase shift between primary and secondary H-bridges. The tank current (and consequently, the output current I_{out}), in a DAB, builds up only if sufficient input voltage (V_{in} a source of energy) is present. This is in direct contrast with the topology characteristics required to maintain the voltage and current requirements of a DCX in an unfolding architecture. Thus, generating the required current becomes increasingly difficult with near-zero input voltages, especially as current demands escalate for high-power loads (can be visualized in Fig. 3).

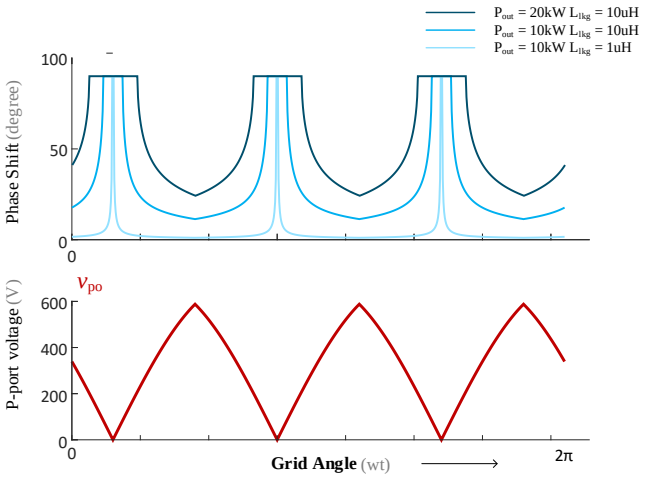


Fig. 3. Variation in phase shift versus grid angle is shown for different leakage inductance values and power levels. The corresponding time-varying p-port dc voltage, V_{po}, is depicted in red. At higher power levels and/or for larger leakage inductance, the phase shift saturates to its maximum possible value for near-zero voltages, indicating a challenge in building the tank current.

Consequently, it becomes imperative to explore topologies that eliminate the need for an input voltage source to build current in the parasitic leakage inductance of the transformer.

B. SB-DCX as the dc-dc topology

The fundamental challenge is addressing the presence of finite leakage inductance in a practical transformer, which impedes the flow of currents to the output significantly at near-zero input voltages. To compensate for leakage inductance physically, a series capacitor is added to form a resonant tank, and the system is operated at its resonant frequency. In steady-state and operation at resonance, the reactive energy required to build current in the leakage inductance is confined within the tank, eliminating the need for additional energy from the input source. In other words, operating the tank precisely at the resonant frequency ensures zero reactive impedance, allowing for finite output currents even at near-zero input voltages hence, allowing for DCX operation with an unfolder.

However, achieving perfect resonance in practice is non-trivial. The capacitor must be precisely tuned to resonate with the leakage inductance. Slight detuning leads to undesirable effects. In uncontrolled DCX operation using a series resonant tank with either a diode secondary bridge [30] or synchronous rectifiers [31], slight detuning results in a drop in output voltage (dependent on the load)—an outcome that is not ideal. Similarly, in configurations with symmetric gate signals applied to the primary and secondary H-bridges and a series resonant tank (as shown in Fig. 4) [21], ideal DCX operation can be achieved, but only if the capacitor is accurately

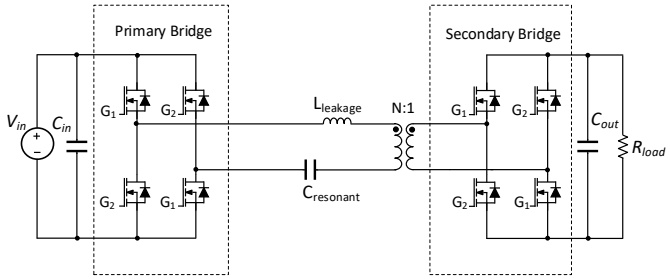


Fig. 4. A series resonant converter with symmetric gating signals for the primary and secondary H-bridges operates as an ideal bidirectional DCX if the series capacitor is tuned with the transformer leakage inductance to achieve perfect resonance.

tuned [22], [32]. Even small deviations from the resonant condition—due to temperature variations or component tolerances—can shift the system off-resonance, causing significant recirculating currents that degrade performance.

While frequency tracking can be employed to ensure precise resonance operation [23]–[25], it introduces additional control complexity and potential reliability concerns that can be avoided.

To address this issue, the tank is modified to include a series bridge (SB), emulating a variable capacitor [26]. This modification ensures exact compensation of the leakage impedance (naturally), resulting in perfect resonance that is tolerant to tuning mismatch. Consequently, this topology naturally behaves as an ideal DCX without any additional controls and is referred to here as Series-Bridge DCX (SB-DCX) (Fig. 5).

A family of similar SB-based resonant DCXs, referred to as Electronic Embedded Transformers (EET)-DCX [27], [33], has been recently proposed. However, these converters have been explored in a different context and cannot be directly applied as DCX in combination with unfolder. EET-DCX features a unique SB switching scheme and design that enables trapezoidal tank currents [27], facilitating natural current sharing for transformer-level paralleling. The time-varying nature of the input voltages imposes limitations on the size of the SB capacitance (denoted as C_{sb} in Fig. 5), which in turn prevents the realization of trapezoidal tank currents and the replication of the used SB switching technique.

This work presents the analysis and steady-state modeling and the design and operation of the SB-DCX suitable for operation with time-varying voltages from an unfolder.

III. Steady-State Operation and Modeling of SB-DCX

The SB-DCX is inherently designed to operate as an ideal voltage source at its output under steady-state conditions. When losses are neglected, the output voltage is directly proportional to the input voltage, scaled by the transformer's turns ratio, as described in (2). This behavior characterizes the SB-DCX as an ideal DCX, with

$$V_{out} = \frac{V_{in}}{N}. \tag{2}$$

For time-varying input voltages, (2) remains valid as long as the input voltage variations occur at a rate significantly slower than the dynamic response of the SB-DCX. This condition is typically satisfied when operating with unfolding-based

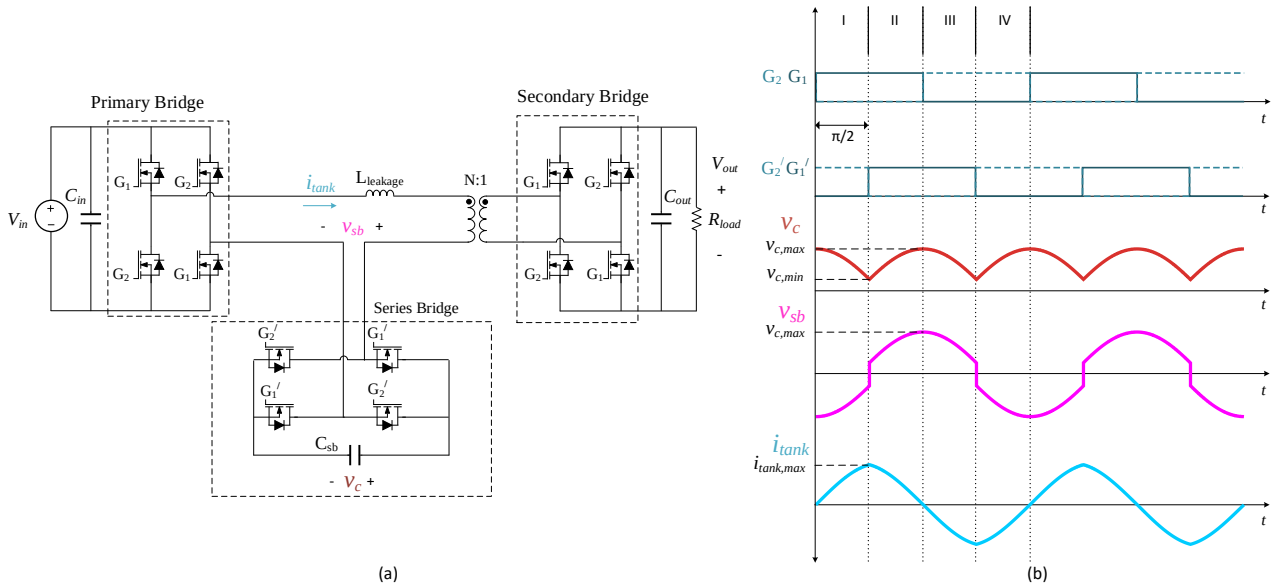


Fig. 5. (a) The SB-DCX topology: a series bridge that emulates a variable capacitance, enabling perfect resonance operation of the tank in a full-bridge dc-dc converter while allowing for higher tolerance to variations in capacitance. (b) The ideal symmetric gating signals of the primary and secondary bridges are shown, with the SB phase shifted by 90 degrees to allow for resistive tank currents. The corresponding tank waveforms for ideal steady-state operation are also depicted.

voltages, V_{po} and V_{on}, which vary on the order of the line frequency. Additionally, the capacitance C_{sb} should not be excessively large and should remain close to the resonance capacitance, C_{res}, to ensure a fast dynamic response of the SB-DCX. Under these conditions, the input voltages can be assumed to be quasi-static for steady-state analysis.

The ideal DCX operation of an SB-DCX is achieved by ensuring perfect series resonance in the tank circuit during steady-state. Perfect resonance resulting from the interaction between the SB and the leakage inductance can be modeled as zero tank reactance (at all input frequencies). Assuming a constant output voltage (neglecting capacitor voltage ripple), the input and output voltage excitations of the tank can be modeled as depicted in Fig. 6. Voltage drops due to series resistance (which represents losses) are neglected. With symmetric gate signals for primary and secondary H-bridges, steady-state operation is achieved only when the output voltage equals the input voltage as required by Kirchhoff's Voltage Law (assuming $N = 1$). Hence, the topology inherently operates as DCX with symmetric gating. A more rigorous proof that shows $V_{\text{out}} = V_{\text{in}}$ (for $N = 1$) is provided in APPENDIX A.

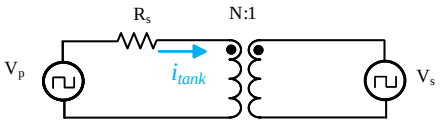


Fig. 6. (a) Steady-state equivalent circuit of SB-DCX, assuming ideal switching transitions and perfect series resonance. The primary and secondary voltages are modeled as square-wave voltage excitations that are in phase due to symmetric gating. The reactance of the leakage inductance and SB combination is zero. R_s models losses due to current conduction.

The perfect series resonance operation of the tank is facilitated by the combined action of the SB and the use of symmetric gate signals for the primary and secondary H-bridges. With symmetric gating, a constant output voltage is maintained only if the tank's reactive impedance is zero. This is because, under symmetric gating, any nonzero tank reactance prevents real current flow through the tank (assuming negligible resistance). The symmetric gating forces the SB to tune the tank capacitance for resonance operation, ensuring zero tank reactance. The SB achieves this naturally by emulating a variable capacitance that continuously adjusts to maintain resonance. It controls the flow of energy to the SB capacitor (C_{sb}) and allows a dc offset in the capacitor voltage (v_{c}). This dc offset enables variation in the tank capacitance as a function of leakage inductance and operating frequency, ensuring precise tuning. An FFT (Fig. 7) of the tank waveforms in an SB-DCX, V_{sb} and I_{tank}, confirms that the tank operates at perfect series resonance in steady-state.

The SB is switched with gate signals at the same frequency and duty cycle as the primary and secondary bridges but with a 90-degree phase lag. The duty cycle of the SB influences the waveshape of the tank current and peak voltage across (C_{sb}). While the phase lag determines the zero-crossing point relative to the main bridges. Operating at full duty cycle allows for a

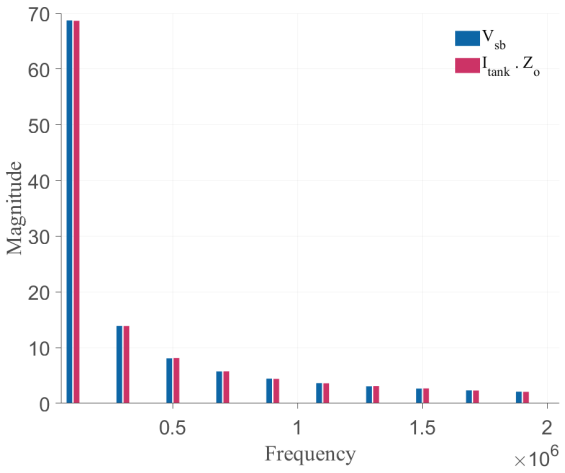


Fig. 7. (a) FFT spectrum of tank waveforms of SB-DCX in steady state, modeling negligible tank energy loss. The frequency spectrum of V_{sb} and I_{tank} (times characteristic impedance at the corresponding frequency) is identical. This highlights a perfect series resonant tank in steady state

lower peak capacitor voltage, faster transient response, and a near sinusoidal tank current. A 90-degree phase lag ensures a resistive tank current.

The gate signals, steady-state waveforms of the tank current, and the SB capacitor voltage (v_{sb}) are shown in Fig. 5(b). The deadtime transitions are small and do not significantly impact the state waveforms. Therefore, they are neglected in the derivation of the steady-state models.

State plane analysis is used to analyze and develop the steady-state model for the SB-DCX that would be useful for designing the converter for different applications. The state-plane analysis technique is well-suited for geometrically analyzing the resonant energy exchange, particularly when there are fewer energy storage elements [34], [35]. Fig. 8 shows the normalized SB capacitor voltage m_C versus normalized tank current j_L. Normalization is performed with respect to the base voltage $V_{\text{base}} = 1$ and the base current $I_{\text{base}} = 1/Z_0$, where $Z_0 = \sqrt{L_{leak}/C_{sb}}$ is the characteristic impedance. Therefore, m_c and j_L are given as

$$m_c = v_c/V_{\text{base}}, \tag{3}$$

$$j_L = i_L/I_{\text{base}}. \tag{4}$$

α represents the normalized period for each switch state combination.

$$\alpha = \frac{\omega_0}{4f_{\text{sw}}}, \tag{5}$$

where $\omega_0 = 1/\sqrt{L_{leak}C_{sb}}$ is the resonant angular frequency.

The steady-state models can be derived by utilizing geometric relationships to determine key normalized values, which are then converted back to time domain. These steady-state models for v_{sb} and i_{tank} are essential for designing and selecting components for hardware implementation. The important relations needed are

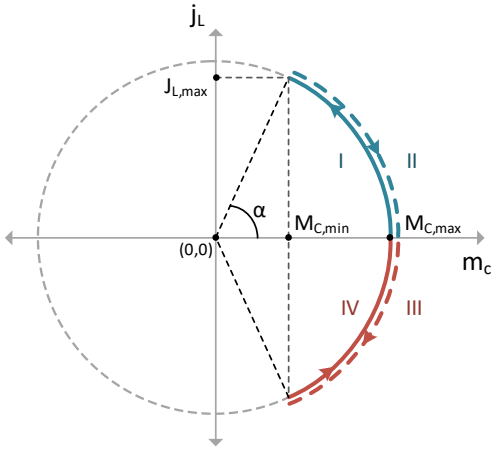


Fig. 8. (a) Normalized state-plane trajectories during the steady-state operation of SB-DCX. The colored solid and dashed state trajectories are used to distinguish different trajectory directions corresponding to different switching combinations; however, they overlap.

$$M_{c,\text{min}} = M_{c,\text{max}} \cos(\alpha), \tag{6}$$
$$J_{l,\text{max}} = M_{c,\text{max}} \sin(\alpha), \tag{7}$$

$$J_{\text{out}} = \frac{1}{\alpha} \int_0^{\alpha} M_{c,\text{max}} \sin\theta \, d\theta = \frac{M_{c,\text{max}}}{\alpha} \left(1 - \cos\alpha\right). \tag{8}$$

Using (5) - (8) and the base values to get the time domain expressions,

$$I_{\text{tank,max}} = \frac{I_{\text{out}} \sin\left(\frac{1}{\sqrt{L_{\text{lkg}} C_{\text{sb}}} \cdot 4 f_{\text{sw}}}\right)}{(4 f_{\text{sw}} \sqrt{L_{\text{lkg}} C_{\text{sb}}}) \cdot \left(1 - \cos\left(\frac{1}{\sqrt{L_{\text{lkg}} C_{\text{sb}}} \cdot 4 f_{\text{sw}}}\right)\right)}, \tag{9}$$

$$V_{\text{c,min}} = \frac{I_{\text{out}} \cdot \cos\left(\frac{1}{\sqrt{L_{\text{lkg}} C_{\text{sb}}} \cdot 4 f_{\text{sw}}}\right)}{4 f_{\text{sw}} C_{\text{sb}} \cdot \left(1 - \cos\left(\frac{1}{\sqrt{L_{\text{lkg}} C_{\text{sb}}} \cdot 4 f_{\text{sw}}}\right)\right)}, \tag{10}$$

$$V_{\text{c,max}} = \frac{I_{\text{out}}}{4 f_{\text{sw}} C_{\text{sb}} \cdot \left(1 - \cos\left(\frac{1}{\sqrt{L_{\text{lkg}} C_{\text{sb}}} \cdot 4 f_{\text{sw}}}\right)\right)}. \tag{11}$$

These can also be written as a function of $I_{\text{tank,max}}$ as

$$V_{\text{c,min}} = \left(\frac{2 f_{\text{sw}}}{I_{\text{out}}}\right) L_{\text{lkg}} I_{\text{tank,max}}^2 - \frac{I_{\text{out}}}{8 f_{\text{sw}} C_{\text{sb}}}, \tag{12}$$
$$V_{\text{c,max}} = \left(\frac{2 f_{\text{sw}}}{I_{\text{out}}}\right) L_{\text{lkg}} I_{\text{tank,max}}^2 + \frac{I_{\text{out}}}{8 f_{\text{sw}} C_{\text{sb}}}, \tag{13}$$

$$\lim_{C_{\text{sb}} \to \infty} V_{\text{c,min}} = \lim_{C_{\text{sb}} \to \infty} V_{\text{c,max}} = 8 f_{\text{sw}} I_{\text{out}} L_{\text{lkg}}. \tag{14}$$

(14) represents the minimum possible peak voltage across C_{sb} for a given output power requirement and aforementioned SB gating. These developed steady-state models form the basis for design to operate with time-varying input voltages.

IV. Design Elements of SB-DCX for Operation with Time-Varying Input Voltages

The time-varying nature of the unfolder voltages presents unique challenges in the design of the SB-DCX. Particularly, in achieving zero-voltage switching (ZVS) for the primary and secondary high-voltage (HV) bridges. ZVS inductors are connected as shown in Fig. 9, to obtain load-independent ZVS and ZCS for all the HV switches. The appropriate sizing of the ZVS inductor and its impact on switch selection is discussed.

Furthermore, the design of the series bridge is analyzed in detail. The SB design involves selecting the capacitance with an appropriate tolerance margin, minimizing the energy storage requirements, and choosing SB switches to reduce losses associated with the SB.

A. Soft switching for Primary and Secondary HV bridges

Achieving ZVS on both the primary and secondary H-bridges is critical, as the hardware operates at high voltage and high frequency (to minimize energy storage requirements). However, the symmetric gating and the time-varying nature of the input voltages complicate achieving ZVS across the line cycle.

To achieve ZVS on the primary bridge, an inductive tank current (lagging in phase relative to the switch-node voltage) is required. The tank current can be made inductive by controlling the phase shift of the SB bridge gate signals relative to the primary (or secondary) gate signals. However, since the secondary bridge switches simultaneously, the tank current does not flow in the correct direction to achieve ZVS for the secondary switches. Furthermore, the time-varying nature of the input voltage causes the required tank current to achieve ZVS to fluctuate throughout the line cycle. Additionally, the tank current is load-dependent and varies over the line cycle as well. As a result, the tank current cannot be relied upon to ensure ZVS for both the primary and secondary switches across all operating conditions.

The magnetizing current of the transformer can be utilized to achieve zero-voltage switching (ZVS). However, enabling ZVS on the primary side requires this current to flow through the SB, leading to increased losses and degraded performance. To address this, ZVS inductors are introduced across each high-voltage (HV) H-bridge to facilitate ZVS (see Fig. 9). The switching transition occurs when the triangular inductor current reaches its peak and is in the correct direction to assist in the soft commutation of the corresponding bridge's switch voltages.

This approach is particularly advantageous because the peak inductor current

$$I_{\text{L,pk}} = \frac{V_{\text{in}}}{4 f_{\text{sw}} L_{\text{zvs}}}, \tag{15}$$

and the required ZVS current

$$I_{\text{zvs,req}} = \frac{2C_{\text{oss}}V_{\text{in}}}{t_{\text{dead}}}, \tag{16}$$

varies proportionately with the input voltage. As a result (assuming constant switch output capacitance C_{oss}) the ZVS design variable,

$$L_{\text{zvs}} = \frac{t_{\text{dead}}}{8f_{\text{sw}}C_{\text{oss}}} \tag{17}$$

solved using (15) and (16), is independent of the input voltage. The analysis here assumes that the inductor current is constant and the tank current is negligible for the switching transition (valid for small dead times and resistive tank currents). Furthermore, (17) also highlights the coupled nature of switch (via C_{oss}) and L_{zvs} selection.

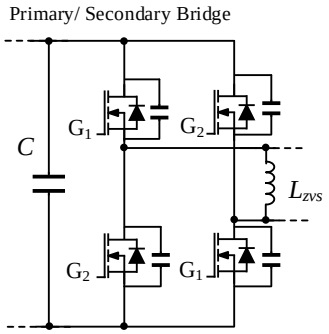


Fig. 9. ZVS inductors are added across the 2-legs of each HV H-bridge to facilitate input voltage and load-independent ZVS. The output capacitance of each switch is modeled for completeness.

A higher C_{oss} (corresponding to a lower $R_{\text{ds,on}}$ for the same device figure of merit (FOM) - $R_{ds,on} \times C_{oss}$ [36]) results in needing higher circulating currents (via decreased L_{zvs}), which helps achieve ZVS but increases the rms currents through the switches. This tradeoff must be carefully managed through switch selection to minimize net conduction losses in the switches for an allowed deadtime.

Further, the parasitic output capacitance of the switches is a non-linear function of the voltage across it (higher charge-equivalent $C_{\text{oss,q}}$ [37] for lower drain-source voltage). This makes L_{zvs} selection challenging when the input voltages vary throughout the line cycle.

Because C_{oss} is a function of voltage, there is no explicit solution for L_{zvs} to achieve ZVS throughout the line cycle. The approach taken here is to select L_{zvs} in combination with the HV bridge's switching device to minimize conduction losses across the line cycle (for a given device FOM) while, ensuring boundary ZVS at the peak input voltage (for an allowed minimum deadtime). To achieve ZVS at all other input voltage levels, the deadtime can be increased as the input voltage decreases to compensate for the increasing charge-equivalent $C_{\text{oss,q}}$.

In conclusion, using the above design approach, load- and input-voltage-independent near ZVS can be achieved throughout the entire line cycle, in the primary and secondary H-bridge. Furthermore, the tank currents are maintained resistive, enabling ZCS as well.

B. Series Bridge Design

The primary design variable for the SB is the floating capacitor C_{sb}. The capacitance of C_{sb} has to be higher than the series resonance capacitance - $C_{\text{res}} = 1((2\pi f_{\text{sw}})^2 L_{\text{lkg}})$. A higher capacitance is needed to allow the SB-DCX to function without $V_{\text{sb,min}}$ going negative (see (Eq. 10)). The higher the capacitance value, the greater is the ability to incorporate resonance tuning mismatch.

However, increasing capacitance C_{sb} increases the tank rms currents and the total required energy storage in the system (shown in Fig. 10). The minimum rms currents and energy storage occur when $C_{\text{sb}} = C_{\text{res}}$. Hence, the plots are normalized to these values. A very high capacitance can allow for trapezoidal tank currents (through different SB gating) [27]. However, with time-varying input voltages, a large capacitance will increase the transient time and make the system unstable. Therefore, the capacitance is chosen based on the maximum amount of LC or frequency variation tolerance required in a practical application. Typically, C_{sb} as 1.5 - 2 times C_{res} is enough for most applications. If ceramic capacitors are used, voltage derating must be considered, if applicable.

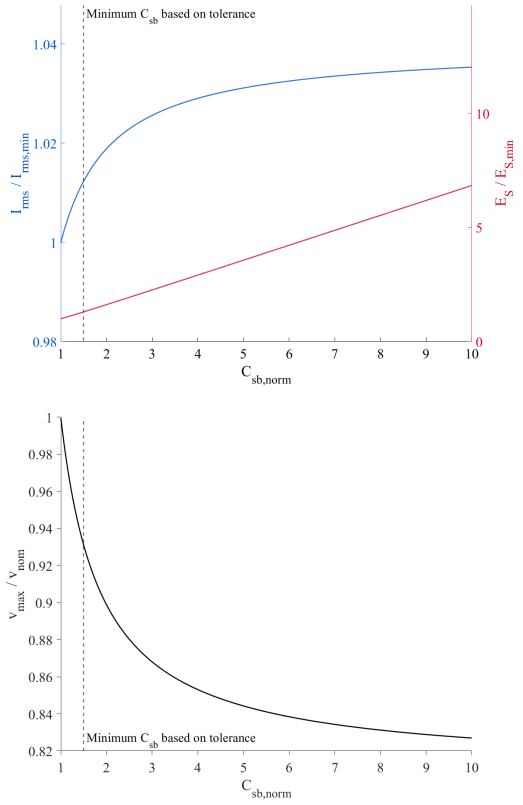


Fig. 10. Normalized plots highlighting the changes in important parameters as a function of increasing C_{sb}

The SB switches must block the peak voltage across C_{sb} during a switching cycle. This peak voltage is determined by the leakage inductance and the power processed by the converter. The maximum peak voltage occurs when the output current reaches its maximum value (output current varies through the line cycle). Therefore, the SB switches should be

rated to withstand this maximum peak voltage across C_{sb} (with appropriate design margins), which occurs at $V_{\text{in}} = V_{\text{in,max}}$ and full power operation. The maximum peak blocking voltage can be found using (11).

To maximize the performance of the converter, the SB switch blocking voltage needs to be kept to a minimum (allowing usage of lower resistance and better FOM devices). The primary design degree of freedom is the leakage inductance (see Eq. 13). Minimizing the leakage inductance should be a priority, especially for high-power designs. High capacitance value for C_{sb} helps decrease the peak voltage across C_{sb} but not significantly (see Fig. 10). Further, as discussed earlier C_{sb} should be kept closer to C_{res}.

For numerical context, the hardware prototype designed in Section V has a leakage inductance of 4.5 μH. For up to 10 kW of power (588 V input), the peak voltage that the SB needs to block is about 65 V. GaN-based MOSFETs (with better FOMs [36], [38] than Si counterpart) are ideal for such applications. Their low $R_{\text{ds,on}}$ minimizes power loss in the SB. Furthermore, all SB switching transition occurs when the tank current is at its peak and has the correct direction to fully achieve ZVS for all switches. This allows the use of extremely low $R_{\text{ds,on}}$ (high C_{oss}), as ZVS currents are sufficient at all operating points within reasonable deadtime. Expression for minimum deadtime for SB switches is given as

$$t_{\text{dead,sb}} \geq \frac{2C_{\text{oss,sb}}}{\sqrt{C_{\text{sb}}}} \cdot \sqrt{L_{\text{lkg}}} \cdot \cot\left(\frac{1}{4f_{\text{sw}}\sqrt{L_{\text{lkg}}C_{\text{sb}}}}\right). \quad (18)$$

If, however, the leakage inductance cannot be reduced beyond a certain point, a modified SB-DCX can be employed similar to [39], [40]. In this configuration, an additional series capacitor C_{s} is added in series with the SB to share the leakage inductance energy storage requirement. This configuration allows the peak voltage across the SB to decrease (as a function of the added capacitance) while maintaining the same LC/ frequency mismatch tolerance.

An appropriate C_{s} can be selected for a given C_{sb} and peak voltage drop ΔV using

$$\Delta V = \frac{I_{\text{out}}}{8C_{\text{sb}}f_{\text{sw}}} + \frac{I_{\text{out}}\sin^2(\alpha)}{8C_{\text{sb}}f_{\text{sw}}\left(\cos(\alpha)-1\right)^2} + \frac{I_{\text{out}}\left(C_{\text{s}}+C_{\text{sb}}\cos(\beta)\right)}{4C_{\text{s}}C_{\text{sb}}f_{\text{sw}}\left(\cos(\beta)-1\right)}, \quad (19)$$

where

$$\alpha = \frac{1}{4\sqrt{C_{\text{sb}}}\sqrt{L_{\text{lkg}}}f_{\text{sw}}}, \quad (20)$$

$$\beta = \frac{1}{4\sqrt{C}\sqrt{L_{\text{lkg}}}f_{\text{sw}}}, \quad (21)$$

$$C = \frac{C_{\text{s}}C_{\text{sb}}}{C_{\text{s}}+C_{\text{sb}}}. \quad (22)$$

Detailed derivation for (19) is provided in APPENDIX B.

V. Hardware Prototype and Experimental Results

A prototype hardware (shown in Fig. 11) has been developed to validate the DCX operation of the SB-DCX topology and to test the DCX module (consists of two SB-DCX converters) in combination with the unfolder circuit. The SB-DCX hardware is designed to handle a 480 V, three-phase ac input voltage through the unfolder and process 5 kW of average power under time-varying input voltage conditions. Operating with soft dc-link voltages (peak voltage of 588 V) as input, the SB-DCX provides isolation and near unity voltage gain, which can be unfolded to deliver a 480 V 3-ϕ ac output. The complete DCX module built using two SB-DCX converters, can process a peak power of 10 kW. These voltage and power specifications (summarized in table I) have been deliberately chosen to closely replicate those of real-world hardware systems, enabling realistic validation of the DCX operation with unfolder and to ascertain its performance.

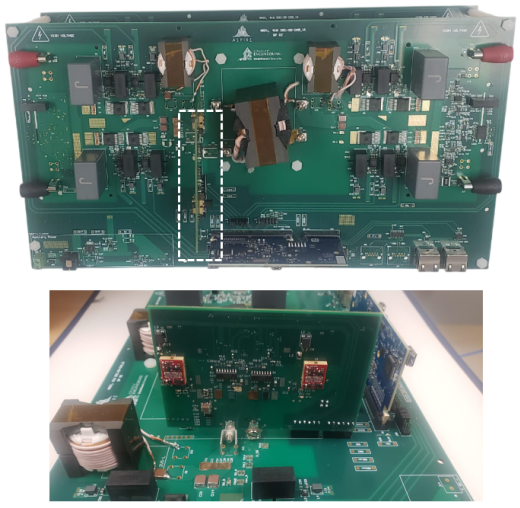


Fig. 11. A 600 V, 5 kW SB-DCX hardware (top) designed to test DCX operation in combination with the unfolder. The GaN-based LV series bridge is highlighted at the bottom.

TABLE I
Electrical Parameters of the SB-DCX Topology

Specification	Value
Input Voltage (Max), V_{in}	600 V
Output Voltage (Max), V_{out}	600 V
Average Power, P_{avg}	5 kW
Peak Power, P_{peak}	10 kW
Switching Frequency, f_{sw}	100 kHz
Transformer Turns Ratio	1:1

TABLE II
Component values for the prototype SB-DCX

C_p	$L_{zvs,p}$	C_{sb}	L_{leak}	N	$L_{zvs,s}$	C_s
2.5 μF	175 μH	1.2 μF	4.5 μH	1	180 μH	2.5 μF

TABLE III
POWER STAGE COMPONENTS

Component	Part / Value
Primary & Secondary MOSFETs	SiC IMBG120R017M2H
Series Bridge (LV) MOSFETs	GaN EPC2361
Input/Output Capacitors	R75QR368050H0J
ZVS Inductor Core	PQ50/50-3C97
Transformer Core	PQ32/30-3C97

For MV systems, dc-dc hardware with similar voltage and current specifications—capable of providing MV isolation—serves as a scalable building block. The overall system power level and voltage transformation can be configured by adjusting the number of these building blocks and the transformer turns ratio.

The prototype circuit parameters and the power stage components are listed in tables II and III. The input and output capacitors are selected to maintain a near 5% voltage ripple at peak voltage and peak output power. L_{zvs} is chosen in conjunction with the switch, as detailed in Section IV(a), using a minimum possible deadtime of 70 ns at peak input voltage. SiC MOSFETs were used as they have higher FOM ($R_{ds,on} \times C_{oss}$) than their Si counterparts for 900-1200 V voltage blocking capacity. The secondary L_{zvs} is slightly larger than the primary due to the magnetizing inductance appearing in parallel. This ensures that the net ZVS current remains the same as that of the primary bridge, thereby preserving symmetry.

C_{sb} is selected to be approximately twice the resonant value. The transformer leakage inductance is calculated assuming the cantilever model for the transformer [41]. With a leakage inductance of 4.5 μH and a peak power of 10 kW, the maximum voltage across the SB is less than 65 V. Consequently, no additional series resonance capacitor is needed, and GaN switches with a 100 V blocking capacity and a minimum $R_{\text{ds,on}}$ of 1 mohms are used to minimize conduction losses, a deadtime of 70 ns is more than sufficient for complete ZVS of the SB switches (verified using (18)).

A. DCX operation of SB-DCX with constant dc-input

The SB-DCX hardware was initially tested with a constant dc input voltage to evaluate its steady-state and transient operation across discrete input voltages and load currents, as well as to measure efficiency. The hardware test used electronic supplies and electronic loads/passive loads. Electronic loads were used for power levels less than 2 kW and passive resistors for all other power levels.

The SB-DCX works as an ideal DCX processing a full-load current of 8.5 A at both 30 V and 600 V input voltages while maintaining similar tank waveforms, as shown in Figs. 12(a) and 12(b). These tank waveforms closely align with the predictions of the developed mathematical models, neglecting dead-time transitions. The designed SB-DCX achieved a peak efficiency of 98.5%.

Transient load performance was evaluated using a 90% load change at a slew rate of 0.5 A/μs, while maintaining a fixed input voltage of 30 V (see Figs. 13(a) and 13(b)). The transient waveforms highlight the topology's load-independent voltage gain (neglecting the series voltage drop due to resistive losses) without requiring any additional controls.

Additionally, the load transient waveforms demonstrate the SB-DCX's fast transient response, with settling times of less than 100 μs. This fast dynamic response is particularly advantageous when operating with time-varying input voltages. The dynamic response is strongly influenced by the value of the SB capacitance (C_{sb}), with the transient time decreasing as the capacitance approaches the resonant value.

B. DCX Module operation with unfolder

Next, the DCX module is tested with an unfolder. The unfolder is powered by a 480 V 3-ϕ ac line, with two SB-DCX dc-dc converters connected at its output ports (p-port and n-port), as shown in the test setup Fig. 14(a). The two SB-DCX dc-dc converters form a complete DCX module. The hardware test using the SB-DCX-based DCX module demonstrated ideal DCX characteristics when operating with time-varying input voltages from the unfolder (see Figs. 15(a) and 15(b)).

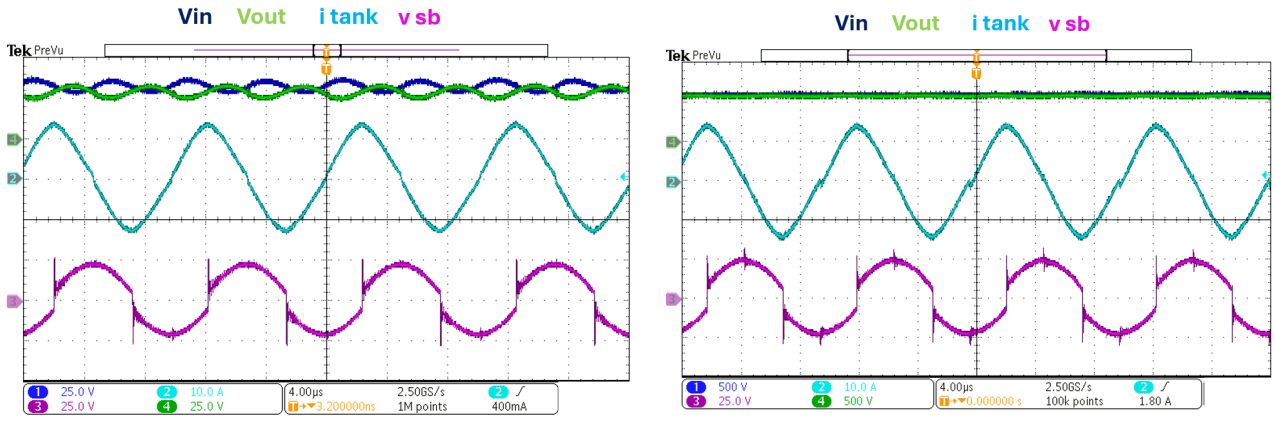
The magnitude and shape of the ac line currents are determined by the load connected to the SB-DCX, as the SB-DCX is not intended to regulate these currents. To ensure that an ideal resistive load is presented to the 3-ϕ grid, a delta-connected combination of load resistors is placed at the output of the dc-dc stage. This resistive load is configured to allow nearly 10 kW of power to be processed by the combined operation of the SB-DCX and the unfolder when operating at a 480 V ac input. It should be noted that to obtain a 3-ϕ ac output, an additional unfolder is required, as shown earlier in Fig. 1. However, the performance of the DCX module can be evaluated without the output unfolder by using delta-connected resistors, which emulate the same loading conditions as those imposed by an unfolder-driven resistive load.

Near ideal 1:1 DCX operation is observed throughout the line cycle. The output voltage tracks the input voltage, as expected for an ideal DCX with unity gain. Notably, near zero voltage crossings, the SB-DCX is capable of processing the required i_p and i_n currents (see Fig. 15(a)), unlike conventional DCX topologies. Perfect resonance, facilitated by the SB and symmetric gating, is key to achieving such ideal DCX characteristics without needing controls.

Overall, the port voltages and output currents of the DCX module observed in the hardware (Fig. 15) are very similar to the ideal expected waveforms shown in Fig. 2, except for the distortion in currents that near zero voltage (or sector change). The causes of these "sector distortions" and control-based solutions are well documented in [42]–[44].

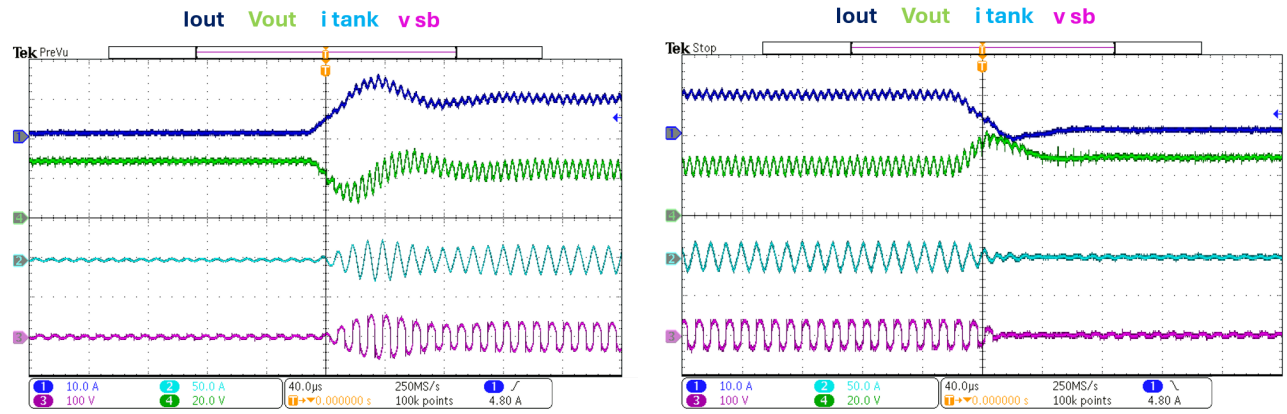
C. Efficiency Measurements

The power conversion efficiency of the designed SB-DCX hardware was measured for various loads at constant dc input voltages. Yokogawa WT1806E power analyzer was used to perform these measurements.



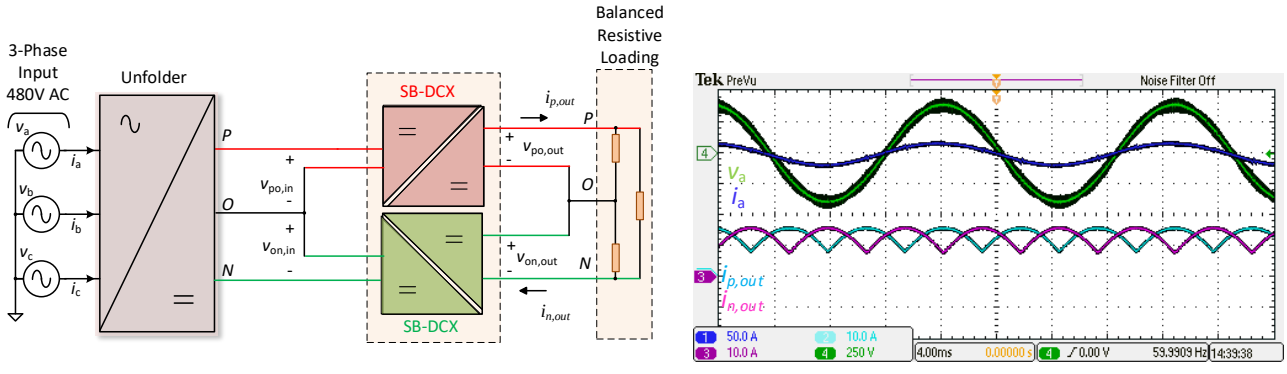
(a) (b)

Fig. 12. (a) Steady-state operation at full load current (8.5 A) with a 30 V input voltage. The input voltage (V_{in}, 25 V/div) and output voltage (V_{out}, 25 V/div) have nearly identical dc values (turns ratio N = 1). The tank current (i_{tank}, 10 A/div) and the SB capacitor voltage (v_{sb}, 25 V/div) closely match the ideal waveforms. (b) Steady-state operation at full load current with a 600 V input voltage. The input and output voltages (V_{in} and V_{out}, 500 V/div) and the tank waveforms are similar to those in (a). These results demonstrate that the SB-DCX can achieve unity gain at full load current, independent of the input voltage.



(a) (b)

Fig. 13. Load transient waveforms at a 30 V input voltage with a load step of 90%. Output current (I_{out}, 10 A/div), tank current (i_{tank}, 50 A/div), and SB capacitor voltage (v_{sb}, 100 V/div) are shown. (A) Load transient waveforms at a 30 V input voltage with a load step from 10% to 100%.(b) Load transient waveforms at a 30 V input voltage with a load step from 100% to 10%. The output voltage waveform (V_{out}, 20 V/div) highlights the intrinsic load-independent voltage gain of the SB-DCX topology.



(a) (b)

Fig. 14. Unfolder + DCX stage hardware test setup and waveforms: (a) 480 V 3-ϕ ac input, delta-connected resistive load at the output of the DCX stage to allow near unity power factor at the input. (b) Phase A input voltage (V_a, 250 V/div) and input current (I_a, 50 A/div) are shown in green and dark blue. The phase current is leading the voltage slightly due to the capacitive loading presented by the filter capacitors. $i_{p,out}$ and $i_{n,out}$ (10 A/div) currents are ideal (similar to Fig. 2(b)), as expected for balanced resistive loading.

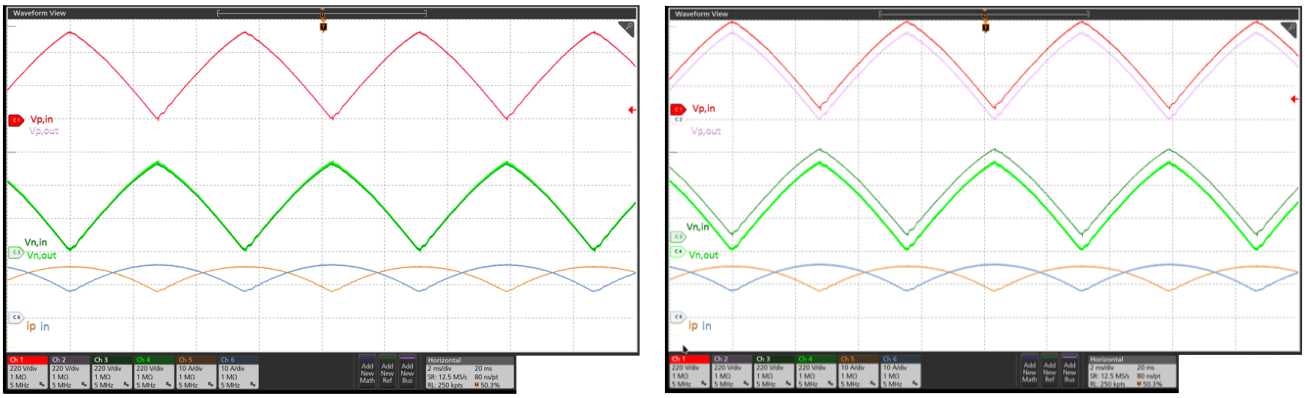


Fig. 15. Unfolder + DCX module: The input and output voltages at the p-port ($v_{p,\text{in}}$ and $v_{p,\text{out}}$, 220 V/div) and the n-port ($v_{n,\text{in}}$ and $v_{n,\text{out}}$, 220 V/div) of the DCX module are shown, along with the corresponding port output currents ($i_{p,\text{out}}$ and $i_{n,\text{out}}$, 10 A/div). (a) The input and output waveforms at each port overlap precisely, illustrating ideal DCX operation throughout the line cycle. (b) Split-view of the voltage waveforms.

The converter efficiencies are plotted for input voltages of 30 V, 150 V, 300 V, and 600 V at different load currents, up to the max continuous load current of 8.5 A, as shown in Fig. 16. The converter achieves a peak efficiency of 98.5% at 300 V input, 4 A load current. And exhibits a relatively flat efficiency profile for input voltages above 150 V. The combination of high efficiency and a flat profile is a key reason for operating the dc-dc converter as a DCX.

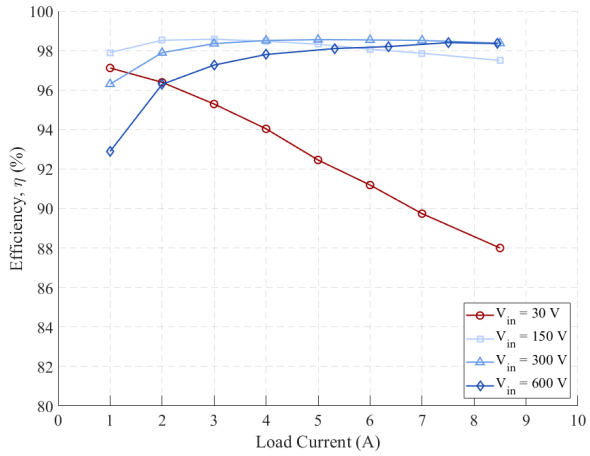


Fig. 16. Efficiency plot of the prototype dc-dc hardware with different dc input voltage and at various load conditions. The hardware achieves a peak efficiency of 98.5% at 300 V input, 4 A load current.

However, for low-voltage (< 80 V), high-current DCX operation, the converter efficiency drops significantly. Mathematical models predict the converter losses well at dc operating conditions Figs. 17 and 18. These models (Fig. 17) indicate that this decline is primarily attributed to conduction losses. The conduction losses are the same as full load power but the processed power decreases proportionally with the input voltage. Thus, conduction power losses are a larger fraction of the power processed and hence, lower efficiency. This behavior is expected, as the dc-dc converter operates over a wide input voltage range while still requiring near-peak currents.

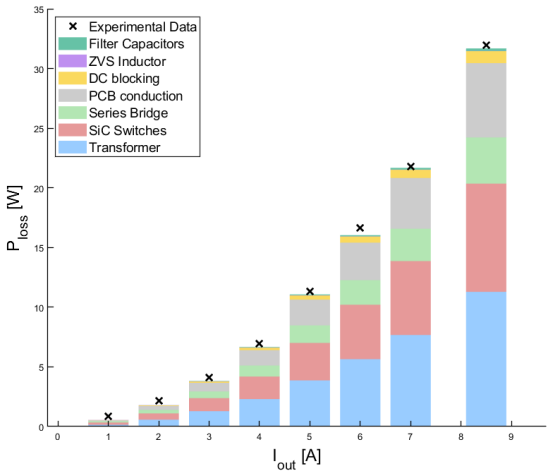


Fig. 17. Measured Loss at 30 V dc input voltage for various loads and the model predicted loss breakdown. Conduction loss in all the components is the dominant loss mechanism.

Using the developed loss model, the efficiency of the complete DCX module (comprising two SB-DCX converters) is plotted across the line cycle in Fig. 19 when operated with time-varying voltages from an unfolder at 10 kW. Nearly all power is processed at efficiencies above 96%, except near zero input voltages, where the processed power is minimal while the output currents remain high. However, the power processed under these low-efficiency conditions is negligible. For the majority of the operating time—corresponding to more than 95% of the total power—the efficiency exceeds 96%, resulting in an overall predicted efficiency of 97.3%.

The predicted efficiency closely matches the measured total efficiency of 97.1% for the DCX module (the efficiency measured doesn't include power loss in the unfolder). For complete ac-ac power conversion using both input and output unfolders, the additional unfolders have a minimal impact on overall efficiency, as unfolders tend to have operating efficiencies above 99.5% [45]. Therefore, the inclusion of additional unfolders

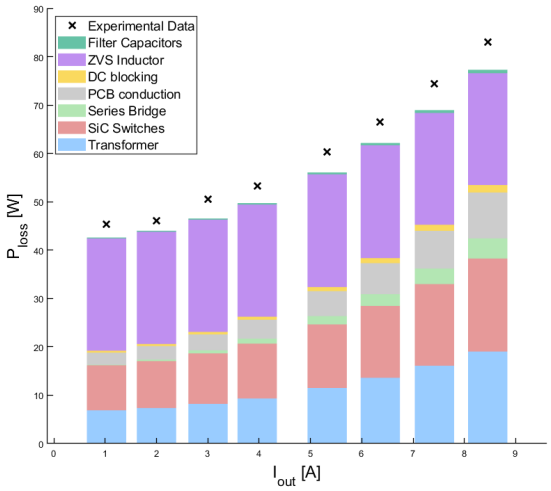


Fig. 18. Measured Loss at 600 V dc input voltage for various loads and the model predicted loss breakdown. The ZVS inductors contribute to a significant portion of the losses due to the high input voltage. They further contribute to conduction losses in the switches due to circulating currents.

slightly reduces the overall ac-ac conversion efficiency, but the total efficiency is expected to remain above 96% with the designed DCX module (two SB-DCX converters). This demonstrates the performance utility of the DCX stage within the proposed unfolding architecture.

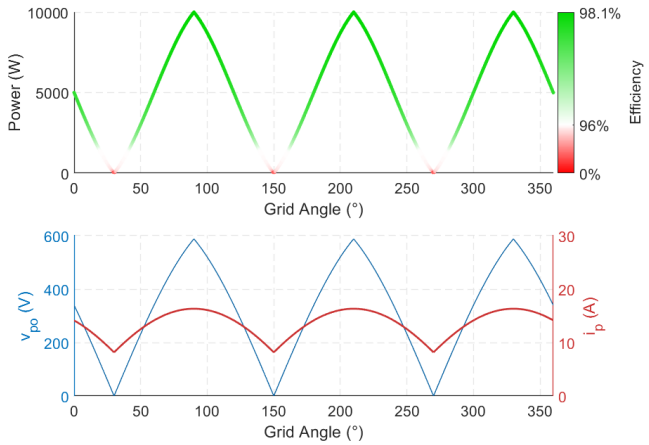


Fig. 19. Instantaneous power conversion efficiency heatmap predicted by the mathematical model for 10 kW of power when operation with time-varying input voltages unfolded for 480 V 3-ϕ ac input.

VI. Conclusion

This article presents the SB-DCX topology as a robust solution for implementing the DCX module in the proposed unfolding-based multi-port SST architecture. The SB-DCX enables natural input voltage sharing in the ISOP modular DCX stage for direct MV-connect applications and in combination with an unfolder, supports single-stage MV-to-LV power conversion. Conventional topologies struggle to achieve DCX operation under the time-varying input voltages introduced by the unfolder. This is primarily due to the absence of sufficient input voltage to build the necessary tank energy during near-zero input voltage conditions. Consequently, resonant converter-based operation is required, which must function precisely at resonance. The SB-DCX naturally achieves perfect series resonance, without requiring precise turning, thus improving practical feasibility. This is enabled by the series bridge and symmetric gating that forces the topology to operate as a DCX in steady-state, as validated through state-plane analysis.

Steady-state models are developed to guide the unique design elements of the SB-DCX and support its operation with time-varying input voltages. Hardware results demonstrate that the SB-DCX provides a reliable, high-performance solution for DCX operation. Efficiency measurements from a 600 V, 5 kW hardware prototype demonstrate a peak efficiency of 98.5%, with minimal energy consumption by the series bridge, further confirming the topology's effectiveness. In combination with an unfolder, the SB-DCX can process finite output currents even at near-zero input voltages, and functions as an ideal DCX. The complete DCX module (with two SB-DCX converters) processes 10 kW of power at an efficiency of 97.1% when operated with an unfolder (480 V 3-ϕ ac input). To obtain a 3-ϕ ac output from the output of the DCX stage (ISOP combination of DCX modules), an additional unfolder is required. Similarly, to obtain a dc output, a secondary dc-dc converter is needed. The DCX module built using SB-DCX dc-dc converters is envisioned as a scalable building block for high-power MV systems within the proposed architecture. By incorporating MV isolation capabilities, similar designs can be adapted for scalable direct-MV-connected power conversion solutions.

Appendix A
Analytical Proof for Inherent DCX Operation of SB-DCX

State-plane analysis [34], [35] is employed to examine the possible steady-state solutions of the SB-DCX topology under symmetric primary and secondary H-bridge gating. In this analysis, the transformer is assumed to have a unity turns ratio for simplicity, without loss of generality. All potential steady-state solutions are analyzed as a combination of state-plane trajectories, each corresponding to a linear time-invariant (LTI) circuit formed by the different switch-state combinations. The possible combinations are determined by the gate signals shown in Fig. 5.

By applying the definition of steady-state to impose constraints on the state variables, namely i_{tank} and v_c, it can be concluded that neglecting resistive losses, the steady-state operation of the SB-DCX is achieved when the output voltage V_{out} equals the input voltage V_{in}.

Not considering the deadtime duration (ignored for the analysis), there are a total of four unique switch-state combinations and, hence, four LTI circuits to analyze. The tank is composed of two energy storage components (L_{leakage} and C_{sb}) operating near resonance. This lends itself well to analyzing the converter using state-plane analysis. Hence, state-plane

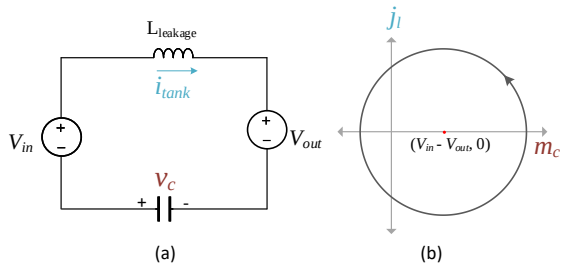


Fig. 20. (a) Equivalent circuit (b) and corresponding state-plane trajectory (ST1) for gating configuration: G_1 and G_2' On, G_2 and G_1' Off

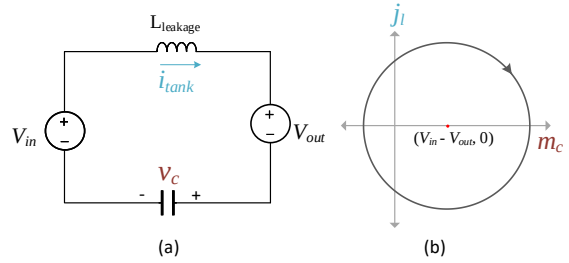


Fig. 21. (a) Equivalent circuit (b) and corresponding state-plane trajectory (ST2) for gating configuration: G_1 and G_1' On, G_2 and G_2' Off

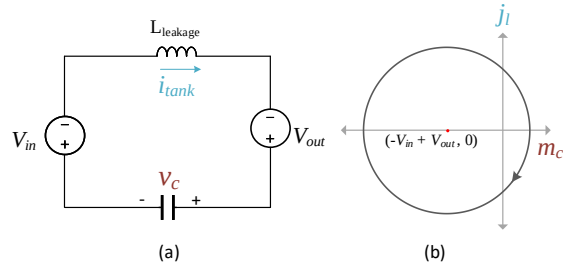


Fig. 22. (a) Equivalent circuit (b) and corresponding state-plane trajectory (ST3) for gating configuration: G_2 and G_1' On, G_1 and G_2' Off

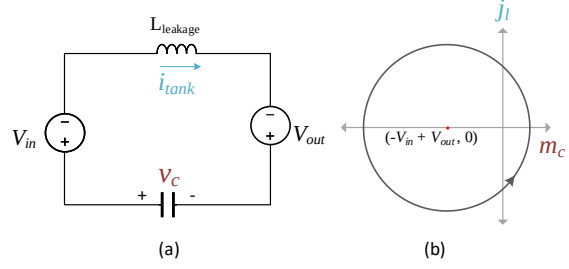


Fig. 23. (a) Equivalent circuit (b) and corresponding state-plane trajectory (ST4) for gating configuration: G_2 and G_2' On, G_1 and G_1' Off

trajectories are studied to understand the steady-state behavior of SB-DCX. It should be noted that analysis using state-plane methods is fundamentally the same as using time-domain mathematical equations. However, state-plane analysis enables the use of geometric intuition, simplifying the analysis.

For the different switch-state combinations (Fig. 5), the corresponding circuit models and the corresponding state-plane trajectories (normalized using equations (3) and (4)) are shown in Figs. 20-23. Losses are neglected to simplify the analysis. It is interesting to note that the shape of the state trajectory does not change from ST1 to ST2; only the tracking direction changes. Similarly, this applies to the transition from ST3 to ST4. Hence, the shape of two state-plane trajectories needs to be studied. ST1 and ST2 trajectory shape is represented as

$$(j_l)^2 + (m_c - V_{\text{in}} + V_{\text{out}})^2 = a^2 \tag{23}$$

and ST3 and ST4 trajectory shape is represented as

$$(j_l)^2 + (m_c + V_{\text{in}} - V_{\text{out}})^2 = b^2, \tag{24}$$

where a and b are proportional to the peak energy in the energy storage elements.

For a steady-state solution of the SB-DCX to exist as a combination of the four state-plane trajectories (ST1–ST4) and switches implemented as shown in Fig. 5, the following conditions must be met:

- The normalized states at the start and the end of a switching cycle must be equal (definition of steady-state).
- There must not be a jump in the normalized state after switching.
- The tank current must be antisymmetric about the half-cycle and must not have a dc offset (gating is symmetric for the positive and negative halves of the switching cycle - half-cycle symmetry).
- m_c must always be greater than zero (to ensure the body diodes of the SB-DCX do not conduct - as corresponding state-trajectories are not considered).

To satisfy the first two conditions, the two trajectories given by (23) and (24) must intersect at least once. Furthermore, for the tank currents to be antisymmetric, a must be equal to b. Therefore, by equating (23) with (24) and considering $a = b$, the two trajectories can intersect only if either

$$m_{c,\text{inters.}} = 0, \tag{25}$$

or

$$V_{\text{in}} = V_{\text{out}}. \tag{26}$$

is met.

The possible state-plane trajectories for the complete switching cycle that meet (25) and/or (26) are shown in Fig. 24. Because m_c must always be positive, the only steady-state solution possible for SB-DCX topology as a combination of the four state-plane trajectories is (26) i.e. $V_{\text{in}} = V_{\text{out}}$ (N = 1). Thus, analytically proving the inherent DCX operation of SB-DCX with symmetric gating.

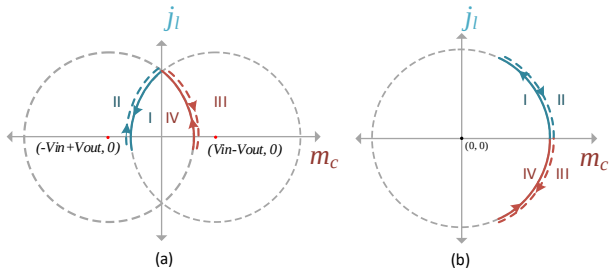


Fig. 24. (a) Steady-state state-plane trajectory for $m_{c,inters.} = 0$ (b) Steady-state state-plane trajectory for $V_{\text{in}} = V_{\text{out}}$.

APPENDIX B
C_{SB} VOLTAGE DECREASE WITH ADDITIONAL SERIES CAPACITANCE

The addition of C_{s} in series with the LV series bridge (SB) reduces the peak voltage (ΔV) across the SB capacitance C_{sb}. The value of ΔV can be determined using (19).

ΔV is the difference in peak voltage across C_{sb} without and with C_{s}. The peak voltage without C_{s} is given by (13). To find the peak voltage with C_{s}, the constraints imposed on capacitive energy requirement and the capacitor charge conservation are used. These constraints are represented as

$$C_{\text{sb}}\left(V_{\text{c,max-new}}^2 - V_{\text{c,min-new}}^2\right) + C_s V_{\text{c,s}}^2 = L_{\text{lkg}} I_{\text{max,new}}^2, \quad (27)$$

$$C_{\text{sb}}\left(V_{\text{c,max-new}} - V_{\text{c,min-new}}\right) = \frac{I_{\text{out}}}{4 f_{\text{sw}}}, \quad (28)$$

$$C_s V_{\text{c,s}} = \frac{I_{\text{out}}}{4 f_{\text{sw}}}, \quad (29)$$

where

$$I_{\text{max,new}} = \frac{I_{\text{out}} \sin\left(\frac{1}{\sqrt{L_{\text{lkg}} C}\cdot 4 f_{\text{sw}}}\right)}{\left(4 f_{\text{sw}}\sqrt{L_{\text{lkg}} C}\right)\cdot\left(1-\cos\left(\frac{1}{\sqrt{L_{\text{lkg}} C}\cdot 4 f_{\text{sw}}}\right)\right)}. \quad (30)$$

Solving (27) – (30) to get an expression for $V_{\text{c,max-new}}$. The voltage difference is obtained using

$$\Delta V = V_{\text{c,max}} - V_{\text{c,max-new}}. \quad (31)$$

REFERENCES

[1] J. Huber, L. Imperiali, D. Menzi, F. Musil, and J. W. Kolar, "Energy efficiency is not enough!" *IEEE Power Electronics Magazine*, vol. 11, no. 1, pp. 18–31, 2024.

[2] R. Singh, P. Paniyil, and Z. Zhang, "Transformative role of power electronics: In solving climate emergency," *IEEE Power Electronics Magazine*, vol. 9, no. 2, pp. 39–47, 2022.

[3] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 861–878, 2019.

[4] J. Huber, P. Wallmeier, R. Pieper, F. Schafmeister, and J. W. Kolar, "Comparative evaluation of mvac-lvdc sst and hybrid transformer concepts for future datacenters," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, 2022, pp. 2027–2034.

[5] J. E. Huber and J. W. Kolar, "Volume/weight/cost comparison of a 1mva 10 kv/400 v solid-state against a conventional low-frequency distribution transformer," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 4545–4552.

[6] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, 2013.

[7] J. Huber, U. Drofenik, F. Canales, and J. W. Kolar, "Comparative evaluation of three-phase-unfolder-based mvac-lvdc solid-state transformers," in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2024, pp. 254–263.

[8] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Swiss rectifier — a novel three-phase buck-type pfc topology for electric vehicle battery charging," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2617–2624.

[9] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase ac–dc power conversion using series-resonant converter modules and a three-phase unfolder," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9001–9012, 2017.

[10] D. B. Yelaverthi, M. Mansour, H. Wang, and R. Zane, "Triple active bridge series resonant converter for three-phase unfolding based isolated converters," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 4924–4930.

[11] D. B. Yelaverthi, R. Hatch, M. Mansour, H. Wang, and R. Zane, "3-level asymmetric full-bridge soft-switched pwm converter for 3-phase unfolding based battery charger topology," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2737–2743.

[12] J. E. Huber and J. W. Kolar, "Applicability of solid-state transformers in today's and future distribution grids," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 317–326, 2019.

[13] S. Roy, M. Joisher, and A. J. Hanson, "A decentralized nonlinear control scheme for modular power sharing in dc-dc converters," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 2798–2805.

[14] F. Gao, R. Kang, J. Cao, and T. Yang, "Primary and secondary control in dc microgrids: a review," *Journal of Modern Power Systems and Clean Energy*, vol. 7, no. 2, pp. 227–242, 2019.

[15] B. Majmunović, S. Mukherjee, T. Martin, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson, and D. Maksimović, "1 kv, 10-kw sic-based quadruple active bridge dcx stage in a dc to three-phase ac module for medium-voltage grid integration," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14 631–14 646, 2022.

[16] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimović, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 5774–5781.

[17] S. Mukherjee, A. Kumar, and S. Chakraborty, "Comparison of dab and llc dc–dc converters in high-step-down fixed-conversion-ratio (dcx) applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4383–4398, 2021.

[18] W. Qin, X. Wu, and J. Zhang, "A family of dc transformer (dcx) topologies based on new zvzcs cells with dc resonant capacitance," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2822–2834, 2017.

[19] J. Kucka and D. Dujic, "Smooth power direction transition of a bidirectional llc resonant converter for dc transformer applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6265–6275, 2021.

[20] B. Zhao, Q. Song, J. Li, Y. Wang, and W. Liu, "Modular multilevel high-frequency-link dc transformer based on dual active phase-shift principle for medium-voltage dc power distribution application," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1779–1791, 2017.

[21] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kv sic-based 7 kv/400 v dc transformer for future data centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, 2019.

[22] A. Esser and H.-C. Skudelny, "A new approach to power supplies for robots," *IEEE Transactions on Industry Applications*, vol. 27, no. 5, pp. 872–875, 1991.

[23] Y. Yin, M. Shirazi, and R. Zane, "Electronic ballast control ic with digital phase control and lamp current regulation," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 11–18, 2008.

[24] S. Jiang, W. Zhang, B. Liu, and F. Wang, "Automatic resonant frequency tracking in unregulated llc resonant converters based on total resonant current harmonic calculation," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 4193–4198.

[25] W. Feng, P. Mattavelli, and F. C. Lee, "Pulsewidth locked loop (pwll) for automatic resonant frequency tracking in llc dc–dc transformer (llc -dcx)," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1862–1869, 2013.

[26] R. Raju, "Series resonant converters with the resonant capacitor replaced by a bridge," in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, 2017, pp. 999–1,002.

[27] Y. Cao and D. Dong, "Design and implementation of a 12 kw scalable electronic-embedded transformer (eet)-based dc transformer (dcx) with trapezoidal current," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 2340–2347.

[28] X. Wang, Y. Peng, J. Chai, Y. Xia, W. Wei, and M. Yu, "An ideal dc transformer for active dc distribution networks based on constant-transformation-ratio dabc," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 2170–2183, 2020.

[29] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3931–3940, 2013.

[30] R. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 174–182, 1988.

[31] Y. Ren, M. Xu, J. Sun, and F. Lee, "A family of high power density unregulated bus converters," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1045–1054, 2005.

[32] S. Lim, A. J. Hanson, J. A. Santiago-González, and D. J. Perreault, "Bus converter using isolation capacitance for zvs and invariant operation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 1971–1982, 2020.

[33] Y. Cao, K. D. T. Ngo, and D. Dong, "Hybrid electronic-embedded transformer-based dc transformer (eet-dcx): A new family of soft-switching dcxs," *IEEE Transactions on Power Electronics*, vol. 39, no. 8, pp. 9661–9679, 2024.

[34] M. Daryaei, S. A. Khajehoddin, J. Mashreghi, and K. K. Afridi, "A new approach to steady-state modeling, analysis, and design of power converters," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12 746–12 768, 2021.

[35] R. Oruganti and F. C. Lee, "Resonant power processors, part i—state plane analysis," *IEEE Transactions on Industry Applications*, vol. IA-21, no. 6, pp. 1453–1460, 1985.

[36] J. Rivas, R. Wahby, J. Shafran, and D. Perreault, "New architectures for radio-frequency dc–dc power conversion," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 380–393, 2006.

[37] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 985–995, 2015.

[38] B. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455–457, 1989.

[39] Y. Cao, K. D. T. Ngo, and D. Dong, "Hybrid electronic-embedded transformer-based dc transformer (eet-dcx): A new family of soft-switching dcxs," *IEEE Transactions on Power Electronics*, vol. 39, no. 8, pp. 9661–9679, 2024.

[40] X. Zhang, H. Liu, P. Wheeler, and F. Wu, "Research on power decoupling and parameter mismatch of three-port isolated resonant dc–dc converter applied switch-controlled capacitor," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 8, pp. 8098–8107, 2023.

[41] A. J. Hanson and D. J. Perreault, "Modeling the magnetic behavior of n-winding components: Approaches for unshackling switching superheroes," *IEEE Power Electronics Magazine*, vol. 7, no. 1, pp. 35–45, 2020.

[42] A. Zade, C. R. Teeneti, S. Gurudiwan, S. Poddar, M. Mansour, and R. Zane, "Analysis and mitigation of sector transition distortions for unfolding-based grid-tied ac-dc converters," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1945–1952.

[43] S. Poddar, M. Mansour, A. Zade, and R. Zane, "Investigation of input current distortion at sector transitions in unfolding-based grid-tied ac-dc converters," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 2238–2244.

[44] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, "Novel swiss rectifier modulation scheme preventing input current distortions at sector boundaries," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5771–5785, 2017.

[45] L. Schrittwieser, M. Leibl, M. Haider, F. Thöny, J. W. Kolar, and T. B. Soeiro, "99.3% efficient three-phase buck-type all-sic swiss rectifier for dc distribution systems," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 126–140, 2019.

CHAPTER 5

Dead Time Modeling and Control of DAB-SRC for DCX operation

The dual-active-bridge series-resonant converter (DAB-SRC) is another converter topology that can be used for DCX operation in combination with a three-phase unfolder. However, this approach requires the resonant tank to be precisely tuned to resonance, which is challenging to achieve in practical systems. This work demonstrates that resonance mistuning can be naturally mitigated by counteracting mechanisms that occur during dead time. Mathematical models have been developed to predict the minimum dead time with high accuracy, enabling the practical use of the DAB-SRC for DCX operation with unfolder.

The DAB-SRC inherently supports the bidirectional operation of the DCX stage in combination with an unfolder. In contrast, the SB-DCX topology enables perfect resonance operation without the need for precise tuning of the series capacitor and has been shown to function effectively as the DCX stage with unfolder in previous chapters. However, for applications requiring bidirectional power flow, implementing the SB-DCX demands 4-Q switches, which drastically increase the number of gate control signals and the associated cost, while also degrading performance. Therefore, the DAB-SRC presents a promising alternative, as it can achieve bidirectional operation with a precisely tuned resonant capacitor and symmetric gating of the two bridges.

Nevertheless, it is practically challenging to maintain exact resonance tuning at all times, and operation can drift away from resonance due to component aging or environmental factors. This work found that the DAB-SRC can continue to function effectively as a DCX even with resonance mistuning, thanks to inherent counteracting mechanisms during dead time. However, a minimum dead time is required, depending on the load and the extent of mistuning. Therefore, it is practically important to develop mathematical models that accurately determine the minimum dead time as a function of load conditions and resonance mistuning.

This chapter presents detailed nonlinear models and simplified linear models (with appropriate approximations) that predict the minimum dead time with good accuracy. These models can be used to design the DAB-SRC for robust DCX operation across a wide range of mistuning or to actively control the DAB-SRC dead time, enabling reliable DCX performance when combined with the unfolder.

The contents of this chapter are a replication of the paper presented at the 2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL) [41].

Estimation of Minimum Dead Time to Counter Resonance Mistuning in DAB-SRC for DCX Operation

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***Abstract*—A DC transformer (DCX) is a dc-dc converter that operates at a fixed voltage conversion ratio, enabling optimized and simplified power converter design. This paper explores the use of a dual-active-bridge series resonant converter (DAB–SRC) topology, in which both bridges are actively switched with symmetric gate signals near the series resonant frequency to achieve uncontrolled, bidirectional DCX operation. It is observed that this topology inherently compensates for resonance mistuning—arising from practical non-idealities—through a counterbalancing mechanism that occurs during the dead time between switching transitions. This paper investigates and models this counterbalancing phenomenon and develops analytical expressions to predict the minimum dead time required for two key cases: stable operation and complete zero-voltage switching (ZVS). The resulting models express the dead time as a function of resonance mistuning and load current, providing a practical framework for designing SRCs that operate as mistuning-tolerant, bidirectional DCXs without the need for feedback control. The proposed models are validated using experimental data collected from a hardware prototype operating at input voltages up to 50 V and power levels up to 200 W. The predicted dead times closely match the measured values, with an error of less than 15%.**

***Index Terms*—DCX, DAB-SRC, resonance, mistuning, tuning, dead time**

I. Introduction

Topologies that operate as DCX are widely employed in applications such as data center power distribution, battery charging systems, and renewable energy interfaces [1]–[4]. The voltage conversion ratio is typically fixed by the transformer turns ratio and circuit topology. This fixed-ratio operation simplifies the control strategy and enables design optimization for high efficiency at a single, well-defined voltage conversion point. As a result, DCXs are well-suited for integration into multi-stage power conversion architectures aimed at achieving high overall performance [5], [6].

The SRC operating in DCM is frequently used as a DCX due to its simple implementation and uncontrolled DCX characteristics [7], [8]. The topology operates at a frequency below resonance and employs passive diodes for the secondary H-bridge, resulting in natural, load-independent DCX behavior without the need for active control. However, the use of passive diodes prevents bidirectional power flow, limiting the flexibility of the topology. Although these diodes can be replaced with synchronous switches, the added control complexity may be undesirable. Additionally, under light-load conditions, severe oscillations caused by mismatches between the semiconductor capacitance of the primary and secondary bridges degrade efficiency and cause EMI challenges [9].

This work investigates an SRC with active switches in both the primary and secondary H-bridges for DCX operation (as shown in Fig. 1). Furthermore, the operation under symmetric gate signals (for primary and secondary H-bridges) and ideally at the series resonant frequency is explored [1], [9]. This approach enables ideal bidirectional power transfer without the need for active control. Although this method has been examined in prior literature, it requires precise tuning of the series capacitors to ensure operation exactly at resonance. In practice, however, component tolerances, manufacturing variability, and aging effects make such precise tuning difficult to maintain. While the operating frequency can be adjusted to track the shifting resonant point [10]–[12], this introduces additional control complexity and potential stability challenges.

This paper demonstrates that the series resonant converter (SRC) with symmetric gating naturally compensates for resonance mistuning by counterbalancing its effects during the dead time. It does so by enabling phase shift between bridge voltages and operating as a naturally phase-shifted dual active bridge (DAB) with DCX characteristics. Section II presents the physical basis of this counterbalancing mechanism and shows that a minimum dead time is required to achieve both stable operation and zero-voltage switching (ZVS) across all switches. In Section III, a detailed time-domain mathematical model is developed in the form of a set of nonlinear constraints, which accurately predict the minimum required dead time. This model can assist in the design and component selection process for SRCs operating as DCXs. Section IV

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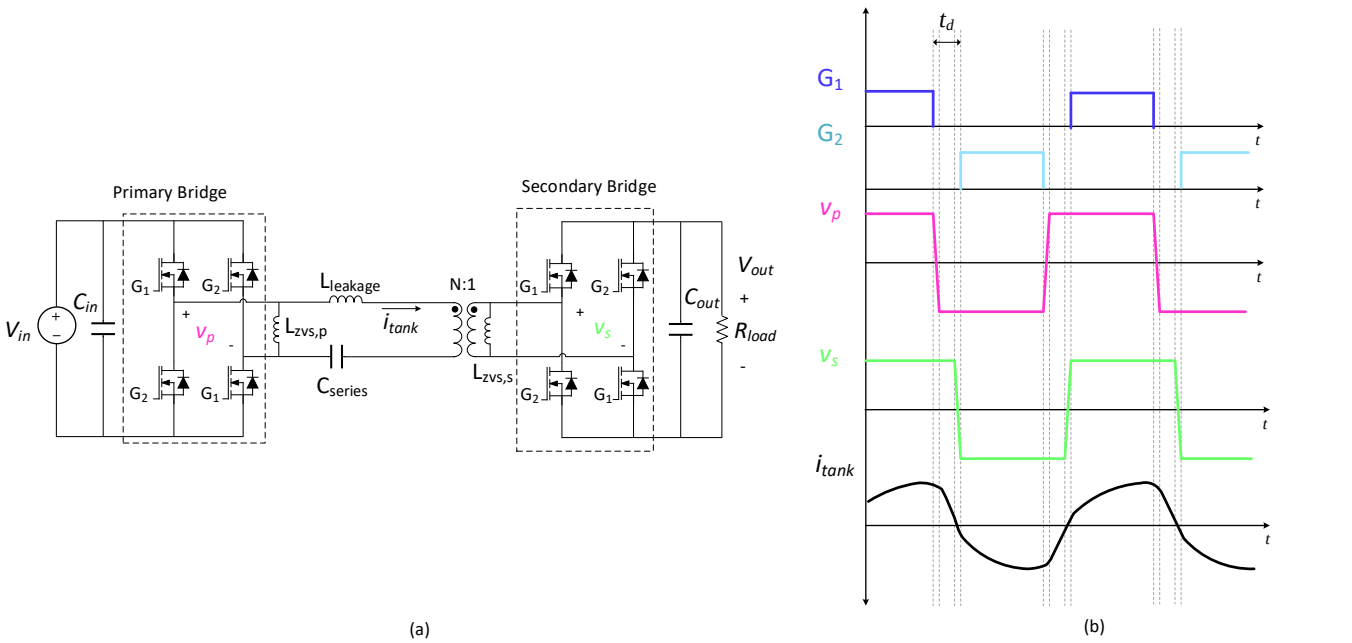


Fig. 1. (a) The DAB-SRC topology: a series resonance tank excited by symmetrically gated (same gating signals for primary and secondary) bridges - ideally operating at resonance. ZVS inductors are added as shown to achieve load-independent ZVS. (b) The tank waveforms for ideal steady-state operation are depicted for $k > 1$. The tank current adjusts its shape naturally to ensure that there's enough phase-shift between the primary and the secondary switch-node voltages during the dead time.

simplifies the nonlinear model to obtain linear equations that estimate the minimum dead time required for both stable operation and soft-switching, as a function of resonance mistuning and converter specifications. The linear model offers good predictive accuracy, with an error margin of less than 15%, and can be used for adaptive dead time tuning based on operating conditions. Finally, Section V validates the proposed models using measurements from a hardware prototype.

II. Mechanism to Counter Resonance Mistuning during Dead Time

Ideally, operating a fully active Series Resonant Converter (SRC) with symmetric gate signals (as shown in Fig. 1), at the resonance frequency, results in natural DCX operation [1], [2]. When the SRC operates exactly at resonance, it facilitates a load-independent voltage gain and enables bidirectional power transfer. This topology exhibits all the characteristics desired in an ideal DCX.

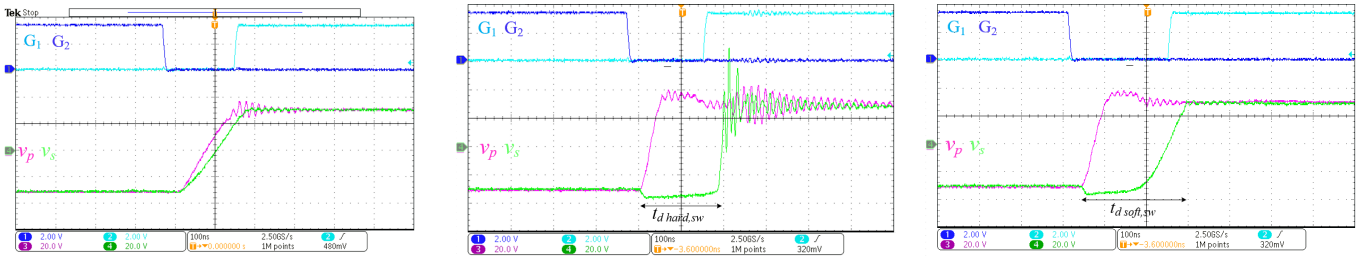
However, it is practically challenging to switch exactly at the resonance frequency due to manufacturing tolerances, operational variations, or aging effects, which lead to tuning mismatch.

Neglecting the dead time duration, the operation can shift away from resonance due to tolerances in C_{res}, L_{leakage}, or the switching frequency f_{sw}. Here, all sources of mistuning are captured in a single parameter k, which quantifies the deviation of series capacitance (C_{series}) from its ideal resonant value (C_{res}). This mismatch can be mathematically represented by a factor k, defined as $k = \frac{C_{\text{series}}}{C_{\text{res}}}$.

This work finds that when $k \neq 1$, a sufficient dead time interval is necessary to achieve a stable output voltage for a given load current. In contrast, for $k = 1$, the SRC is inherently stable and operates exactly at resonance, regardless of whether dead time is applied, as established in prior literature [2]. This is because, under symmetric gating, real power transfer—and thus regulation of the output voltage—requires the tank impedance to be zero, a condition that is inherently satisfied at resonance.

However, with mistuning ($k \neq 1$), the tank impedance becomes finite. Assuming a constant output voltage, the presence of finite tank impedance under symmetric gating prevents real power flow through the tank (neglecting series resistance losses), thereby violating the assumption of output voltage stability. It is observed that introducing dead time mitigates this issue by enabling power transfer, thus restoring stable operation.

To achieve power transfer and maintain a stable output voltage, the tank current adjusts itself to introduce a phase shift between the primary and secondary bridge voltages (v_p and v_s in Fig. 1(a)) during the dead time. This behavior is illustrated in the hardware waveforms shown in Fig. 2(a–c) for the mistuned case where $k = 1.6$ (or an inductive tank impedance). The tank current naturally evolves to enable zero-voltage switching (ZVS) commutation of the primary switch-node voltage (v_p) at the beginning of the dead time, and that of the secondary voltage (v_s) at the end. Assuming negligible ZVS transition time, the dead time t_d effectively represents the phase shift required to build real current in the inductive



(a) (b) (c)

Fig. 2. Hardware waveforms illustrating the dead time duration for an input voltage of 30 V and $k = 1.6$. (a) For a load current of 0.2 A, a dead time of 180 ns is more than sufficient to achieve the required phase shift. (b) For a load current of 2 A, a dead time of 190 ns is the minimum required to ensure stable operation, with the secondary bridge experiencing hard switching. (c) For a load current of 2 A, a dead time of 260 ns is sufficient to achieve stable operation and enable soft switching on both bridges. This paper develops models to predict these dead times as a function of system parameters.

tank (for $k > 1$), thereby enabling power transfer. Hence, a minimum dead time is necessary to maintain a stable output voltage and support the required output current under mistuned conditions.

III. Detailed Modeling to Predict Minimum Dead Time Required for Resonance Mistuning Tolerance

It is useful to obtain steady-state models that predict the minimum required dead time to achieve stable operation. These models can be used to design the DCX to operate reliably under the maximum permissible mistuning (characterized by k). Furthermore, the dead time can be adjusted in real-time as a function of load current depending on the maximum mistuning. For this, one needs simple linear models that predict the minimum required dead time for both hard-switched and soft-switched cases.

For $k > 1$, a minimum dead time—denoted as $t_{\text{d,hard,sw}}$ in Fig. 2(b)—is required to ensure stable operation for a given load current, with minimal deviation in output voltage from the ideal DCX value. However, achieving soft switching on both the primary and secondary H-bridges necessitates additional dead time. The total dead time required for stable operation with soft switching on both bridges is denoted $t_{\text{d,soft,sw}}$, as shown in Fig. 2(c).

Time-domain analysis is used to develop detailed non-linear models to more accurately characterize the system behavior in steady state. This model will be simplified to derive closed-form expressions for $t_{\text{d,hard,sw}}$ and $t_{\text{d,soft,sw}}$ as functions of the load current, resonance mistuning, and relevant circuit parameters.

For each LTI circuit that results from different switch-state combinations, the state variables are tracked as a function of time. Since the time-domain waveforms are antisymmetric about $T_{\text{sw}}/2$, it is sufficient to track the state variables over this half-cycle interval to obtain complete information for the entire switching cycle, which repeats under steady-state conditions. Constraints for steady-state are imposed on the state variable that results in a system of non-linear equations that can be numerically solved to obtain the required minimum dead times. The analysis presented here focuses on the mistuning case where $k > 1$, but it can be readily extended to scenarios with $k < 1$.

The equivalent circuits for each subinterval (corresponding to a unique switch-state combination) are shown in Fig. 3, for the case of $k > 1$. These circuits represent one-half of the switching period, $T_{\text{sw}}/2$. The corresponding subintervals and ideal waveforms for the complete switching cycle are shown in Fig. 4(a).

To enable load-independent zero-voltage switching (ZVS) for both bridges, dedicated ZVS inductors are added, as shown in Fig. 1(a). These inductors are assumed to behave as constant current sources, carrying peak tank currents $I_{\text{pk},1}$ and $I_{\text{pk},2}$ during the dead time interval. The switch output capacitance C_{oss} is modeled using the charge-equivalent capacitance evaluated at the corresponding voltage.

In Subinterval I, switch G2 is ON and G1 is OFF. Subintervals II–IV correspond to the dead time transition period for a fully soft-switched operation, with the associated circuits illustrated in Fig. 3(b)–(d).

As detailed earlier, the tank current adjusts itself to ensure a phase shift exists between the tank excitation voltages v_p and v_s, to counteract the effect of non-zero tank impedance. This adjustment is achieved by time-shifting the soft-switching resonant transitions of the primary and secondary bridges accordingly, within the minimum possible dead time—denoted as $t_{\text{d,soft,sw}}$. This behavior is illustrated in Fig. 4(b), which shows a zoomed-in view of the waveforms during the dead time interval.

For $k > 1$, the tank current naturally adjusts to enable zero-voltage switching (ZVS) of the primary-side switches at the beginning of subinterval II. The circuit behavior during this interval corresponds to Fig. 3(b), where the primary bridge undergoes ZVS transition while the body diodes on the secondary side conduct. Subintervals III (natural phase shift) and IV (secondary-side ZVS) are represented by the circuits shown in Fig. 3(c) and Fig. 3(d), respectively.

If the applied dead time ($< t_{\text{d,soft,sw}}$) is insufficient to ensure soft switching, stable operation (with minimal drop in output voltage) can still be maintained by setting the dead time to $t_{\text{d,hard,sw}}$, in which case the secondary bridge undergoes hard switching. The corresponding waveforms are shown in

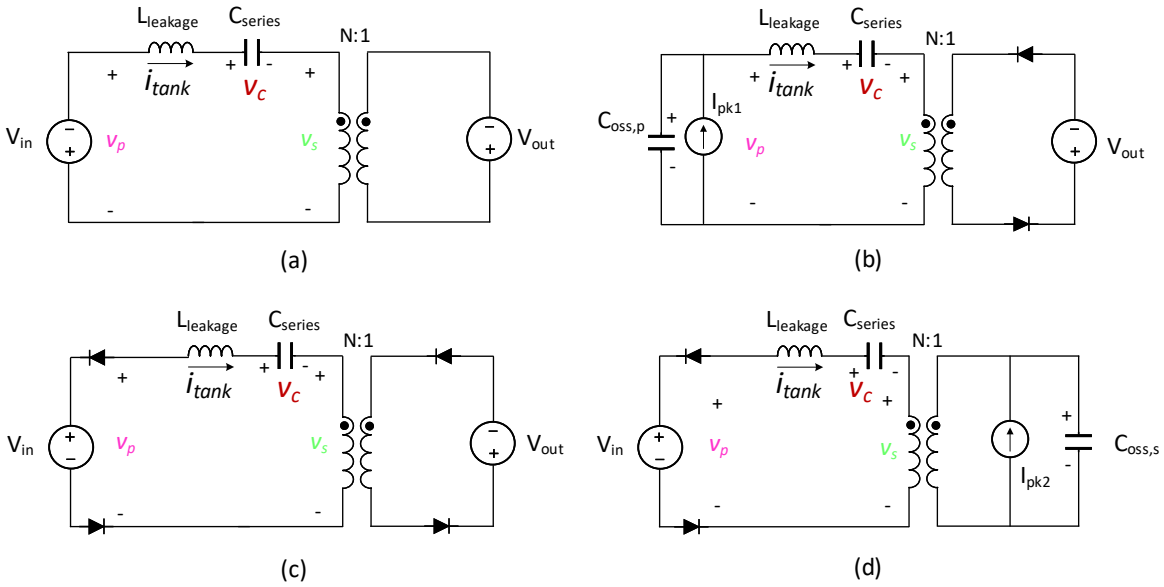


Fig. 3. Equivalent circuits of the SRC for different subintervals within a $T_{\text{sw}}/2$ switching cycle, depicted for $k > 1$: (a) Subinterval I, (b) Subinterval II, (c) Subinterval III, (d) Subinterval IV.

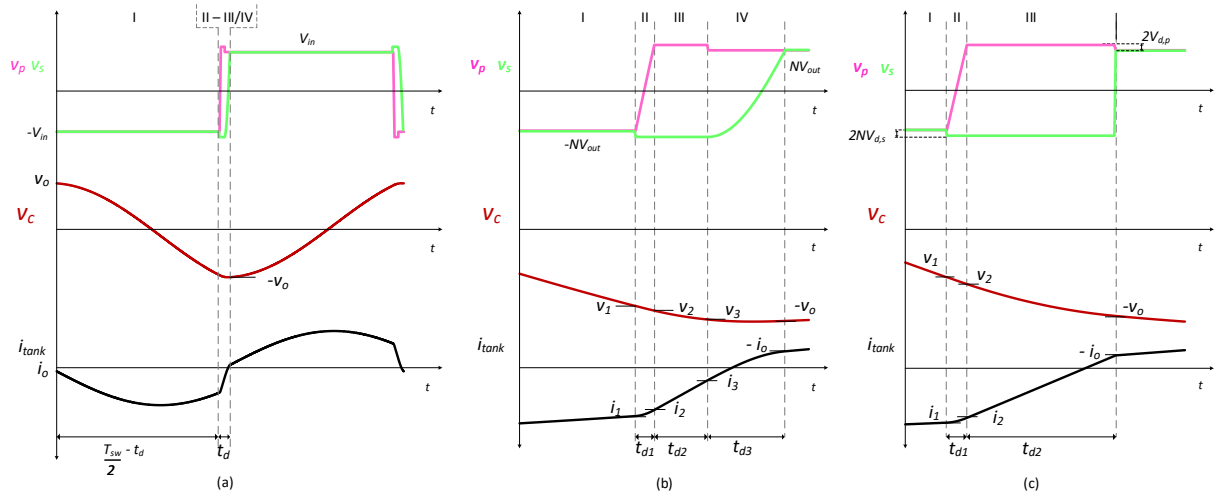


Fig. 4. (a) Ideal time-domain waveforms for a complete switching cycle in steady state for $k > 1$. Because the gate signals are symmetric, the tank current and tank capacitor voltage waveforms are antisymmetric about $t = T_{\text{sw}}/2$. (b) Zoomed-in view of the dead time transition when both the primary and secondary are soft-switched. (c) Zoomed-in view of the dead time transition when the secondary is hard-switched.

Fig. 4(c). Note that subinterval IV is absent in the hard-switched case, and the boundary conditions on the tank current (i_{tank}) and tank capacitor voltage (v_c) are modified accordingly.

The set of nonlinear equations derived from the time-domain analysis used to compute the minimum dead time required for complete soft-switching ($t_{\text{d,soft,sw}}$), is summarized in Table I. The value of $t_{\text{d,soft,sw}}$ can be obtained by solving for t_{dead} using a numerical solver.

Eqs. (3)–(12) are derived by applying boundary conditions and enforcing steady-state operation on the evolution of state variables obtained by solving the equivalent linear circuits (from subinterval I-IV) shown in Fig. 3. In particular, steady-state antisymmetry about $T_{\text{sw}}/2$ is invoked, where $v_c(T_{\text{sw}}/2) = -v_c(0) = -v_o$ and $i_{\text{tank}}(T_{\text{sw}}/2) = -i_{\text{tank}}(0) = -i_o$. (1) imposes a constraint that the average tank current must equal the output current in steady-state. Similarly, (2) constrains the total dead time to not exceed the minimum duration required for a complete ZVS transition.

The analysis assumes a high tank quality factor and negligible FET on-resistance—approximations that are valid for most design cases and significantly simplify the derivation. In addition, the voltage ripple on the input and output capacitors is neglected, and the capacitors are modeled as ideal voltage sources, V_{in} and V_{out}, respectively. While this assumption

TABLE I
NONLINEAR EQUATIONS NEEDED TO SOLVE FOR t_{dead} TO OBTAIN $t_{d,soft,sw}$

$$C_{\text{series}} \cdot \frac{v_o - v_3}{T_{\text{sw}}/2} = \frac{I_{\text{out}}}{N} \tag{1}$$

$$t_{d1} + t_{d2} + t_{d3} = t_{\text{dead}} \tag{2}$$

$$v_1 = (v_o - \Delta V)\cos\left(\omega\left(\frac{T_{\text{sw}}}{2} - t_{\text{dead}}\right)\right) + i_o Z \sin\left(\omega\left(\frac{T_{\text{sw}}}{2} - t_{\text{dead}}\right)\right) + \Delta V, \quad \Delta V = NV_{\text{out}} - V_{\text{in}} \tag{3}$$

$$i_1 = -\frac{(v_o - \Delta V)}{Z}\sin\left(\omega\left(\frac{T_{\text{sw}}}{2} - t_{\text{dead}}\right)\right) + i_o \cos\left(\omega\left(\frac{T_{\text{sw}}}{2} - t_{\text{dead}}\right)\right) \tag{4}$$

$$v_2 = v_1 + \frac{i_1 - I_{\text{split}}}{\omega_{\text{eq},p} C_{\text{series}}}\sin(\omega_{\text{eq},p} t_{d1}) + \frac{-V_{\text{in}} - v_1 + N(V_{\text{out}} + 2V_{d,s})}{L(\omega_{\text{eq},p})^2 C_{\text{series}}}(1 - \cos(\omega_{\text{eq},p} t_{d1})) + \frac{I_{\text{split}}}{C_{\text{series}}} t_{d1} \tag{5}$$

$$V_{\text{in}} = -V_{\text{in}} - \frac{(i_1 - I_{\text{split}})}{\omega_{\text{eq},p} C_{\text{oss},p}}\sin(\omega_{\text{eq},p} t_{d1}) - \frac{(-V_{\text{in}} - v_1 + N(V_{\text{out}} + 2V_{d,s}))}{L(\omega_{\text{eq},p})^2 C_{\text{oss},p}}(1 - \cos(\omega_{\text{eq},p} t_{d1})) + \frac{dI_{\text{split}}}{C_{\text{oss},p}} t_{d1} \tag{6}$$

$$i_2 = (i_1 - I_{\text{split}})\cos(\omega_{\text{eq},p} t_{d1}) + \frac{-V_{\text{in}} - v_1 + N(V_{\text{out}} + 2V_{d,s})}{L\omega_{\text{eq},p}}\sin(\omega_{\text{eq},p} t_{d1}) + I_{\text{split}} \tag{7}$$

$$-\frac{I_{\text{pk},2}}{N} = i_2 \cos(\omega t_{d2}) - \frac{(v_2 - (V_{\text{in}} + 2V_{d,p} + N(V_{\text{out}} + 2V_{d,s})))\sin(\omega t_{d2})}{Z} \tag{8}$$

$$v_3 = Z i_2 \sin(\omega t_{d2}) + (v_2 - (V_{\text{in}} + 2V_{d,p} + N(V_{\text{out}} + 2V_{d,s})))\cos(\omega t_{d2}) + V_{\text{in}} + 2V_{d,p} + N(V_{\text{out}} + 2V_{d,s}) \tag{9}$$

$$-i_o = -I_{p,\cos}\cos(\omega_{\text{eq},s} t_{d3}) + \frac{-v_3 + N(V_{\text{out}} + 2V_{d,s}) + V_{\text{in}} + 2V_{d,p}}{L\omega_{\text{eq},s}}\sin(\omega_{\text{eq},s} t_{d3}) - I_{s,\text{dc}} \tag{10}$$

$$NV_{\text{out}} = -N(V_{\text{out}} + 2V_{d,s}) - \frac{I_{p,\cos}}{\omega_{\text{eq},s} C_{\text{oss},s,r}}\sin(\omega_{\text{eq},s} t_{d3}) - \frac{(v_3 - N(V_{\text{out}} + 2V_{d,s}) - (V_{\text{in}} + 2V_{d,p}))}{L(\omega_{\text{eq},s})^2 C_{\text{oss},s,r}}(1 - \cos(\omega_{\text{eq},s} t_{d3})) + \frac{I_{p,\cos}}{C_{\text{oss},s,r}} t_{d3} \tag{11}$$

$$-v_o = v_3 - \frac{I_{p,\cos}}{\omega_{\text{eq},s} C_{\text{series}}}\sin(\omega_{\text{eq},s} t_{d3}) - \frac{(v_3 - N(V_{\text{out}} + 2V_{d,s}) - (V_{\text{in}} + 2V_{d,p}))}{L(\omega_{\text{eq},s})^2 C_{\text{series}}}(1 - \cos(\omega_{\text{eq},s} t_{d3})) - \frac{I_{s,\text{dc}}}{C_{\text{series}}} t_{d3} \tag{12}$$

simplifies the model, it leads to a slight overestimation of the required dead times (approximately 5–20%). This limitation is revisited in Section IV, where the impact of voltage ripple is incorporated—using physical intuition—into a simplified model as a function of the load.

In table I, $V_{d,p}$ and $V_{d,s}$ model the voltage drops across the body diodes of the primary and secondary FETs, respectively. The following variables are derived from the circuit and switching parameters and are used in the nonlinear dead-time modeling equations.

The characteristic impedance and angular frequency of the series-resonant tank are defined as

$$Z = \sqrt{\frac{L}{C_{\text{series}}}}, \quad \omega = \frac{1}{\sqrt{LC_{\text{series}}}}, \tag{13}$$

where $L = L_{\text{leakage}}$. The effective output capacitance of the secondary-side bridge, referred to the primary side, is

$$C_{\text{oss,s,r}} = \frac{C_{\text{oss,s}}}{N^2}. \tag{14}$$

The equivalent capacitance during the primary-side and secondary-side ZVS transitions are

$$C_{\text{eq},p} = \frac{C_{\text{oss},p} \cdot C_{\text{series}}}{C_{\text{oss},p} + C_{\text{series}}}, \quad C_{\text{eq},s} = \frac{C_{\text{oss,s,r}} \cdot C_{\text{series}}}{C_{\text{oss,s,r}} + C_{\text{series}}}. \tag{15}$$

The corresponding resonant impedance and angular frequency for the primary-side transition are

$$Z_{\text{eq},p} = \sqrt{\frac{L}{C_{\text{eq},p}}}, \quad \omega_{\text{eq},p} = \frac{1}{\sqrt{LC_{\text{eq},p}}}, \tag{16}$$

and for the secondary-side transition,

$$Z_{\text{eq},s} = \sqrt{\frac{L}{C_{\text{eq},s}}}, \quad \omega_{\text{eq},s} = \frac{1}{\sqrt{LC_{\text{eq},s}}}. \tag{17}$$

The peak ZVS inductor currents for the primary and secondary sides, assumed constant during ZVS transitions are

$$I_{\text{pk,1}} = \frac{T_{\text{sw}} V_{\text{in}}}{4L_{zvs,p}}, \quad I_{\text{pk,2}} = \frac{T_{\text{sw}} V_{\text{out}}}{4L_{zvs,s}}. \tag{18}$$

During the primary-side ZVS transition, the peak inductor current $I_{\text{pk},1}$ splits as

$$I_{\text{split}} = I_{\text{pk},1} \cdot \frac{C_{\text{series}}}{C_{\text{oss},p} + C_{\text{series}}}, \quad dI_{\text{split}} = I_{\text{pk},1} \cdot \frac{C_{\text{oss},p}}{C_{\text{oss},p} + C_{\text{series}}}. \tag{19}$$

For the secondary-side transition, the reflected peak current $I_{\text{pk},2}$ splits as

$$I_{s,\text{dc}} = \frac{I_{\text{pk},2} \cdot C_{\text{series}}}{C_{\text{series}} + C_{\text{oss,s,r}}} \cdot \frac{1}{N}, \quad I_{p,\cos} = \frac{I_{\text{pk},2} \cdot C_{\text{oss,s,r}}}{C_{\text{series}} + C_{\text{oss,s,r}}} \cdot \frac{1}{N}. \tag{20}$$

To obtain $t_{\text{d,hard,sw}}$, the same set of equations is solved with the modification that t_{d3} is set to zero, effectively removing the secondary-side ZVS transition. In this case, Eqs. (10)–(12) are omitted, and additional boundary conditions are applied: the initial tank current is fixed as $i_o = I_{\text{pk},2}/N$, and the final tank capacitor voltage $v_3 = -v_o$.

The nonlinear system of equations was solved numerically using MATLAB's `fsolve` function, resulting in highly accurate predictions of the required dead times $t_{\text{d,soft,sw}}$ and $t_{\text{d,hard,sw}}$. For the circuit parameters listed in Table II, the model consistently overestimates the required dead time, with an average error of approximately 5%, increasing to as much as 20% at higher load currents. The error at low currents is primarily due to the assumption of constant ZVS inductor current during the dead time transition, particularly in Subinterval IV (duration t_{d3}). At higher currents, the dominant source of error is the voltage ripple across the input and output capacitors—which is negligible in the presence of large capacitance—but otherwise contributes additional volt-seconds to the tank inductor during the dead time interval.

Despite these limitations, the nonlinear model is sufficiently accurate to guide component selection and design for mistuning-tolerant SRC-based DCX systems without requiring feedback control.

IV. Approximate Linear Model for Predicting the Required Dead time

To simplify the nonlinear system of equations, the output voltage is assumed to be $V_{\text{out}} = V_{\text{in}}/N$. This assumption holds when circulating currents in the resonant tank are minimized, which naturally occurs when the tuning factor k is close to unity. As k deviates from 1, circulating energy becomes necessary due to the finite tank impedance. However, this energy can be reduced by appropriately designing the ZVS inductors to limit the required shift in tank current—which can introduce asymmetry in the switching cycle—to generate the necessary phase difference during dead time.

In addition, small-angle approximations and linearized transition behaviors are applied where appropriate, enabling the derivation of a simplified set of linear equations that predict the required dead times with good accuracy.

Assuming instantaneous resonant ZVS transitions and ideal DCX operation (i.e., $V_{\text{in}} \approx NV_{\text{out}}$), the minimum dead time required for stable operation can be estimated using the implicit expression

$$\frac{8 \cdot C_{\text{series}} \cdot V_{\text{in,d}} \cdot \sin\left(\frac{\omega(T_{\text{sw}}/2 - t_{d,\min})}{2}\right) \cdot \sin\left(\frac{\omega t_{d,\min}}{2}\right)}{T_{\text{sw}} \cdot \cos\left(\frac{\omega T_{\text{sw}}}{4}\right)} = \frac{I_{\text{out}}}{N}, \tag{21}$$

where $V_{\text{in,d}} = V_{\text{in}} + V_{\text{d,p}} + NV_{\text{d,s}} + \Delta V$, and ΔV loosely models the additional volt-seconds applied to the tank inductor during dead time due to voltage ripple caused by the finite output capacitance. The ripple term is approximated as

$$\Delta V = \frac{NI_{\text{out}}}{16 C_{\text{out}} f_{\text{s}}}, \tag{22}$$

which is a crude estimate used to capture the influence of capacitor ripple—typically difficult to model precisely.

To account for the finite duration of the primary-side ZVS transition, a linear switch node voltage transition is assumed. The total minimum dead time required for stable hard-switched operation therefore includes the time needed to complete only the primary bridge's ZVS. The primary-side ZVS time $t_{\text{ZVS},p}$ is obtained by solving the nonlinear expression

$$\begin{aligned} -2V_{\text{in}} = {} & (-v_o - 2NV_{\text{d,s}}) \cos(\omega_{\text{eq},p} t_{\text{ZVS},p}) \\ & + Z_{\text{eq},p} (i_{\text{ZVS}} - I_{\text{pk},1}) \sin(\omega_{\text{eq},p} t_{\text{ZVS},p}) \\ & + v_o + 2NV_{\text{d,s}} \end{aligned} \tag{23}$$

where, the maximum voltage across the C_{series} is

$$v_o = \frac{I_{\text{out}}}{4kC_{\text{res}} f_{\text{s}} N} \tag{24}$$

and the tank current at the start of the ZVS interval is

$$i_{\text{ZVS}} = -v_o \cdot \frac{\sin\left(\omega\left(\frac{T_{\text{sw}}}{2} - t_{d,\min}\right)\right)}{Z}. \tag{25}$$

This derivation assumes that C_{series} behaves as a constant voltage source during the ZVS interval, i.e., $v_c = -v_o$. Based on a linear ZVS transition for the switch node voltage v_p, the total minimum dead time required for hard-switched operation is

$$t_{d,\text{hard,sw}} = t_{d,\min} + \frac{t_{\text{ZVS},p}}{2}. \tag{26}$$

Applying a small-angle approximation to $t_{d,\min}$ and $t_{\text{ZVS},p}$ yields

$$t_{d,\min} = \frac{I_{\text{out}} L_{\text{leakage}} \pi}{2NV_{\text{in,d}} \tan\left(\frac{\pi}{2\sqrt{k}}\right) \sqrt{k}}. \tag{27}$$

and

$$t_{\text{d,hard,sw}} = \frac{1}{2} \left(\frac{2V_{\text{in}} C_{\text{oss,p}}}{I_{\text{pk},1} + \frac{T_{\text{sw}} I_{\text{out}}}{4NkC_{\text{res}}} \frac{\sin\left(\omega\left(\frac{T_{\text{sw}}}{2} - t_{\text{d,min}}\right)\right)}{Z}} \right) + t_{\text{d,min}} \tag{28}$$

Similarly, the ZVS time for the secondary-side switch-node commutation can be found by solving the following expression for $t_{\text{ZVS},s}$,

$$V_{\text{in}} = (-2V_{\text{in}} - 2NV_{\text{d,s}} - 2V_{\text{d,p}} - v_o)\cos(\omega_{eq,s}t_{\text{ZVS},s}) + V_{\text{in}} + 2V_{\text{d,p}} + v_o. \quad (29)$$

Assuming a linear commutation, the total dead time required for complete soft switching is

$$t_{\text{d,soft,sw}} = t_{\text{d,hard,sw}} + \frac{1}{\omega_{eq,s}e} \cdot \cos^{-1}\left(\frac{v_o + 2V_{\text{d,p}}}{2V_{\text{in,d}} + v_o}\right). \quad (30)$$

where, $t_{\text{d,hard,sw}}$ is given by (28).

It should be noted that the linear model in (28) is derived under the assumptions that $V_{\text{in}} \approx NV_{\text{out}}$ and that the small-angle approximation holds, implying that the required dead time is relatively short—typically less than 10% of $T_{\text{sw}}/2$. The accuracy of the linear model degrades when the dead time exceeds this range. However, the full nonlinear system of equations (Table I) remains valid with minimal assumptions, and the simplified nonlinear models in (21), (26) and (30) also remain applicable over a wider operating range, with slightly higher error primarily due to the $V_{\text{in}} \approx NV_{\text{out}}$ approximation.

V. Experimental Validation of the Developed Models

To validate the developed models, the predicted dead times are compared against measurements obtained from a hardware prototype over a range of input voltages and load currents. The circuit parameters used in the prototype are listed in Table II, and the corresponding power stage components are provided in Table III.

Simulation results (using a switched model in PLECS) and experimental data for $t_{\text{d,hard,sw}}$ and $t_{\text{d,soft,sw}}$ are collected under various input voltages and power levels. This is performed by analyzing dead time waveforms, as illustrated in Fig. 2(b) and Fig. 2(c). The collected hardware data is then used to validate the accuracy of the proposed models.

TABLE II
Circuit Parameters for SRC

Parameter	Value	Parameter	Value
T_{sw}	10 μs	L_{leakage}	8.95 μH
C_{res}	0.28μF	$C_{\text{in}} = C_{\text{out}}$	1.5 μF
C_{series} $(k = 1.6)$	0.453 μF	N	1
$C_{\text{oss},p}$	1451 pF	$C_{\text{oss},s}$	1451 pF
$V_{\text{d},p}$	3 V	$V_{\text{d},s}$	3 V
$L_{\text{zvs},p}$	130 μH	$L_{\text{zvs},s}$	120 μH

The predictions obtained from the non-linear system of equations (Table I) are first compared with simulation results using large filter capacitances. These comparisons yield an error of less than 5%, demonstrating high model accuracy under idealized conditions. When compared with experimental hardware data, the error remains low at lower current levels but increases as currents rise. This discrepancy is primarily attributed to the output capacitor voltage ripple, which is not included in the non-linear formulation. The corresponding results for $t_{\text{d,soft,sw}}$ are shown in Table IV.

TABLE III
Power Stage Components

Component	Part / Value
Primary & Secondary MOSFETs	SiC IMBG120R017M2H
Input/Output Capacitors	R75QR368050H0J
Transformer Core	PQ50/50-3C97
ZVS Inductor Core	PQ32/30-3C97

TABLE IV
Comparison of $t_{\text{D,SOFT,SW}}$ from Non-Linear Model (Table I), Simulation, and Experiment for $k = 1.6$ at 30 V Input

Load Current	**Model (ns)**	**Sim. (ns)**	**Exp. (ns)**
2 A	285	275	260
4 A	496	475	420

The match with hardware measurements improves at higher load currents when using the approximate nonlinear model, given by (21), (23), (28), and (30), incorporates the effect of finite output voltage ripple via (22). This model assumes $V_{\text{in}} \approx NV_{\text{out}}$, with its implications discussed in Section IV. As shown in Table V, the results exhibit better agreement with experimental data, particularly at higher currents.

TABLE V
Comparison of $t_{\text{D,SOFT,SW}}$ from Approximate Non-linear Model (considers output Ripple), Simulation, and Experiment for $k = 1.6$ at 30 V Input

Load Current	**Approx. Model (ns)**	**Sim. (ns)**	**Exp. (ns)**
2 A	280	275	260
4 A	480	475	420

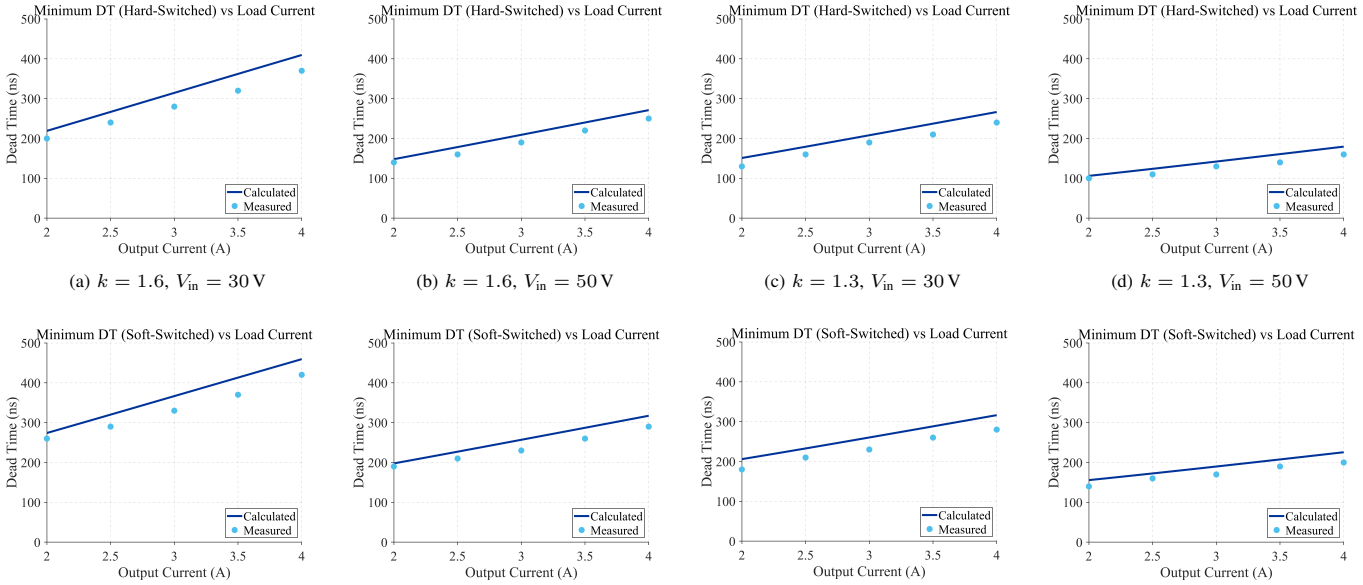
The linearized model—given by (27), (28), and (30)—relies on the most assumptions among the presented models, but it does account for finite output voltage ripple. Model predictions are compared with hardware measurements across a wide range of operating conditions, as shown in Fig. 5(a)–(h). The comparison includes two input voltages (30 V and 50 V), load currents ranging from 2 A to 4 A, and mistuning factors of $k = 1.3$ and $k = 1.6$. Across all data points, the prediction error remains below 15%.

The primary modeling assumptions include $V_{\text{in}} \approx NV_{\text{out}}$ and constant current in the ZVS inductors during the dead time. Additional sources of error stem from the small-angle approximation used to linearize the system.

An interesting trend observed across all models is a consistent overestimation of the dead time. Although the precise cause is unclear, it is likely linked to the coarse treatment of voltage ripple via (22). This aspect presents an opportunity for future refinement of the model.

VI. Conclusion

This paper has demonstrated that a Series Resonant Converter (SRC) with dual active bridges operating under sym-



(a) $k = 1.6$, $V_{\text{in}} = 30\,\text{V}$ (b) $k = 1.6$, $V_{\text{in}} = 50\,\text{V}$ (c) $k = 1.3$, $V_{\text{in}} = 30\,\text{V}$ (d) $k = 1.3$, $V_{\text{in}} = 50\,\text{V}$

(e) $k = 1.6$, $V_{\text{in}} = 30$ V (f) $k = 1.6$, $V_{\text{in}} = 50$ V (g) $k = 1.3$, $V_{\text{in}} = 30$ V (h) $k = 1.3$, $V_{\text{in}} = 50$ V

Fig. 5. Comparison of calculated (based on linear models from Section IV) and measured minimum dead times (hardware) for hard-switched (top row) and soft-switched (bottom row) operation across various load currents, mistuning levels, and input voltages.

metric gate signals functions as an ideal bidirectional DCX. A key insight is the topology exhibits inherent tolerance to resonance mistuning, governed by the presence of dead time. During dead time, a phase shift naturally develops between the primary and secondary switch node voltages, which mitigates the effects of mistuning. However, achieving this benefit requires a minimum dead time, which depends on the mistuning factor ($k \neq 1$) and load conditions. A trade-off of this approach is increased recirculating energy during dead time, which causes a slight deviation in output voltage from the ideal DCX value, especially at higher load currents.

In addition to this behavioral analysis, the paper presents a set of accurate non-linear equations and approximate steady-state models that predict the minimum dead time required for stable and ZVS operation of both bridges. These models have been validated against simulation and experimental results. The full non-linear model is effective for design scenarios with minimal output ripple, maintaining an error of less than 5%. The approximate non-linear and linearized models include output voltage ripple and achieve error margins within 15% across varying operating conditions. Any observed discrepancies are primarily due to the small-angle and linearization assumptions made for tractability. Overall, the modeling framework and validation results provide practical design tools for implementing robust, mistuning-tolerant bidirectional DCX systems across a range of applications.

REFERENCES

[1] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kv sic-based 7 kv/400 v dc transformer for future data centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, 2019.

[2] S. Lim, A. J. Hanson, J. A. Santiago-González, and D. J. Perreault, "Bus converter using isolation capacitance for zvs and invariant operation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 1971–1982, 2020.

[3] B. Majmunović, S. Mukherjee, T. Martin, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson, and D. Maksimović, "1 kv, 10-kw sic-based quadruple active bridge dcx stage in a dc to three-phase ac module for medium-voltage grid integration," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14 631–14 646, 2022.

[4] S. Poddar and R. Zane, "Dynamic modeling of the resonant series-bridge dcx converter," in *2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2025.

[5] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimović, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 5774–5781.

[6] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3931–3940, 2013.

[7] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri, and P. Stefanutti, "Power electronic traction transformer—medium voltage prototype," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257–3268, 2014.

[8] J. E. Huber, J. Miniböck, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle dcm series resonant converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 4–7, 2018.

[9] T. Guillod, D. Rothmund, and J. W. Kolar, "Active magnetizing current splitting zvs modulation of a 7 kv/400 v dc transformer," *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1293–1305, 2020.

[10] Y. Yin, M. Shirazi, and R. Zane, "Electronic ballast control ic with digital phase control and lamp current regulation," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 11–18, 2008.

[11] S. Jiang, W. Zhang, B. Liu, and F. Wang, "Automatic resonant frequency tracking in unregulated llc resonant converters based on total resonant current harmonic calculation," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 4193–4198.

[12] W. Feng, P. Mattavelli, and F. C. Lee, "Pulsewidth locked loop (pwll) for automatic resonant frequency tracking in llc dc–dc transformer (llc -dcx)," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1862–1869, 2013.

CHAPTER 6

Dynamic Modeling of the Series Bridge-DCX Topology

The SB-DCX topology, used for the implementation of the DCX stage (see Chapter 4) within the proposed architecture, has recently been investigated for DCX operation. However, a convenient and scalable dynamic model has not yet been developed. This work presents an LTI dynamic model for the SB-DCX topology using a half-cycle averaging technique. The model enables the SB-DCX to be designed with an appropriate minimum settling time when operated with an unfolder, and it can also be used to assess the stability of the DCX stage.

An LTI dynamic model for the SB-DCX is essential for properly designing the DCX stage and evaluating its closed-loop stability. Switched converters such as the SB-DCX require high-level LTI models that abstract away the switching behavior, facilitating the application of well-established frequency-domain techniques to analyze their dynamic performance. Such models support the design of converters with dynamic responses tailored to specific application requirements. Additionally, for assessing overall system stability in configurations where the SB-DCX is integrated with other power converters, a dynamic model becomes indispensable.

This chapter develops an LTI dynamic model for the SB-DCX topology using a half-cycle averaging approach. The resulting large-signal LTI model features a straightforward circuit representation and is readily scalable. The complete mathematical derivation and analytical steps are detailed herein. This work has been submitted as a journal publication. Furthermore, the model can also be constructed by tracking the energy flow through the converter, as presented in the related conference publication at IEEE COMPEL 2025 [42].

Half-cycle Averaged Dynamic Model for Resonant Series-Bridge DCX Converter using Time Domain Analysis

Sanat Poddar, *Student Member, IEEE,* Regan Zane, *Fellow, IEEE*

***Abstract*—A DC transformer (DCX) is a dc-dc converter that operates at a fixed voltage conversion ratio and provides galvanic isolation. This fixed-ratio operation enables system-level advantages such as improved efficiency and simplified control. The resonant Series-Bridge DCX (SB-DCX) topology has recently gained attention due to its natural ability to achieve DCX operation without active regulation. However, a scalable and time-invariant dynamic model for this topology is lacking. This paper presents a complete time-domain derivation of a linear time-invariant (LTI) dynamic model for the SB-DCX using a half-cycle averaging approach. The derivation includes step-by-step analysis and outlines the necessary assumptions for obtaining a valid model. The resulting circuit-based representation captures both steady-state and large-signal dynamic behavior while suppressing switching-level details. Simulation results show strong agreement between the predicted and observed dynamics using a switched model. Additionally, experimental validation is performed using a 500 W hardware prototype at 50 V output, with results shown for a 50% load transient. The model accurately predicts the average output voltage and the envelope of the tank current, demonstrating its practical relevance for system-level design and analysis.**

***Index Terms*—Dynamic Modeling, DCX, half-cycle averaging, time-domain, series-bridge, SB-DCX, series-resonance, resonance, local-averaging**

I. Introduction

Fixed voltage conversion ratio dc-dc converters with galvanic isolation are commonly referred to as DC transformers (DCX). They are widely employed in applications such as data center power delivery, battery charging, and renewable energy systems [1]–[5]. By operating at a fixed conversion ratio, these converters simplify control strategies and achieve high efficiency under nominal operating conditions. In addition to providing galvanic isolation, they offer architectural advantages in modular and cascaded converter systems, particularly in scenarios where intermediate voltage regulation is unnecessary [3].

Among various DCX topologies, the Series-Bridge DCX (SB-DCX) has recently gained attention due to its inherent ability to maintain resonant operation without the need for precise tuning [6]–[8]. As illustrated in Fig. 1(a), the SB-DCX replaces the conventional series capacitor in the resonant tank with an active bridge. This configuration allows the converter to automatically self-adjust to resonance, enabling symmetric gating of both the primary and secondary bridges and naturally enforcing DCX behavior. Consequently, the SB-DCX topology offers robustness against component variations and scalability for use in modular power systems.

To enable system-level design and control of power conversion architectures, an accurate dynamic model of the converter is essential. While the SB-DCX exhibits DCX behavior under steady-state conditions, capturing its transient response, particularly during events such as load steps, start-up, or fault recovery, is critical for design and performance assessment [9]. This requires a dynamic model that accurately reflects its time-domain behavior.

Due to the inherent switching action in power converters such as the SB-DCX, the system exhibits time-varying behavior. Consequently, numerical techniques based on piecewise linear modeling are commonly employed through computational tools to analyze their dynamic performance [10]. While these methods can accurately capture both transient and steady-state behavior, they are often computationally intensive and lack the analytical tractability needed for control design and system-level integration.

In this context, linear time-invariant (LTI) models are especially valuable. They support the application of classical control methodologies, including transfer function analysis, loop-shaping, and stability evaluation within interconnected converter systems [11], [12].

Deriving time-invariant models from switching converters involves reducing the system's informational complexity by eliminating explicit switching behavior. This is achieved through various techniques such as state averaging, harmonic analysis, or discrete-time sampling [13], [14]. These approaches aim to abstract essential dynamic characteristics while suppressing the fast-scale switching details, yielding a simplified model that retains the dominant system dynamics.

However, developing accurate dynamic models for the SB-DCX poses significant challenges. Traditional modeling techniques such as state-space averaging [15], [16] and phasor-domain analysis [17], [18] are not well-suited to this topology. As illustrated in Fig. 1(b), the SB-DCX exhibits half-cycle anti-symmetry and highly non-sinusoidal waveforms within its resonant tank. Notably, the tank current lacks a dc component, rendering conventional state-space averaging inapplicable. Moreover, the topology relies heavily on higher-order harmonics to sustain resonance. As a result, phasor-domain techniques—typically used for resonant converters by modeling only the fundamental component—fail to capture the essential harmonic interactions governing SB-DCX operation. These characteristics undermine the assumptions inherent in conventional modeling techniques, necessitating alternative approaches tailored to the unique operating principles of the

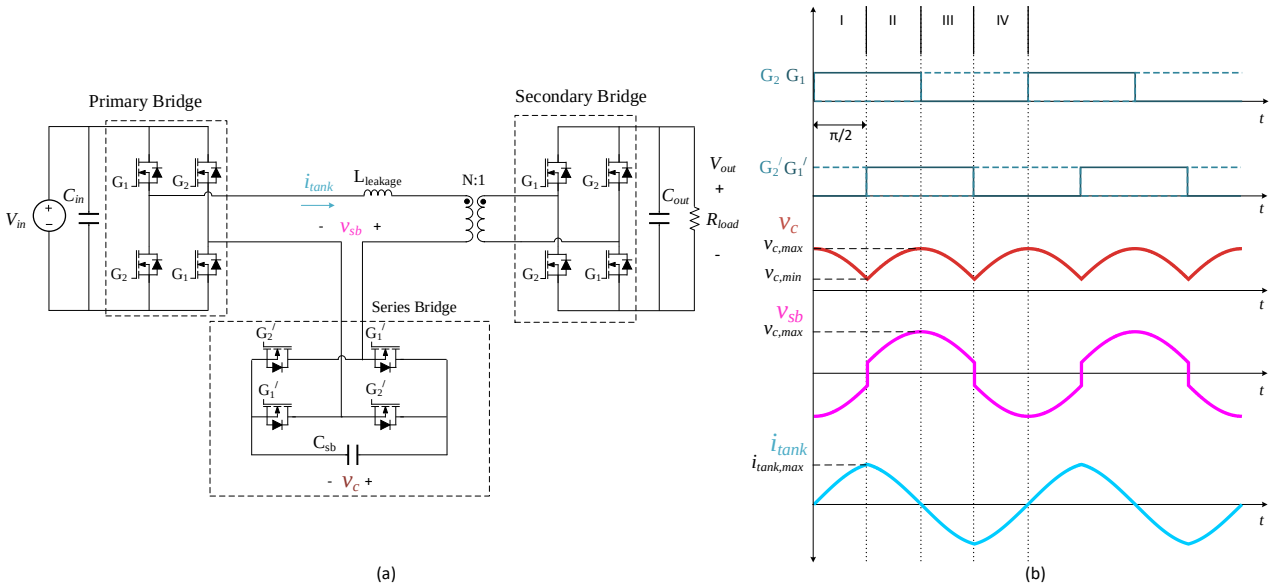


Fig. 1. (a) The SB-DCX topology: a series bridge that emulates a variable capacitance, enabling perfect resonance operation while allowing for higher tolerance to variations in capacitance. (b) The ideal symmetric gating signals of the primary and secondary bridges are shown, with the SB phase shifted by 90 degrees to allow for resistive tank currents. The corresponding tank waveforms for ideal steady-state operation are depicted.

SB-DCX.

While generalized state-space averaging (GSSA) [19] is mathematically feasible, it often obscures circuit-level insight and presents challenges in terms of scalability and physical interpretability. Furthermore, in the SB-DCX topology, the dominant harmonics that influence dynamic behavior are strongly dependent on the degree of mistuning. As mistuning increases, higher-frequency harmonic content becomes more pronounced, further complicating the modeling process and diminishing the effectiveness of GSSA. For similar reasons, the extended describing function (EDF) method, which has previously been applied to model resonant converters [20], is also inadequate for capturing the essential dynamics of the SB-DCX.

Similarly, discrete-time modeling techniques [21], [22], while theoretically applicable, become computationally intensive as the number of state variables to be tracked increases—particularly in the case of the SB-DCX. Moreover, these methods tend to obscure circuit-level intuition, making it difficult to gain physical insight into the converter's behavior.

Recently, half-cycle averaging has been successfully explored to develop a linear time-invariant (LTI) dynamic model of the SB-DCX topology [8]. Half-cycle averaging is a technique that averages the state variables over each half-switching cycle [23]. Unlike traditional state-space averaging [15], which fails in cases where the tank current lacks a dc component, half-cycle averaging preserves essential harmonic behavior while eliminating high-frequency switching ripple. This enables the derivation of a time-invariant model that captures the dominant large-signal dynamics of the resonant tank.

However, the modeling approach in [8] relied on a heuristic, energy-based formulation similar to that used in [24], [25]. While effective, this method does not fully reflect the underlying half-cycle averaging process or explicitly state its assumptions and limitations.

This article builds upon the work presented in [8] by deriving the half-cycle averaged model directly from time-domain analysis based on first principles. The model is developed by systematically tracking the relevant tank state variables across all switching intervals and formulating their evolution as a function of the converter's terminal parameters. These dynamics are subsequently consolidated into a passive, circuit-based representation that is both intuitive and scalable. All underlying assumptions are explicitly stated, and their implications are carefully examined. In addition to the mathematical formulation, a physical interpretation is provided, establishing a clear correspondence between model parameters and measurable waveform features—thereby enabling parameter identification from both simulation and experimental data. Furthermore, the exact time-domain methodology introduced here can be generalized to derive half-cycle averaged models for other resonant converter topologies.

To summarize, this paper extends the preliminary work presented by the authors in [8], with the following additional contributions:

- A complete and rigorous time-domain derivation of the half-cycle averaged model based on first principles.
- Explicit articulation of modeling assumptions and a discussion of their implications, along with a physical interpretation of the time-domain formulation and the resulting circuit-based model.
- Additional hardware results across a wider span of voltages and power levels to further substantiate the model's accuracy.

Section II provides details about the SB-DCX topology, the switching pattern, and the working principle that naturally

leads to DCX characteristics and precise resonance operation. Section III presents the detailed mathematical analysis, which employs half-cycle averaging to consolidate the time-domain information of the state variables and derive an LTI dynamic model under certain assumptions. The resulting mathematical formulation, its projection to the circuit model shown in Fig. 7, and its physical interpretation are discussed in Section IV. Section V verifies the developed model for different cases using PLECS simulations based on the complete switched model. Further, Section V presents experimental validation with prototype hardware, demonstrating good agreement with the developed model across various operating conditions, including peak power operation at 500 W and 50 V output (unity gain converter).

II. Operation and Working Principle of the SB-DCX topology

The SB-DCX topology replaces the series capacitor in conventional series-resonant converters with an active series bridge (SB), similar in concept to reactive compensators used in AC transmission systems [6]. The primary advantage of the SB is that it enables precise resonant operation even in the presence of tuning mismatches, thereby supporting ideal resonant DCX behavior. Such ideal resonant DCX operation has many practical applications, including transformer-level paralleling in modular converter architectures [7].

The gate control signals for all switches are shown in Fig. 1(b). The primary and secondary H-bridges use identical gate signals (G_1 and G_2) for their symmetric switches; hence, the term "symmetric gating." The gating of the SB determines the phase of the tank current relative to the switch-node voltages. To achieve a resistive tank current—desirable for zero-current switching (ZCS)—the SB is phase-lagged by 90° relative to the primary and secondary bridges. Ignoring dead time, the switching cycle consists of four distinct switch-state combinations (I–IV), as shown in Fig. 1(b).

The combination of the SB and symmetric gating forces the topology to always operate at resonance, thereby exhibiting DCX behavior. Under symmetric gating, a constant output voltage is maintained only if the reactive impedance of the tank is zero. Any nonzero tank reactance would inhibit real power transfer by blocking current flow, violating the assumption of a constant output voltage. The SB ensures zero tank impedance by enabling precise resonant operation. It effectively emulates a variable capacitance that adjusts naturally to compensate for any tank inductance. This capability makes the topology robust to mistuning caused by component tolerances or variations in tank parameters due to aging. As a result, the tank's reactive impedance is regulated to zero, and the output voltage is determined solely by the input voltage and the transformer turns ratio:

$$V_{\text{out}} = \frac{V_{\text{in}}}{N}, \tag{1}$$

where N is the transformer turns ratio, realizing ideal DCX operation in steady state.

The SB emulates this variable capacitance by allowing a dc bias ($V_{c,\text{min}}$) to develop across the SB capacitor (C_{sb}). The extent of this dc bias increases with mistuning, enabling the SB to compensate precisely for the tank inductance L_{leakage} and maintain precise resonant operation.

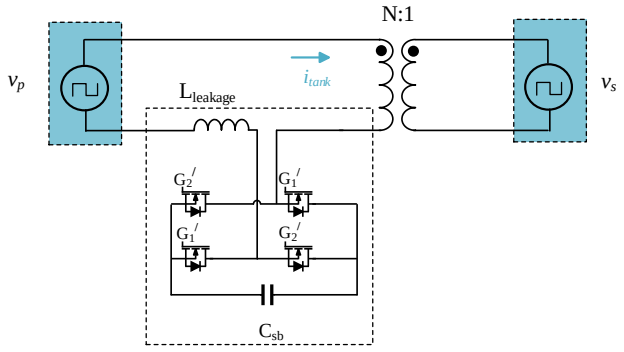


Fig. 2. The primary and the secondary H-bridges have symmetric gate signals and hence, the pushing force on the resonant tank can be modeled as +/- Δv depending on the switching state of the H-bridges

III. Half-Cycle Averaged Model Using Time-Domain Analysis

To develop the dynamic model using half-cycle averaging, time-domain equations are first used to track the relevant state variables from the beginning to the end of each half-cycle. These state variables are then averaged over the half-cycle, resulting in discrete-time updates of their averaged values. By assuming that the converter's dynamics evolve on a timescale much slower than the switching period, these discrete updates can be approximated by a continuous-time representation.

Half-cycle averaging eliminates high-frequency switching dynamics while preserving the dominant large-signal behavior of the system, resulting in a time-invariant model. For the SB-DCX converter, the key state variables—namely, the tank current (i_{tank}) and the series-bridge capacitor voltage (v_{c})—are tracked using time-domain equations across different switching states during transients.

To monitor the evolution of the tank state variables during a transient, the SB-DCX is simplified to an equivalent circuit, as shown in Fig. 2. Any deviation in the input and/or output voltage from the steady-state operating point (defined by (1)) results in a net *pushing force* on the resonant tank—comprising the series bridge (SB) and the leakage inductance—as illustrated in Fig. 2. The goal is to express the tank state variables as functions of this voltage disturbance. This pushing force is modeled as a voltage deviation, denoted by Δv, defined as

$$\Delta v = V_{\text{in}} - N V_{\text{out}}, \tag{2}$$

where N is the transformer turns ratio. This voltage deviation Δv quantifies the departure from the ideal input-output voltage relationship inherent to DCX operation.

To obtain the converter's dynamic behavior, the circuit is solved over each subinterval of the switching cycle, with particular attention to the tank current. This current is then averaged over the half-cycle interval $T_{\text{sw}}/2$, as illustrated in

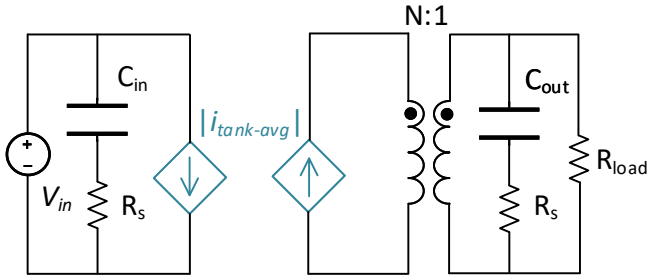


Fig. 3. The SB-DCX can be modeled as shown. The current source represents the magnitude of the half-cycle averaged tank current. This model suppresses the switching information of the tank currents to simplify the analysis.

Fig. 4(a). The resulting half-cycle averaged tank current is significant, as its magnitude reflects the net energy transferred during each half-cycle. Consequently, it serves as a key quantity in modeling the converter's input characteristics. When appropriately scaled by the transformer turns ratio, this current also characterizes the output behavior, as represented in the simplified behavioral model shown in Fig. 3. To facilitate dynamic analysis, a continuous-time approximation of the half-cycle averaged current, denoted $|i_{\text{tank,avg}}|$, is constructed by interpolating the discrete-time values across successive half-cycles.

The discrete half-cycle averaged tank current is computed based on the capacitor voltage v_c at the beginning and end of each switching state defined by the SB-DCX switching cycle (as illustrated in Fig. 1(b)). Specifically, the magnitude of the half-cycle averaged tank current during the n^{th} cycle is

$$|i_{\text{tank-avg},n}| = 2C_{\text{sb}} f_{\text{sw}} \left(|v_{2n}| + |v_{2n-2}| - 2|v_{2n-1}|\right) \tag{3}$$

where $|v_{2n}|$, $|v_{2n-2}|$, and $|v_{2n-1}|$ represent the absolute values of the capacitor voltage across C_{sb}, sampled at the corresponding switching instants, as indicated in Fig. 4(a). Here, n denotes the index of the half-cycle.

To find the general expressions for v_{2n}, v_{2n-2}, and v_{2n-1}, the capacitor voltage v_c at the end of each switch state combination (I–IV) is determined using the time-domain equations derived from the equivalent circuits shown in Fig. 4(b). These capacitor voltages are denoted as v_0 to v_6, while the tank currents at the end of each unique switching state are denoted as i_0 to i_5. These voltages and currents are then used to obtain the general expressions for v_{2n} and v_{2n-1}. The time-domain solution equations assuming an underdamped resonant tank are

$$v_1 = (v_o - \Delta v)k \cdot e^{-x} + \Delta v \tag{4}$$
$$i_1 = -(v_o - \Delta v) \cdot e^{-x} \cdot \frac{\sin a}{Z_L} \tag{5}$$
$$v_2 = \Delta v + e^{-x}\left[(-v_1 - \Delta v)k + i_1 Z_C \sin a\right] \tag{6}$$
$$i_2 = e^{-x}\left[i_1 \cos a - \left(\frac{-v_1 - \Delta v}{Z_L} + \frac{\alpha i_1}{\omega_d}\right)\sin a\right] \tag{7}$$
$$v_3 = -\Delta v + e^{-x}\left[(v_2 + \Delta v)k + i_2 Z_C \sin a\right] \tag{8}$$
$$i_3 = e^{-x}\left[i_2 \cos a - \left(\frac{v_2 + \Delta v}{Z_L} + \frac{\alpha i_2}{\omega_d}\right)\sin a\right] \tag{9}$$
$$v_4 = -\Delta v + e^{-x}\left[(-v_3 + \Delta v)k + i_3 Z_C \sin a\right] \tag{10}$$
$$i_4 = e^{-x}\left[i_3 \cos a - \left(\frac{-v_3 + \Delta v}{Z_L} + \frac{\alpha i_3}{\omega_d}\right)\sin a\right] \tag{11}$$
$$v_5 = \Delta v + e^{-x}\left[(v_4 - \Delta v)k + i_4 Z_C \sin a\right] \tag{12}$$
$$i_5 = e^{-x}\left[i_4 \cos a - \left(\frac{v_4 - \Delta v}{Z_L} + \frac{\alpha i_1}{\omega_d}\right)\sin a\right] \tag{13}$$
$$v_6 = \Delta v + e^{-x}\left[(-v_5 - \Delta v)k + i_5 Z_C \sin a\right] \tag{14}$$

where

$$x = \frac{\alpha\pi}{2\omega_{\text{sw}}}, \quad r = \frac{\omega_{\text{sw}}}{\omega_d}, \quad a = \frac{\pi}{2r},$$
$$\omega_d = \sqrt{\omega_r^2 - \alpha^2}, \quad \omega_r = \frac{1}{\sqrt{C_{\text{sb}} L_{\text{leakage}}}}, Z_L = L_{\text{leakage}}\omega_d$$
$$\alpha = \frac{R_p}{2L_{\text{leakage}}}, \quad Z_C = \frac{1}{C_{\text{sb}}\omega_d}, \quad k = \cos a + \frac{\alpha}{\omega_d}\sin a, \tag{15}$$

and v_o is the initial voltage across C_{sb}, R_p is the parasitic series resistance modeling the total series resistive losses in the tank (assuming ideal switches), and ω_{sw} is the switching angular frequency.

To simplify the analysis the tank current at the start of the half-cycle is approximated as

$$i_{2n} \approx 0. \tag{16}$$

This assumption does not majorly impact the half-cycle averaged value of the tank current, as i_{2n} remains close to zero throughout the switching cycle, as observed in Fig. 4. Furthermore, when the tank quality factor is high, it is reasonable to assume that $Z_L \approx Z_C$.

Using equations (4)–(14), the expressions for $|v_1|$, $|v_3|$, and $|v_5|$ are

$$|v_1| = -(v_0 - \Delta v)\, k\, e^{-x} - \Delta v, \tag{17}$$
$$|v_3| = -(v_0 - \Delta v)\, k(k^2 + \sin^2 a)\, e^{-3x} + 2\Delta v\, k\, e^{-x} - 2\Delta v\, k^2\, e^{-2x} - \Delta v, \tag{18}$$
$$|v_5| = -(v_0 - \Delta v)\, k(k^2 + \sin^2 a)^2\, e^{-5x} + 2\Delta v\, k\, e^{-x} - 2\Delta v\, k^2\, e^{-2x} + 2\Delta v\, k(k^2 + \sin^2 a)\, e^{-3x} - 2\Delta v\, k^2(k^2 + \sin^2 a)\, e^{-4x} - \Delta v. \tag{19}$$

Similarly,

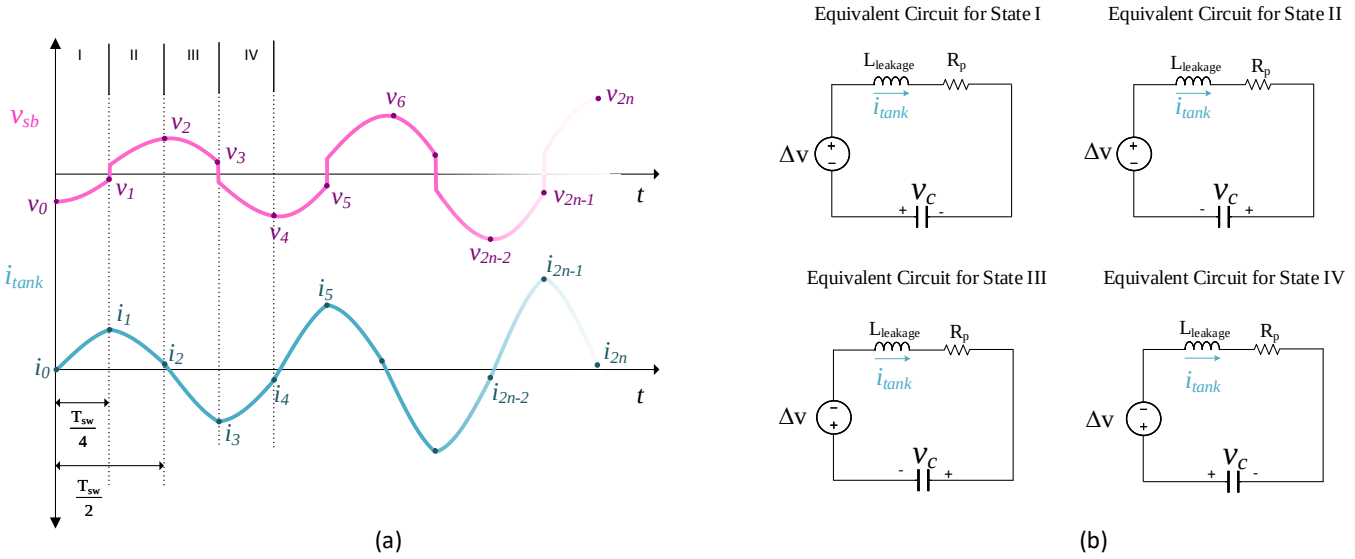


Fig. 4. (a) Representative evolution of the state variables during a dynamic event, such as a load transient. (b) Equivalent circuits of the SB-DCX topology for the four different switching state combinations, used to obtain time-domain information about the state variables at the necessary sampling instants.

$$|v_2| = -(v_0 - \Delta v)(k^2 + \sin^2 a)\, e^{-2x} - 2\Delta v\, k\, e^{-x} + \Delta v, \tag{20}$$

$$\begin{aligned} |v_4| = &-(v_0 - \Delta v)(k^2 + \sin^2 a)^2\, e^{-4x} \\ &- 2\Delta v\, k\, e^{-x} + 2\Delta v(k^2 + \sin^2 a)\, e^{-2x} \\ &- 2\Delta v\, k(k^2 + \sin^2 a)\, e^{-3x} + \Delta v, \end{aligned} \tag{21}$$

$$\begin{aligned} |v_6| = &-(v_0 - \Delta v)(k^2 + \sin^2 a)^3\, e^{-6x} \\ &- 2\Delta v\, k\, e^{-x} + 2\Delta v(k^2 + \sin^2 a)\, e^{-2x} \\ &- 2\Delta v\, k(k^2 + \sin^2 a)\, e^{-3x} + 2\Delta v(k^2 + \sin^2 a)^2\, e^{-4x} \\ &- 2\Delta v\, k(k^2 + \sin^2 a)^2\, e^{-5x} + \Delta v. \end{aligned} \tag{22}$$

The general expression for $|v_{2n-1}|$, based on equations (17)–(19) is

$$\begin{aligned} |v_{2n-1}| = &-(v_0 - \Delta v)\, k\, (k^2 + \sin^2 a)^{n-1} e^{-(2n-1)x} \\ &+ 2\Delta v \sum_{i=1}^{n-1} \left[k(k^2 + \sin^2 a)^{i-1} e^{-x(2i-1)} \right] \\ &- 2\Delta v \sum_{i=1}^{n-1} \left[k^2 (k^2 + \sin^2 a)^{i-1} e^{-2ix} \right] \\ &- \Delta v. \end{aligned} \tag{23}$$

Similarly, the general expression for $|v_{2n|}$, based on equations (20)–(22) is

$$\begin{aligned} |v_{2n}| = &-(v_0 - \Delta v)\, (k^2 + \sin^2 a)^n\, e^{-2nx} \\ &+ 2\Delta v \sum_{i=1}^{n-1} (k^2 + \sin^2 a)^i\, e^{-2ix} \\ &- 2\Delta v\, k \sum_{i=1}^{n} (k^2 + \sin^2 a)^{i-1}\, e^{-(2i-1)x} \\ &+ \Delta v. \end{aligned} \tag{24}$$

Equations (23) and (24) can be further simplified under the condition that $|\theta e^{-2x}| < 1$, where $\theta = k^2 + \sin^2 a$. This corresponds to the tank's series resonance damping factor $\alpha > 0$, a condition that is always physically satisfied.

$$\begin{aligned} |v_{2n-1}| = &-(v_0 - \Delta v)\, k\, \theta^{n-1} e^{-x(2n-1)} \\ &- 2\Delta v\, k^2 \cdot \frac{e^{-2x}(1 - (\theta e^{-2x})^{n-1})}{1 - \theta e^{-2x}} \\ &+ 2\Delta v\, k \cdot \frac{e^{-x}(1 - (\theta e^{-2x})^{n-1})}{1 - \theta e^{-2x}} \\ &- \Delta v, \end{aligned} \tag{25}$$

$$\begin{aligned} |v_{2n}| = &-(v_0 - \Delta v)\, \theta^n\, e^{-2nx} \\ &+ 2\Delta v\, \theta \cdot \frac{e^{-2x}\left(1 - (\theta e^{-2x})^{n-1}\right)}{1 - \theta e^{-2x}} \\ &- 2\Delta v\, k \cdot \frac{e^{-x}\left(1 - (\theta e^{-2x})^{n}\right)}{1 - \theta e^{-2x}} \\ &+ \Delta v, \end{aligned} \tag{26}$$

Using the expression for $|i_{\text{tank-avg},n}|$ given in (3), and substituting the closed-form expressions from (25)–(26), the detailed result shown in (27) is obtained, as presented in Table I. While analytically complete, the expression in (27) is too complex for practical interpretation and requires further simplification.

To this end, a first-order Taylor series approximation is applied to e^x and θ under the assumption that $\alpha \ll 1$. Physically, this corresponds to a low parasitic resistance or, equivalently, a high tank quality factor, which is a valid assumption for well-designed resonant converters. Under this condition, the parameter θ can be approximated as

$$\theta \approx 1 + \frac{2\alpha}{\omega_d} \sin a \cos a. \tag{29}$$

Consequently the term θ^n is approximated using the exponential expansion

$$\theta^n \approx e^{n(\theta-1)} = e^{n\frac{2\alpha}{\omega_d}\sin a\cos a}. \tag{30}$$

The exponential functions simplify to

$$e^x \approx 1 + x. \tag{31}$$

These approximations lead directly to the compact form presented in (28).

Furthermore, the sampled form of the expression can be converted into a continuous-time representation by approximating the cycle index n as

$$n \approx \frac{\omega_{\text{sw}} t}{\pi}, \tag{32}$$

based on the assumption that the half-cycle averaged tank current evolves much more slowly than the switching frequency. This condition generally holds for most practical converter designs. The resulting continuous-time expression

$$\begin{aligned}|i_{\text{tank-avg}}(t)| = {} & \frac{-2C_{\text{sb}}v_{\text{o}}}{T_{\text{sw}}}\cdot e^{-\lambda t}\left(1 + e^{\frac{\alpha\pi}{\omega_{\text{sw}}}} - 2\cos a\cdot e^{\frac{\alpha\pi}{2\omega_{\text{sw}}}}\right) \\ & + \frac{2\omega_{\text{d}}^2\Delta v}{\omega_{\text{r}}^2\, a\,(a-\cos a\,\sin a)}(1-\cos a)^2 \\ & - \frac{2\omega_{\text{d}}^2\Delta v}{\omega_{\text{r}}^2\, a\,(a-\cos a\,\sin a)}(1-\cos a)^2\cdot e^{-\lambda t}\end{aligned} \tag{33}$$

where

$$\lambda = \alpha\cdot\frac{a-\sin a\cos a}{a}. \tag{34}$$

This expression has a clear physical interpretation and serves as the foundation for the equivalent circuit model presented in Fig. 7.

The quantity $i_{\text{tank-avg-0}}$ denotes the half-cycle averaged tank current prior to the transient event and is given as

$$i_{\text{tank-avg,0}} = -2C_{\text{sb}}v_{\text{o}}f_{\text{sw}}\cdot\left(1+\theta^{-1}e^{\frac{\alpha\pi}{\omega_{\text{sw}}}} - 2k\theta^{-1}\cdot e^{\frac{\alpha\pi}{2\omega_{\text{sw}}}}\right). \tag{35}$$

Using (33) and (35)

$$\begin{aligned}|i_{\text{tank-avg}}|(t) = {} & i_{\text{tank-avg,0}}\cdot e^{-\lambda t} \\ & + \frac{2\omega_{\text{d}}^2\Delta v(1-\cos a)^2}{\omega_{\text{r}}^2 a(a-\cos a\,\sin a)}(1-e^{-\lambda t}).\end{aligned} \tag{36}$$

This expression represents a first-order response for the magnitude of half-cycle averaged tank current under a voltage excitation of Δv and can be represented as

$$\begin{aligned}|i_{\text{tank-avg}}(t)| = {} & i_{\text{tank-avg,0}}\cdot e^{-\frac{R_{\text{eq}}}{L_{\text{eq}}}t} \\ & + \frac{\Delta v}{R_{\text{eq}}}\left(1-e^{-\frac{R_{\text{eq}}}{L_{\text{eq}}}t}\right),\end{aligned} \tag{37}$$

where

$$\begin{aligned}R_{\text{eq}} &= (a-\cos(a)\sin(a))\cdot\frac{a}{2(1-\cos(a))^2}\cdot R_{\text{p}}, \\ L_{\text{eq}} &= \frac{a^2}{(1-\cos(a))^2}\cdot L_{\text{leakage}}.\end{aligned} \tag{38}$$

This behavior can be equivalently represented by the circuit model shown in Fig. 6(a). The circuit effectively captures the dynamic evolution of the magnitude of the half-cycle averaged tank current in the SB-DCX converter. The continuous-time model is valid under the assumption that the system dynamics are much slower than the switching frequency and that the tank has a high quality factor.

Figure 5 compares the discrete-time model and its continuous-time approximation for the case of $\Delta v = 0.05$, using SB-DCX circuit parameters identical to those employed in the hardware experiments presented in Section V. The results confirm that the continuous-time model provides a good approximation of the sampled-average model for a practical

TABLE I
DETAILED AND SIMPLIFIED EXPRESSIONS FOR $|i_{\text{TANK-AVG},n}|$.

Full detailed expression without approximations	$\begin{aligned}\left\|i_{\text{tank-avg},n}\right\| = 2\,C_{\text{sb}}\,f_{\text{sw}}\Bigg\{ & -\,v_0\,\theta^n e^{-2nx}\left(1+\theta^{-1}e^{2x}-2k\,\theta^{-1}e^{x}\right) \\ & + \frac{4\,\Delta v\left(1-ke^{-x}\right)^2}{1-\theta e^{-2x}} \\ & + \frac{\Delta v\,\theta^n e^{-2nx}\left(-\theta^{-1}e^{2x}-\theta e^{-2x}-2+k\left(4\theta^{-1}e^{x}+4e^{-x}\right)-4k^2\theta^{-1}\right)}{1-\theta e^{-2x}}\Bigg\}\end{aligned}$	(27)
Simplified expression using first-order taylor approximation assuming $\alpha \ll 1$	$\begin{aligned}\left\|i_{\text{tank-avg},n}\right\| = 2C_{\text{sb}}f_{\text{sw}}\Bigg\{ & -v_0\,e^{\theta-1}e^{-2nx}\left(1+\theta^{-1}e^{2x}-2k\theta^{-1}e^{x}\right) \\ & + \frac{4\Delta v\,(1-\cos a)^2}{1-\theta e^{-2x}} \\ & - \frac{\Delta v\,e^{n(\theta-1)}e^{-2nx}}{1-\theta e^{-2x}}\left[4(1-\cos a)^2\right]\Bigg\}\end{aligned}$	(28)

converter implementation. It accurately captures the tank current dynamics while inherently filtering out high-frequency switching components. However, the approximation begins to break down when the output filter capacitance is very small, causing the system dynamics to shift closer to the switching frequency.

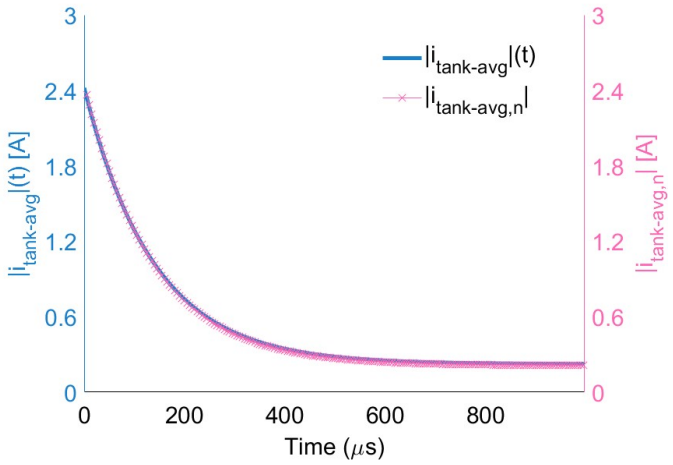


Fig. 5. Comparison between the discrete-time model and its continuous-time approximation for the half-cycle averaged tank current, with $\Delta v = 0.05$ and SB-DCX circuit parameters as given in Section V.

IV. Circuit Model and its Interpretation

Based on the expression derived for the half-cycle averaged tank current in (36) in Section III, a complete terminal circuit model (Fig. 7) that captures both the steady-state and dynamic behavior of the SB-DCX is developed. Furthermore, the physical interpretation of the model is presented, highlighting its connection to the SB-DCX circuit parameters and corresponding operational waveforms. This interpretation enables the extraction of terminal model parameters directly from simulation waveforms, thereby significantly enhancing the practical utility of the model.

A. Resulting terminal circuit model

The circuit shown in Fig. 6(a) represents the dynamics of the half-cycle averaged tank current in response to a voltage disturbance modeled as Δv given by (36), where Δv is defined in (2). This half-cycle averaged tank current can, in turn, be used to drive a current source that captures the time-varying behavior of the SB-DCX shown in Fig. 6(b). Fig. 6(b) is an extension of Fig. 3. The two equivalent circuit representations (Fig. 6(a) and (b)) can be combined to obtain a complete circuit model shown in Fig. 6(c), which accurately captures the dynamic behavior of SB-DCX.

To incorporate the steady-state behavior accurately, R_1 is introduced following the approach in [25], [26], where

$$R_1 = (\beta^2 - 1)(R_s + N^2 R_s) \tag{39}$$

models the losses in the input and output capacitors, C_{in} and C_{out} due to losses in ESR of filter capacitors due to high-frequency currents. R_s is the ESR of the filter capacitors. The parameter β is defined as

$$\beta^2 = \frac{1}{2} \cdot (a - \cos(a)\sin(a)) \cdot \frac{a}{(1-\cos(a))^2}, \tag{40}$$

where $a = \frac{\pi}{2r}$ and $r = \omega_{\text{sw}}/\omega_{\text{d}}$.

To further account for complete resistive losses, the total equivalent resistance $R_{\text{eq,total}}$ is given as

$$R_{\text{eq,total}} = R_p \cdot \beta^2 + R_1 \tag{41}$$

This results in a complete terminal model, shown in Fig. 7, that captures both the dynamic and steady-state behavior of the SB-DCX converter. The model is a large-signal representation that eliminates the explicit time-varying nature of the circuit by assuming that the system dynamics evolve much slower than the switching frequency, and by assuming the tank has a high quality factor.

The model accurately predicts both the output voltage and the magnitude of the half-cycle averaged tank current, denoted as i_{m}. The envelope of the instantaneous tank current, $i_{\text{tank,env}}$, can be extracted from i_{m} using

$$i_{\text{tank,env}} = i_{\text{m}} \cdot \gamma, \qquad \gamma = \frac{a}{(1-\cos(a))} \cdot \sin(a). \tag{42}$$

The model has been validated by both simulation and hardware results in Section V.

B. Physical interpretation

The complete circuit model can also be derived by tracking energy flow through the converter. The equivalent inductance, L_{eq}, can be divided as

$$L_{\text{eq}} = L_{\text{sb}} + L_{\text{dc}}, \tag{43}$$

where

$$\begin{aligned} L_{\text{sb}} &= L_{\text{leakage}} \left(\frac{a\cos a}{1-\cos a} \right)^2 = C_{\text{sb}} \cdot \delta^2 \\ &= C_{\text{sb}} \left(\frac{\cos a}{(1-\cos a) \cdot 4 f_{\text{sw}} C_{\text{sb}}} \right)^2, \end{aligned} \tag{44}$$

and

$$L_{\text{dc}} = L_{\text{leakage}} \left(\frac{a\sin a}{1-\cos a} \right)^2 = L_{\text{leakage}} \cdot \gamma^2. \tag{45}$$

Here L_{dc} models the peak energy stored in the leakage inductance during steady state, which is given as

$$\frac{1}{2} L_{\text{leakage}} i_{\text{tank,max}}^2 = \frac{1}{2} L_{\text{dc}} |i_{\text{tank,avg}}|^2. \tag{46}$$

Similarly, L_{sb} models the extra energy that can accumulate in the tank due to the DC offset $v_{c,\text{min}}$ permitted on the series bridge capacitor C_{sb}, expressed as

$$\frac{1}{2} C_{\text{sb}} v_{c,\text{min}}^2 = \frac{1}{2} L_{\text{sb}} |i_{\text{tank,avg}}|^2. \tag{47}$$

The physical intuition behind these terms is that L_{dc} models the energy stored in the leakage inductance as a function of

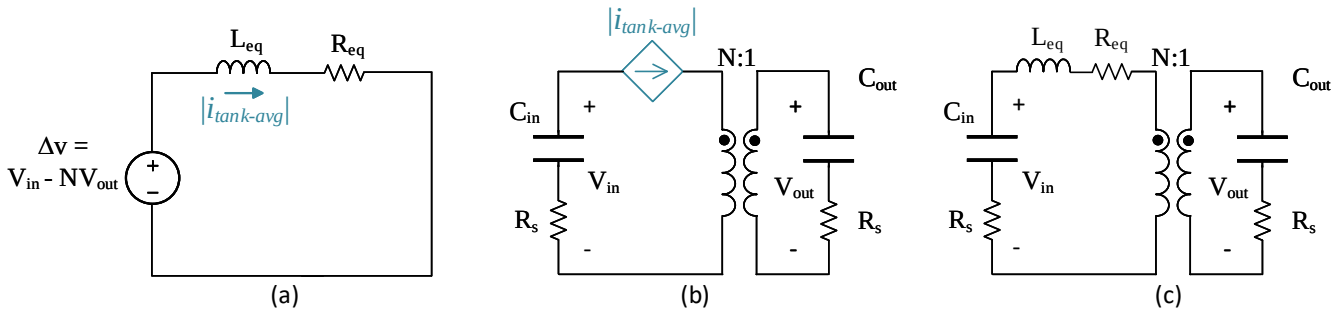


Fig. 6. (a) Circuit model representing the dynamics of the half-cycle averaged tank current in the SB-DCX converter during transients, as described by (36). (b) The averaged tank current drives a current source that interacts with the input and output capacitors, capturing the time-varying behavior of the converter - same as Fig. 3. (c) Combining (a) and (b) yields a complete circuit model that accurately represents the transient behavior of the tank current.

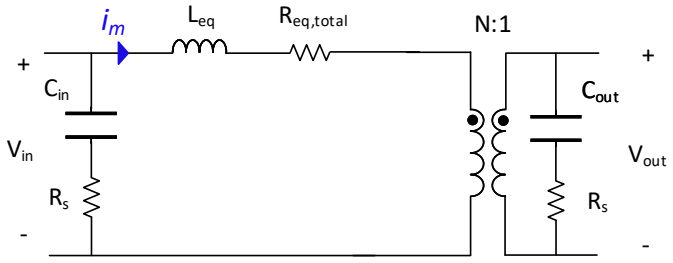


Fig. 7. Developed LTI circuit dynamic model that predicts the terminal behavior of SB-DCX.

half-cycle averaged tank current, and L_{sb} accounts for the extra energy accumulated in the series bridge capacitor due to the dc offset $v_{c,\text{min}}$. Furthermore, $R_{\text{eq, total}}$ models the total loss in the circuit due to R_p and R_s, as described by the expression in Eq. (41).

Based on this physical intuition, the important variables that relate the SB-DCX circuit variables to the developed model's circuit parameters, namely β, γ, and δ, can be found from the information about tank state variables using simulation or hardware data to improve the accuracy of the model for practical applications.

$$\beta = \frac{i_{\text{tank,rms}}}{|i_{\text{tank,avg}}|} \tag{48}$$

$$\gamma = \frac{i_{\text{tank,max}}}{|i_{\text{tank,avg}}|} \tag{49}$$

$$\delta = \frac{v_{c,\text{min}}}{|i_{\text{tank,avg}}|} \tag{50}$$

V. Simulation and Prototype Hardware Verification

To validate the developed half-cycle averaged model (Fig. 7), its predicted dynamic behavior was compared against the results of a switched-mode circuit simulation performed in PLECS. The SB-DCX circuit parameters used in the simulation are listed in Table II, and the corresponding terminal model parameters, derived from the proposed modeling framework, are provided in Table III.

The developed model provides half-cycle averaged values of key circuit variables, including the output voltage and the tank current (i_m). While the model does not capture switching ripple or high-frequency behavior, it effectively predicts the low-frequency envelope of the tank current. To estimate the peak or envelope of the tank current from its averaged value, the analytical expression given in (42) can be used.

The evaluation focused on a 50% load step—specifically, from 3 A to 6 A (step-up) and from 6 A to 3 A (step-down)—at an input voltage of 30 V. These transient conditions are representative of typical system-level dynamics in modular DCX applications. As shown in Figs. 8 and 9, the developed model accurately predicts the average output voltage and closely matches the envelope of the tank current observed in the simulation for both transient scenarios. This agreement confirms the model's capability to capture the dominant dynamic behavior of the SB-DCX topology.

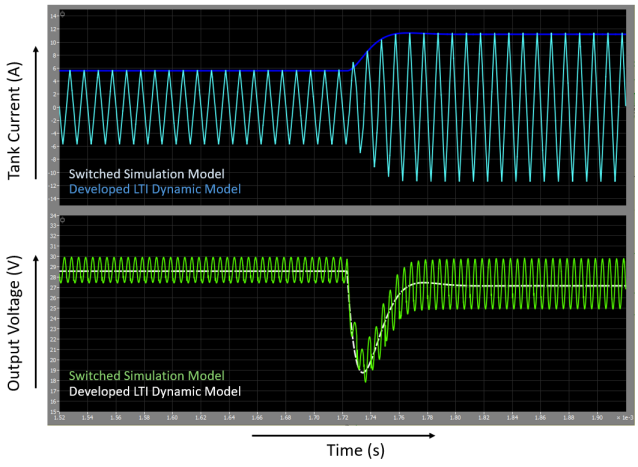


Fig. 8. Simulated dynamic response of the SB-DCX topology to a 3–6 A load step at 30 V input, comparing the switched-mode model with the developed linear circuit model.

TABLE II
Circuit Parameters for the Simulation and Prototype SB-DCX

f_{sw}	C_{in}	C_{sb}	L_{leak}	N	R_p	C_{out}
100 kHz	1.6 μF	1.28 μF	8.95 μH	1	0.403 Ω	1.6 μF

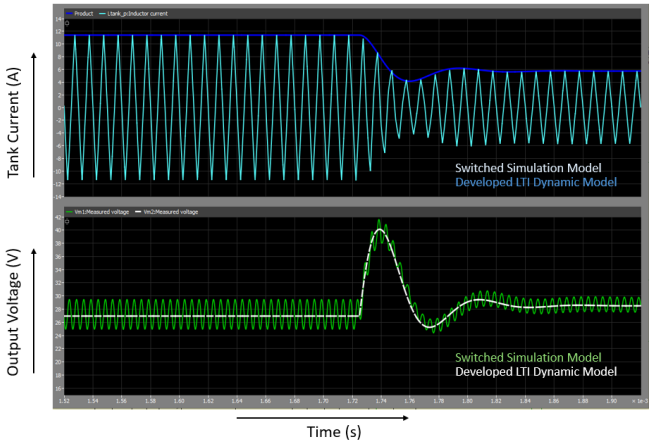


Fig. 9. Simulated dynamic response of the SB-DCX topology to a 6-3 A load step at 30 V input, comparing the switched-mode model with the developed linear circuit model.

TABLE III
SB-DCX TERMINAL MODEL PARAMETERS FOR CIRCUIT PARAMETERS GIVEN IN TABLE II

L_{eq}	β	γ	a	$R_{eq,total}$
71.89 μF	1.144	1.908	0.7386	0.53 Ω

Additionally, a prototype hardware (as shown in Fig. 10) was developed to evaluate the actual dynamic response. The circuit parameters used match those listed in Table II, and the power stage components are detailed in Table IV. An electronic switch and passive resistors were employed to generate the load step. The transient response for a 3–6 A load step at a 30 V input is shown in Fig. 11. For direct comparison, the measured waveform data were overlaid on the model's predicted response, as shown in Fig. 12. The close agreement between the measurement and the model confirms that the developed model accurately predicts both the tank current envelope and the average output voltage, validating its effectiveness.

TABLE IV
POWER STAGE COMPONENTS

Component	Part / Value
Primary & Secondary MOSFETs	SiC IMBG120R017M2H
Series Bridge (LV) MOSFETs	GaN EPC2361
Input/Output Capacitors	R75QR368050H0J
Transformer Core	PQ50/50-3C97

Similarly, step-down transients for a current step from 6–3 A were captured under two different dead time settings: 100 ns and 70 ns, as shown in Figs. 13 and 14, respectively. From the output voltage plots, it can be observed that the hardware results with a 70 ns dead time align more closely with the model predictions. This behavior arises because the proposed model does not account for dead time duration, and in step-down transitions, the resulting damping is not

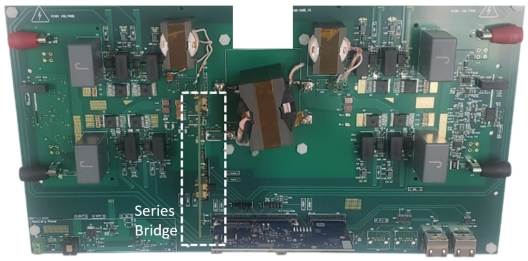


Fig. 10. SB-DCX hardware used to test load transient behavior for comparison with the developed DC terminal model.

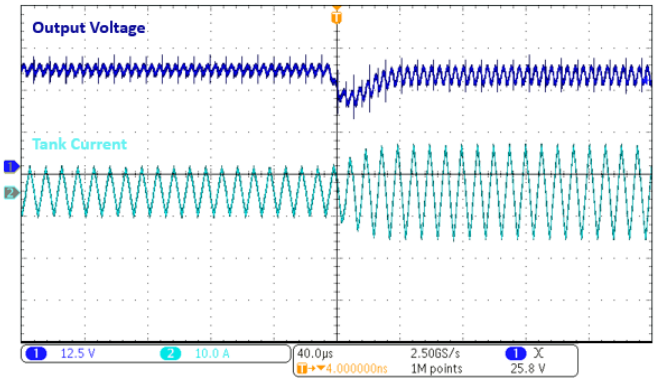


Fig. 11. Hardware dynamic response of the SB-DCX topology to a 3–6 A load step at 30 V input, comparing the switched-mode model with the developed linear circuit model.

solely governed by load impedance. Instead, longer dead times introduce additional damping effects, which are not captured by the developed LTI model. Consequently, a shorter dead time (70 ns) leads to hardware behavior that more accurately reflects the model's assumptions, resulting in improved agreement.

To further assess the model's generality, additional hardware experiments were conducted at a higher input voltage of 50 V. A step-up transient from 5–10 A is shown in Fig. 15, again demonstrating strong agreement between the model and the measured response. This consistency across varying input conditions highlights the robustness and predictive accuracy of the developed model.

Finally, a step-down transient from 10–5 A at 50 V input is presented in Fig. 16. In this case, the match between the model and measurement is slightly less accurate, which can be attributed to the 100 ns dead time used during operation. As the model does not account for dead time effects, the additional damping introduced in hardware is not captured, resulting in minor discrepancies during the transient. Nonetheless, the overall dynamic trends remain well-represented.

These results collectively confirm that the half-cycle averaged model provides a reliable and scalable framework for predicting the large-signal dynamics of the SB-DCX topology. Although the model does not account for dead time—leading to slight mismatches during step-down transients—the overall accuracy remains high, and the dominant system behavior is still well captured.

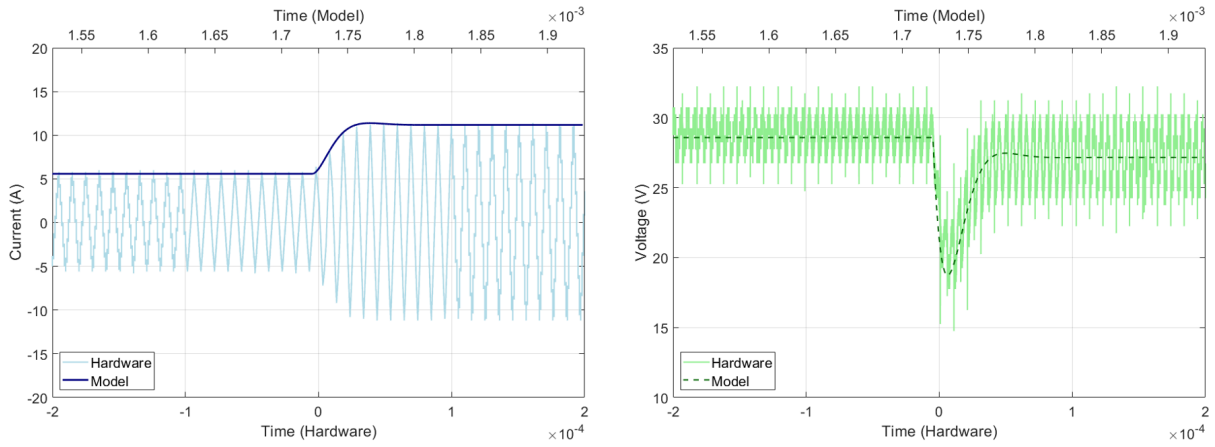


Fig. 12. Hardware load transient dynamics (3–6 A step at 30 V input) compared with model predictions: (a) Tank current envelope (model – dark blue) vs. measured tank current (light blue). (b) Output voltage without ripple (model – dark green) vs. measured output voltage (light green).

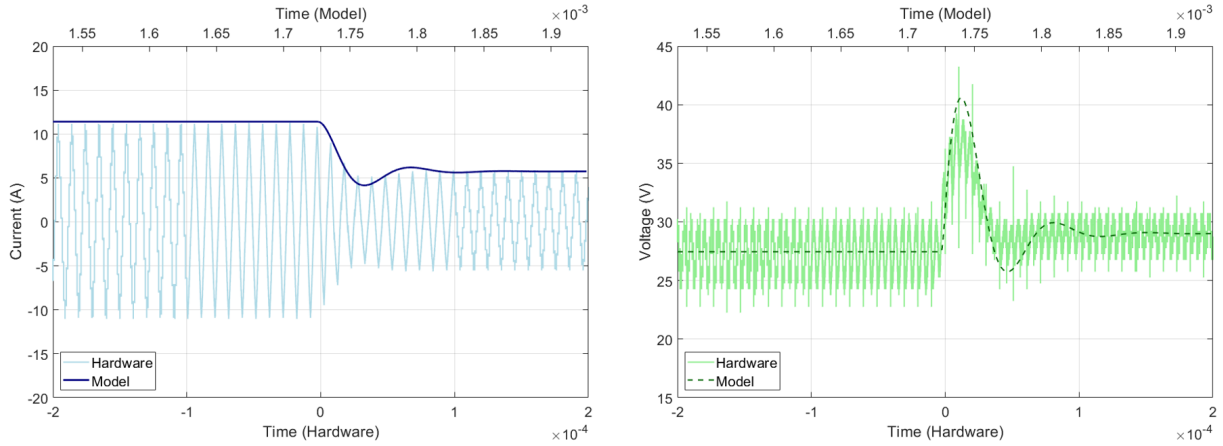


Fig. 13. Hardware load transient dynamics (6–3 A step at 30 V input with 100 ns dead time) compared with model predictions: (a) Tank current envelope (model – dark blue) vs. measured tank current (light blue). (b) Output voltage without ripple (model – dark green) vs. measured output voltage (light green).

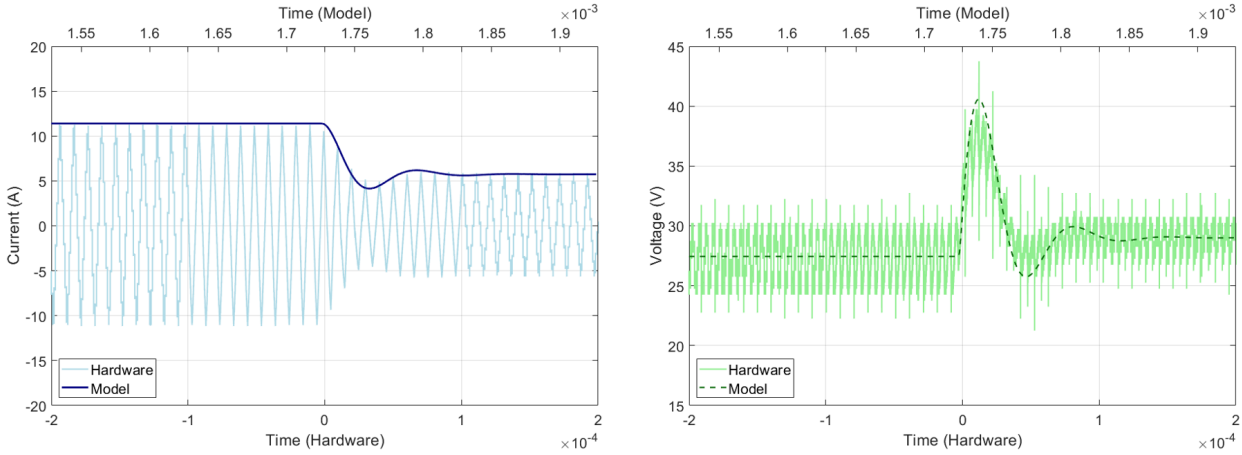


Fig. 14. Hardware load transient dynamics (6–3 A step at 30 V input) compared with model predictions: (a) Tank current envelope (model – dark blue) vs. measured tank current (light blue). (b) Output voltage without ripple (model – dark green) vs. measured output voltage (light green).

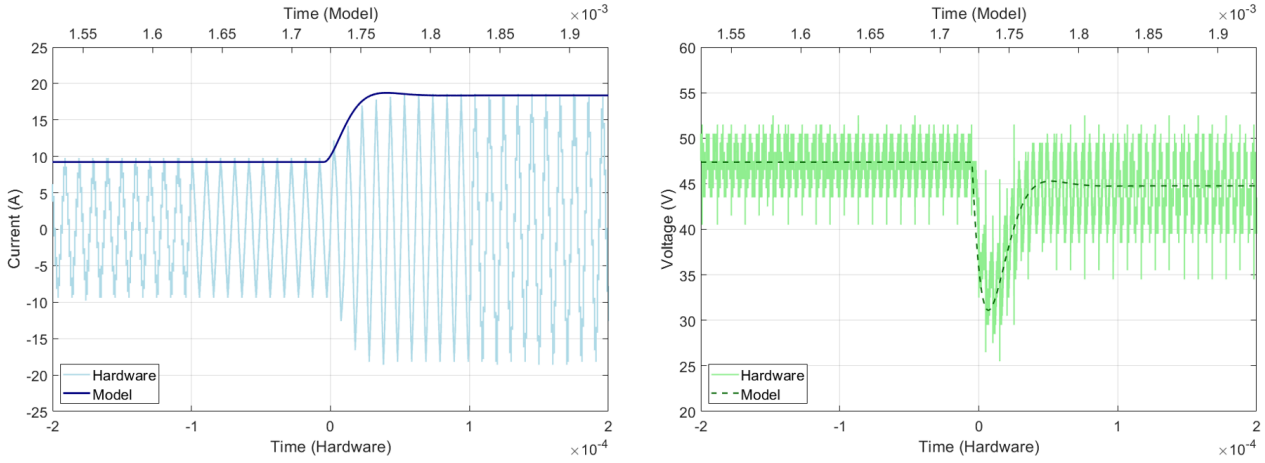


Fig. 15. Hardware load transient dynamics (5–10 A step at 50 V input with 100 ns dead time) compared with model predictions: (a) Tank current envelope (model – dark blue) vs. measured tank current (light blue). (b) Output voltage without ripple (model – dark green) vs. measured output voltage (light green).

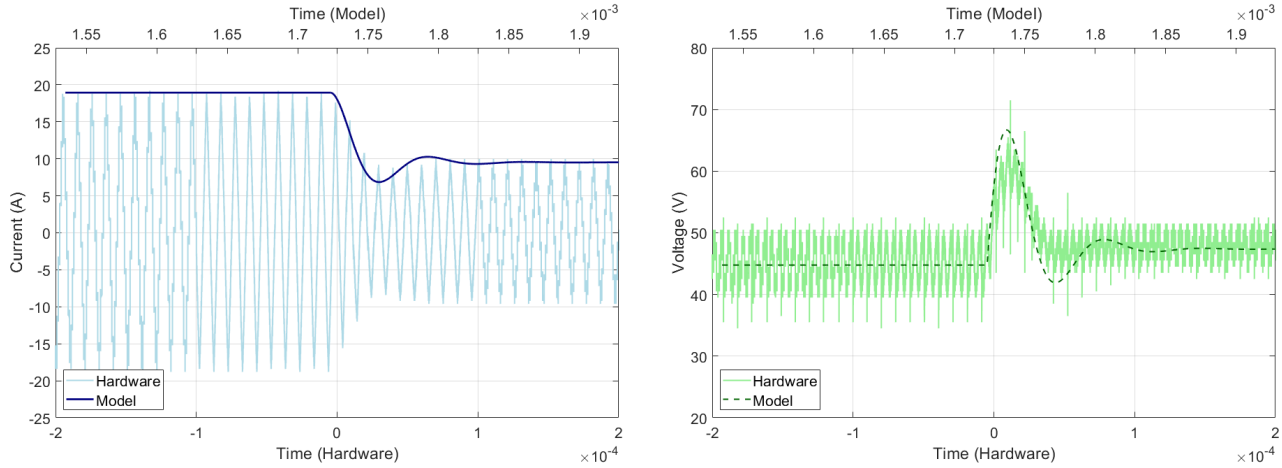


Fig. 16. Hardware load transient dynamics (10–5 A step at 50 V input with 100 ns dead time) compared with model predictions: (a) Tank current envelope (model – dark blue) vs. measured tank current (light blue). (b) Output voltage without ripple (model – dark green) vs. measured output voltage (light green).

VI. Conclusion

This article presents a linear time-invariant (LTI) dynamic model for the terminal characteristics of the Series Bridge-DCX (SB-DCX) topology, which has recently gained attention for DCX applications. By operating precisely at resonance, the SB-DCX inherently behaves as a DC transformer (DCX). A key advantage of this topology is that the SB acts as a variable capacitor, allowing it to tolerate tuning mismatches and ensuring robust resonant operation. This makes the topology practically attractive for modular converter architectures. An LTI dynamic model is essential for analyzing such systems using standard linear techniques and frequency-domain tools. Conventional approaches such as state-space averaging and phasor-domain analysis are not directly applicable to this topology.

To address this gap, an LTI model was derived using half-cycle averaging, resulting in a terminal model with a simple and scalable circuit-based representation. A complete time-domain derivation is provided, detailing the modeling assumptions and intermediate steps that support the final circuit formulation. The model's validity is demonstrated across a wide operating range through both switched-mode simulations and extensive hardware experiments at 30 V and 50 V input, with load transients up to 500 W. The modeling framework also facilitates the prediction of tank current envelopes and averaged output voltage under large-signal disturbances. While it does not account for dead time—and minor discrepancies arise during step-down transients where dead-time-induced damping is non-negligible—the model still offers accurate insight into dominant dynamic behavior. Overall, it serves as a practical and generalizable tool for the design and system-level analysis of SB-DCX converters.

References

[1] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99% efficient 10 kv sic-based 7 kv/400 v dc transformer for future data centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 753–767, 2019.

[2] S. Lim, A. J. Hanson, J. A. Santiago-González, and D. J. Perreault, "Bus converter using isolation capacitance for zvs and invariant operation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 1971–1982, 2020.

[3] B. Majmunović, S. Mukherjee, T. Martin, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson, and D. Maksimović, "1 kv, 10-kw sic-based quadruple active bridge dcx stage in a dc to three-phase ac module for medium-voltage grid integration," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 14 631–14 646, 2022.

[4] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimović, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 5774–5781.

[5] S. Poddar and R. Zane, "Estimation of minimum dead time to counter resonance mistuning in dab-src for dcx operation," in *2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2025.

[6] R. Raju, "Series resonant converters with the resonant capacitor replaced by a bridge," in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, 2017, pp. 999–1,002.

[7] Y. Cao and D. Dong, "Design and implementation of a 12 kw scalable electronic-embedded transformer (eet)-based dc transformer (dcx) with trapezoidal current," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 2340–2347.

[8] S. Poddar and R. Zane, "Dynamic modeling of the resonant series-bridge dcx converter," in *2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2025.

[9] D. Maksimovic, A. Stankovic, V. Thottuvelil, and G. Verghese, "Modeling and simulation of power electronic converters," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 898–912, 2001.

[10] R. J. Dirkman, "The simulation of general circuits containing ideal switches," in *1987 IEEE Power Electronics Specialists Conference*, 1987, pp. 185–194.

[11] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proceedings of the IEEE Industry Applications Society Annual Meeting*. IEEE, 1976, pp. 366–382.

[12] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3075–3078, 2011.

[13] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*. Addison-Wesley, 1991.

[14] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Springer, 2001.

[15] S. Sanders and G. Verghese, "Synthesis of averaged circuit models for switched power converters," *IEEE Transactions on Circuits and Systems*, vol. 38, no. 8, pp. 905–915, 1991.

[16] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *1976 IEEE Power Electronics Specialists Conference*, 1976, pp. 18–34.

[17] C. Rim and G. Cho, "Phasor transformation and its application to the dc/ac analyses of frequency phase-controlled series resonant converters (src)," *IEEE Transactions on Power Electronics*, vol. 5, no. 2, pp. 201–211, 1990.

[18] D. Seltzer, L. Corradini, D. Bloomquist, R. Zane, and D. Maksimović, "Small signal phasor modeling of dual active bridge series resonant dc/dc converters with multi-angle phase shift modulation," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 2757–2764.

[19] S. Sanders, J. Noworolski, X. Liu, and G. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 251–259, 1991.

[20] E. Yang, F. Lee, and M. Jovanovic, "Small-signal modeling of lcc resonant converter," in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 941–948 vol.2.

[21] M. Elbuluk, G. Verghese, and J. Kassakian, "Sampled-data modeling and digital control of resonant converters," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 344–354, 1988.

[22] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled pwm converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2552–2556, 2007.

[23] Z. Jia, Z. Wang, X. Zhao, Y. Jiao, B. Li, and D. Xu, "The dc terminal dynamic model of resonant converter," in *2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia)*, 2023, pp. 1892–1897.

[24] J. E. Huber, J. Miniböck, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle dcm series resonant converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 4–7, 2018.

[25] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio dc/dc converter cells for phase-modular solid-state transformers," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 5021–5029.

[26] M. Steiner, "Seriegeschaltete gleichspannungszwischenkreisumrichter in traktionsanwendungen am wechselspannungsfahrdraht," Ph.D. dissertation, ETH Zurich, 2000, phD Dissertation, in German.

CHAPTER 7

Investigation of Sector Distortion in Unfolder Architectures

Unfolder architectures often experience grid current distortions during transitions between sectors. This chapter investigates the underlying causes of these sector distortion phenomena and proposes a control solution in the context of a feedback-controlled DC–DC conversion stage. Minimizing sector distortion is essential for improving the practical applicability and overall performance of any unfolding-based architecture.

A 3-ϕ unfolder switches six times in each 60 Hz grid cycle, with each subinterval referred to as a sector. Every time the unfolder transitions from one sector to another, distortions are introduced into the grid currents, negatively impacting the total harmonic distortion (THD), which must be kept within specified limits to comply with grid requirements. Multiple factors can contribute to sector distortion, as detailed in this chapter. The most straightforward approach to mitigate these distortions is to increase high-frequency passive damping; however, this solution is bulky and costly.

Alternatively, the DC-DC stage can be controlled to emulate a resistor at the frequency of interest—a technique known as active damping. This method minimizes sector distortion regardless of its specific source and has been shown, as part of this work [43, 44], to significantly reduce sector distortion. However, active damping is fundamentally a reactive measure that mitigates the symptoms rather than addressing the root cause.

If the dominant cause of sector distortion can be identified, it becomes possible to eliminate the distortion at its source, leading to the most effective solution. This precise approach is explored in this chapter, as detailed in the work published in [44], where the exact mechanism causing sector distortion in feedback-controlled DC-DC conversion stages is identified and a targeted control strategy is developed to eliminate it at its origin.

from [44]. Minor edits have been made to correct typographical errors and improve clarity.

Investigation of Input Current Distortion at Sector Transitions in Unfolding-based Feedback Current Controlled AC-DC converters

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***Abstract*—Compared to state-of-the-art two-stage 3-ϕ ac-dc converters, unfolding-based topologies offer a more efficient and power-dense alternative by using a single dc-dc stage connected to an unfolding low frequency rectifier. However, the unfolding approach tends to suffer from input current distortion during sector transitions. These distortion impact the input power factor (PF), input current total harmonic distortion (THD), and input filter requirements. Existing understanding and models in literature do not predict the higher distortion that is observed with increasing filter capacitance or increasing ac line frequency. This paper provides reasoning, analysis, and a control solution to mitigate input current sector distortion in unfolding-based topologies. The source of the distortion is identified and analyzed as interactions between the input filter capacitors and dc-dc stage feedback control of the input currents. The proposed control is tested at 3-ϕ 50 V_{ac}, 50 W output power. Hardware results highlight a significant decrease in THD from 8.5% to 4.5%.**

***Index Terms*—Unfolder, 3-ϕ grid-tied converters, ac-dc converters, sector distortion, total harmonic distortion, power factor correction.**

I. Introduction

Modern 3-ϕ power converters are expected to process power at greater efficiencies and power density. 3-ϕ power converters enable the integration of high-power dc loads and sources with the grid. The rapid adoption of electric vehicles (EVs), the expanding infrastructure for data centers, and the increasing generation of renewable energy are all propelling an exponential surge in the demand for power conversion that needs to interface with 3-ϕ grid. Hence, a concerted effort is underway in the field toward deploying highly efficient, power-dense, and reliable 3-ϕ power converters.

To interface high-power dc loads with the grid, a 3-ϕ ac-dc converter typically employs a two-stage architecture [1]. The converter's targeted functionalities are: providing a controlled power at the required output voltage, controlling input power factor (PF) and total harmonic distortion (THD), and maintaining galvanic isolation. The two-stage architecture consists of two cascade-connected converters - an active front-end (AFE) rectifier followed by a dc-dc converter [1]. An AFE rectifier performs power factor correction (PFC). The dc-dc converter provides isolation and tight regulation of the output voltage. A two-stage architecture often employs a large "decoupling" capacitor to decouple the dynamics of two power conversion stages. This architecture simplifies hardware and controller design but limits performance.

The unfolding-based single-stage architecture offers an energy-efficient and power-dense alternative [2]–[4]. The basic architecture consists of a line-switched unfolder (also referred to as an input voltage selector) followed by a dc-dc converter. The unfolder switches at line frequency, and hence, it exhibits negligible switching loss (Section II details unfolder operation). The dc-dc converter fulfills all three of the primary ac-dc converter objectives: voltage regulation, PFC, and isolation (if required). Owing to a single high-frequency power processing stage, unfolding-based ac-dc architectures have the potential to achieve higher efficiency and power density when compared to two-stage architectures [2].

Adversely, unfolding-based 3-ϕ ac-dc converters suffer from input current distortions at sector transitions [5]. This results in a degraded performance - higher THD and, in turn, a lower input PF. This problem is attributed to non-ideal behavior during the sector transitions. The non-idealities can be due to: body diode conduction associated with high-frequency voltage ripple across input filter capacitors and/or finite unfolder commutation time [5]–[8]. The solutions include: modulation of the unfolder, passive damping, or a modified unfolder topology. These solutions tend to diminish the benefits of the unfolder architecture. These challenges are documented for open-loop or feed-forward PFC current control [5], [8]. However, feedback control of input currents in combination with the reactive current drawn by the filter capacitors leads to additional distortion during sector changes. This mechanism leads to even higher distortion with increasing filter capacitance, low loads, and at high ac input frequency. A synchronous frame controller [9] or a model predictive control [11] does help alleviate the problem however, the implementation and computation complexity can be avoided. Modeling and eliminating this additional source of sector distortion is the primary focus of this paper.

This paper provides analysis and control solutions to es-

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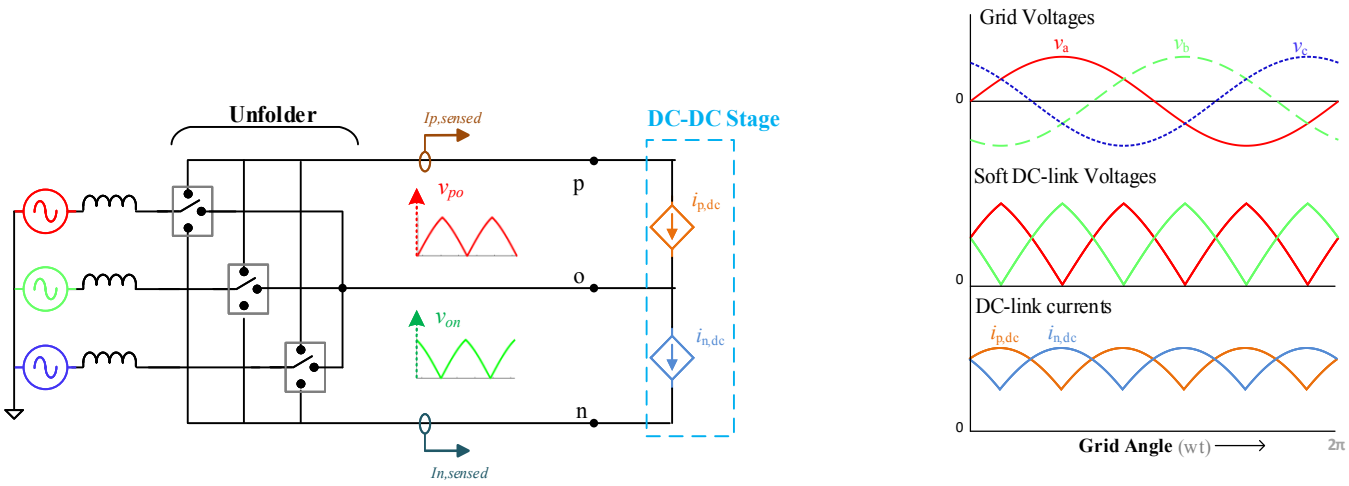

Fig. 1. (a) Architecture - a grid-tied unfolder followed by a dc-dc stage with the grid and grid filter inductors modeled for completeness. The line switched unfolder, a combination of single-pole triple-throw switches, is switched once every "sector" to obtain time-varying dc voltages from the 3-ϕ ac. The soft dc-link capacitors filter high-frequency current ripple from the dc-dc stage. The dc-dc converter is modeled with current sources at the input ports and a constant power source at the output port. Input and output ports are galvanically isolated. (b) Normalized balanced 3-ϕ grid voltages, soft dc-link voltages (in a complete grid cycle), and ideal dc-dc currents to emulate resistive input currents - assuming negligible capacitance.

sentially eliminate sector distortion owing to capacitive filter currents and input current feedback control and additionally minimize sector distortion from the remaining mechanisms. Section II details the working of a 3-ϕ unfolding-based ac-dc converter - the architecture, unfolder operation, and dc-dc control implementation. Section III explains sector distortion - from all the various sources. Section IV proposes a simple yet effective solution to minimize sector distortion from all the different sources without disturbing the line frequency operation of the unfolder (i.e., the proposed solution minimizes the problem while preserving the inherent advantages of the unfolder). The control solution is based on a combination of active damping and current reference correction terms. Detailed hardware implementation and experimental results (at 3-ϕ 208 V_{ac}, 300W output power) are provided in Section V and demonstrate a significant reduction in harmonic distortion with a decrease in THD from 8.5% to 4.5%.

II. Unfolding-based 3-ϕ ac-dc converter architecture and controls

A. Architecture

An unfolding-based single-stage 3-ϕ ac-dc converter architecture consists of a line-switched unfolder followed by a dc-dc power processing stage. A block diagram is shown in Fig. 1(a). The dc-dc converter shapes the input currents and controls the output power.

The unfolder is a combination of line-frequency operated switches - operated to obtain the time-varying dc voltages (V_{po} and V_{on}) from 3-ϕ ac voltages as shown in Fig. 1(b). The unfolder switches at the start of every "sector", to change the connection between the 3-ϕ ac input and the input ports of the dc-dc converter (the input ports are also referred to as the "soft" dc-links). An ac input cycle is divided into six sectors that signify the different unfolder switching configurations. Refer [2], [4] for the exact unfolder switching.

An unfolding-based architecture has a single controlled power-processing stage (the downstream dc-dc converter) and doesn't require intermediate bulk energy storage. The unfolder facilitates a direct connection between the ac input and the downstream dc-dc stage. This direct connection changes every sector. It doesn't control power and hence, doesn't have any switching frequency-dependent energy buffering (therefore, no associated dynamics). To summarize, the advantage of an unfolder is - two time-varying dc voltages are obtained from a 3-ϕ ac input without the need for energy storage (no dynamics and minimal losses). Hence, the unfolding-based architecture has the potential to be more power-dense and efficient than a two-stage architecture.

The downstream dc-dc stage handles all the power control objectives. The dc-dc input ports can be modeled as two current sources (I_p^{dc} and I_n^{dc}) - one each across the two soft dc-links. Ignoring the dc-link capacitors, I_p^{dc} and I_n^{dc} needs to be controlled as shown in Fig. 1(b).

B. DC-DC controls implementation

As seen from Fig. 1(a), the two input ports of the dc-dc converter are controlled to behave as two independent current sources. The shape of the dc-dc converter currents is controlled for PFC and the magnitude is controlled to regulate output power. Hence, all that's needed is: to control the shape and the magnitude of the currents I_p^{dc} and I_n^{dc} to fulfill all the dc-dc control objectives.

More fundamentally, it can be inferred that at least two independent dc-dc currents or electrical quantities are to be controlled to fulfill the converter's targeted functionalities. It is mathematically proven ([12], Section IV-A pg. 187) that

control of any one unfolder current and maintaining a constant output power can be sufficient for PFC.

It is important to note that the control design is specific to the dc-dc topology. To keep the sector distortion analysis generalized, we discuss a sector distortion control solution (Section IV) assuming independent control over dc-dc currents - I_p^{dc} and I_n^{dc}. The control block diagram is highlighted in Fig. 2.

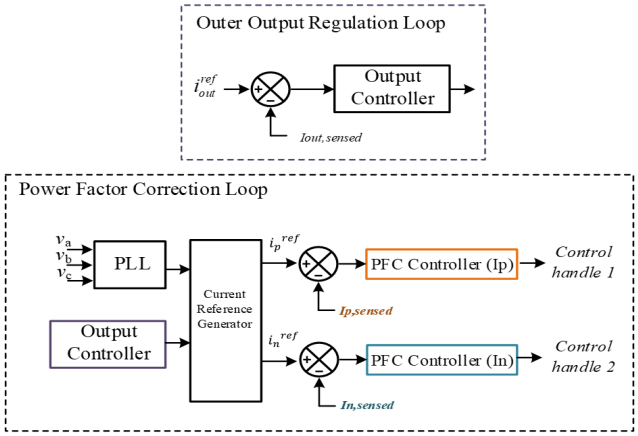

Fig. 2. Control block diagram for output power regulation and PFC. The current reference generator uses the grid angle information and power regulation loop output to generate the dc-dc current reference. It is assumed that I_p^{dc} and I_n^{dc} can each be controlled by independent control handles

III. Sector Transition Distortion

The current distortion in the 3-ϕ ac input currents during sector transition in an unfolding-based architecture is referred to as the sector transition distortion. Multiple factors, depending on the control scheme and the constraints related to the hardware implementation lead to sector distortion. Most explanations in the literature are in the context of open-loop or feedforward-based input current control [5], [8]. DC-DC stage feedback input current control - often implemented to counteract modeling inaccuracies - leads to additional distortion. The analysis and a model to predict the additional distortion are provided here.

A. Different factors contributing to sector distortion

Sector transition distortion mechanisms can be categorized as non-idealities induced due to: practical hardware constraints or input current control schemes.

Non-idealities in hardware implementation are often attributed as the dominating factor of sector distortion. These non-idealities include: finite switching time for the unfolder switches [7], [8] and/or the body diode conduction of the downstream dc-dc or the unfolder [5], [6]. The finite switching time of the unfolder switches leads to overlapping of the switch commutation trajectories. This shorts the dc-dc filter capacitors resulting in sector distortion. Additionally, high-frequency ripple across the filter capacitor leads to undesired conduction of the dc-dc or the unfolder body diode - near sector transition. This builds energy in the input inductors resulting in distortion. This distortion mechanism predicts a higher filter capacitance (lower voltage ripple), which means a shorter duration of body diode conduction, results in lower distortion.

Open-loop or feed-forward input current control is often used for the downstream dc-dc converter. However, a low-fidelity model can lead to poor THD performance, and an accurate model [10] leads to substantial computational complexity. Alternatively, feedback control is used to correct model inaccuracies but leads to a different distortion mechanism. This mechanism predicts that a higher filter capacitance results in higher distortion. This mechanism dominates at light loads and at higher ac input frequencies.

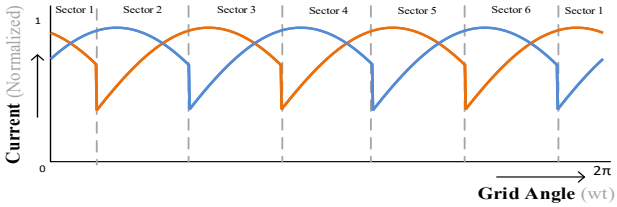

Fig. 3. Ideal currents I_p^{dc} and I_n^{dc} as required for unity power factor - including the reactive current due to the finite filter capacitance. I_p^{dc} and I_n^{dc} must have a perfect step change after sector change to ensure balanced loading to the grid. If the control isn't able to track the step - it creates an imbalance during sector transition.

B. Sector distortion mechanism due to feedback control of input currents

The interactions between the dc-dc filter capacitors and the dc-dc stage feedback control of input currents cause additional sector distortion. An increase in the input ac frequency and the dc-dc filter capacitance results in higher distortion (in contrast with other distortion mechanisms).

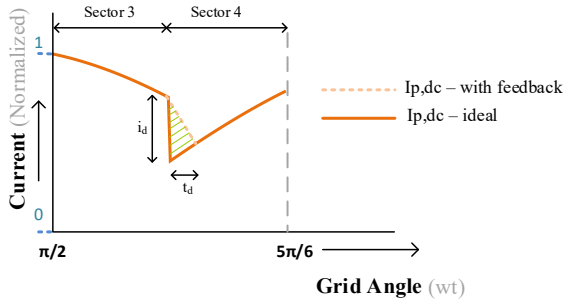

Fig. 4. I_p^{dc} during transition from sector 3 to sector 4. A finite control bandwidth results in an imperfect tracking of the reference current. The difference in the desired and the actual currents (dashed area) creates a current imbalance in the system after transition.

Ideally, to obtain a unity input power factor, dc-dc currents I_p^{dc} and I_n^{dc} are to be controlled as shown in Fig. 1(b). These ideal dc-dc currents assume negligible currents drawn by the

input filter capacitors. The input filter capacitors are used to shunt the high-frequency dc-dc current ripple. They can be added in delta or star configuration - to act as a balanced load to the grid. Hence, in a given sector, the filter capacitors and the controlled dc-dc current sources combine to act as a balanced resistive load. However, during sector transitions, an imbalance is created that results in distortion.

The current drawn by the filter capacitors and the finite dc-dc feedback current control bandwidth causes imbalance after a sector transition - resulting in sector distortion. Consider a finite filter capacitance that draws a 10% (of real current) reactive current. I_p^{dc} and I_n^{dc} for a unity power factor, is shown in Fig. 3. These have significant steps after the sector transition - proportional to the filter capacitor current. This step change worsens (comparatively) at light loads. Finite control bandwidth ($<<$ switching frequency) means, feedback controlled I_p^{dc} and I_n^{dc} cannot track ideal dc-dc currents perfectly. This creates an imbalance in the system after the sector transition as highlighted in Fig. 4. This results in sector transition distortion.

To solve the problem, it is imperative to model and physically understand the distortion mechanism. Consider an equivalent circuit before and after the transition as shown in Fig. 5. The filter capacitors are star-connected - for modeling convenience. The dc-dc input emulates ideal currents (Fig. 3) (for a unity input power factor) before the sector transition. This results in a balanced-resistive loading to the grid. After the sector transition, the non-ideal tracking of the dc-dc current (I_p^{dc} in this sector) is modeled as a balanced system in combination with a current pulse that represents an imbalance - in an already balanced system. The effect of the imbalance on the input currents can be studied using superposition (the equivalent model is linear and time-invariant in a given sector). The model can be simplified into a single-phase equivalent circuit as shown in Fig. 6. I_d is the current step amplitude as given by (1) and t_d is approximated to be a function of τ. Where τ is the time constant for a step response of the dc-dc stage feedback-controlled current. The step response is approximated to be a first-order response for a linear time-invariant (LTI) system. τ can be expressed as the feedback controller's bandwidth as given in (3).

$$I_d = 2I_a sin(\phi) \tag{1}$$

$$\phi = tan^{-1}(\frac{Q}{P}), \qquad Q = 9wC_{filter}(V_{ph,rms})^2 \tag{2}$$

$$\tau = \frac{1}{2\pi f_{bw}} \tag{3}$$

Here, I_a is the phase current amplitude, ω is the ac input angular frequency, P is the real power processed, and Q is the reactive power. It is important to note that the reactive power Q is assumed to be only due to the input capacitive filters. The reactive power consumed by the grid filter inductance is negligible.

Physically, the imperfect tracking of I_p^{dc} and I_n^{dc} forces the state of the energy storage elements to change suddenly - leading to push-back manifesting itself as sector distortion. With dc-dc stage feedback control, reactive currents are supplied by the dc-dc converter. During the transition, the dc-dc converter doesn't accurately track the step change in ideal dc-dc currents (for unity input pf). An energy imbalance is created that forces the energy storage elements to react. This imbalance (as shown in Fig. 6) can be modeled as a triangular current pulse. This pulse excites the resonant frequency of the input filter creating an LC oscillation. This oscillation can be damped - using passive elements or active control. However, damping is reactive mitigation.

As mathematically modeled by (2), the sector distortion current is a function of the filter capacitance, input frequency, and input voltage. An increase in the ac input frequency increases the capacitive current draw resulting in an increase in the ideal dc-dc current step and hence, higher sector distortion. Applications that have higher input frequency would have significant distortion solely from the dc-dc stage feedback current control-induced distortion mechanism. Moreover, at light loads, the step change in current is more pronounced - leading to higher distortion. All these factors necessitate a control solution to minimize the impact.

IV. Control solution

The control solution proposes to eliminate the capacitive current-dependent distortion by ensuring that the dc-dc currents track the ideal dc-dc current reference (Fig. 3). This is done using a current reference correction term. Active damping in combination with the reference correction term minimizes distortion from all the other mechanisms.

Sector distortion (independent of the source) can be damped - either by physical energy-storage enabled passive damping or by a controlled current source that emulates a passive resistor (active damping). The dc-dc stage already emulates the current sources for PFC. Hence, extending the dc-dc to employ active damping is often a preferred solution [6], [8], [13].

However, the elimination of the prominent cause of distortion facilitates superior converter performance. With feedback input current control, the capacitive current-dependent sector distortion dominates. Especially, at light loads. To eliminate this distortion and maintain ideal balanced conditions - the capacitor current demand must be met from the dc-dc converter. The proposed control solution works on this very principle.

The sector distortion control changes the input current reference - I_p^{ref} and I_n^{ref} - during sector change. The current reference and the change in the current reference are highlighted in Fig. 7. With an unchanged current reference, the feedback current controller needs to react to a step change in currents I_p^{dc} and I_n^{dc}, which is reflected on the sensed currents $I_{p,sense}$ and $I_{n,sense}$ (shown in Fig. 1(a)). With a finite bandwidth, the dc-dc stage feedback controller cannot immediately respond to the step requirement of dc-dc currents. To overcome this limitation, the proposed control provides the step change information to the compensator by changing the

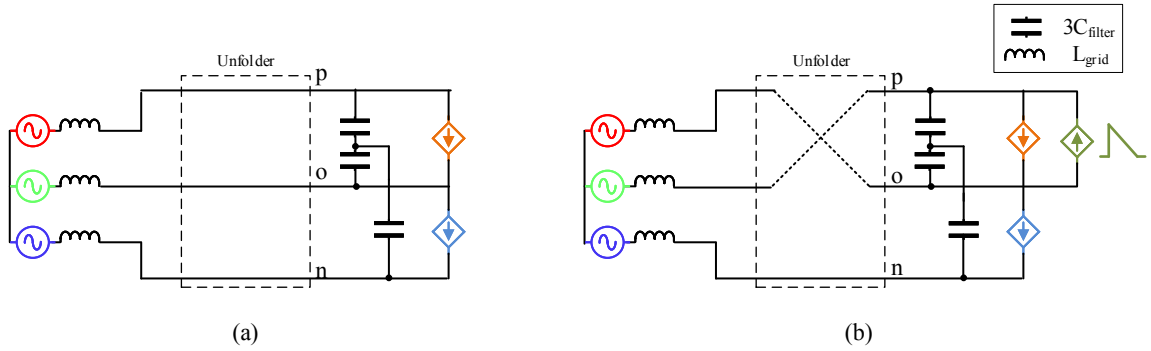

Fig. 5. (a) Equivalent circuit during sector 3. The unfolder is a fixed connection between the ac input and the dc-dc converter. The dc-dc converter is modeled as two ideal current sources that maintain a balanced system and ensures a unity power factor. (b) The equivalent circuit after the unfolder transitions to sector 4. The dc-dc is modeled as an ideal balanced current source system + a current imbalance (modeled as a triangular pulse just after the transition). The equivalent circuit is a linear time-invariant circuit in any given sector

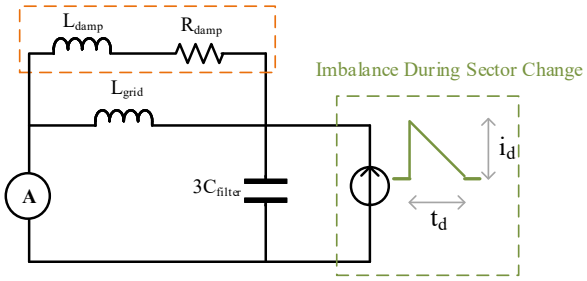

Fig. 6. A single phase ac equivalent circuit to predict the amplitude of sector distortion - as a function of capacitive current(id), control bandwidth (td), and grid frequency. The voltage source is short, and grid inductance and the passive damping circuit are added to model the prototype.

current reference ahead of time. Hence, instead of reacting, preempting the step change and responding accordingly. The math for the change in the current reference uses the mathematical model developed in section III. Where, I_{ctrl} is the same as I_a and t_{ctrl} is τ.

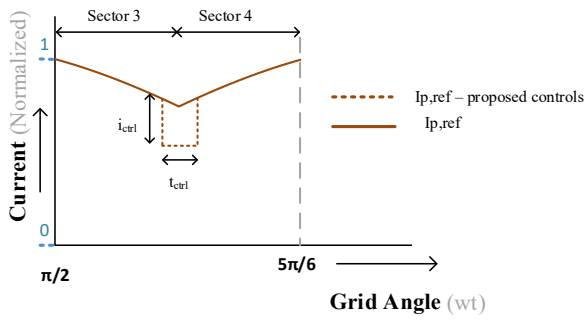

Fig. 7. I_p^{ref} during transition from sector 3 to sector 4. A feedforward term is used to modify the current reference to minimize the impact of sector distortion.

This current reference change is a feed-forward correction term that maintains near-perfect step tracking as required by the ideal unfolder currents - I_p and I_n - for a unity input power factor. Additionally, the current reference change is used in combination with active damping to minimize distortion from all the other sources (control diagram - Fig. 8). The control solutions are validated through hardware shown in Fig. 9.

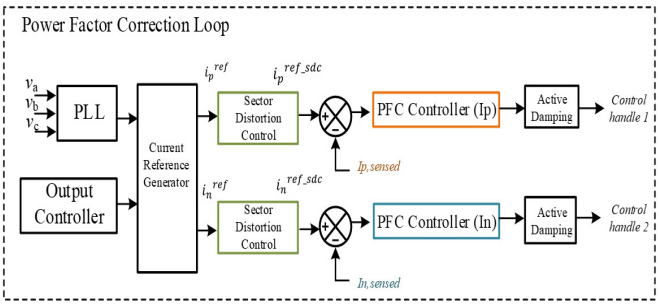

Fig. 8. Control block diagram highlighting the addition of sector distortion control and active damping to minimize distortion from all the sources.

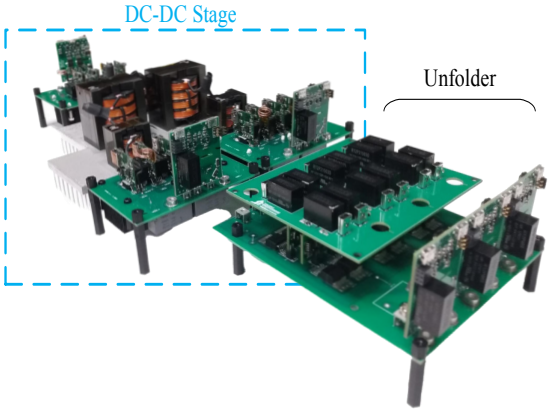

Fig. 9. 2 kW hardware setup to test and validate the proposed control solution. 3-ϕ line frequency-switched unfolder and dc-dc converter connected to the 3-port output of the unfolder - for PFC, power regulation, and isolation.

V. Hardware Implementation and Results

A 3-ϕ 480 V_{ac} - 600 V_{dc}, 2kW prototype is developed that uses a triple active bridge topology [4] for the dc-dc

stage. A digital controller is used to implement the proposed controls. Loop delay ([12]), sensing, and communication delay need to be managed to ensure expected performance improvement. Power analyzer (Yokogawa WT1806E) results highlight a significant decrease in input current THD.

A. Managing delays in sensing and control loop

The sensing and the communication delay impact the grid angle information as generated by the Phase-locked loop (PLL). Therefore, the current references I_p^{ref} and I_n^{ref} are not synchronized with the actual ac voltages. However, if the delay is known, it can be accounted for by appropriately shifting the PLL-generated angle θ.

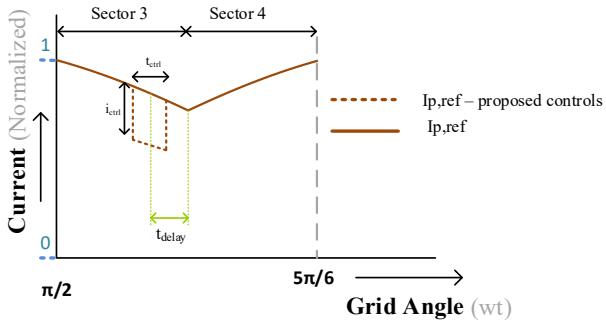

Fig. 10. I_p^{ref} feed-forward term for sector distortion control - accounting for loop delay.

Similarly, loop delay significantly affects the proposed control's performance. This is because the change in the current reference needs to be enabled exactly near the sector transition. The solution is to account for the delay by shifting (in time) the feedforward term as shown in Fig. 10. The soft-dc link voltages V_{po} and V_{on} are sensed and are used as substitutes for t_{ctrl} to activate the feedforward term. Alternatively, the PLL-based grid angle can also be used.

B. Hardware results

The sector distortion mechanism due to the dc-dc stage feedback-current control is significant at light load operation. Hence, the hardware results are at 3-ϕ 50 V_{ac} input voltage (line-line), 50 W output power. Fig. 11 shows the hardware results with the conventional approach - actively damping the oscillation by controlling the DC-DC near the sector transition. This approach is independent of the source of the sector distortion as it reacts to the symptom of the problem. Results for the proposed controls are shown in Fig. 12. The sector transition distortion is significantly lower and the improved performance is highlighted by the THD reduction from 8.5% to 4.5%. The additional improvement highlights the preemptive approach of the proposed controls.

VI. Conclusion

This paper explains and models the source of sector transition distortion in unfolding-based topologies - specific to the interactions between the capacitive filter currents and the dc-dc

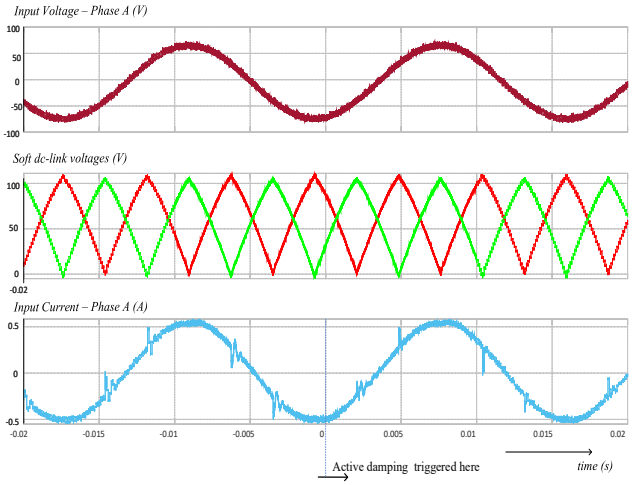

Fig. 11. Experimental results highlight increased damping near sector transition in input current I_a - after triggering active damping. Measurements show THD reduction from 8.5% to 7%.

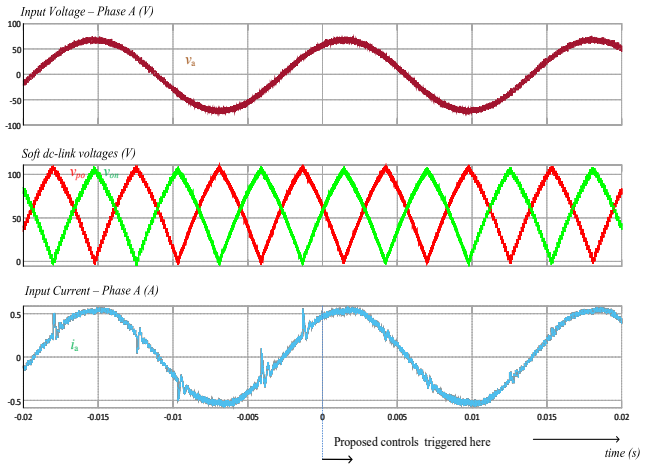

Fig. 12. Experimental results highlight a significant reduction in the input current (Ia) distortion - after triggering the proposed controls. The reduction in distortion is much higher compared to active damping controls only

stage feedback control of the input currents. A control solution is proposed that preempts the sector distortion. The control solution preserves the advantages of the unfolder and is easy to implement - without any hardware modification. Moreover, the full control solution minimizes any distortion pertaining to sector transitions. Hardware results highlight a significant reduction in distortion, which is corroborated by a 47% THD reduction.

References

[1] J. W. Kolar and T. Friedli, "The Essence of Three-Phase PFC Rectifier Systems—Part I," in IEEE Transactions on Power Electronics, vol. 28, no. 1, pp. 176-198, Jan. 2013, doi: 10.1109/TPEL.2012.2197867.

[2] T. B. Soeiro, T. Friedli and J. W. Kolar, "Swiss rectifier — A novel three-phase buck-type PFC topology for Electric Vehicle battery charging," 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2012, pp. 2617-2624, doi: 10.1109/APEC.2012.6166192.

[3] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase ac–dc power conversion using series-resonant converter modules and a three-phase unfolder," IEEE Transactions on Power Electronics, vol. 32, no. 12, pp. 9001–9012, 2017.
[4] D. B. Yelaverthi, M. Mansour, H. Wang, and R. Zane, "Triple active bridge series resonant converter for three-phase unfolding based isolated converters," in IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, vol. 1, 2019, pp. 4924–4930.
[5] L. Schrittwieser, J. W. Kolar, and T. B. Soeiro, "Novel swiss rectifier modulation scheme preventing input current distortions at sector boundaries," IEEE Transactions on Power Elec- tronics, vol. 32, no. 7, pp. 5771–5785, 2017.
[6] R. Chen, Y. Yao, L. Zhao, and M. Xu, "Inhibiting mains current distortion for swiss rectifier - a three-phase buck-type harmonic current injection pfc converter," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, pp. 1850–1854.
[7] Q. Zhang, Z. Dong, D. Zhang, H. Zeng, X. Zheng, and W. Lin, "An improved swiss rectifier and its nonlinear control for lower thd," CPSS Transactions on Power Electronics and Applications, vol. 7, no. 3, pp. 319–327, 2022.
[8] H. P. N., T. Mannen, and K. Wada, "A current source three-phase ac-ac converter using cur- rent unfolding and active damping principles," in 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 6239–6245.
[9] W. W. Chen and R. Zane, "Active rectifier system using three-phase unfolder and series resonant converters controlled in synchronous rotating frame," in 2016 IEEE International Telecommu- nications Energy Conference (INTELEC), 2016, pp. 1–7.
[10] B. Zhang, S. Xie, X. Wang and J. Xu, "Modulation Method and Control Strategy for Full-Bridge-Based Swiss Rectifier to Achieve ZVS Operation and Suppress Low-Order Harmonics of Injected Current," in IEEE Transactions on Power Electronics, vol. 35, no. 6, pp. 6512-6522, June 2020, doi: 10.1109/TPEL.2019.2951795.
[11] Y. Kokuhennadige, B. Ahmad and J. Kyyrä, "Model Predictive Control for Three-Phase Buck-Type PFC Rectifier in Aircraft Applications," 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, 2021, pp. 1-10, doi: 10.23919/EPE21ECCEEurope50061.2021.9570484.
[12] J. W. Kolar and T. Friedli, "The Essence of Three-Phase PFC Rectifier Systems—Part I," in IEEE Transactions on Power Electronics, vol. 28, no. 1, pp. 176-198, Jan. 2013, doi: 10.1109/TPEL.2012.2197867.
[13] A. Zade, C. R. Teeneti, S. Gurudiwan, S. Poddar, M. Mansour and R. Zane, "Analysis and Mitigation of Sector Transition Distortions for Unfolding-based Grid-tied AC-DC Converters," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1945-1952, doi: 10.1109/APEC43580.2023.10131393.
[14] L. Corradini, , D. Maksimovic, P. Mattavelli, and R. Zane, Digital Control of High-Frequency Switched-Mode Power Converters. Wiley-IEEE Press, 2015.

CHAPTER 8

Conclusion and Future Work

This dissertation proposes a novel three-phase unfolding-based, direct medium-voltage (MV)-connected architecture for interfacing high-power loads—such as DC fast charging stations (DCFCs)—with the three-phase (3-ϕ) AC grid. The objective is to enhance the performance and reliability of power conversion systems that are central to the operation of DCFCs. The complete proposed architecture is validated through megawatt-scale simulations and a lab-scale hardware prototype.

Furthermore, this work addresses several fundamental challenges critical to the viability of the proposed architecture. These include the design of various converters within the system, comprehensive steady-state and dynamic modeling of the DC-DC converters, and the development of control strategies to minimize sector distortion and improve the total harmonic distortion (THD) performance of unfolding-based architectures. Collectively, these contributions not only enable the realization of the proposed architecture but also offer insights applicable to a broader range of power electronics systems beyond this specific application.

In addition, this dissertation outlines the future work required to make the proposed architecture ready for pilot deployment in real-world environments.

Improvement in MV-connected unfolding-based architectures with hybrid distribution

Unfolding-based quasi-single-stage architectures have been shown to offer superior performance metrics compared to traditional multi-stage approaches. Hybrid distribution, which incorporates both AC and DC buses, enables improved hardware utilization. Current state-of-the-art systems employ a modular unfolding-based 3-ϕ AC-DC converter to generate a DC bus, along with an additional DC-AC converter to supply an AC bus. However, the modular structure typically relies on a centralized controller for power sharing,

which reduces system reliability and increases the design complexity of the DC-DC stage. In addition, the AC-AC power conversion path involves two cascaded stages, resulting in additional losses and complexity. This work addresses and improves upon these limitations.

The proposed architecture introduces a novel unfolding-based system with a hybrid output to maximize the utilization of MV-connected hardware. It includes a modular DC-DC stage, referred to as the DCX stage. Each module within the DCX stage operates in a passive DC transformer (DCX) mode, enabling natural voltage sharing across series-connected modules and supporting fully decentralized power-sharing control. Furthermore, the AC-AC power conversion is accomplished using a single high-frequency stage, significantly improving both system efficiency and simplicity.

Experimental hardware validates the feasibility of the proposed architecture, demonstrating key advantages such as hybrid distribution capability, natural voltage sharing, and improved AC-AC conversion performance. The DCX stage achieved efficiencies exceeding 97%, with overall three-phase AC-AC conversion efficiency reaching 96.5%. These results represent a significant improvement over conventional multi-stage implementations. The hardware implementations and results for the complete architecture are intended for publication in a peer-reviewed journal and are currently under internal review. Furthermore, a patent application is currently in progress for the proposed architecture.

Additionally, a major contribution of this dissertation is the development of a topology and control framework for the energy storage integration converter within the proposed architecture. This includes the appropriate selection and operation of the converter topology to enable reactive power control while interfacing with the time-varying voltage output of the unfolder. The proposed approach has been validated through hardware experiments, demonstrating effective reactive power control. The framework supports both reactive power regulation and seamless battery integration, thereby enhancing grid compatibility for high-power, intermittent loads such as DC fast chargers.

DCX Stage Design, Modeling and Hardware Validation

The design and topology selection of the DCX stage, within the context of unfolding-based architectures, revealed several key challenges that necessitate the use of topologies capable of operating near or precisely at resonance. Through detailed analysis and foundational modeling, topologies such as the Series-Bridge DCX (SB-DCX) and the dead-time-controlled Dual Active Bridge with Series Resonant Converter (DAB-SRC) were identified as practically viable candidates for integration with the unfolder.

This dissertation develops and presents modeling tools that enable the effective application of these topologies in unfolder-based systems and in broader scenarios where DCX operation is beneficial. For the SB-DCX topology, design and hardware validation were carried out using a 10 kW prototype integrated with an unfolder, achieving efficiencies up to 97%. Steady-state models based on state-plane analysis have been developed to support the topology design under the unique requirements of unfolder operation. The results are intended for publication in a peer-reviewed journal and are currently undergoing internal review. Furthermore, appropriate design considerations for scaling the modules to higher power levels are presented in Chapter 4.

For the DAB-SRC topology, it was identified that a minimum dead time is required to ensure stable DCX operation with an unfolder while maintaining tolerance to practical mistuning. Mathematical models were developed to predict this minimum dead time requirement, enabling its robust operation not only in unfolding-based systems but also in other applications that demand DCX functionality. These results have been published in a peer-reviewed conference proceeding [41].

Dynamic Modeling of the SB-DCX Topology

The SB-DCX topology has recently gained attention for DCX applications; however, its dynamic modeling has not been thoroughly explored. Dynamic models are essential for designing the converter and analyzing the stability of the complete system. This work investigates several approaches to dynamic modeling of the SB-DCX and proposes the use of half-cycle-averaged modeling. This method yields convenient, scalable, and linear time-invariant (LTI) dynamic models suitable for system-level analysis.

Such models have been largely absent in the existing literature. This dissertation presents intuitive and systematic techniques to derive half-cycle-averaged dynamic models that capture the large-signal behavior of the SB-DCX topology. The proposed model is validated through both simulations and hardware experiments. These results, which demonstrate the accuracy and applicability of the modeling approach, have been published in a peer-reviewed conference [42]. The developed models significantly improve the converter design process and enable comprehensive system-level stability analysis.

Controls to Minimize Sector Distortion

Unfolder-based architectures are susceptible to grid current distortions caused by switching events that occur six times per grid cycle—referred to as sector distortions. This dissertation develops and validates control strategies specifically aimed at minimizing such distortions, resulting in significant reductions in total harmonic distortion (THD).

Active damping is employed to mitigate distortion regardless of its origin, leading to an approximate 50% reduction in THD for a 20 kW system. These results have been published in a peer-reviewed conference [43]. Furthermore, the various causes of sector distortion are systematically analyzed, and a predictive control mechanism is designed to anticipate and suppress distortion before it occurs. The effectiveness of the proposed control method has been demonstrated in another peer-reviewed conference [44], confirming its applicability across a wide range of unfolding-based architectures and addressing one of the key drawbacks of such systems.

8.1 Future Work

Future research efforts are required to build upon this dissertation and enable the development of a complete multi-megawatt system suitable for pilot deployment of the proposed architecture. Key aspects to address include:

8.1.1 System-level Design and Stability Study for Optimized Performance and Reliability

A comprehensive system-level design procedure for multi-megawatt power processing

capacities needs to be developed. This includes sizing the energy-storage interfacing converter and determining the optimal sizing of each DC-DC module interfacing with the EVs. Furthermore, conducting detailed system-level stability analyses (using the proposed SB-DCX dynamic model) of the complete architecture is essential, encompassing interactions with the grid, multiple charging modules, and the DCX stage under varying operating conditions.

8.1.2 DCX Module Failure Analysis for Enhanced System Robustness

A key limitation of the proposed converter architecture is its response to the failure of one or more DCX modules in the DCX stage. In the current design, the failure of a single DCX module can cause the 3-ϕ output bus voltage to rise above the intended level. Since the DCX stage is unregulated, this overvoltage could necessitate shutting down the AC bus if no secondary mechanism exists to control the output voltage. A detailed analysis of such failure scenarios is needed to develop strategies that allow continued operation despite module failures, thereby improving overall system robustness.

8.1.3 DCX Stage Design Optimization to Improve Performance

Optimizing the design of the DCX stage at multi-megawatt power levels for enhanced power density, efficiency, and cost-effectiveness, with consideration of advanced magnetic and thermal management strategies. This includes determining the optimal number of DCX modules in the ISOP configuration, accounting for factors such as switching device technology, series-bridge losses, transformer size and losses, and grid-filter sizing. Additionally, incorporating transformer-level paralleling into the analysis could further improve performance and design flexibility. Finally, performing a comprehensive failure-mode analysis of the DCX stage will help establish system-level operating strategies and control procedures to maintain functionality in the event of a DCX module failure.

8.1.4 Bidirectional DCX Topology Study to Enable Bidirectional Power Transfer

Future work will focus on validating DCX topologies capable of supporting bidirectional power flow. While the current implementation of the SB-DCX topology operates unidirectionally, enabling bidirectional operation requires bidirectional switches and appropriate control strategies. To achieve bidirectional capability with improved efficiency and reduced complexity, alternative solutions that avoid the need for bidirectional switches in the SB should be explored. One promising approach is the use of the DAB-SRC topology with dead-time control, which offers potential for bidirectional operation when combined with an unfolder; however, hardware validation remains necessary to confirm performance under mistuning conditions. Additionally, implementing an SB capacitor, as illustrated in Fig. 8.1, could further reduce the number of required switches in the SB, providing a simpler and more cost-effective solution.

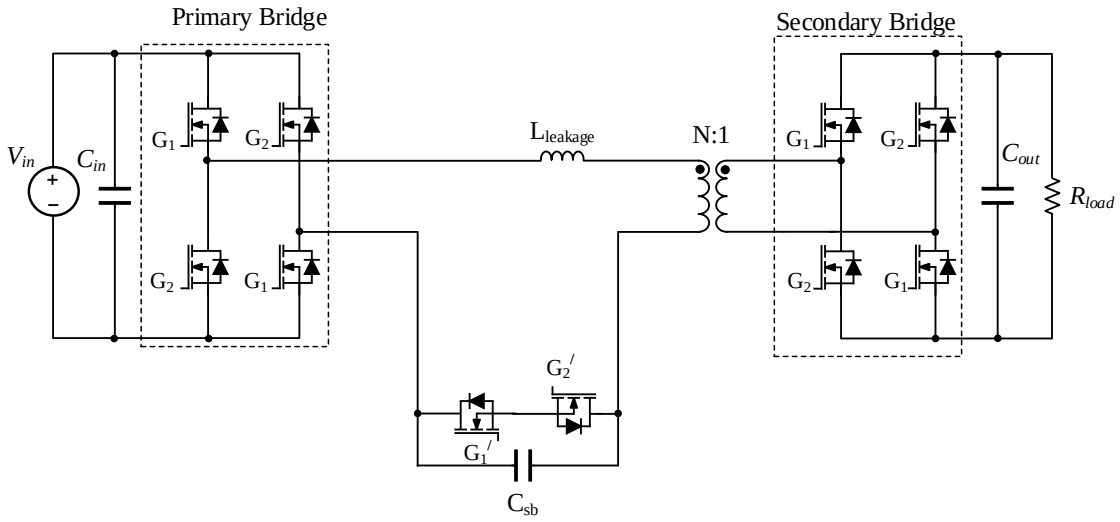

Fig. 8.1: Modified Series Bridge to enable bidirectional operation without increase switch count

REFERENCES

[1] [Online]. Available: https://www.eia.gov/totalenergy/data/monthly/pdf/sec2.pdf

[2] C. Ledna, M. Muratori, A. Brooker, E. Wood, and D. Greene, "How to support ev adoption: Tradeoffs between charging infrastructure investments and vehicle subsidies in california," *Energy Policy*, vol. 165, p. 112931, 2022. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0301421522001562

[3] A. Pamidimukkala, S. Kermanshachi, J. M. Rosenberger, and G. Hladik, "Barriers and motivators to the adoption of electric vehicles: A global review," *Green Energy and Intelligent Transportation*, p. 100153, 2024. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2773153724000057

[4] M. Neaimeh, S. D. Salisbury, G. A. Hill, P. T. Blythe, D. R. Scoffield, and J. E. Francfort, "Analysing the usage and evidencing the importance of fast chargers for the adoption of battery electric vehicles," *Energy Policy*, vol. 108, pp. 474–486, 2017. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0301421517303877

[5] [Online]. Available: https://www.nrel.gov/docs/fy20osti/75705.pdf

[6] B. Borlaug, F. Yang, E. Pritchard, E. Wood, and J. Gonder, "Public electric vehicle charging station utilization in the united states," *Transportation Research Part D: Transport and Environment*, vol. 114, p. 103564, 2023. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S136192092200390X

[7] L. Wang, Z. Qin, T. Slangen, P. Bauer, and T. van Wijk, "Grid impact of electric vehicle fast charging stations: Trends, standards, issues and mitigation measures - an overview," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 56–74, 2021.

[8] S. Srdic and S. Lukic, "Toward extreme fast charging: Challenges and opportunities in directly connecting to medium-voltage line," *IEEE Electrification Magazine*, vol. 7, no. 1, pp. 22–31, 2019.

[9] D. Larcher and J.-M. Tarascon, "Critical review of state of the art lithium-ion batteries for electric vehicles and stationary storage applications," *Energy Environmental Science*, vol. 8, no. 12, pp. 3239–3254, 2015.

[10] N. Nitta, F. Wu, J. Lee, and G. Yushin, "Li-ion battery materials: present and future," *Materials Today*, vol. 18, no. 5, pp. 252–264, 2015.

[11] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii, and I. Batarseh, "A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications," *IEEE Access*, vol. 10, pp. 40 753–40 793, 2022.

[12] H. Tu, H. Feng, S. Srdic, and S. Lukic, "Extreme fast charging of electric vehicles: A technology overview," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 861–878, 2019.

[13] S. Rivera, S. Kouro, S. Vazquez, S. M. Goetz, R. Lizana, and E. Romero-Cadaval, "Electric vehicle charging infrastructure: From grid to battery," *IEEE Industrial Electronics Magazine*, vol. 15, no. 2, pp. 37–51, 2021.

[14] A. Agius, "What's involved in the construction of an ultra-rapid electric car charging station?" Online, n.d., accessed: 2025-07-04. [Online]. Available: https://www.drivezero.com.au/charging/whats-involved-in-the-construction-of-an-ultra-rapid-electric-car-charging-station/

[15] *Electric Vehicle Conductive Charging System—Part 23: DC Electric Vehicle Charging Station*, International Electrotechnical Commission (IEC) Std. IEC 61 851-23:2014, Mar. 2014, standard published March 2014.

[16] X. She, A. Q. Huang, and R. Burgos, "Review of solid-state transformer technologies and their application in power distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186–198, 2013.

[17] F. Wald, H. V. M., O. Gomis-Bellmunt, H. Ji, M. Davoudi, A. Bidram, M. Syed, M. Josevski, S. Brüske, C. Kumar, R. P. Alzola, I. Colak, S. Pannala, M. Liserre, and G. D. Carne, "Applications and services of solid-state transformers in active distribution networks—a critical review," *IEEE Transactions on Smart Grid*, May 2025, early Access; IEEE PES Task Force on Solid-State Transformer Integration in Distribution Grids.

[18] X. She, A. Q. Huang, S. Lukic, and M. E. Baran, "On integration of solid-state transformer with zonal dc microgrid," *IEEE Transactions on Smart Grid*, vol. 3, no. 2, pp. 975–985, 2012.

[19] A. Anurag, S. Acharya, Y. Prabowo, V. Jakka, and S. Bhattacharya, "Design of a medium voltage mobile utilities support equipment based solid state transformer (muse-sst) with 10 kv sic mosfets for grid interconnection," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2018, pp. 1–8.

[20] J. W. Kolar and T. Friedli, "The essence of three-phase pfc rectifier systems—part i," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 176–198, 2013.

[21] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 29–42, 2016.

[22] P. K. Achanta, B. B. Johnson, G.-S. Seo, and D. Maksimovic, "A multilevel dc to three-phase ac architecture for photovoltaic power plants," *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, pp. 181–190, 2019.

[23] D. Das, N. Weise, K. Basu, R. Baranwal, and N. Mohan, "A bidirectional soft-switched dab-based single-stage three-phase ac–dc converter for v2g application," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 1, pp. 186–199, 2019.

[24] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase ac–dc power conversion using series-resonant converter modules and a three-phase unfolder," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9001–9012, 2017.

[25] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Swiss rectifier — a novel three-phase buck-type pfc topology for electric vehicle battery charging," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2617–2624.

[26] F. Wang, G. Wang, A. Huang, W. Yu, and X. Ni, "Design and operation of a 3.6kv high performance solid state transformer based on 13kv sic mosfet and jbs diode," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2014, pp. 4553–4560.

[27] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99.1% efficient 10 kv sic-based medium-voltage zvs bidirectional single-phase pfc ac/dc stage," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 779–797, 2019.

[28] R. Peña-Alzola, G. Gohil, L. Mathe, M. Liserre, and F. Blaabjerg, "Review of modular power converters solutions for smart transformer in distribution system," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 380–387.

[29] S. Roy, M. Joisher, and A. J. Hanson, "A decentralized nonlinear control scheme for modular power sharing in dc-dc converters," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 2798–2805.

[30] F. Gao, R. Kang, J. Cao, and T. Yang, "Primary and secondary control in dc microgrids: a review," *Journal of Modern Power Systems and Clean Energy*, vol. 7, no. 2, pp. 227–242, 2019.

[31] L. Shu, W. Chen, and X. Jiang, "Decentralized control for fully modular input-series output-parallel (isop) inverter system based on the active power inverse-droop method," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7521–7530, 2018.

[32] G. Xu, D. Sha, and X. Liao, "Decentralized inverse-droop control for input-series–output-parallel dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 4621–4625, 2015.

[33] D. Perreault, R. Selders, and J. Kassakian, "Frequency-based current-sharing techniques for paralleled power converters," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 626–634, 1998.

[34] X. Zhao, Y. Lei, H. Wang, X. Quan, and A. Q. Huang, "Design of a medium voltage solid-state transformer based on modular ac-ac resonant converter and an input-series-output-parallel architecture," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 5791–5797.

[35] D. B. Yelaverthi, "Three-phase unfolding based soft DC-link converter topologies for AC to DC applications," Ph.D. Dissertation, Utah State University, Logan, Utah, USA, May 2021, all Graduate Theses and Dissertations, Paper 8015. [Online]. Available: https://digitalcommons.usu.edu/etd/8015

[36] D. B. Yelaverthi, M. Mansour, H. Wang, and R. Zane, "Triple active bridge series resonant converter for three-phase unfolding based isolated converters," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 4924–4930.

[37] J. Huber, U. Drofenik, F. Canales, and J. W. Kolar, "Comparative evaluation of three-phase-unfolder-based mvac-lvdc solid-state transformers," in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2024, pp. 254–263.

[38] M. Mansour, D. B. Yelaverthi, and R. Zane, "Voltage balancing control for input-series-output-parallel three-port series resonant converter modules," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 01–08.

[39] J. D. van Wyk and F. C. Lee, "On a future for power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59–72, 2013.

[40] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimovic, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 101–110, 2016.

[41] S. Poddar and R. Zane, "Estimation of minimum dead time to counter resonance mistuning in dab-src for dcx operation," in *2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2025.

[42] ——, "Dynamic modeling of the resonant series-bridge dcx converter," in *2025 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2025.

[43] A. Zade, C. R. Teeneti, S. Gurudiwan, S. Poddar, M. Mansour, and R. Zane, "Analysis and mitigation of sector transition distortions for unfolding-based grid-tied ac-dc converters," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2023, pp. 1945–1952.

[44] S. Poddar, M. Mansour, A. Zade, and R. Zane, "Investigation of input current distortion at sector transitions in unfolding-based grid-tied ac-dc converters," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 2238–2244.

CURRICULUM VITAE

Sanat R. Poddar

Journal Articles (In Submission)

- S. Poddar, M. Mansour, R. Zane, "Three-Phase Unfolding-based Modular Solid State Transformer with Multi-port Output", in submission
- S. Poddar, M. Mansour, R. Zane, "DCX Module in a Three-Phase Unfolding-based Solid State Transformer with Multi-port Output", in submission
- S. Poddar, R. Zane, "Half-cycle Averaged Dynamic Model for Resonant Series-Bridge DCX Converter using Time Domain Analysis", in submission

Published Conference Papers

- Dynamic Modeling of Resonant Series-Bridge DCX Converter, S. Poddar and R. Zane, IEEE Workshop in Controls and Modeling of Power Electronics (COMPEL), Knoxville, TN, USA, 2025, pp. 2238-2244
- Estimation of Minimum Dead time to Counter Resonance Mistuning in DAB-SRC for DCX operation, S. Poddar and R. Zane, IEEE Workshop in Controls and Modeling of Power Electronics (COMPEL), Knoxville, TN, USA, 2025, pp. 2238-2244
- Investigation of Input Current Distortion at Sector Transitions in Unfolding-based Grid-tied AC-DC converters, S. Poddar, M. Mansour, A. Zade and R. Zane, IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 2238-2244

- Analysis and Mitigation of Sector Transition Distortions for Unfolding-based Grid-tied AC-DC Converters, A. Zade, C. R. Teeneti, S. Gurudiwan, S. Poddar, M. Mansour and R. Zane, IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1945-1952 2004.