THREE-PHASE UNFOLDING BASED SOFT DC-LINK CONVERTER TOPOLOGIES FOR AC TO DC APPLICATIONS

by

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ABSTRACT

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by

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Department: Electrical and Computer Engineering

Battery electric vehicles (BEVs) and plugin hybrid electric vehicles (PHEVs) are more efficient than internal combustion-based vehicles. Adoption of EVs will help reduce the carbon emissions produced by the transportation sector. The charging infrastructure has to grow at a rapid pace to encourage EV adoption. Installing higher capacity fast chargers will help alleviate the range anxiety of battery electric vehicle customers. More public charging stations are required for the full adoption of EVs. Utility power is distributed as 'alternating current.' A battery requires 'direct current' (DC) source to charge it. Hence a power converter that converts AC source to DC source is required to charge an electric vehicle battery.

Public transportation is another sector that is adopting electric vehicles at a fast pace. These vehicles require more power to operate and hence have huge battery packs. These vehicles require ultra-high-power charger to keep the charging time reasonable. A 60 Hz stepdown transformer is required at the facility to use the power. The cost and time to install this heavy transformer will inhibit the setting up a charging station. Power converters than can connect to medium voltage directly will eliminate the need for the step-down transformer saving space and cost.

Commercially available state-of-the-art fast charging converters are adapted from general purpose commercial and industrial application rectifiers. The efficiencies of these converters tend to be lower (around 94%) due to the two-stage power conversion architecture. All the power that flows from the AC utility grid to charge the battery will be processed and filtered through two power conversion stages. Due to the anticipated increase in demand, there is a renewed interest in developing power converter topologies specific to battery charging applications. The objective here is to develop cheaper and compact power converters for battery charging.

This dissertation proposes an innovative quasi-single stage power converter topologies for battery charging applications and direct medium voltage connected converters. The proposed topology fundamentally can achieve higher efficiency and power density than the conventional two-stage based converters. Only one stage requires filtering and incurs power conversion losses. Control burden is usually higher for single stage topologies. Innovative control approaches are presented to simplify the control complexity.

(138 pages)

PUBLIC ABSTRACT

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Dorai Babu Yelaverthi

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ACRONYMS

AC	alternating current
DAB	dual active bridge
DC	direct current
EV	electric vehicle
HF	high frequency
IGBT	insulated-gate bipolar transistor
MOSFET	metal oxide semiconductor field effect transistor
MV	medium voltage
MVHF	medium voltage high frequency
PD	partial discharge
PWM	pulse width modulation
SOA	state-of-the-Art
SST	solid state transformer
TAB	triple active bridge
THD	total harmonic distortion
VSC	voltage source converter
ZVS	zero voltage switching

CHAPTER 1

INTRODUCTION

1.1 Background

Over 2.1 million electric cars were sold in 2019, a 40% year-on-year increase, boosting the total to 7.2 million [1]. This step towards electrification is necessary to reduce carbon emission from the transportation sector. Fast improvements in battery performance and the simultaneous reduction in price has increased the appeal for electric vehicles. The charging infrastructure has to grow with this proliferation of battery electric vehicles (BEVs) and plugin hybrid electric vehicles (PHEVs). Fast chargers (50 kW capacity) are essential to further increase the appeal of EVs. Studies have shown that in areas where drivers have access to 50 kW or higher capacity fast-charging stations, the EV miles traveled increased by over 25%, and helped alleviate the "range anxiety" for BEV customers [2].

Rapid electrification is also expected in light and medium commercial vehicle markets. This is partly driven by the fact that the operational cost of EV fleets has reached cost parity with internal combustion fleets. Government regulation is another major primary factor driving the adoption. Public transportation is another sector that is adapting electric vehicles at a fast pace. Many municipalities are choosing electric buses to add to their existing fleet. Full electric heavy trucks are either announced or already in the market from prominent manufacturers such as Tesla Motors, Nicola Corporation. These large vehicles require more power to operate and hence have huge battery packs. To charge these battery packs in a reasonable time would require ultra-high-power chargers. The charging infrastructure must all grow at a rapid pace to get the unconstrained use of these vehicles.

High power DC fast charging requires power conversion from three-phase utilities (480 V or 208 V) AC voltage to a DC voltage ranging between 50 V to 500 V that can be used to charge the battery. Typically, these applications also require galvanic isolation

and hence require an isolation transformer. The growing need for charging infrastructure also drives the need for more battery charging power converters. This demand creates new opportunities to research further to find more efficient, cheaper, power dense converter topologies.

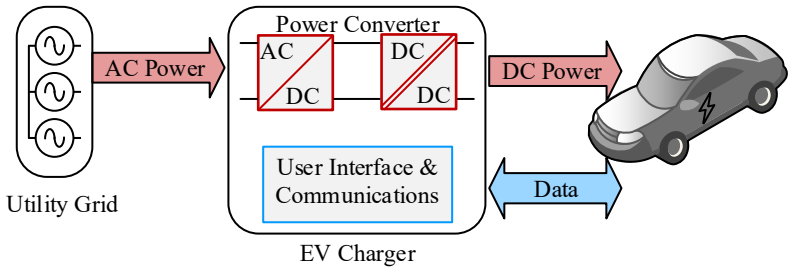


Fig. 1.1: Structure of EV charging system

Commercially available state-of-the-art DCFC converters are adapted from general purpose commercial and industrial application rectifiers. The efficiencies of these converters tend to be lower (around 94%) due to the two-stage power conversion architecture [3, 4]. Due to the anticipated increase in demand, there is a renewed interest in developing power converter topologies specific to battery charging applications. Active research is ongoing to develop cheaper and compact power converters for battery charging applications.

A large EV fast charging station with multiple charging stalls is an ideal candidate for DC microgrid implementation [5]. Microgrids allow the use of local distributed generation and energy storage to reduce the peak demands on the utility grid. Renewable energy sources and energy storage systems which are predominantly DC can be easily integrated to shave peak loads. A typical DC grid based EV charging station implementation is shown in Fig.1.2. Power distribution is done at medium voltage (4.16 kV and higher). A line frequency transformer is used at the facility to step down the voltage for use. A three-phase AC to DC converter is used to rectify the AC voltage to DC. The generated DC voltage is distributed across the station. DC distribution enables simple integration of renewable sources and onsite energy storage. Installing a service line frequency transformer has been reported as a significant cost contributing factor to DC fast charging stations [6].

Direct medium voltage connect AC to DC converters will eliminate the need for the step-down LF transformer. Converters capable of doing this are popularly known as DC Solid State Transformer (SST) or DC Power Electronic Transformer (PET). These converters will eliminate the need for line frequency transformer to step down medium voltage AC to low-voltage DC. The SST unit will perform the functionality of the LF transformer and also the LV AC-DC converter. The DC SST serves as the grid interface converter for the charging station. Single line diagram of a charging station using this approach is shown in Fig 1.3. In [7], it is shown for a 1 MVA SST system the losses are only about half compared to the LFT-based system, and the volume and the weight are reduced to about one third. But developing cost-effective DC SST is still an ongoing research topic and there is still progress to be made before this becomes main stream.

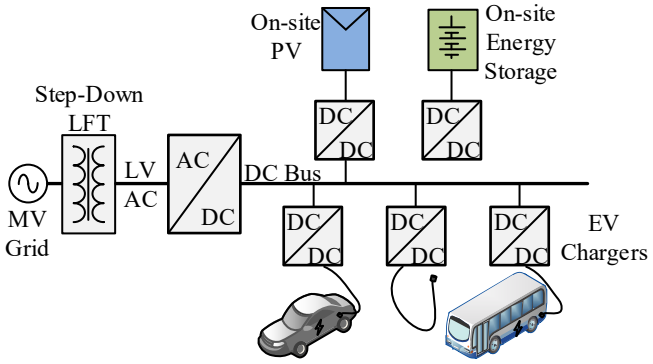


Fig. 1.2: Grid connection through line frequency transformer for the charging station

This dissertation aims at proposing isolated AC to DC converter topologies for DC fast charging (DCFC) applications and grid connected medium voltage converter for DC microgrid type applications. Both these applications have similarities that the input is three-phase utility mains voltage and output is DC. Battery chargers require efficient wide voltage range operation. SST requires efficient wide load range operation.

1.2 Research Objectives

This dissertation objective is to work towards reducing the cost and volume of power

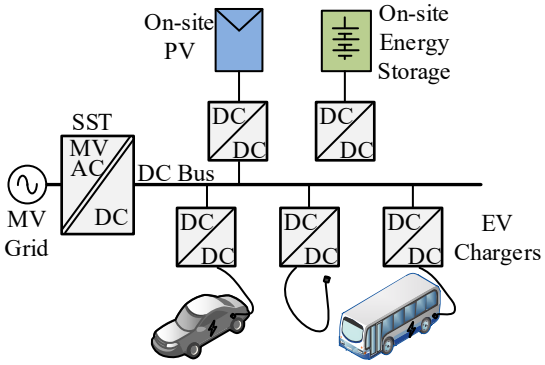


Fig. 1.3: Grid connection through solid state transformer for the charging station

converters required for electric vehicle charging applications. To achieve this objective the focus was placed predominately on reducing the number of power processing stages and also reducing the size of passive components per stage. The solutions used to achieve these objectives are

- to use high frequency transformer for galvanic isolation;
- connect directly to medium voltage distribution grid to eliminate the need for service transformer;
- eliminate the need for large grid-side filters.

1.3 Contributions

Three-phase unfolding based converters help reduce the component size compared to the state-of-the-art approaches. But the implementation methods proposed in literature have fundamental short comings that limit the benefits they are capable of achieving. These shortcomings are identified, and solutions are proposed to improve the performance significantly.

This dissertation proposes a unique approach that improves the performance of the unfolding converters. The control of topologies based on the unfolding approach is another contribution since these new topologies have a unique switching scheme.

Based on the unfolding approach, a new quasi-single stage rectifier topology is proposed that is tailored and optimized for high power battery charging applications, resulting in a 20% reduction in losses and up to 95% reduction in grid filter size. A 2 kW prototype of this novel converter topology is built that serves as proof of concept and technology demonstrator.

The same unfolding approach used for battery charger is also utilized for conceptualizing an SST. Because of the unfolding approach, commercially available low-cost semiconductor devices are used to realize the medium voltage SST. A new galvanically isolated three-port converter is proposed for the DC-DC stage for the unfolding SST. High voltage isolation is one of the significant challenges to achieving a cost-effective SST. A simple yet effective insulation concept is proposed in this dissertation. The approach dramatically simplifies the fabrication process of the isolation transformer.

1.4 Dissertation Organization

- Chapter 2 provides a broad overview of three-phase AC to DC converter topologies. Power converter topologies used in State-of-the-Art battery chargers is discussed. An overview of direct medium voltage grid connected converters is also given.

- Chapter 3 presents the original work on a new approach to implementing three-phase unfolding converters. A first-order comparison of the proposed method versus the State-of-the-Art is given.

- In Chapter 4, the original idea presented in chapter-3, is used to realize a battery charging power converter topology. Switching techniques and control concepts developed for this new topology are presented. Validation of the topology and control concepts are provided through the demonstration of 2 kW battery charger prototype.

- In chapter 5, the concept of medium voltage unfolding is introduced. A new DC-DC topology is proposed. Switching techniques and control concepts developed for this

new topology are presented. The feasibility of this new topology is confirmed through experimental results on a 2 kW prototype.

- Chapter 6 provides the design and fabrication details of a 560 kW AC to DC Solid State Transformer. A unique insulation approach is presented. Hardware results of an 80 kW DC-DC converter module are discussed.

- Chapter 7 summarizes the contributions of this dissertation and provides new research directions.

CHAPTER 2

Review of AC to DC Isolated Topologies

Literature review on isolated three-phase AC to DC topologies is presented in this chapter. Three-phase high power rectifiers are very common industrial and commercial power converter application. Every time a DC load has to be serviced from a utility grid, an AC to DC converter is required. For high power applications, three-phase mains is used and hence three-phase converters are required to provide power to the load.

2.1 Classification of AC to DC Isolated Topologies

Three are numerous applications that require AC to DC isolated power conversion. This application is very mature and well study in literature. Numerous topologies have been proposed and many types of topologies are used in practice based on the application needs. Based on the number of high frequency switching stages the AC to DC topologies can be broadly classified as one of these three approaches:

- Two stage approach
- Single stage approach
- Quasi single stage Approach

The block diagram representation of these three approaches are shown in Fig. 2.1.

2.1.1 Two-Stage Approach

State-of-the-art (SOA) solutions for high power battery charging systems are typically implemented as two-stage systems, comprising a Power Factor Correction (PFC) rectifier input stage followed by a DC/DC converter [5, 8, 9]. This approach allows use of a simple and well-understood AC/DC Active Front End (AFE) rectifier and standard 2-level H-bridge in the DC/DC stage. A 2-level Voltage Source Converter (VSC) is commonly used

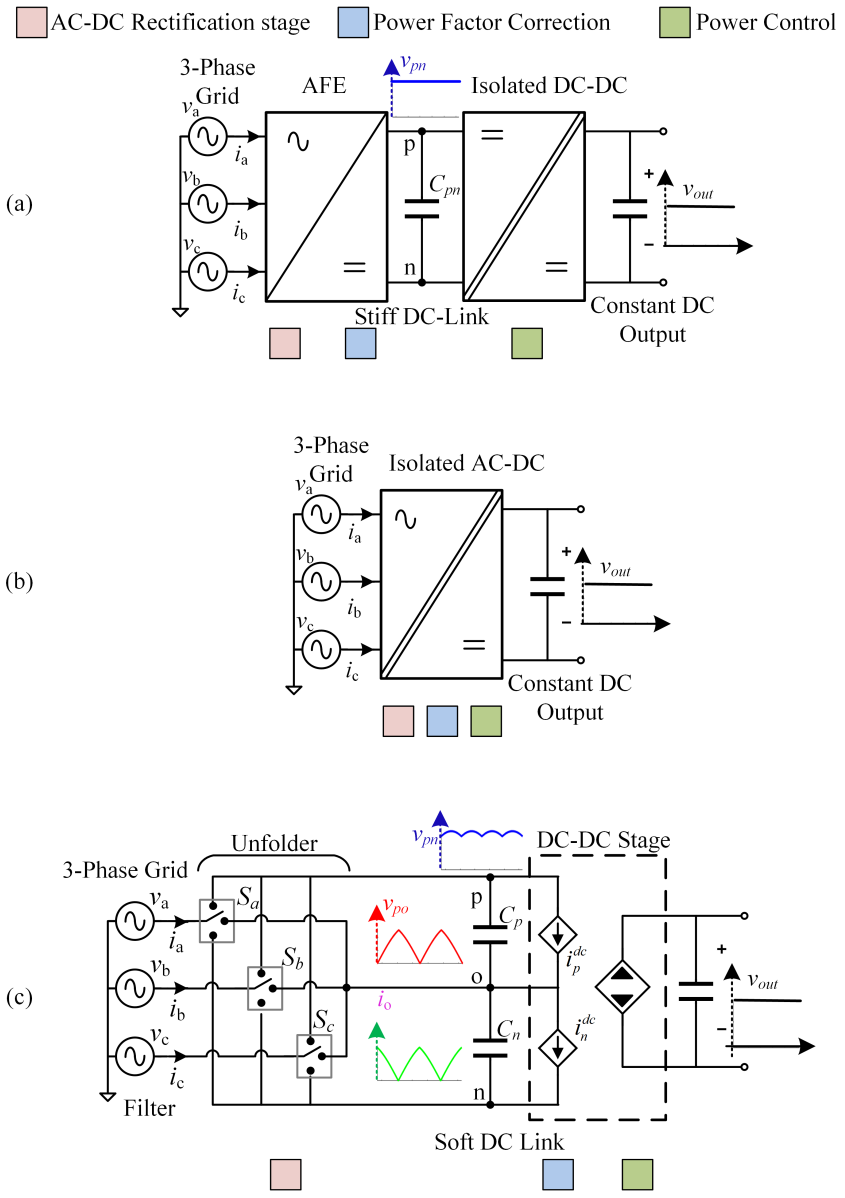


Fig. 2.1: Block diagrams of three-phase isolated AC to DC converter topologies (a) Two-stage approach (b) Single-stage approach (c) Quasi-single stage unfolding approach

as AFE. The VSC is Pulse Width Modulated (PWM) to shape the line currents sinusoidal and maintains a stiff intermediate DC link. The intermediate stiff DC-link capacitor acts as energy buffer. An input LCL grid filter is typically employed to attenuate the harmonics to be compliant to the harmonic injection standards. The cascade DC-DC converter has a high frequency transformer to provide galvanic isolation. The two–stage approach gives tight, highly dynamic control of the output voltage levels to disturbance to grid side voltages.

EV charging applications do not require high dynamic performance since battery charging applications do not have fast dynamics and having a stiff DC-link is not necessary. The state -of-the-art 50 kW chargers have an efficiency of 94% at nominal load [4].

The features of the two-stage approach are:

- Simple control implementation due to the decoupling provided by the intermediate energy storage.
- Can provide stable DC output even during unbalanced grid conditions.
- Relatively high switching losses and reverse recovery losses limit the operating switching frequency (to less than 20 kHz), resulting in large filter size and hence, high cost system mainly due to the required magnetic materials.
- Relative high complexity of the entire power and control circuit (high number of filter elements, separate controls for each converter stage) results in a relatively high realization effort.
- Two-fold power conversion limits the overall system efficiency (94%).

2.1.2 Single-Stage Matrix Converter Approach

In single-stage matrix converter type topologies, the line frequency AC voltage is directly converted to high-frequency AC voltage that is applied across an isolation transformer [10]. The secondary voltage from this transformer is then rectified to the required DC output. These converters have the potential to achieve the highest power density due to reduce number of components. The four-quadrant (4-Q) switches require to be switching at high frequency. Two switching devices are connected in series to realize a 4-Q. Hence two devices conduction loss is encountered per switch. So the selection of these devices will be trade-off between conduction losses and switching performance.

In matrix approach, the back to back device configuration leads to higher parasitic switching loop inductance. This higher loop inductance will limit the device switching speed. The matrix switch network side device switching is critical. At every switching

instant it has to be ensured that there is no open circuit of the HF link inductor and also no short-circuit of the three-phase supply side [11].

Features of single-stage matrix approach are:

- High power density and efficiency is achievable.
- No intermediate storage.
- The PFC control is typically implemented using look up tables to feed-forward the control action [12, 13].
- Output contains low frequency ripple when working with unbalanced grid conditions due to lack of intermediate storage [14].

2.1.3 Quasi-Single Stage Unfolding Approach

In the unfolding based approach, only the DC/DC stage operates at a high frequency, requiring filtering while the input AC/DC rectification stage operates at the line frequency with a soft DC link [15–21]. Since, this rectification has no high frequency switching, the grid-filtering requirement is reduced by 95 %. The uniqueness in the AC/DC rectifier stage is that the line frequency ripple is not filtered but is passed on to the soft DC link. The line to line voltages are just unfolded in to two series connected DC link capacitors. This generates a soft DC link with capacitor voltages as shown in figure. The front-end unfolding rectifier is called Unfolder. The AC to DC stage only rectifies the line voltages. Neither the DC link is controlled nor are the line currents shaped by the AC to DC converter. Hence, this does not require to pulse width modulate (PWM) the rectifier converter. The dc link is soft – time varying/unregulated and the line current shaping task is performed by the high frequency (HF) inverter. The same HF inverter also controls power sent to DC side. Both the tasks of power control and power factor correction (PFC) that require high frequency switching are done in just one converter stage. There are multiple ways to realize the Unfolder, 3-level neutral point clamped (NPC) legs are used in [15] and T-type

unidirectional legs were used in Swiss rectifier [16, 17] and T-type bidirectional legs were used in [18].

Features of quasi-single stage unfolding approach are:

- Can achieve power density and efficiency comparable to that of a single stage power conversion while having the simplicity in control of regular two-stage conversion.
- Has unique advantage for high power converter implementation where multiple DC-DC modules can connect to a single Unfolder.
- The grid-side inductor which is usually the largest component in the rectifier system can be reduced to 5 % of its typical value leading to significant improvements in power density.
- Output contains low frequency ripple when working with unbalanced grid conditions due to lack of intermediate storage [14].

2.2 State-of-the-Art Battery Charging Power Converters

Galvanic isolation is preferred or required to meet the safety requirement of the standards [22, 23] for EV charging when connecting to the utility grid [8, 24]. Reinforced or double insulation is required to meet IEEE EV fast charger standard [23]. The EV body must be connected to earth during charging. When the charger has no internal electrical separation, isolation monitoring is essential, and the battery must be isolated from the car body. Galvanic isolation within the converter will eliminate the need for a separate isolation transformer on the utility side.

Good efficiency over a wide output voltage is a required feature for battery chargers. The open circuit voltage of a battery can change significantly from full state of charge to zero state of charge. Hence, the converter should be able to efficiently operate over wide voltage range. Higher efficiency at full load means lower thermal requirements. This will allow lower cost cooling options or lower volume for cooling. With larger battery packs in bus, trucks and other heavy vehicles the charging rate is usually limited by the charger power

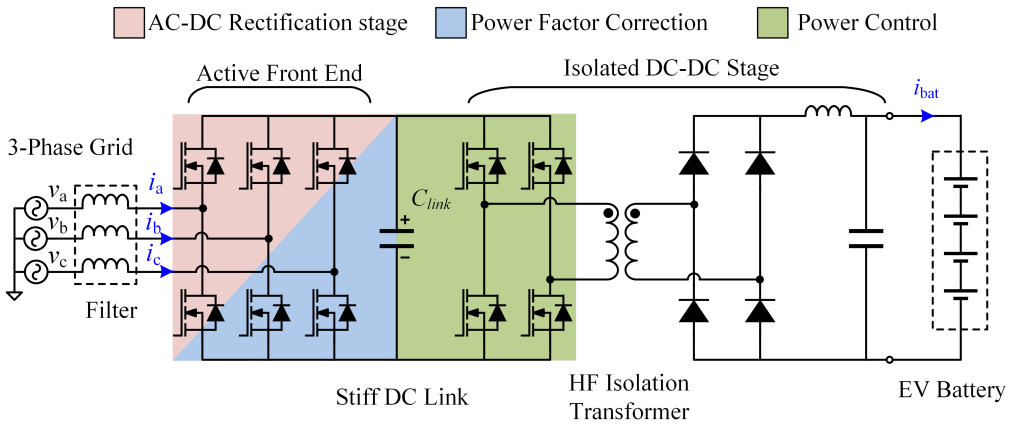


Fig. 2.2: State-of-the-art converter topology for high power battery charging

rating. Also, electric cars with battery packs with high charge rate are being introduced by car manufacturers. These applications demand very high power chargers. Power converter topologies capable for handling high power are required.

Battery charging applications also require a current and a voltage source characteristic of the power supply, which means it has to be able to control the output voltage and to limit the output current in case of a short circuit.

State-of-the-art (SOA) solutions for high power battery charging systems are typically implemented as two-stage systems, comprising a Power Factor Correction (PFC) rectifier input stage followed by an isolated DC-DC converter [5, 8, 9]. This approach allows the use of a simple and well-understood AC/DC Active Front End (AFE) rectifier and standard 2-level isolated H-bridge topologies in the DC-DC stage. Different topologies are possible for the AC-DC and DC-DC stages. A review of some of the possible converter topologies in given in [25]. A 2-level Voltage Source Converter (VSC) is commonly used as AFE. The VSC is Pulse Width Modulated (PWM) to shape the line currents sinusoidal and maintains a stiff intermediate DC link. An input LCL grid filter is typically employed to attenuate the harmonics to be compliant to the harmonic injection standards. The cascade DC-DC converter has a high-frequency transformer to provide galvanic isolation. For high power chargers three-level AC-DC rectifiers are gaining popularity. Due to the three-level

switching, the voltage stress on the devices is lower, switching loss per device is reduced allowing a higher frequency switching. The 3-level switching node also reduces the required attenuation for grid filter.

LLC resonant converter and phase-shifted full-bridge converter are two of the most popular topologies used in this stage [5, 9, 26]. In the topology shown in Fig. 2.2, a phase-shift full-bridge (PSFB) topology is used for the dc-dc stage. PSFB is extensively used for various DC-DC applications and well-studied in literature [27]. Dedicated control ICs are available to implement the control. This topology continues to get attention from researchers and new modulation techniques are being reported that improve the performance of this topology further [28, 29]. 50 kW PSFB designs are reported in [30] for DC fast charging application . A study between single-phase and three-phase is presented in this work.

This topology has the advantage of an easy controllability with a single control parameter (i.e phase-shift between the H-bridge legs) and of a high efficiency due to ZVS where only a small circulating energy is required. The drawback of the PSFB converter is the over-voltage occurring at the secondary rectifier devices due to resonances between parasitic elements. A snubber or a clamp circuit is necessary, as discussed later in this chapter. Multiple effective methods have reported to address the parasitic resonance [31, 32]. PSFB is uniquely suitable for battery charging system requirements. Usually, the system specification requires a current source and a voltage source characteristic of the power supply, which means it has to be able to control the output voltage and to limit the output current in case of a short circuit. This requirement can be easily fulfilled by the PSFB topology. To summarize about PSFB, the topology is simple, reliable, and proven to be effective for battery charging applications.

In two-stage approach the dc-link voltage is actively controlled by the AC-DC stage. This allows to change the DC-link voltage to optimize the converter performance based on the operating point. This additional flexibility provided can used to reduce the voltage gain variation for the DC-DC stage. With narrow voltage gain specification, resonant DC-DC topologies can be effective option. In particular, LLC resonant topology has been explored

for battery charging application. Half bridge LLC topology have been very popular with consumer electronics power supply industry. Low profile planar transformers are required in power supplies for flat TVs. Leakage inductance of these transformer tend to be higher. LLC is preferred topology since this topology effectively utilizes the leakage inductance of the transformer as a circuit element for power transfer. For higher power (>500 W) Full-bridge LLC is preferred because of better utilization of the transformer and reduction in current stress of the components.

Compared to PSFB the output filter capacitor can be larger. Higher capacitance value is required to meet the ripple criteria and large number of capacitors are usually required to meet the ripple current rating. The wide choice of design parameters available in LLC topology make the optimal design of LLC difficult. Full order analysis is involving, fundamental harmonic approximation is typically used which has lower accuracy. Nonetheless, researchers have been exploring to use LLC for battery charging application [33, 34]. Using variable DC-link voltage the voltage range required for LLC is reduced. To reduce the output filter capacitance interleaving of converter modules can be used. There is on-going research on advanced modulation techniques for efficient operation over a wider voltage range [34, 35].

The two-stage approach gives tight, highly dynamic control of the output voltage levels to disturbances on grid side voltages. Simple control techniques are adequate due to the decoupling provided by the intermediate DC link. EV charging applications do not demand high dynamic performance from the converter. Since the reference commands to the charger in both constant current (C.C) and constant voltage (C.V.) output modes of charging are slow varying values, high dynamic performance is not required, and having a stiff DC-link is not necessary. Stiff dc link is usually necessary when energy buffering is required, for example, to provide some hold-up time after grid failure. Since both the converter stages are switching at high frequency, switching loss occurs, and filters are required in the two stages. And usually, the AFE is a hard-switched topology that limits the operating frequency (below 20 kHz) and hence power density. Switching frequency in the range below

20 kHz cause audible noise, and hence noise attenuation measurements are required. The state-of-the-art commercial 50 kW chargers have an efficiency of around 94% at nominal load [4, 25].

Compared to the SOA stiff DC-link, soft DC-link based two-stage rectifier topologies improve the achievable efficiency and power density [14, 15, 36–39]. The improvements are achieved by reducing the duration for which the front-end rectifier is switched at high frequency. For example, in [14] , the devices in the VSC operate at HF for just 1/3rd of the time.

Three-phase unfolding based rectification is one such method that completely avoids high frequency switching in the front-end AC-DC stage. This eliminates the switching loss in the front-end rectification stage and also minimizes the filtering requirement on the utility side [15, 18, 40]. System efficiency and power density can be improved by using three-phase unfolding rectification. The unfolding based converters can meet all the application requirements while greatly improving efficiency and power density. The idea is similar to the popular 1-phase unfolding approach typically used for solar inverters [41–43] but adapted for 3-ph 3 wire systems. A detailed description of the approach is given in the next chapter.

2.3 Direct Medium Voltage Connect Three-phase AC to DC Converters

An emerging application for AC to DC converter is the use of high frequency galvanic isolation for medium voltage grid applications to eliminate the need for distribution step-down transformer [44, 45]. Typically, a line frequency transformer (50 or 60 Hz) is used to scale the distribution level medium voltage to low voltage for commercial and household use. Power electronics based high frequency (HF) galvanic isolation has the potential to improve the power density and efficiency. This HF conversion based voltage scaling unit is known as Solid State Transformer (SST) or Power Electronic Transformer (PET). The power density and efficiency of the system is improved due HF transformer. The additional control features allow to actively regulate the active and reactive power and provide other ancillary utility services.

High power DC loads like EV charging stations and data centers can further benefit

from this approach [3, 7, 46]. These high power loads are usually serviced by medium voltage distribution. A step-down transformer and low-voltage rectifier are used in the conventional state-of-the-art approach. The benefits of using SST technology is significant since the DC output is generated directly by SST eliminating the need for LV rectifier. Both the functionalities of galvanic isolation and three-phase rectification are performed by the SST unit.

Multiple topological approaches are reported in literature to implement an SST [44, 47, 48]. These can broadly be classified into two based on the voltage rating of the semiconductor devices used. First approach is to use high voltage wide band gap (HV WBG) devices with conventional or multi-level topologies and the second approach is multi-module approach with cascaded LV modules.

2.3.1 High Voltage Wide Band Gap Device Based SST

HV WBG devices can be used to realized converters that can interface directly to the MV grid [49, 50]. SiC Mosfet upto 15kV at 20 kHz switching and 25 kV SiC IGBT are reported by device manufacturers [51]. Engineering samples for 10kV SiC mosfet are available from CREE. The HV WBG devices are a promising approach to realize a MV converter. These devices can lead to simpler MV-connected converter by reducing the number of switches and associated isolated gate drivers compared to modular MV converters based on lower voltage devices.

But there are many challenges that should be addressed before these types of SSTs can be commercially deployed [52]. To begin with, the HV WBG device technology itself has not reached the maturity level to engage in large volume production. SiC devices have high power density and small chip area compared to Si devices. Hence these devices have low parasitic inductance and device capacitances. This makes it possible to switch them at high di/dt and dv/dt. Switching a high dc link voltage at fast switching speeds will reduce switching loss [53].But this will also increase the EMI filtering requirements to compensate the detrimental effects of fast dv/dt transitions at the pole voltages. The coupling capacitance to ground can be significant as the size/volume of the passive components and

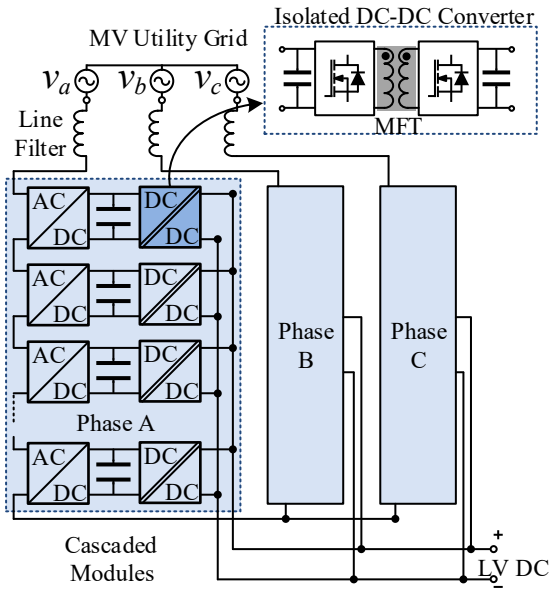


Fig. 2.3: Block diagram of ISOP phase modular SST

heat-sink size will be large for high power converter with low switching frequency (<10 kHz). This high coupling capacitance paired with extreme dv/dt makes the design of the converters very challenging. The phase leg configuration setup is more prone to partial shoot-through due to high dv/dt conditions, and hence leads to more switching losses than expected [54]. The gate drivers needs to be specifically designed to eliminate cross talk while maintaining high isolation requirements.

In summary, extremely high di/dt and dv/dt complicate the system-level design of the converter. MV device protection, MV EMI filtering, insulation under high voltage and high frequency voltage stress still need further research before HV WBG based SST can be commercialized.

2.3.2 Cascaded Two-Stage Low Voltage Converter Modules Based SST

The second approach is a modular approach that uses LV converter modules typically realized using 1200 V or 1700 V devices. These low voltage modules are connected in series on the MV side and in parallel on the LV side. There are a few different structures proposed

in literature [44, 47, 48]. The most popular and well explored is the two-stage conversion approach. Figure 2.3 shows the concept of this modular series input and parallel output structure. AC to DC stage rectifies and regulates a floating DC capacitor voltage and an isolated DC/DC stage uses this floating capacitor and connects to the LV bus through a HF transformer. These isolated DC-DC converters are the key element in the structure. Commercially available reliable LV devices are used in the power modules. Devices from multiple vendors with proven reliable operation are available at this voltage levels. Grid filtering can be reduced by effectively interleaving the switching instants for the AC-DC modules in one series string [55].

The downside of this approach is that the large number of discrete components used in the structure can potentially reduce the size and volume reduction benefits expected from an SST. Especially the capacitors necessary to provide the bulk DC link capacitance form the major share. Large number of auxiliary components are required for isolated communications, sensors, gate drivees, auxiliary power supplies. For all the modules, the subcomponents on the high voltage need to insulate for the full system voltage. This requires high creepage and clearance for these subcomponents to the ground referenced parts. System-level control complexity is higher. Active voltage or power sharing between modules is necessary for stable operation. The front-end AC/DC stage is typically implemented as hard-switching boost-type rectification that leads to a higher DC link voltage than the input AC peak voltage, increasing the system voltage further. Hard switching complicates the EMI and thermal management.

2.3.3 Medium Voltage Unfolding Based SST

Line frequency unfolding can also be implemented at medium voltages. Since the unfolding is done at line voltage frequency (60 Hz), silicon HV IGBTs can be used to realize the unfolding stage. Minimal literature is available on the unfolding approach for medium voltage applications. Most of this report literature is limit to single-phase unfolding. Unidirectional AC to AC SST based on the single-phase unfolding approach is presented in [56]. 5 kV rated silicon diode are used on the MV AC side, and current-fed series

resonant converter switching at 37 kHz is used for the DC-DC stage. The converter is able to soft-switch all devices, and an excellent peak efficiency of 97.8% is reported. Since this is an AC to AC SST, to generate DC output, an LV AC-DC converter will be additionally required. Unregulated 1 MVA, bidirectional, single-phase AC to AC SST based on unfolding is reported in [57]. For the AC voltage unfolding standard press-packed series 4.15 kV IGBT stacks were used. Three-phase unfolding for medium voltage is reported in [58]. But in the implementation reported, the unfolding is just used to converter the three-phase system to a two-phase system. Each of the single-phase stack still realized using two-stage conversion similar to conventional ISOP SST. MV unfolding based SST can reduce the cost of implementation of SST The line frequency unfolding stage can be implemented using silicon high voltage (HV) IGBTs and diodes. LV silicon carbide devices can be used for efficient and power-dense implementation of DC-DC modules. Since the HV silicon devices (up to 6.5 kV) are reliable and low cost, drastic reduction in SST manufacturing cost is expected using MV unfolding approach. This appraoch is discussed in subsequent chapters and a novel implementation of MV unfolding will be presented in chapter 5.

2.4 Summary

A general overview of various AC-DC power conversion approaches is presented. Unique features of each of these approaches are summarized. State-of-the-Art battery chargers are implemented using the two-stage approach. This leads to simpler implementations, but the final designs suffer from lower power density and efficiency. Quasi-single stage unfolding approaches can achieve higher performance than the SOA. This approach is explored in detail for battery charger applications in the next chapter. Using Solid State Transformer for grid interface of higher power DC loads is identified as a promising approach to eliminate the need for a line-frequency service transformer. Both space and time for service transformer installation will be saved. Literature review of this emerging topic is given. The cost of implementation of these converters is still high, and this higher cost limits their adoption. In chapter 5, an unfolding based SST topology is introduced that can significantly reduce the implementation costs.

CHAPTER 3

Improved Unfolding Based Topologies - Proposed Improvements

This chapter begins by discussing the requirements for a battery charging power converter and State-of-the-Art (SOA) power converter topologies used for this application. Then an emerging approach based on soft dc-link, referred to as three-phase unfolding approach, is introduced. The advantages of this approach and the challenges it introduces in the DC-DC stage are discussed. A brief discussion on various implementations reported in the literature is presented. The shortcomings are identified in the published literature, and a novel approach is presented that overcomes these limitations. To compare the performance of the proposed approach with the conventional approach, performance indices are first defined, and these values are provided for both traditional two-stage approach and three-phase unfolding approach.

3.1 3-Phase Unfolding Approach

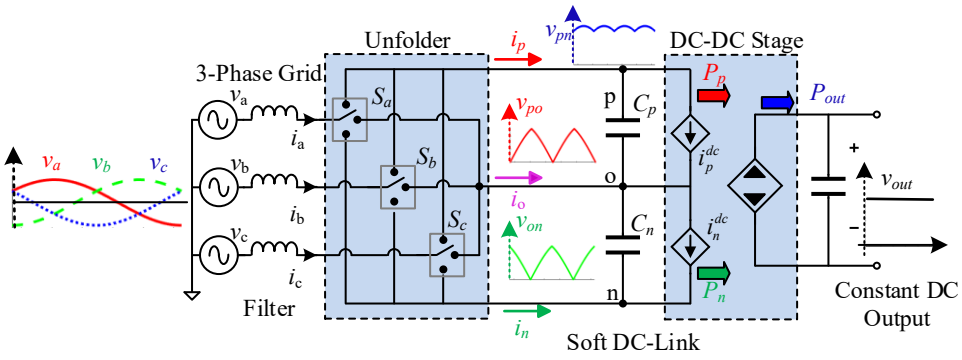


Fig. 3.1: Functional block diagram of 3-phase unfolding based AC to DC topology.

A generalized description of the 3-ph unfolding based converter is explained in this section. The functional block diagram for the unfolding based rectification approach is given in Fig. 3.1. The AC to DC stage, referred here as Unfolder, only rectifies the line

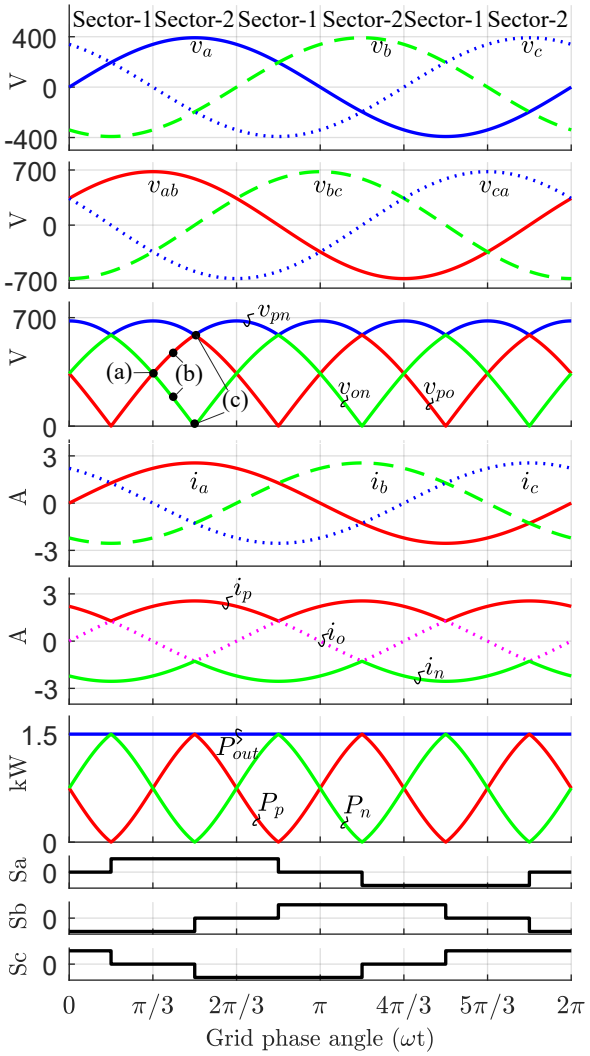


Fig. 3.2: Ideal waveforms for 480 V, 1.5 kW, 3-phase unfolded soft DC-link based converters.

voltages. Neither the DC link is controlled nor the line currents are shaped by the AC to DC converter. Hence, this converter stage does not require to be pulse-width modulated (PWM). The intermediate DC link is soft,time-varying and unregulated. The line current shaping task is performed by the subsequent high frequency (HF) DC-DC stage. The same DC-DC stage also regulates the output bus voltage. The HF transformers in the DC-DC modules provide isolation and voltage transformation. Both the tasks of power factor correction (PFC) and output bus voltage regulation that require high-frequency switching are performed only in the DC-DC converter stage.

Each phase of the Unfolder can be functionally represented by a single-pole triple-throw switch (SPTT). As shown in Fig. 3.1, the SPTT switches S_a, S_b, S_c can be connected to either 'p', 'o' or 'n' terminals of the soft DC-link. The switching states p(1), o(0) or n(−1) (see Fig. 3.2) for these devices are such that the instantaneous highest phase voltage connects to 'p' terminal and instantaneous lowest phase voltage connects to 'n' terminal, and the remaining phase gets connected to the midpoint rail 'o'. The resulting soft DC link voltages v_{po} and v_{on} are piece-wise sinusoidal as shown in Fig. 3.2. The devices in the Unfolder switch at twice line frequency and switching takes place at zero volts across the devices. This essentially means that there are practically negligible switching loss in the Unfolder devices, only conduction loss occur in this stage. These voltage magnitudes are time-varying between 0 to $(\sqrt{3}/2)v_m$. Here, v_m is the line to line voltage magnitude of the utility grid. The currents drawn from the soft DC-links i_p^{dc} and i_n^{dc} by the DC-DC stage have to be controlled such that sinusoidal currents in phase with the voltage are drawn on the grid side. There is no bulk capacitance in the DC-link, capacitor C_p and C_n are designed to just filter out the switching ripple produced by the DC-DC stage. Hence, to achieve unity power factor (UPF) action, the switching average of the currents i_p^{dc} and i_n^{dc} drawn by the DC-DC stage should follow the i_p and $-i_n$. To represent this requirement, the input ports of the DC-DC stage are represented by controlled current sources and the output port as dependent power source. The instantaneous powers P_p, P_n that should be drawn from each soft DC-link is time varying, between 0 to P_{out}. If the DC-DC stage is realized using one converter per DC-link then each of these converters has to be peak power rated to P_{out}, resulting in a peak power rating for DC-DC stage to be twice the average output power.

3.1.1 Practical Implementation

There are multiple ways to implement the unfolder switches. Three-level bridge legs used in some of the popular three-level converters can be used to realize the Unfolder. Few typical 3-level legs are shown in Fig. 3.3. For inverter or bi-directional applications, 3-level active legs are required to realize the Unfolder switches. If the application just requires rectification (power flow from AC to DC) then rectifier variants should be sufficient which

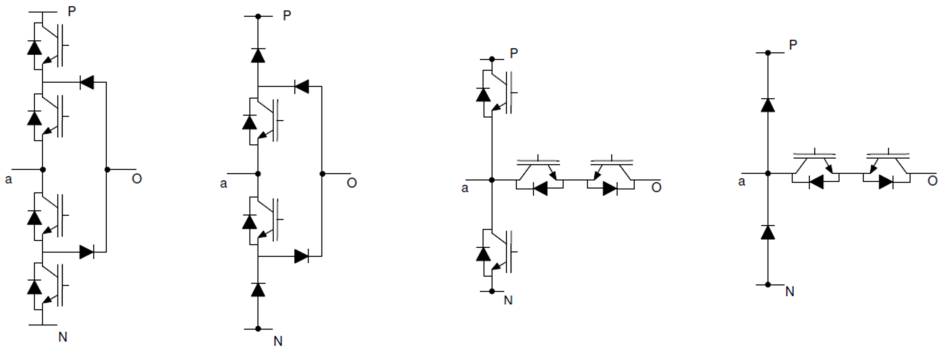


Fig. 3.3: 3-level lags for Unfolder Realization (a) NPC (b) NPC Rectifier (c) T-type (d) T-type Rectifier.

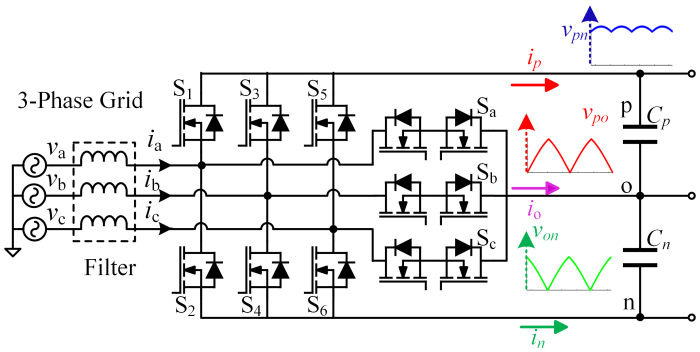


Fig. 3.4: Bi-directional T-type realization of the Unfolder.

have less number of active devices. The T-type bridge has an active bi-directional switch to the dc-link midpoint. Compared to NPC, this leg has two diodes less and also has lower conduction losses. This is because just one device is conducting per leg for the full voltage states. Compared to a 2-level leg the 3-level leg only needs on additional isolated supplies for gate driver when the 4-quadrant device is realized as common Emitter or Source configuration. As an example, Unfolder realization using 3-level T-type active legs is shown in Fig. 3.4. The schematic of this Unfolder looks similar to the 3-level PWM converter but the difference is in the switching pattern and frequency. For high power Unfolder realization, IGBTs will be preferred since the conduction losses are lower for IGBT compared to a MOSFET for the same price point in 1200 V device class.

The DC-DC stage has to work with time-varying power. If the DC-DC stage is realized using one converter per DC-link then each of these converters has to be peak power rated to P_{out}, resulting in a peak power rating for DC-DC stage to be twice the average output power. Each of the soft DC-link voltage has extremely wide voltage swing from zero voltage to $(\sqrt{3}/2)v_m$. Designing a DC-DC converter that can work efficiently with such wide input voltage is challenging. Multiple three-phase converter topologies previously reported in the literature that can be classified under this rectification approach [15,18,59]. A bi-directional isolated topology based on unfolding approach with soft DC-link is presented in [15]. This topology used neutral point clamp 3-level legs for Unfolder and two separate dc-dc converter for each of the two soft dc-link. Series resonant dual active bridge converter is used as the DC-DC converter. Since each of the DABSRC converters have a wide variation in input voltage, the converters tend to be less efficient due to limited zero voltage switching (ZVS) range and higher RMS tank current [60]. To maintain soft switching, advanced triple phase-shift modulation along with active ZVS assistance circuits are used for each switch leg. Due to the lower utilization of components and higher stress on the devices, the efficiency and power density achieved is low.

Another topology called the Swiss Rectifier [59] uses the 3-phase unfolding approach without the use of intermediate soft-dc link capacitors. The Unfolding task is performed by

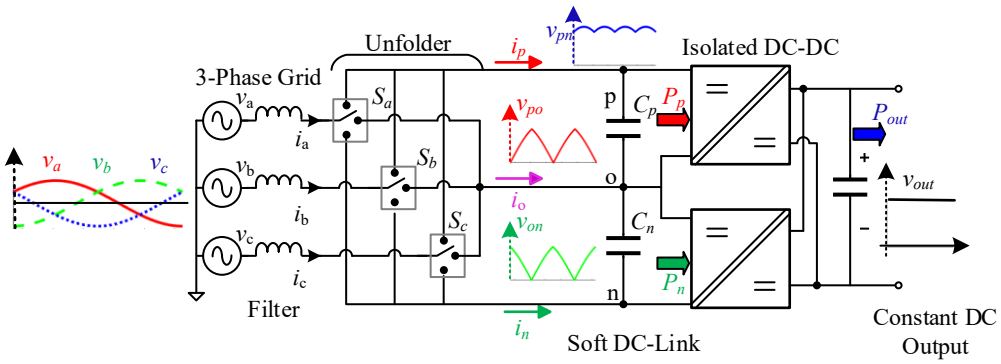


Fig. 3.5: Implementation of 3-phase unfolding approach using two DC-DC converter modules.

the part of the converter authors named as 'Input Voltage Selector' (IVS). 3-level T-type legs were used to realize the Unfolder. The output of the IVS is directly connected to two series buck converters that do both PFC action on grid side and regulate the output voltage. With the recent improvement in the Swiss Rectifier topology proposed in [18] to move the input filter capacitor to the dc side of the IVS, this topology also uses the intermediate soft-dc link unfolding approach. Isolated versions of the Swiss Rectifier without the intermediate soft-DC link are reported in literature [19–21, 61, 62]. These works have replaced the buck converter with an isolated buck-derived DC/DC converter. Two forward converters are used for the DC-DC stage [19]. The secondary side of forward converters feed to the same output filter. The topology is hard-switching. This topology is not very ideal for implementing high power converters since the transformer and device utilization is lower in a forward converter. The topologies reported in [62] and [19] use series connection of transformer secondary windings. The resultant secondary voltage is rectified through LC filter to produce a smooth DC voltage. In all the above topologies, the basic idea is to use two dc-dc converter feeding power to a common DC output. Each of the two dc-dc converters have to be designed for a peak power equal to rated power of the rectifier. This roughly translates to twice as many components in the DC-DC stage compared to the SOA two-stage approach.

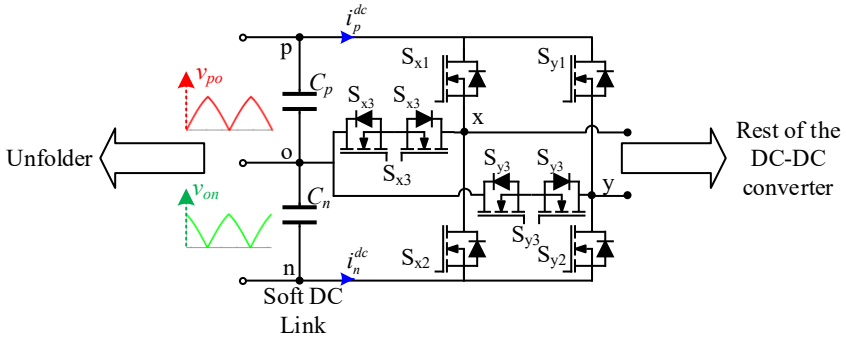


Fig. 3.6: Three-Level Asymmetrical Bridge implementation of DC-DC Stage

3.2 Proposed Three-Level Asymmetrical Bridge Implementation of DC-DC Stage

In the unfolding approach, the front-end AC-DC stage only rectifies the voltage. The DC-DC stage handles the burden of PFC. Hence, the DC-DC stage is required to have the ability to draw different average values of current from the soft DC-link capacitors. To achieve this control objective, two individual DC-DC converters are typically used. In this dissertation, a new bridge topology is proposed to be used on the soft dc-link side of the DC-DC converter. This bridge is referred to as '3-Level Asymmetrical Full Bridge' (3LAFB). The portion 'Asymmetrical' is to convey the asymmetrical DC-link voltages and modulation employed for the bridge, and the portion '3-Level' is to convey that each leg can connect to either of the three nodes of the soft DC-link 'p', 'o' or 'n'.

The schematic of the 3LAFB is given in Fig 3.6. Identifying the fact that the two soft DC-link voltages v_{po} and v_{on} are interleaved and their instantaneous sum has far lower variation, a new bridge topology is proposed that utilizes a combination of the two DC link voltages in one switching cycle to drive the transformer. The bridge also allows for individual control of each soft DC-link. The idea is to use both the input soft DC-link voltages to combine the power at the primary bridge, so that rest of the converter components need to be just designed for the rated output power. The resultant primary voltage will have a low variation in amplitude over the entire grid line cycle, allowing the converter to be designed with higher efficiency. The power from the two soft DC-links is combined in the

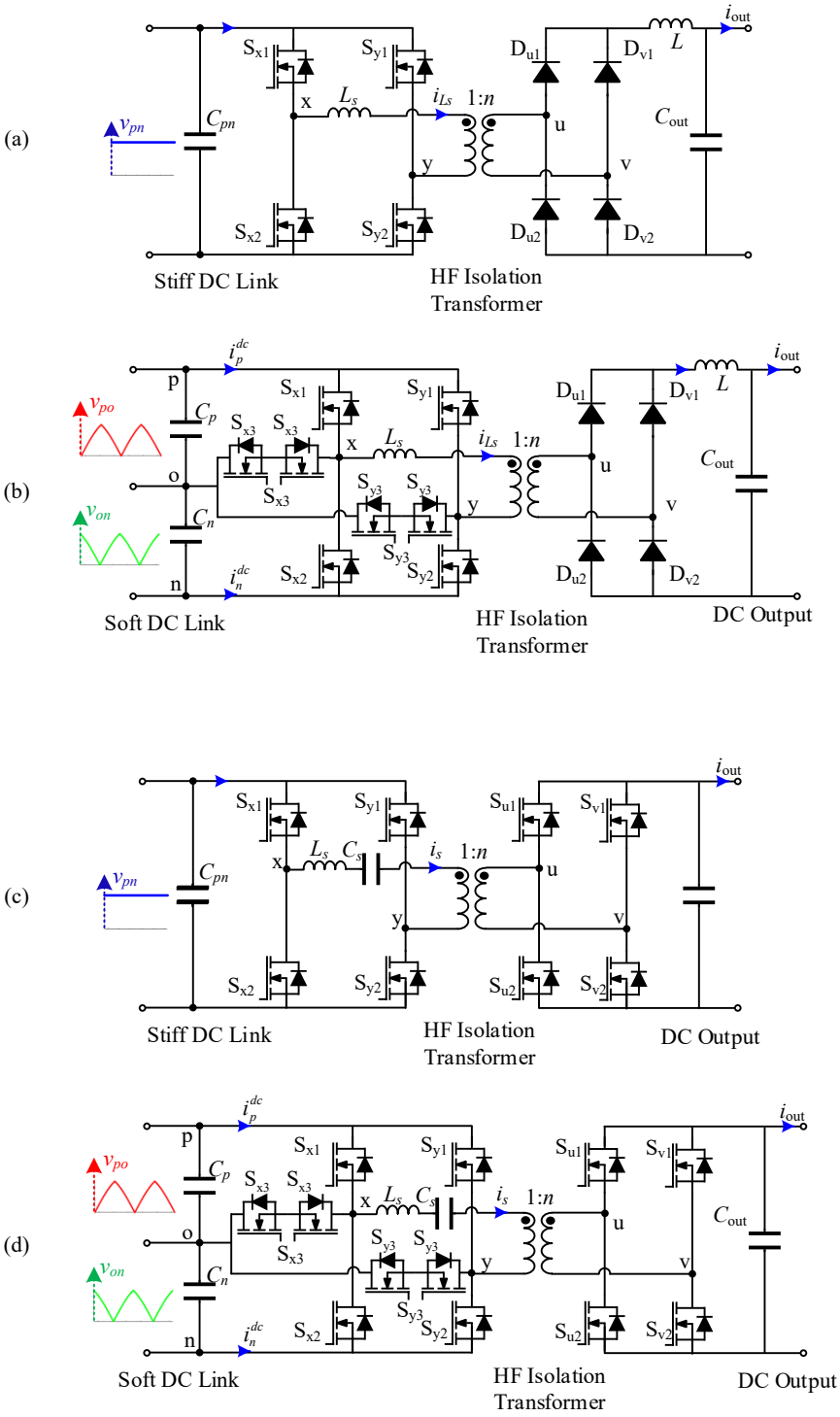


Fig. 3.7: (a) Phase-Shift Full Bridge (PSFB) converter topology (b) 3LAFB variant of PSFB topology (c) Series Resonant Dual Active Bridge (DABSRC) converter topology (d) 3LAFB variant of DABSRC topology.

Table 3.1: 3-level leg switching states and bridge voltages.

Leg-x state	Leg-y state	Pole-x voltage	Pole-y voltage	Bridge voltage (v_{xy})
x_1	y_1	v_{pn}	v_{pn}	0
x_1	y_2	v_{pn}	0	v_{pn}
x_1	y_3	v_{pn}	v_{on}	v_{po}
x_2	y_1	0	v_{pn}	-v_{pn}
x_2	y_2	0	0	0
x_2	y_3	0	v_{on}	-v_{on}
x_3	y_1	v_{on}	v_{pn}	-v_{po}
x_3	y_2	v_{on}	0	v_{on}
x_3	y_3	v_{on}	v_{on}	0

primary bridge. This fundamentally reduces the size of the DC-DC considerably. High-efficiency designs are possible. The 3LAFB bridge has two four-quadrant (4-Q) switches more compare to the conventional H-bridge. These 4-Q switches connect the bridge pole voltage to the mid-point of the soft dc link.

Most DC-DC topologies that have H-bridge on the primary side can be easily adapted to work with Unfolder using the 3LAFB on the primary side. Modified versions of two popular DC-DC topologies (a) Phase-Shift Full Bridge Converter (b) Series Resonant Dual Active Bridge variants are shown in Fig. 3.7. For resonant converter realizations, one resonant tank and one secondary bridge need to be designed as opposed to two resonant tanks and two secondary bridges in the earlier reported resonant topology [15], where power gets combined at the DC output bus.

3.2.1 3LAFB modulation

The modulation approach will have similarities but will also vary from topology to topology. The benefits of increased efficiency and reduced volume will also depend on case to case application.

The three-level legs in the bridge can be used to connect the bridge output poles to either positive (p), mid-point(o), or negative (n) bus of the DC-link. For conventional 3-L H-bridge with equal DC link voltages ($v_{po} = v_{on}$), only 5 unique output states are present

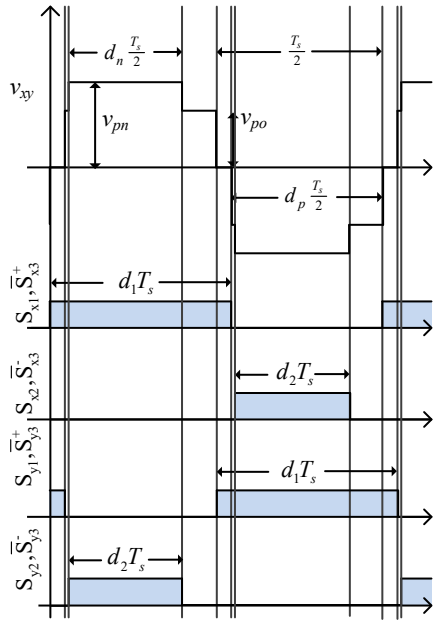


Fig. 3.8: Typical 3-level bridge output voltage waveform with corresponding device states.

with 2 redundant states possible for the half voltages and 3 redundant states possible for zero voltage states. But with unequal dc link voltages at bus 'p' and bus 'n', a total of 7 unique states are possible for the bridge voltage. The bridge voltage for all the possible states of legs 'x' and 'y' are given in Table 3.1. Zero-voltage is the only redundant state with 3 possible realizations $[x_1,y_1]$, $[x_2,y_2]$, and $[x_3,y_3]$. The modulation strategy is an important aspect to keep the efficiency high. Modulation scheme used for the bridge should minimizing 4-quadrant (4-Q) switch conduction and ZVS all the 8 switches in the 3-level legs is proposed. Below are the criteria for selecting the switching scheme:

1. The conduction duration of the 4-quadrant (4-Q) switches S_{x3},S_{y3} should be minimized. Since, each device has conduction loss due to two MOSFETs. Only the zero-states $[x_1,y_1]$ and $[x_2,y_2]$, are to be used.

2. The commutation sequence of incoming and outcoming devices should favor zero-voltage soft-switching.

The 3LAFB will generate voltage waveforms with three unique voltage magnitudes. The relative duration of each of these unique states (d_p and d_n) can be controlled by pulse width modulating the devices. Figure 3.8 shows an example of this waveform and respectively switching states for the devices. d_1 and d_2 are the resultant duty cycles for the devices S_{x1} and S_{x2} respectively. S_{x3}^{+} and S_{x3}^{-} are switched complimentary to S_{x1} and S_{x2} respectively. The same modulation is applied for the second leg -y but are phase-shifted by 180°. This approach ensures to minimize the conduction losses, the duration for which the 4-Q switches conduct are minimized. The 4-Q switches should only be used to conduct the differential current required for PFC on the grid-side. To apply the zero voltage state only the devices in the H-bridge are used. Specific operation of the topologies with 3LAFB are discussed in subsequent chapters.

3.3 Performance Indices for Comparative Analysis

To provide a first order comparison between topologies, one needs to identify performance indices which are independent of operating frequency, system voltage and power rating. Performance indices for semiconductor losses and grid filter size are derived in the subsequent subsections.

3.3.1 Semiconductor Losses:

Power switching devices experience two types of losses: Conduction and Switching losses.

Performance Index for Conduction Stress

For a MOSFET, conduction loss is given by:

$$P_c = I_{ds,rms}^2\{R_{ds,on}\}, \tag{3.1}$$

where $I_{ds,rms}$ is the RMS of current flowing through the MOSFET. $R_{ds,on}$ is the on-state resistance of the MOSFET. Typically, sum of the square of the RMS currents flowing

through the all the devices is used to compare current stress between topologies. But this stress parameter will not provide a fair comparison between topologies when the devices used are rated for different voltages.

$R_{ds,on}$ parameter is dependent on the device blocking voltage rating. Devices with higher blocking voltage have higher resistance for the same silicon die area.

$$Specific\ On-resistance\ [\Omega - cm^2] \triangleq R_{ds,on}A_{die} \propto V_{BV}^{n}, \tag{3.2}$$

where, A_{die} is the die area of the semiconductor device and V_{BV} is the device breakdown voltage and n is between 2.4 to 2.6 for commercial devices. Theoretically, n can be as low as 2. Equation (3.2) can then be reduced to

$$R_{ds,on}A_{die} \propto V_{BV}^{2}. \tag{3.3}$$

Using the relation from (3.3) in (3.2),

$$P_c \propto I_{ds,rms}^{2}V_{BV}^{2}. \tag{3.4}$$

Assuming semiconductor die area per switch is same for the topologies under consideration, normalized performance index for conduction loss is selected as

$$\tau_c = \frac{\sum_{k=1}^{n} I_{ds,rms,k}^{2}V_{BV,k}^{2}}{P_{rated}^{2}}, \tag{3.5}$$

where P_{rated} is the rated power of the converter and $V_{BV,k}$ is decided by the peak voltage stress on the k^{th} device.

Performance Index for Switching Loss:

For a MOSFET, at a given operating voltage, the switching energy (turn-on + turn-off) lost per cycle is a function of the switching instant current (I_{sw}) and can be given as

$$E_{sw}(I_{sw}) = K_0(V_{ds}) + K_1 I_{sw}, \tag{3.6}$$

where, K_0 is a function of switching voltage (V_{ds})) and can be given as

$$K_0(V_{ds}) = Q_{oss}(V_{ds})V_{ds}. \tag{3.7}$$

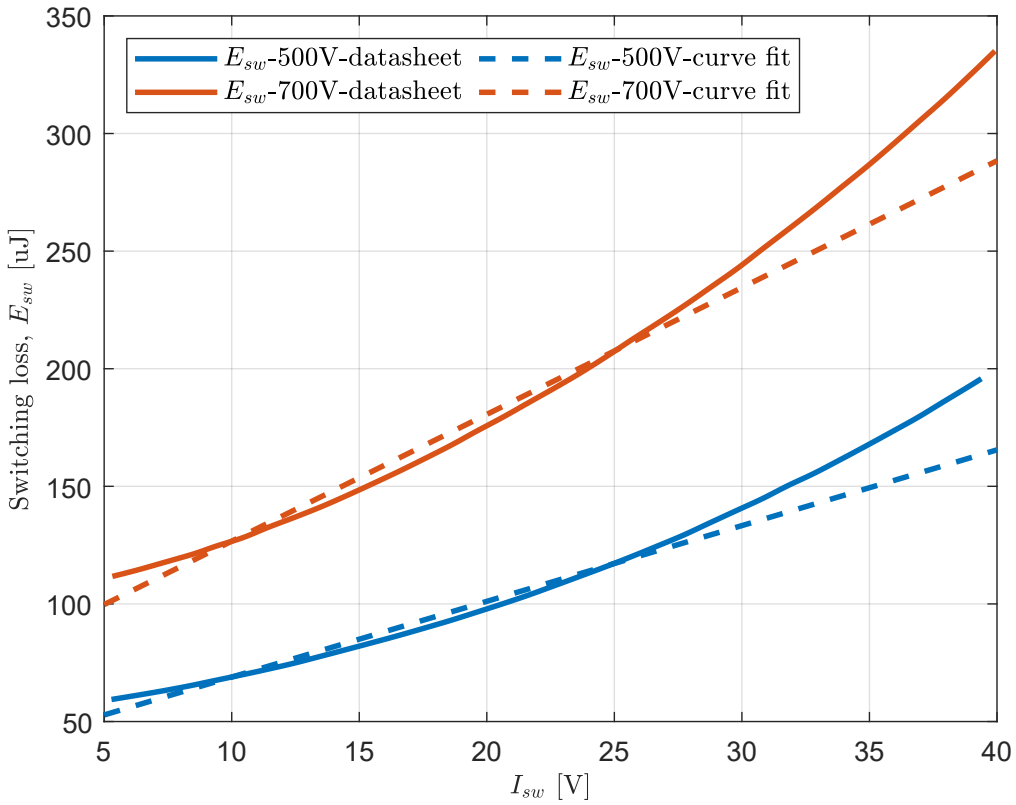


Fig. 3.9: Switching loss data extracted from datasheet

Both K_0 and K_1 are dependent on the operating voltage (V_{ds}) and are constant for a given operating voltage. $Q_{oss}(V_{ds})$ is the charge stored in C_{oss} at a operating voltage V_{ds}.

As observed in eq. 3.7, K_0 is independent of I_{sw} and is usually relatively small compared to the E_{sw} at rated current. Hence, eq. 3.6 can be simplified to eq. 3.8 without introducing significant error

$$E_{sw}(I_{sw}) \propto K_1 I_{sw}. \tag{3.8}$$

E_{sw} for a 1200 V, 40 A MOSFET at switching voltage of 500 V and 700 V are extracted from datasheet and plotted in Fig. From the E_{sw} curves, it can be assumed that switching energy scales linearly with current below the rated current range of the device. Similarly, it is fair to assume that the switching energy scales linearly with switching voltage (V_{ds}) as given by

$$E_{sw} \propto V_{ds} I_{sw}. \tag{3.9}$$

Switching loss (P_{sw}) in a MOSFET operating at a switching frequency (f_{sw}) is given as:

$$P_{sw} = E_{sw} f_{sw}. \tag{3.10}$$

Hence, for a given switching frequency,

$$P_{sw} \propto V_{ds} I_{sw}. \tag{3.11}$$

If the switching frequency is relatively higher compared to the variation in input or output voltages, then

$$P_{sw} \propto < v_{ds}(t) i_{ds}(t) >_{T_{period}}, \tag{3.12}$$

where $<>_{T_{period}}$ represents the average over one periodic cycle. Typically, for a PWM rectifier $f_{sw} \geq 10$ kHz and the input varies at 60 Hz and hence, the above assumption is justified.

Switching loss performance index (τ_{sw}) is taken as the cumulative $< v_{ds}(t) i_{ds}(t) >_{T_{period}}$ across all devices and is given as

$$\tau_{sw} = \frac{\sum_{k=1}^{n} < v_k . i_k >_{T_s}}{P_{rated}}. \tag{3.13}$$

3.3.2 Comparision Between Two-Stage Appraoch and Unfolding Approach

Now that the loss performance metrics have been formally defined, the calculations for first-order comparison of differnet AC-DC topologies can be computed. The topologies that will be considered are the traditional 2-stage (front-end PFC, stiff DC-link, and DC-DC), Unfolder with a 3LAFB DC-DC converter. The analysis is performed for ideal scenario and for a output bridge with inductive filter feeding a battery.

Performance Indices for Two-Stage Approach

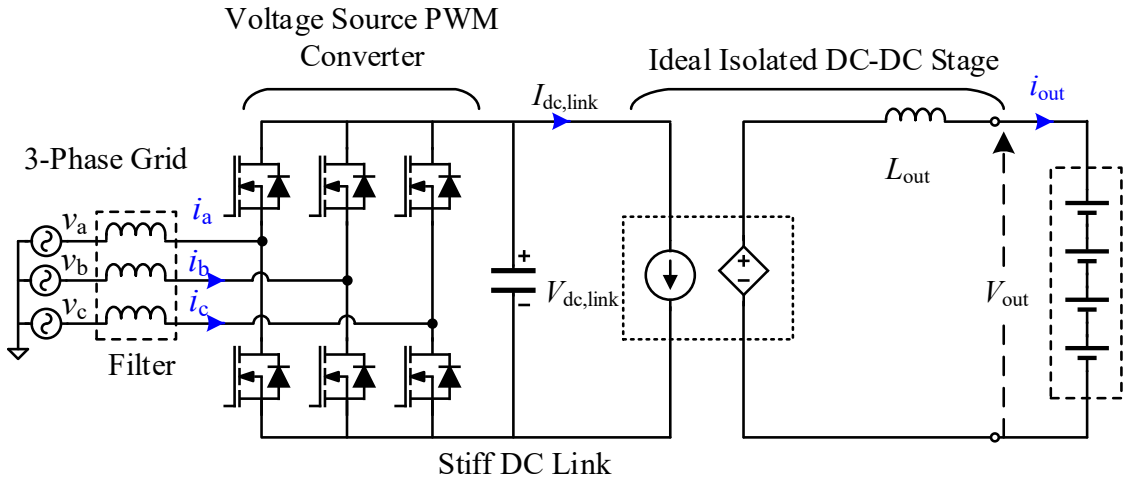


Fig. 3.10: Simplified schematic of the SOA two-stage converter

Consider the traditional two-stage rectification approach that uses a front-end hard-switching PWM converter and a DC-DC to regulate the output power. A simplified schematic of this approach for the performance indices calculation is shown in Fig. 3.10. The DC-DC stage is represented by a ideal current source at the primary side and voltage source at the secondary side. In reality the primary and secondary are implemented as H-bridges. The current in the output filter inductor is assumed to be ripple free for the analysis.

The performance metrics can be computed for both stages independently and then summed together to find the performance metric for the combined system. Lets assume

that the PFC stage is able to operate at UPF. Then the grid phase voltages and currents can be defined as

$$\begin{aligned} v_a &= V_{ph,m}\sin(\omega t), \\ v_b &= V_{ph,m}\sin(\omega t - \frac{2\pi}{3}), \\ v_c &= V_{ph,m}\sin(\omega t + \frac{2\pi}{3}), \end{aligned} \tag{3.14}$$

$$\begin{aligned} i_a &= I_m\sin(\omega t), \\ i_b &= I_m\sin(\omega t - \frac{2\pi}{3}), \\ i_c &= I_m\sin(\omega t + \frac{2\pi}{3}). \end{aligned} \tag{3.15}$$

Where $V_{ph,m}$ and I_m are the amplitude of phase voltage and current respectively. ω is the grid phase angle in radians.

The switching voltage of the 3-phase bridge is the constant DC-link voltage, $V_{dc,link}$; however, the switching instant current is sinusoidal varying over one line cycle. Out of the six devices, three will always be hard-switching. Hence the switching stress can be calculated as

$$\tau_{sw,VSC} = \frac{3\frac{2}{T_{grid}}\int_0^{\frac{T_{grid}}{2}} V_{sw}I_{sw}}{P_{rated}}. \tag{3.16}$$

For space vector modulation,

$$V_{dc,link} = \frac{\sqrt{3}}{M}V_{ph,m}. \tag{3.17}$$

where M is the modulation index of the PWM scheme.

Assuming 100% efficiency from input to output of the converter,

$$P_{rated} = \frac{3}{2}I_m V_{ph,m}. \tag{3.18}$$

Using the relationship between the the DC link voltage and the grid voltage magnitude, $V_{ph,m}$, and the modulation index, M, and the 3 phase power equation, the switching loss performance metric for VSC can be arrived at

$$\tau_{sw,VSC} = \frac{4\sqrt{3}}{\pi M}. \tag{3.19}$$

The switching stress on the VSC devices is a function of modulation index. As the operating moduation index reduces the τ_{sw} increases. A modulation index of 0.95 or lower is typically used for VSC to have sufficient margin. The metric comes out to be $\tau_{sw,AC-DC} = 2.205$ at a optimistic value of $M = 1$. The switching performance metric for the DC-DC stage is simply $\tau_{sw,DC-DC} = 0$ becuase at rated power the DC-DC design should be capable of soft-switching all devices for a high performance design.

For the 2-stage stage design, blocking voltage of the devices is assumed equal to the DC link voltage for both the AC-DC and DC-DC potions of the converter. In practice, the rated blocking voltage of the device is selected to be higher than the voltage it experiences by a reasonable margin (30% to 50% margin). In the VSC, each of the grid currents are always flowing through a single switch so,

$$\begin{aligned} \tau_{c,VSC} &= \frac{3I_m^2 V_{dc,link}^2}{2P_{rated}^2}, \\ &= \frac{2}{M^2}. \end{aligned} \tag{3.20}$$

To calculate the conduction metric for the DC-DC stage the input current is determined from power balance and is given as

$$I_{dc,link} = \frac{\sqrt{3}}{2} M I_m. \tag{3.21}$$

The primary bridge current flows through two devices always so the primary side of the DC-DC converter has the following conduction loss metric,

$$\begin{aligned}\tau_{c,DC-DC,pri} &= 2\frac{I_{dc,link}^2 V_{dc,link}^2}{P_{rated}^2}, \\ &= 2.\end{aligned} \tag{3.22}$$

Given that the isolated DC-DC converter has a turns ratio equal to 1 then the secondary side has the exactly same conduction loss metric as the primary. Hence, $\tau_{c,DC-DC,sec} = 2$.

Summing the switching and conduction losses for all stages, the loss metrics for the two-stage rectifier approach can be concluded as

$$\tau_{sw,2-stage} = \frac{4\sqrt{3}}{\pi M}, \tag{3.23}$$

$$\tau_{c,2-stage} = \frac{2}{M^2} + 2 + 2. \tag{3.24}$$

3.3.3 Performance Indices for Unfolding Approach

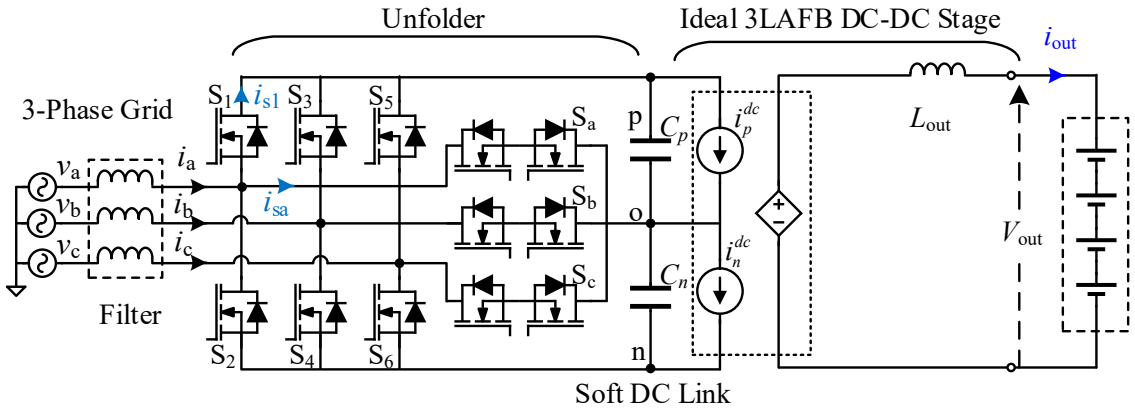


Fig. 3.11: Simplified schematic of the Unfolder with 3LAFB DC-DC converter

The performance indices are calculated here with similar assumptions made for two-stage calculations. The simplified schematic of this approach for performance indices calculation is shown in Fig 3.11. The 3LAFB primary is represented by two current sources and the secondary bridge is represented by the voltage source. The DC-DC stage is assumed to be ideal with 1:1 transformer. Note that the output voltage here will not be same as in the case for two-stage. But this does not effect the performance indices calculations.

The Unfolder commutes at twice the grid frequency and always switches at zero volts, so the switching loss metric for the Unfolder can be considered to be 0. Hence,

$$\tau_{sw,Unfolder} = 0. \tag{3.25}$$

The conduction loss for the Unfolder can be calculated as follows. The RMS currents flowing through the devices that are located in the full-bridge portion of the Unfolder is defined by $I_{s1,RMS}$ and the current flowing through the back-back devices is defined by $I_{sa,RMS}$. These can be calculated as

$$I_{s1,RMS} = I_m\sqrt{\frac{1}{6} + \frac{\sqrt{3}}{8\pi}}, \tag{3.26}$$

$$I_{sa,RMS} = I_m\sqrt{\frac{1}{6} - \frac{\sqrt{3}}{4\pi}}. \tag{3.27}$$

There are six devices that carry the RMS current of $I_{s1,RMS}$ and three 4-Q devices that carry $I_{sa,RMS}$. The blocking voltage for the devices S_1 to S_6 is V_m and for devices S_a, S_b and S_c is $\frac{\sqrt{3}}{2}V_m$. Using the above, conduction loss metric for the Unfolder can be calculated as,

$$\begin{aligned}\tau_{c,Unfolder} &= \frac{(6I_{s1,RMS}^2V_m^2 + (3\times 2)I_{sa,RMS}^2(\frac{\sqrt{3}}{2}V_m)^2)}{P_{rated}^2}, \\ &= \frac{7}{8} - \frac{3\sqrt{3}}{16\pi}.\end{aligned} \tag{3.28}$$

For the 3LAFB DC-DC stress analysis, it is assumed that the design of the converter is such that it is able to ZVS all the devices in the primary and secondary bridges. This assume is fairly true and the designs presented in later chapter validate this assumptions. Since, all the devices soft-switch, the switching stress is zero and switching stress index for the 3LAFB based DC-DC converter, $\tau_{sw,3LAFB} = 0$.

The 4-Q switches in the 3LAFB should conduct the ideal 1:1 transformer current for a duration of $|dp - dn|Ts/2$ in one half switching cycle. The main H-bridge devices will conduct the current during rest of the switching cycle. Assuming the ripple in the output inductor is negligible, the instantaneous RMS currents for a 4-Q switch and main switches are given by

$$I_{sx1,RMS} = I_{out}\sqrt{1 - \frac{|d_p - d_n|}{2}}, \tag{3.29}$$

$$I_{sx3,RMS} = I_{out}\sqrt{\frac{|d_p - d_n|}{2}}. \tag{3.30}$$

The blocking voltage of the main devices is V_m and the 4-Q is $\frac{\sqrt{3}}{2}V_m$. The conduction loss index for the 3LAFB primary bridge ($\tau_{c,3LAFB,pri}$) is then derived as

$$\tau_{c,3LAFB,pri} = \frac{8}{3} + 2\frac{2 - \sqrt{3}}{\pi}. \tag{3.31}$$

For the secondary bridge conduction stress calculations, the block voltage per device is V_m. The output current is always flowing through two device of the secondary bridge. This results in conduction stress index for the secondary bridge to be

$$\begin{aligned} \tau_{c,3LAFB,sec} &= \frac{6I_{out}^2 V_{ph,m}^2}{P_{rated}^2} \\ &= \frac{8}{3} \end{aligned} \tag{3.32}$$

3.3.4 Filter Inductor Performance Index

For the VSC PWM converter a grid filter is required to attenuate the switching harmonics in the phase leg voltage. The Unfolder does not switch the DC-link voltage and hence does not need filtering. But a small amount of filtering is still required to reduce the harmonic content generated by the switching of the back-end DC-DC converter. For the same core loss density and copper loss density, the window area-product [63] of the magnetic core required is proportional to the product of volt-second applied across it and the RMS current rating. The volume of the inductor is proportional to (area-product) raised to 3/4. Since the filter in both the cases have the same RMS current rating, the relative volume reduction expected in the unfolding approach can be given as

$$Relative - volume = \left[\frac{volt - sec_{VSC}}{volt - sec_{Unfolder}}\right]^{3/4}, \tag{3.33}$$

where $volt - sec_{VSC}$ and $volt - sec_{Unfolder}$ are the worse-case volt-second applied across the filter for VSC and Unfolder respectively. For a traditional PWM VSC, the pole voltages are switched between full DC-link voltage, whereas, for the Unfolder, only the voltage ripple in the soft DC-link is applied across the filter inductors which is usually less than 5% of the DC-link voltage. The worst-case volt-sec for VSC and Unfolder is estimated as

$$volt - sec_{VSC} = V_{DC,link}(0.5/f_{sw}), \tag{3.34}$$

$$volt - sec_{unf} = 0.05V_{ph,m}(0.5/f_{sw}). \tag{3.35}$$

$Relative - volume$ from the above three relations can be calculated as

$$Relative - volume = 0.05^{3/4} = 0.106. \tag{3.36}$$

From the first-order volume estimates, the grid filter size for the unfolding approach is only 10% that of the two-stage approach.

Table 3.2: Summary of performance indices for two-stage approach and unfolding based approach using 3LAFB.

Approach	Switching Loss Index			Conduction Loss Index			*Relative-volume*
	AC-DC	DC-DC primary	DC-DC secondary	AC-DC	DC-DC primary	DC-DC secondary	
2-stage	2.205	0	0	2	2	2	1
Unfolding	0	0	0	2	2.837	2.667	0.106

As a summary, the conduction and switching stress performance indices and relative grid filter volumes for both the approaches are given in Table 3.2.

3.4 Summary

In this chapter, State-of-the-Art (SOA) power converter topologies for battery chargers are discussed. A new emerging approach based on soft DC-link, referred to as three-phase unfolding approach, is identified as an ideal approach to realize battery charger topologies. A novel three-level bridge named as Three-Level Asymmetrical Full Bridge is proposed to improve the power density and efficiency of the unfolding based converters. First-order comparison for conduction loss, switching loss, and filter size are provided for the SOA and the unfolding approach with 3LAFB. Compared to SOA, the switching losses are completely eliminated at the cost of 25% increase in conduction losses. Grid filter size is estimated to be reduced by 90% in volume. In the next chapter, the design of a 2 kW battery charger will be presented with the proposed approach.

CHAPTER 4

2 kW Battery Charger Design and Hardware Results

In this chapter, a new power converter topology tailored for battery charging application is discussed. The Three-Level Asymmetrical Full Bridge proposed in the previous chapter is used on the primary side of this converter. The converter is referred to as Three-Level Asymmetrical Full Bridge converter. Operation of the converter is discussed. Design steps for a 2 kW converter are given. A simple approach is suggested for control implementation. Hardware prototype was built to validate the claims of improved power density and efficiency.

4.1 Three-Level Asymmetrical Full-Bridge Converter

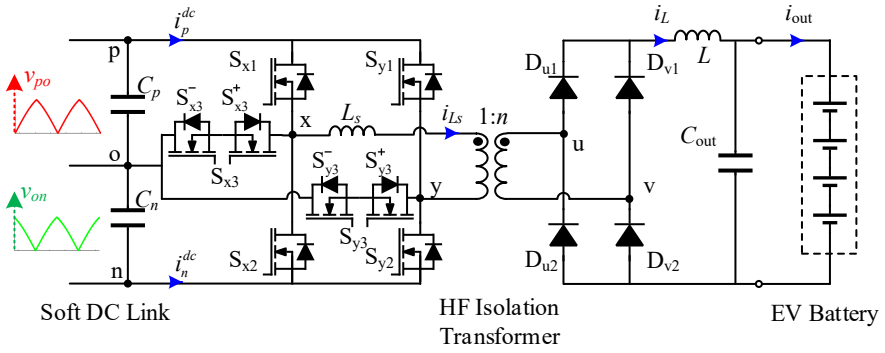


Fig. 4.1: Proposed 3-level Asymmetric Full-Bridge (3LAFB) converter for the dc-dc stage.

Inductive filtered bridges are better at handling wide voltage range. Converter topologies such as PSFB with inductive filter on the secondary bridge are preferred for wide voltage range applications. Since battery charging requires wide voltage range the proposed converter has an inductive bridge at the secondary side. 3LAFB is used on the primary side. Everything down stream to the transformer primary winding in the topology operates similar to a PSFB. The main difference is the high frequency voltage applied on the primary side

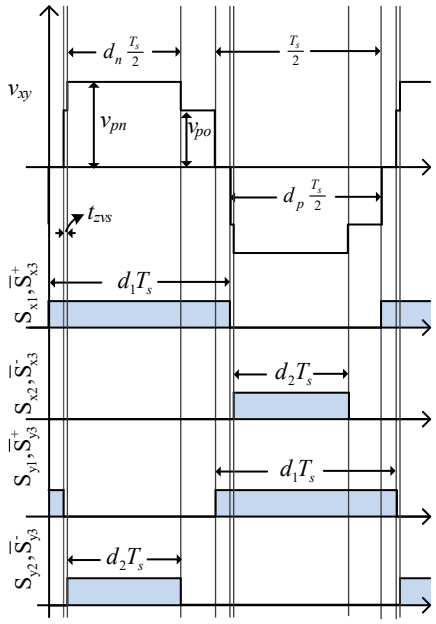


Fig. 4.2: 3-level bridge output voltage with proposed gating sequence.

of the transformer. The 3LAFB generates a multilevel high frequency AC voltage across the primary winding of the transformer. The voltage is scaled by the turns ratio of the transformer (N_t). This scaled voltage is then rectified by the diode bridge on the secondary side of the transformer. Finally, this rectified voltage gets filtered to generate a clean DC output voltage.

The characteristics of the proposed converter are also similar to that of the PSFB converter. Features such as voltage source output characteristics, ZVS switching for all primary devices, ringing between transformer leakage inductance and rectifier diode capacitance, higher voltage stress on the rectifier diodes.

4.2 Operating Principle and Modulation Method

The proposed 3LAFB topology essentially acts as a three-port converter with two series connected input ports and an output port. The 3-L legs simultaneously process power from both the soft dc-links.The bridge generates a high frequency (HF) multilevel voltage waveform v_{xy} as shown in Fig. 4.2. The levels of this HF voltage are either v_{po},

v_{on} or v_{pn}. The relative duration for which v_{po} is used is d_p and v_{on} is used is d_n. These relative times are actively controlled to achieve PFC action and output voltage/current control. The three-level legs in the bridge can be used to connect the bridge output poles to either positive (p), mid-point(o), or negative (n) bus of the DC-link. For conventional 3-L H-bridge with equal DC link voltages ($v_{po} = v_{on}$), only 5 unique output states are present with 2 redundant states possible for the half voltages and 3 redundant states possible for zero voltage states. But with unequal dc link voltages at bus 'p' and bus 'n', a total of 7 unique states are possible for the bridge voltage. The bridge voltage for all the possible states of legs 'x' and 'y' are given in Table 3.1. Zero-voltage is the only redundant state with 3 possible realizations [x_1,y_1], [x_2,y_2], and [x_3,y_3].

The modulation strategy is an important aspect to keep the efficiency high. Modulation scheme for minimizing 4-quadrant (4-Q) switch conduction and to ZVS all the 8 switches in the 3-level legs is proposed. The pulse-widths (d_1 and d_2) of the gate signals of the devices is such that the multilevel waveform is generated while minimize the use of 4-Q switches. An example of this switching pattern is given in Fig. 4.2.

The resulting waveforms in the converter when a multilevel waveforms is applied to the transformer is shown in Fig. 4.3. These waveforms are for ideal conditions, no resistance or parasitic capacitances are being simulated. For the particular scenario shown, d_p is greater than d_n. It can be seen that the average value of i_p^{dc} is greater than i_n^{dc}. Hence by controlling the relative pulse duration of each of the voltage levels in v_{xy}, the relative current sharing between the two soft DC-link can be controlled. The absolute values of d_p and d_n and the instantaneous soft DC-link voltages decide the average value of rectified voltage. Neglecting the duty cycle loss due to L_s, the average input currents and average output voltage can be given as,

$$< i_p^{dc} >_{T_s} = N_t d_p < i_L >_{T_s}, \tag{4.1}$$

$$< i_n^{dc} >_{T_s} = N_t d_n < i_L >_{T_s}, \tag{4.2}$$

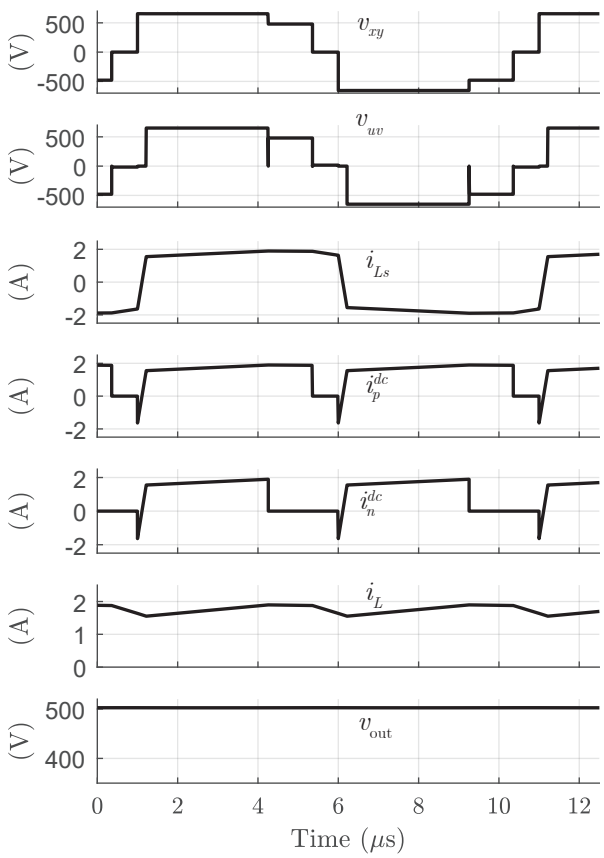


Fig. 4.3: Ideal converter simulation result for operating condition v_p= 480 V, v_n= 175 V, $d_p = 0.87$, $d_n = 0.65$, $v_{out} = 500$ V, $i_{out} = 3.5$ A.

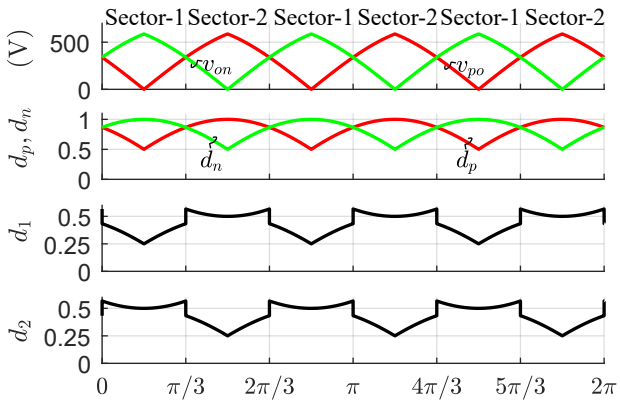


Fig. 4.4: Typical variation of pulse durations d_p and d_n for 3-L voltage waveform, the derived duty cycles d_1 and d_2 of devices S_{x1-3} and S_{y1-3} over one line cycle.

$$< v_{out} >_{T_s} = N_t[d_p < v_{po} >_{T_s} + d_n < v_{on} >_{T_s}]. \tag{4.3}$$

Here,$<>_{T_s}$ represents the average of a variable over a switching period, Ts.

Table 4.1: Control parameters based on the input operating point

	Sector-1	**Sector-2**
Operating condition	$d_p < d_n$	$d_p > d_n$
Top device duty, d_1	$\frac{d_p}{2}$	$\frac{2-d_p}{2}$
Bottom device duty, d_2	$\frac{2-d_n}{2}$	$\frac{d_n}{2}$
Zero-state	$[x_2,y_2]$	$[x_1,y_1]$

As the grid phase angle changes, d_p and d_n have to be adapted accordingly to achieve sinusoidal current shapes. Same set of input operating conditions repeat after 60° grid phase angle and the operating conditions can be divided into two sectors, Sector-1 and Sector-2. The timing diagram given in the Fig. 4.2 is for Sector-2 where, $v_p > v_n$. In these sectors, v_{po} is used for longer duration than v_{on} in the 3L voltage waveform so that $< i_p^{dc} >$ is greater than $< i_n^{dc} >$. Hence, top devices are turned on for longer than bottom devices. The same top devices are also used to generate the zero-voltage states in these sectors, that

is, [x_1,y_1] is for zero-voltage state. The duty cycle d_1 of the top devices is greater than 0.5 in Sector-2. The roles of top switches and bottom switches are interchanged in the other sector. Bottom devices are used to generate the zero-voltage state in Sector-1. This creates a discontinuity in the modulation at the sector boundaries. At the intersection of the two sectors when $v_p = v_n$, the zero-voltage state from the previous sector can be used. The summary of the above control approach and the derivation of duty cycles for the switches is given in Table. 4.1. A typical variation of these parameters are plotted in Fig. 4.4 for visualizing the evolution of these variables with respect to grid angle.

4.3 Zero-Voltage Switching and Duty Cycle Loss

To ensure ZVS for all the devices, the zero-voltage state is distributed asymmetrically over the switching half cycle. The duration of the zero-state, t_{zvs} on the rising edge of the voltage has to be minimized to increase ZVS probability. A t_{zvs} equal to the dead-time used for the complementary devices is recommend. This small zero state on the rising edge is kept to ensure that only one pair of devices commutate at a given time and ZVS of the 4-Q switches are achieved even when the DC-link voltages v_p, v_n are unequal.

The proposed modulation minimizes the conduction of 4-Q switches by avoiding the use of the zero-voltage state [x_3,y_3]. The switching instants are sequenced such that all the devices soft-switch over the entire input voltage range of 60 Hz line cycle. As with conventional PSFB, for complete ZVS of the devices there should be enough energy in the series inductor (L_s) to discharge the device output capacitance. One additional advantage of the proposed duty-cycle modulation is that both the legs have similar switching and conduction losses, unlike in a phase-shifted bridge where the lagging leg devices might experience higher switching loss compared to leading leg devices.

The series inductance (L_s) helps in soft-switching the primary devices. The load range over which the converter completely ZVS depends on the deadtime used and inductance value. Higher is the inductance value, wider is the ZVS load range. But this series inductance reduces the average value of the rectified secondary voltage. The secondary side voltage will remain at zero until the series inductance current (i_{Ls}) equals the instanta-

neous value of filter inductor current (i_L). This can be seen in the ideal simulation provided in Fig. 4.3. With the raising edge aligned modulation, the duty cycle loss (ΔD) can be calculated from (4.4) and the resultant output voltage is given by (4.5).

$$\Delta D = \frac{4nI_{out}L_s}{v_{pn}T_s}. \tag{4.4}$$

$$< v_{out} >_{T_s} = n[d_p < v_{po} >_{T_s} + d_n < v_{on} >_{T_s} - \frac{4L_sI_{out}}{T_s}]. \tag{4.5}$$

For the above calculation, T_{zvs} is neglected and assumed to be zero. The duty cycle loss is a function of output load current and also the total soft DC-link voltage (v_{pn}). As the load current increases the output voltage reduces for the same duty cycles.

$$< i_p^{dc} >_{T_s} = N_t[d_pI_{out} - \frac{Re < i_L >^2}{T_sv_{pn}}], \tag{4.6}$$

$$< i_n^{dc} >_{T_s} = N_t[d_nI_{out} - \frac{Re < i_L >^2}{T_sv_{pn}}], \tag{4.7}$$

The duty cycle loss also effects the current drawn from each of the soft DC-link. The i_p^{dc} and i_n^{dc} considering duty cycle loss are given in (4.6) and (4.7). These equation show that average currents are lower than estimated through ideal scenario given in (4.1) and (4.2).

4.4 2 kW Battery Charger Design and Fabrication Details

A 2 kW battery charger design is given in this section. The input and output specifications for the converter design are given in Table. 4.2. 5% tolerance is assumed for the grid voltage. For the Unfolder, a T-type bidirectional realization is used for this prototype. For battery charging application, unidirectional Unfolder is sufficient. But a bidirectional Unfolder is being fabricated to reuse this a future bidirectional prototype. The schematic of the entire converter consisting of the Unfolder and the 3LAFB converter is shown in Fig 4.5.

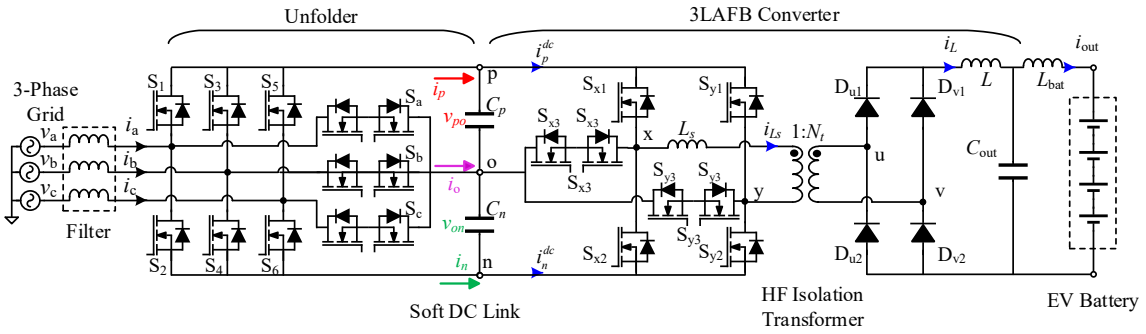


Fig. 4.5: Schematic of the battery charger using the Unfolder and the 3LAFB converter.

Table 4.2: Specifications for the prototype battery charger.

Parameter	**Prototype specification**
Nominal Input	480 V_{AC} RMS voltage
Maximum output power	2000 W
Maximum output voltage	500 V_{DC}
Maximum output current	4 A_{DC}

4.4.1 Transformer Integrated with Series Inductor

3LAFB converter is a buck derived topology. The turns ratio for the transformer is decided by the highest output voltage ($V_{out,max}$) and the lowest input voltage ($V_{pn,min}$). The effective rectified voltage will be at its lowest at rated output current. To meet the peak output voltage rating appropriate turns ratio must be selected. Selecting the turns ratio (N_t) is an iterative method. A worse case duty cycle loss of 10% is assumed. The design is carried out and at the end verified for all the design constraints. Minimizing N_t ensures the converter is operating at its highest duty cycle at rated power. This minimizes the RMS current through the transformer and the switches. The lowest value of N_t that meets the requirement is used. The above constraint can be captured through the (4.8).

$$N_t > \frac{V_{out,max}}{V_{pn,min} D_{eff,max}}. \tag{4.8}$$

From the converter specifications table, the limiting conditions for the transformer turns ratio are identified as $V_{out,max}$=500 V; $V_{pn,min}$=0.95*(3/2V_m); $D_{eff,max}$=0.9. Using

these values, $N_t > 0.9948$. N_t of 1 is finalized for the design.

Effective duty cycle has to be greater than 0.9 to meet the maximum voltage specification. Hence, the duty cycle loss due to series inductor can not be more than 0.1 at the worse operation point. The maximum value of L_s so that the ΔD at worse operating point meets the design criteria can be calculated as,

Transformer leakage inductance is used to realize the series inductance (L_s). Integrating small inductors into the transformer results in total overall size. This also simplifies the mechanical layout, eliminates the losses and space required by the wire terminations, screws or solder contacts. PQ series of cores are considered for the design. With the available Litz wire options in stock, PQ 50-50 core is identified as the ideal size to realize the transformer. 32 turns for primary and secondary windings is selected since this gives a good balance between core and winding loss. Leakage energy stored between the windings is designed to realize the transformer. Various winding patterns are considered and leakage inductances are estimated for each pattern. The estimated and measured values of the fabricated transformer are given in Table. 4.4. The fabrication details are summarized in Table 4.3. The fabricated transformer is shown in Fig. 4.6.

Switch Selection: For a given device technology the Eoss and Coss increase with die size and Rds-on reduce with the die size. Devices with lower R_{ds} tend to have higher switching loss or require higher stored energy in the series inductor to soft-switch. For the current design absolute losses are minimized while also trying to maintain high efficiency over the voltage range. Since the charging profile of the Lithium/ EV battery is such that in CC the current stays constant, this also means that same amount of energy is available for soft-switching during the CC mode irrespective of output power. So, R_{ds} is given more preference while selecting the devices. The device C3M0120100J, 1000 V, $R_{ds} =$ 120 mΩ are used both on 3LAFB bridge and also for the Unfolder. The is in a 7-lead D2 package, the lower inductance of this package makes it more immune to higher di/dt for a given induced voltage spike across the drain to source and also gate to source, allowing for higher turn-off and turn-on speeds for the same overshoot voltages.

Table 4.3: Fabrication details of 3LAFB converters' transformer.

Component	**Fabrication Details**
Core	PQ 50-50, N97 ferrite material
Primary winding	32 turns arranged in 2 sections of 4 layers of 4 turns per layer Wire: 650 strands of 44 AWG with single nylon serving Insulation: 10 mil TEFLON tape between layers
Secondary winding	32 turns arranged in 2 sections of 4 layers of 4 turns per layer Wire: 650 strands of 44 AWG with single nylon serving Insulation: 10 mil TEFLON tape between layers
Clamp winding	28 turns arranged in 2 sections of 3 layers of 5, 5 and 4 turns Wire: 26 strands of 42 AWG with single nylon serving Insulation: 2 mil Kapton tape between layers
Switching Frequency	100 kHz

Table 4.4: Estimated and measured values for the designed transformer.

Parameter	**Estimated**	**Measured**
DC resistance, R_{dc}	98 mΩ	97 mΩ
Resistance at 100 kHz, R_{ac}	0.127 Ω	0.158 Ω
Leakage inductance, L_s	28.7 μH	30.76 μH

The rest of the components of the converter can be designed similar to the two-stage converter approach. The L filter of the secondary bridge is chosen such that the peak to peak ripple is less than 20%. This ensures the converter operates in CCM down to 10% load current. Output filter capacitor of 0.5 μF or higher will result a peak to peak of less than 1%. L_{bat} is used to attenuate the ripple in the battery current. The grid-side LC filter is designed to provide an attenuation of 60 dB or higher at 100 kHz. Summary of selected components is provided in Table. 4.5. The prototype of the full converter is shown in Fig. 4.7.

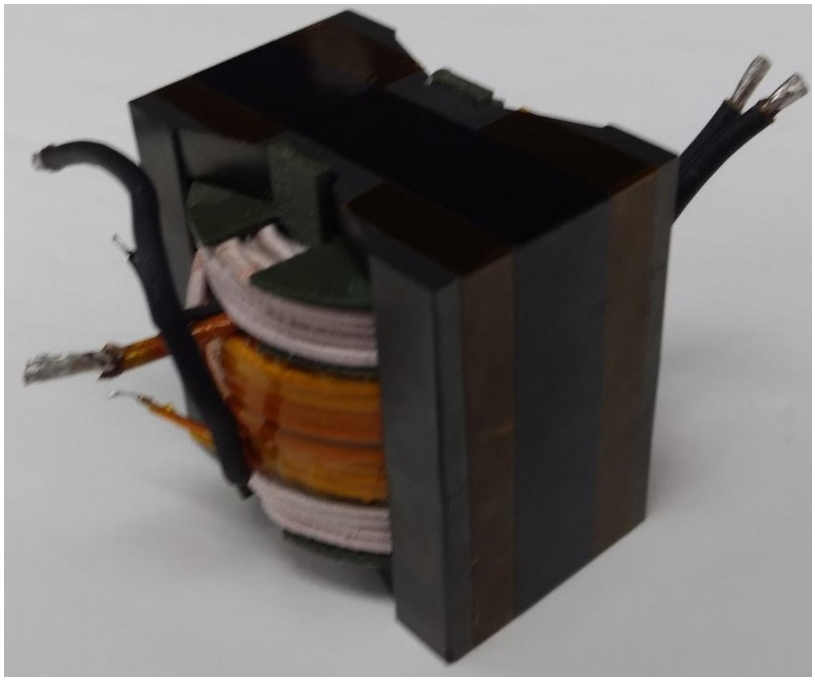


Fig. 4.6: Picture of the fabricated transformer

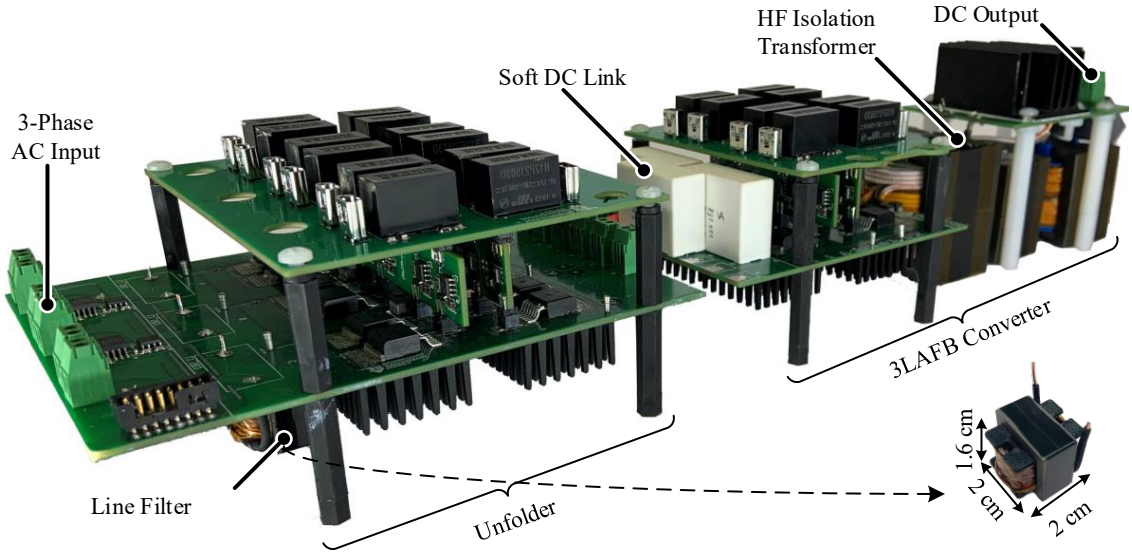


Fig. 4.7: Picture of the 2 kW battery charger designed with the proposed 3LAFB topology.

Table 4.5: Prototype design parameters.

Component	**Design**
MOSFETS	C3M0120100J, 1000 V, 120 mΩ
Rectifier Diodes	C4D08120E, 1200 V, 8 A Schottky diodes
Transformer Turns Ratio, N_t	1:1:0.875 turns ratio (Primary: Secondary: Clamp winding)
ZVS series Inductor,L_s	30.76 µH
Input capacitors, C_p, C_n	1.8 µF, 1100 V, film capacitor
Grid Inductor, L_{grid}	30 µH
Output Inductor, L	1.3 mH
Output Capacitor, C_{out}	1.5 µF, 1100 V, film capacitor.
Battery Inductor L_{bat}	1.495 µH
Switching Frequency	100 kHz

4.5 Hardware Results for DC operating Points

The 3LAFB converter prototype operation is validated at there unique DC link operating points. These three points cover all the possible extremes of the soft DC-link voltages. This validation will confirm that 3LAFB is able to operate efficiently at all the DC-link voltages generated by the Unfolder.

DC power supplies are used to emulate the soft DC-link voltages at three of these operating points. Electronic load is used to set the required load behave at the output. Unfolder is connected and gated to the required state. Duty cycles d_p and d_n are adjusted to get the desired i_p and i_n. Switching waveforms for operating (a) are given in Fig. 4.8. At this point the soft DC-link voltages are equal. The total DC-link voltage(v_{pn}) is at its highest point. Equal amounts of current are required in the soft DC-link at this operating point. Hence the duty cycles are equal. The high frequency voltage generated by the 3LAFB will only have 2-level waveforms. At operating point (b) i_p needs to be higher than i_n and so d_p will be greater than d_n. A distinct 3-level waveform is generated by the primary bridge for this operating point. At operating point (c) v_{on} is close to zero and i_n should be half of

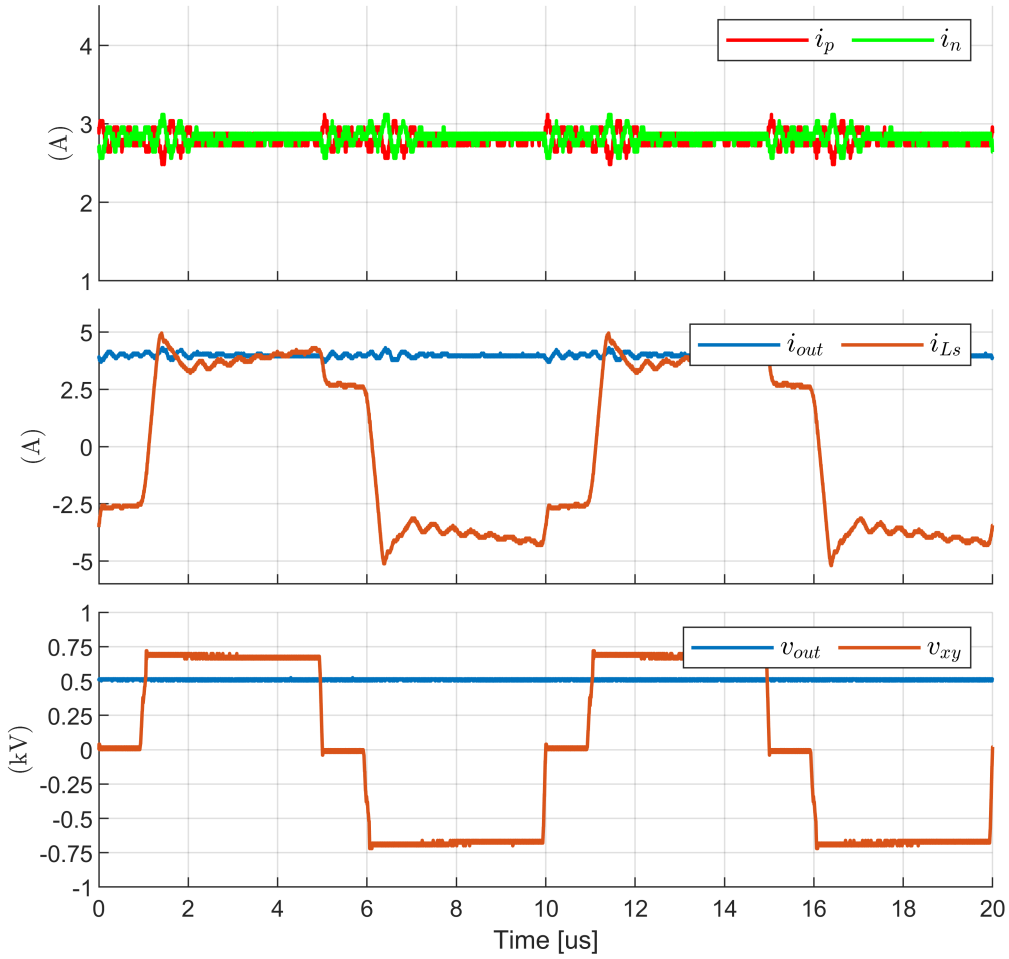


Fig. 4.8: 2 kW experimental waveforms at input operating point (a) v_{po} = 339 V, v_{on} = 339 V.

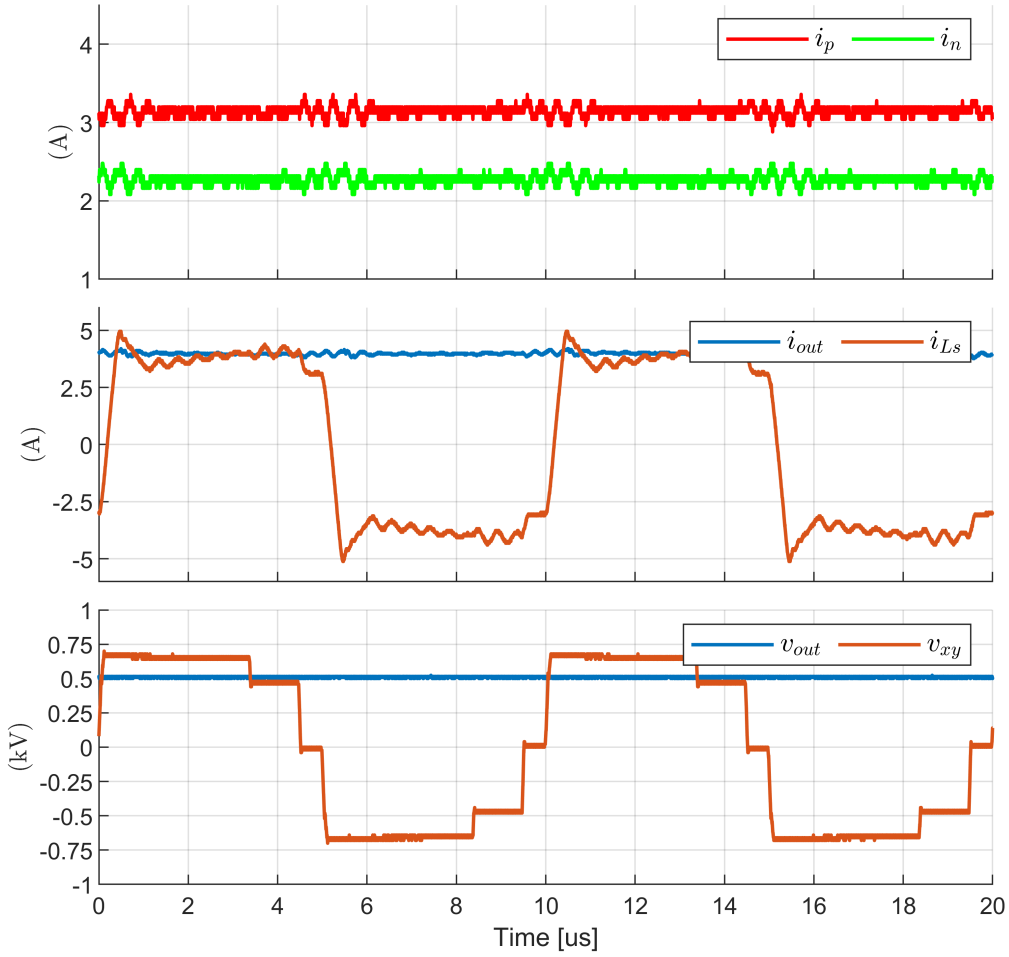


Fig. 4.9: 2 kW experimental waveforms at input operating point (b) $v_{po} = 480$ V, $v_{on} = 176$ V.

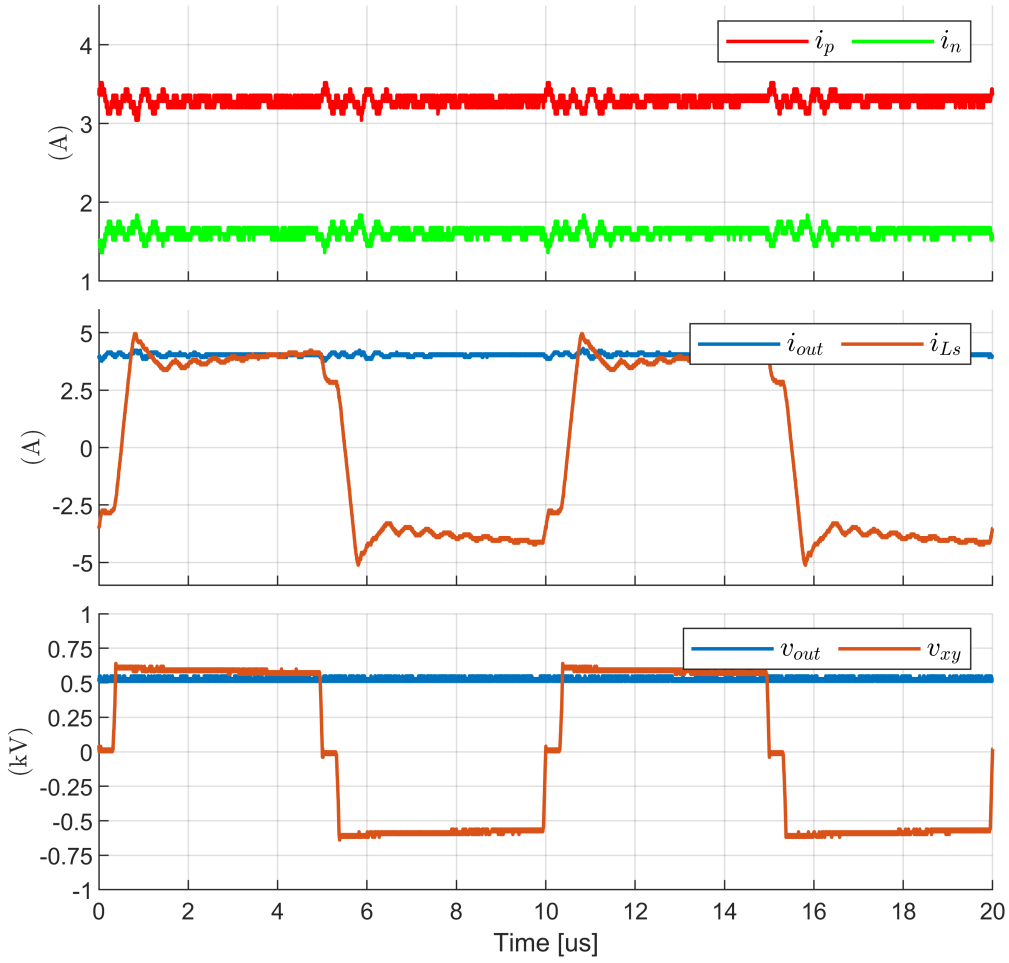


Fig. 4.10: 2 kW experimental waveforms at input operating point (c) $v_{po} = 585$ V, $v_{on} = 6$ V.

i_p . The bridge voltage appears to be a 2-L waveform even though the duty cycles are of different values because of v_{on} being much smaller than v_{po}.

When operating with three-phase source, the input conditions of the 3LAFB converter will be constantly changing. The duty cycles d_p and d_n also change accordingly to adapt the changing grid angle. This changing operating conditions for the 3LAFB will lead to different amount of losses in the components and hence will lead to different levels of efficiency at different grid angles. A detailed efficiency measurement is carried out at these three distinct operating points. At each input condition, different output current and output voltages are set at the load side. Four different output voltages are considered from 200 V to 500 V in steps of 100 V and 9 different output currents are considered from 0.8 A (20% rated) to 4.0 A (100% rated) in steps of 0.4 A (10% rated). The efficiency results for these measured are plotted in Fig. 4.11 to 4.12.

4.6 Closed-Loop Control for Grid Connection

In the proposed topology, one DC-DC converter has to perform both the tasks of output current regulation and input PFC action. These two control objectives are strongly coupled. This can be achieved by directly controlling i_p and i_n through d_p and d_n. But this would require a multivariable control approach. The system dynamics are also complicated to model since it depends on the converter operating point. To simplify the control, a new approach is presented in this section. The approach defines new control variables that are inherently weakly coupled. This allows for the control to be implemented as two independent control loops. Simple linear controllers can be used for control loop implementation.

To achieve the PFC action, the grid currents are indirectly controlled by controlling the soft DC-link currents. At unity power factor operation, the ratio of i_p and i_n has a unique value for a given particular grid angle. This ratio ($k_{p/n}$) is independent of the output load condition and only a function of grid angle. From the ideal current equations, it can be identified that ($k_{p/n}$) is a strong function of d_p/d_n. Hence, by choosing a new control input $d_{p/n}$, defined as in 4.10, a load independent control loop can be arrived at. The transfer

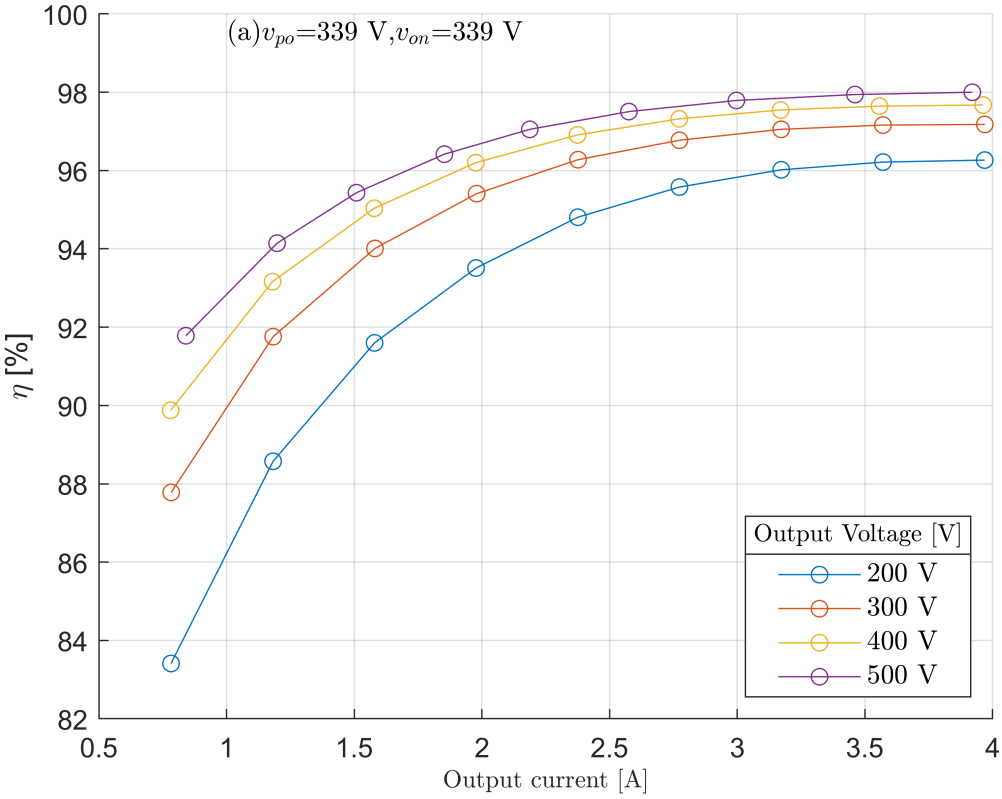


Fig. 4.11: Experimental efficiency data at input operating point (a) v_{po} = 339 V, v_{on} = 339 V.

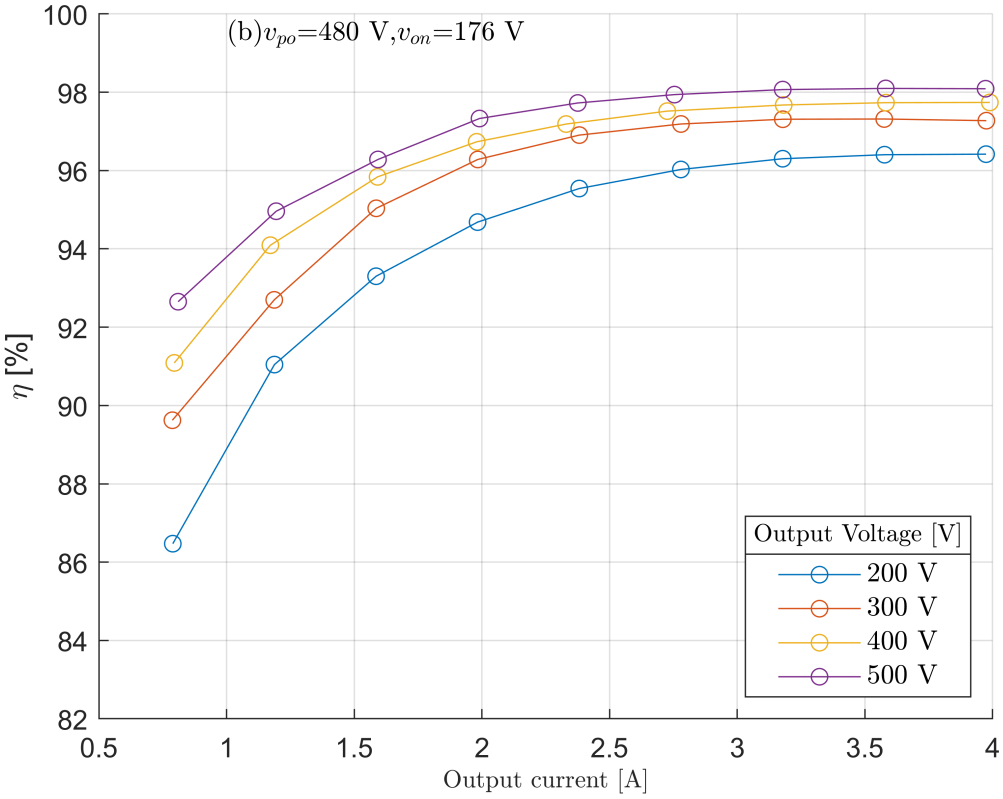


Fig. 4.12: Experimental efficiency data at input operating point (b) v_{po} = 480 V, v_{on} = 176 V.

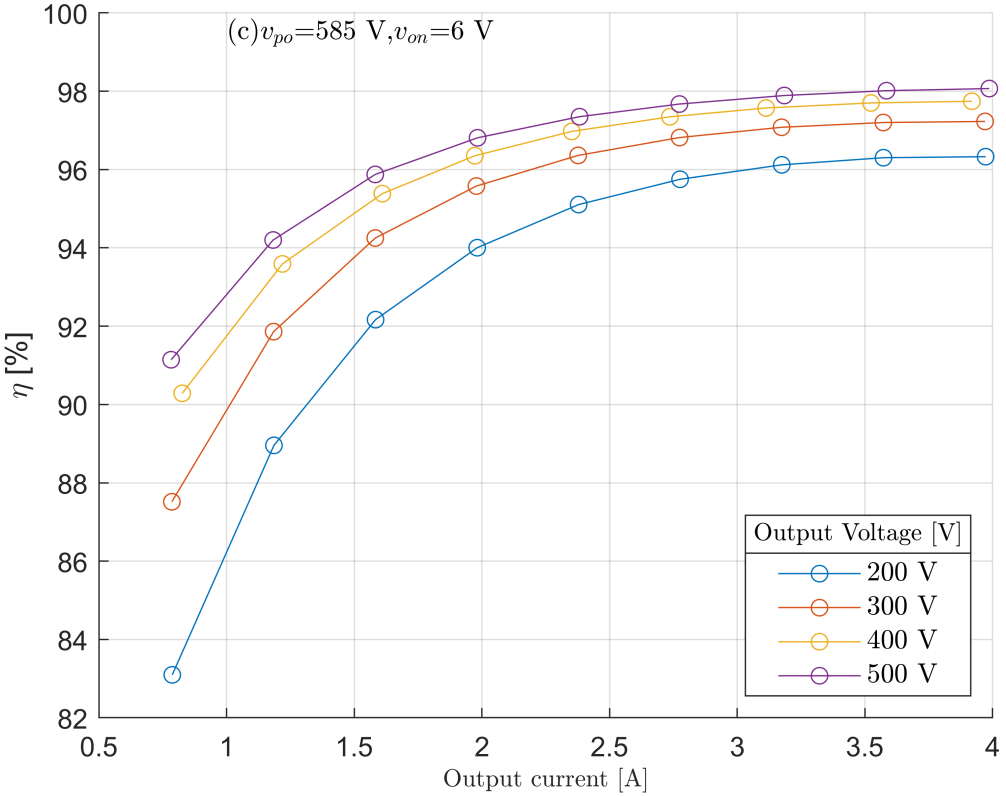


Fig. 4.13: Experimental efficiency data at input operating point (c) $v_{po} = 585$ V, $v_{on} = 6$ V.

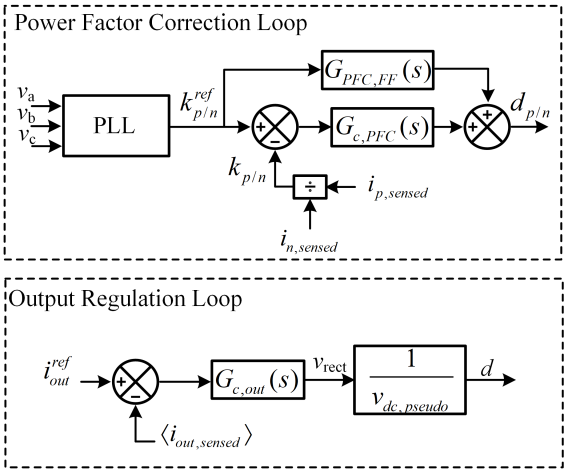


Fig. 4.14: Block diagram of the control implementation for the proposed topology.

function for this loop is given by,

$$G_{PFC}(s) = \frac{k_{p/n}(s)}{d_{p/n}(s)}, \tag{4.9}$$

$$d_{p/n}(s) = \frac{d_p(s)}{d_n(s)}, \tag{4.10}$$

$$k_{p/n}(s) = \frac{i_p(s)}{i_n(s)}. \tag{4.11}$$

The block diagram implementation of this loop is given in Fig. 4.14. A feed-forward term $G_{pfc,FF}$ is added to the control output to compensate for duty cycle loss (ΔD), as estimated in eq(). The PFC loop sets the value of dp/dn to maintain the $K_{p/n}^{ref}$ set by the PLL. This dp/dn has to be respected at every instant in time by the output current loop. This limits the available volt-sec that can be generated by the 3LAFB within one-half cycle. A new variable, $v_{dc,pseudo}$, quantifies the maximum average voltage the 3LAFB can generate. The calculation for $v_{dc,pseudo}$ depends on the magnitude of $d_{p/n}$ is given in the Table 4.6. The new control input (d) is a measure for the absolute values of d_p and d_n and

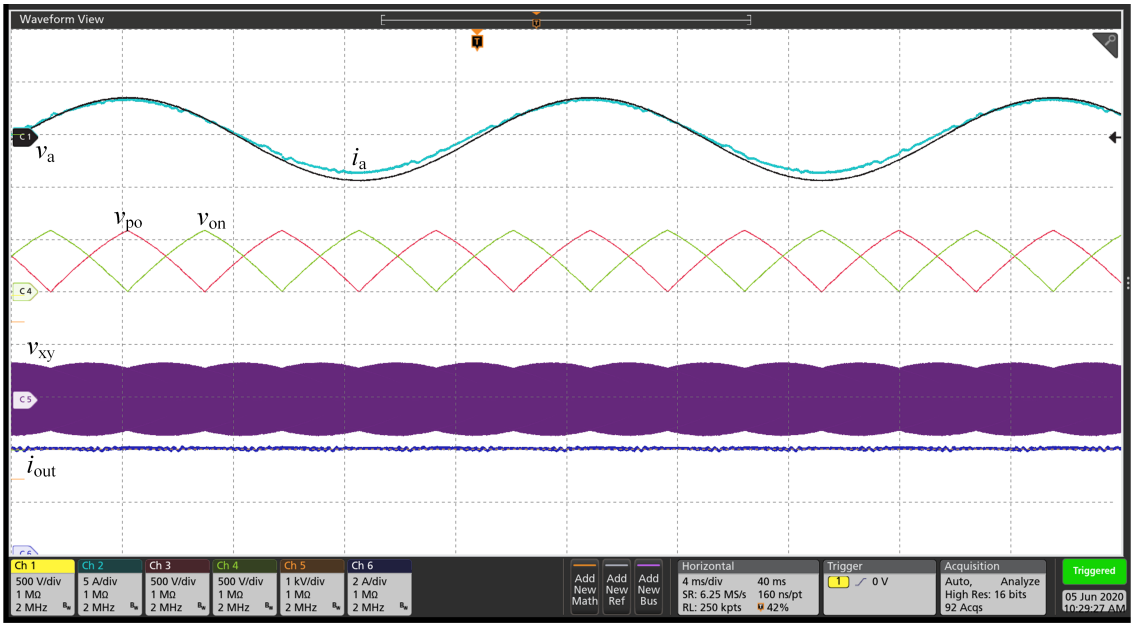


Fig. 4.15: Steady-State experimental result with three-phase AC supply at rated output power of 2 kW.

can by related to the topology as,

$$v_{rect} = d v_{dc,pseudo}. \tag{4.12}$$

Table 4.6: Calculation of d_p and d_n based on the control inputs

Parameter	$d_{p/n} < 1$	$d_{p/n} > 1$
$v_{dc,pseudo}$	$v_{po} d_{p/n} + v_{on}$	$v_{po} + v_{on}/d_{p/n}$
d_p	$d_{p/n} d$	d
d_n	d	$\frac{d}{d_{p/n}}$

4.7 Summary

In this chapter, a new battery charger topology is developed based on the Three-Level Asymmetrical Full Bridge (3LAFB) proposed in the previous chapter. Ideal operation of the converter is presented, and the phenomenon of duty cycle loss is discussed. Modulation for

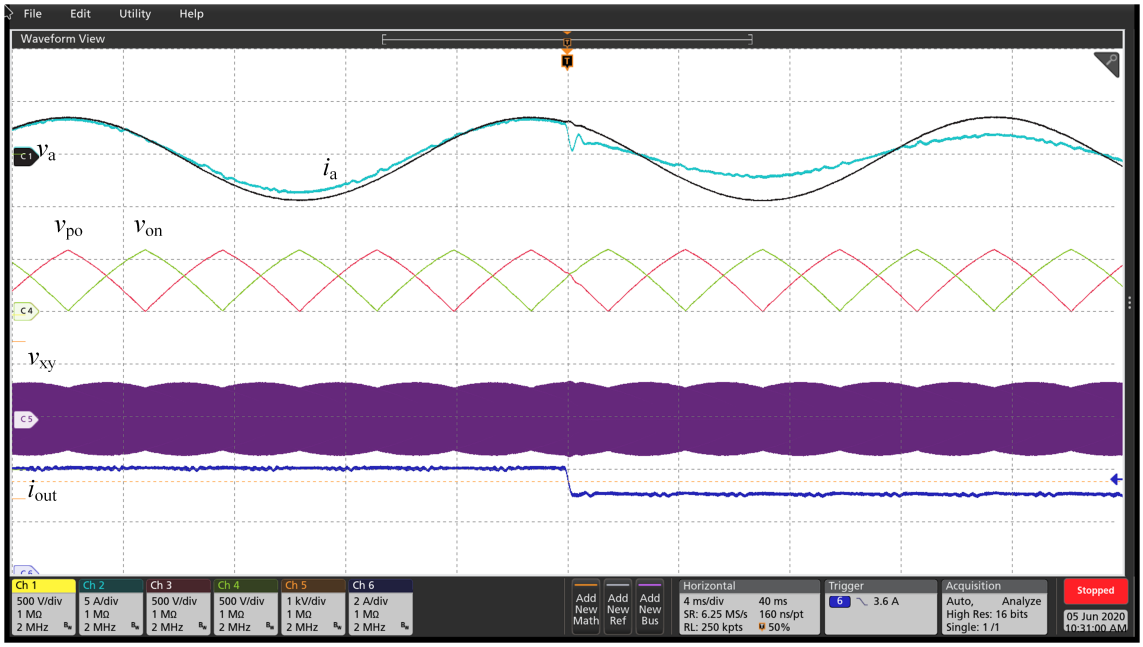


Fig. 4.16: Experimental result for step change of output current from 4 A to 3 A at 500 V output voltage.

3LAFB converter is proposed that allows the converter to soft-switch across all grid angles. The proposed modulation also minimizes the conduction loss of the 3LAFB devices. Design procedure for a 2 kW battery charger is given. Detailed efficiency measurement results at different output voltage and output current loading conditions for three unique input soft DC-link points are given. Simple closed-loop control is proposed for grid synchronization. The proposed control approach uses two independent linear control loops to achieve the power factor correction and output current regulation. Hardware prototype is built, and experimental results are presented to validate the claims of improved power density and efficiency.

CHAPTER 5

Unfolding Based Solid State Transformer

Solid State Transformers (SSTs) are typically realized using multiple converter modules (cells) that are input-series output-parallel arranged. The modules are based on the two-stage conversion approach. In this chapter, the unfolding approach is proposed for the implementation of an AC to DC SST. The proposed approach results in a quasi-single stage SST. This implementation reduces the cost of the SST. A new three-port magnetically coupled DC-DC topology is proposed as the module to be stack in series. Steady-state analysis is done for this new topology. Hardware validation on a 2 kW prototype confirms the feasibility of operation and high efficiency claims. To the end, a closed-loop control structure is provided for one module. Simulation results are provided that validate the approach.

5.1 Proposed Unfolding Based AC to DC SST topology

A generalized description of the three-phase unfolding approach has been provided in chapter 3. Three-phase unfolding based AC to DC converters are proposed in literature for low voltage applications (up to 480 V). This approach can be very beneficial to be applied for medium voltage application. The cost of realizing an AC to DC SST can be reduced. The line frequency unfolding stage can be implemented using silicon high voltage (HV) IGBTs and diodes. These HV silicon devices (up to 6.5 kV) have been widely used in the traction industry for over two decades. These devices can be connected in series to form higher voltage devices. The DC-DC stage is realized using input series output parallel (ISOP) connection of multi DC-DC modules. To achieve high efficiency and power density these modules are built with 1.2 kV SiC devices. These LV devices are readily available in market and have proven to be reliable.

In Fig. 5.1, the block diagram of the proposed topology is shown. The three-phase

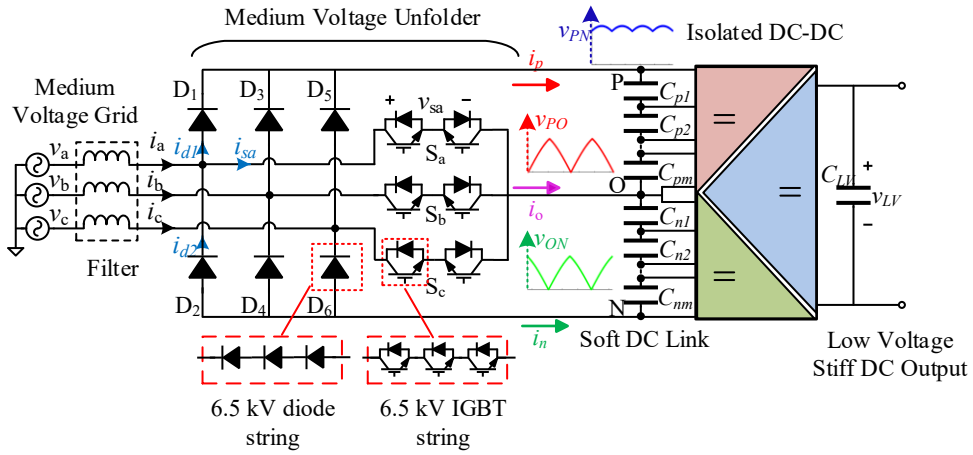


Fig. 5.1: Block diagram of three-phase unfolding based AC to DC solid state transformer

Unfolder is realized using T-type unidirectional legs. For bi-directional applications, the diodes (D1 to D6) should be replaced by IGBTs with anti-parallel diodes. The medium voltage Unfolder just unfolds the line voltage across two series connected capacitors. The effective capacitance of the string is kept low and this results in a soft DC-link. The soft dc-link voltages v_{PO} and v_{ON} are just piece-wise waveforms of the line to line voltages.

The DC-DC stage will regulate the soft dc-link currents i_p and i_n such that grid currents i_a, i_b and i_c are sinusoidal and in phase with voltages. The DC-DC stage consists of series input parallel output connected three-port converters. Triple active bridge series resonant converter (TABSRC) is proposed as the three-port converter building block of the dc-dc stage. One capacitor from P-string and one capacitor from N-string feed the inputs for a triple active bridge. The block diagram of the ISOP DC-DC three port converter is shown in Fig. 5.2. The schematic of each DC-DC module is shown in Fig. 5.3. The TABSRC has good utilization and soft switching over entire line cycle. This allows the TABSRC to be designed to achieve high efficiencies.

The operation details of one module are discussed later in the chapter. The duty cycle of the primary bridges and phase-shifts with respect to the secondary bridge are used to regulate the output power per module. The output power is actively shared between the two input ports to maintain voltage balance across the capacitor string. Higher power density

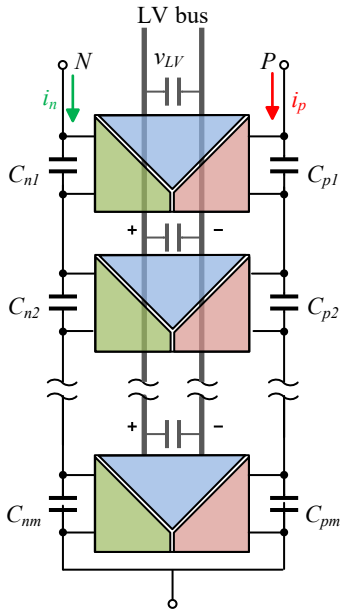


Fig. 5.2: Block diagram of input series output parallel connected three-port converter modules

is expected relatively to conventional multicell approach since only the DC-DC stage is implemented in modular approach. The rectification is implemented centrally leading to low component count and ease of implementation. Very low losses are incurred in the Unfolder which allows for a very high-power density implementation.

Merits of this topology are summarized here:

- Very low frequency switching (120 Hz) of MV IGBTS. Zero voltage during switching instants. This eliminates the needed for fast dynamic voltage sharing during turn-on and turn-off transition.
- Zero voltage switching of all the devices in the DC-DC modules enable HF operation.
- Lower number of passive components relative to the traditional two stage multi-cell approach.
- No bulk capacitance required in the modules. Stored energy in the medium voltage DC link is relatively low which improves the safety.

5.2 Triple Active Bridge DC-DC Module for Unfolding SST

To select an appropriate DC-DC module converter topology for SST, the desired features need to be identified first. SSTs are typically realized using multiple converter modules (cells) that are input-series output-parallel (ISOP) arranged. The structure is modular as shown in Fig. 2.3. Each module consists of AC-DC rectifier and DC-DC isolation stage. Each module is only rated for a fraction of the full DC link voltage. The DC-DC converter submodules are the key component in the SST structure [64–66]. Other multi-cell approaches with slight modifications are possible [48]. The isolation requirements for the MFT are more or less similar in all these structures. Each MFT must be designed for full system voltage isolation. This reduces the potential power density benefits achievable with this modular approach. Usually the isolated DC-DC converter is operated at a fixed voltage transformation ratio in the multicell SST structure. The AC-DC stage is typically used to regulate the intermediate floating DC link voltage. The isolation enables the DC-DC modules to be input series and output parallel connected. Due the series stacking at the input the voltage stress on the MF transformer is high and the insulation must be designed to withstand high DC bias voltage across the isolation barrier. Although the insulation must also withstand HF stress, the magnitude of the HF component is relatively lower compared to the DC voltage stress. Preferred features for the DC-DC modules:

- High insulation capability
- Operate with soft-switching to enable efficient HF operation for higher power density
- Bi-directional capability

The high voltage isolation requirements lead to a reasonable leakage energy in the transformer. Ideal DC-DC topology candidates will effectively use this a part as a circuit element. Many SST topologies reported in literature, for example in [67]and [68] can not effectively utilized the leakage energy of the transformer and hence achieve a lower performance.

Dual active bridge is the most widely reported DC-DC topology used as the DC-DC building block in the multi-cell SST [45]. The converter can achieve soft switching for all the devices. Seamless control transition from positive to negative power levels is possible for this topology. High power DAB design is reported in [69].

LLC converter is the preferred topology used in most field demonstrated PETs [66,70].

LLC topology is asymmetrical and preferred for uni-directional applications. For bi-directional application, a modifications to LLC topology are proposed in literature. Most promising one being the CLLLC topology. This topology has symmetrical resonant tank. Operates with frequency modulation. This topology is not a true bi-directional topology. At any given point in time only one bridge is actively controlled, the other bridge is operated as synchronous rectifier. The closed loop controller has to identify the power flow direction and change the modulation strategy accordingly. The UL standard or IEC standard recommends a certain creepage and clearance. The dielectric strength of the insulation should also meet the standards' recommendations. There are only a few reported works in literature that has address the isolation requirements of the DC-DC modules [71]. The voltage isolation requirements can significantly alter the suitability of a DC-DC topology.

This thesis proposes the use of a three-port resonant triple active bridge as the backend DC/DC converter for the unfolding rectifier approach. Resonant topology allows for effective utilization of the transformer leakage inductance. The uniqueness of the proposed topology is in the series AC connection of the secondary windings of the transformers, which adds up the two primary bridge voltages. The resultant primary voltage will have a low variation in amplitude over the entire grid line cycle, allowing the converter to be designed with higher efficiency. The power from the two soft DC-links is combined on the secondary side of the transformer. Only one resonant tank and one secondary bridge need to be designed as opposed to two resonant tanks and two secondary bridges in the earlier reported resonant topology [15], where power gets combined at the DC output bus. In [15], since each DC/DC converter has wide variation in input voltage, the converters tend to be less efficient due to limited zero voltage switching (ZVS) range and higher RMS tank current [60].

5.2.1 Topology Description

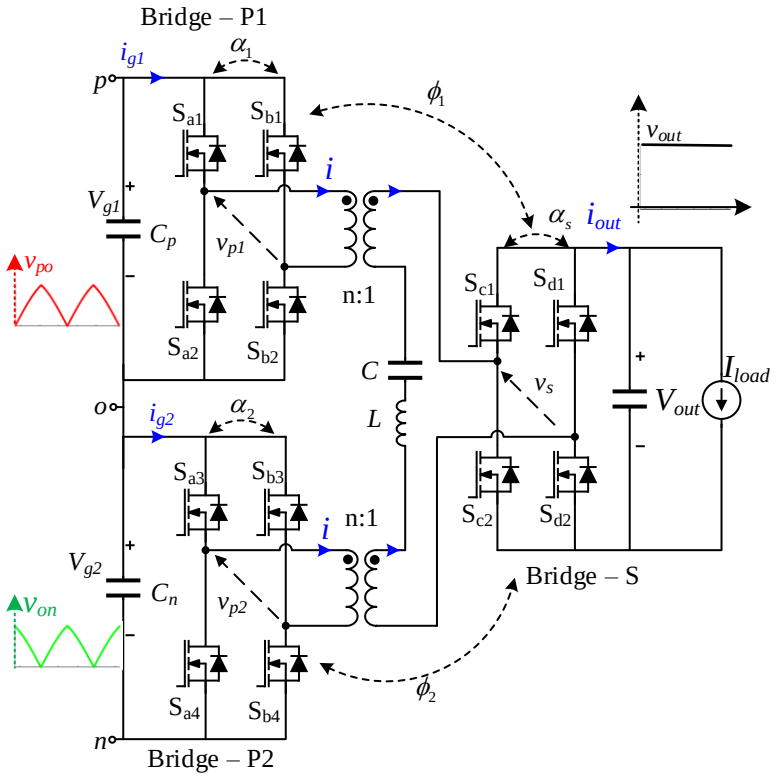


Fig. 5.3: Schematic of the proposed Triple Active Bridge

Identifying the fact that the two soft DC-link voltages v_{po} and v_{on} are interleaved and their instantaneous sum has far lower variation, a new triple active bridge topology is proposed that utilizes a combination of the two DC link voltages in one switching cycle to drive a common LC tank .

The previously reported resonant based topology [15] with two dual active bridge series resonant converters (DABSRC) cannot soft switch over the complete AC line cycle at any given load due to the wide variation in the input DC link voltages. With the proposed modification of connecting the transformer secondaries in series, the DC/DC stage can soft switch over the entire line cycle without the need for any assistance circuit. Because of the minimum current required for ZVS to discharge the parasitic output capacitance of the MOSFETs, the converter can only achieve partial ZVS below a certain load. This

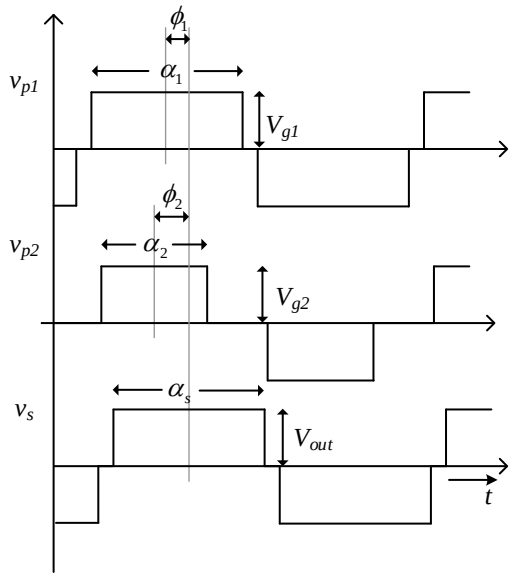


Fig. 5.4: Phase-shift and duty cycle definitions for bridge voltages

limitation is inherent to traditional DABSRC and is also the case with most of DC/DC isolated topologies. Even though the two DC link voltages vary over a wide range, the variation in amplitude of the resultant voltage driving the resonant tank is less, and hence the tank can be designed to be more efficient.

The topology consists of three active bridges, and each generates a quasi-square wave voltage with duty cycle (α). The relative phase shifts of the primary bridge voltages (ϕ_1, ϕ_2) with respect to the secondary bridge voltage are also control parameters. A total of five control parameters are possible while operating at constant frequency.

5.2.2 Operating Principle and Sinusoidal Analysis

The operation of the proposed TABSRC is explained in this section. V_{g1}, V_{g2} are the DC-link voltages at the primary bridges and V_{out} is the DC-link voltage at the output bridge. For the analysis of the TABSRC, these DC link voltages are assumed to be constant. This assumption is valid as long as the switching frequency (f_s) of the TABSRC is considerably higher (e.g. two orders of magnitude higher) than that of the grid voltage frequency, such that the dynamics of the TABSRC settle down must faster compared to the variation of

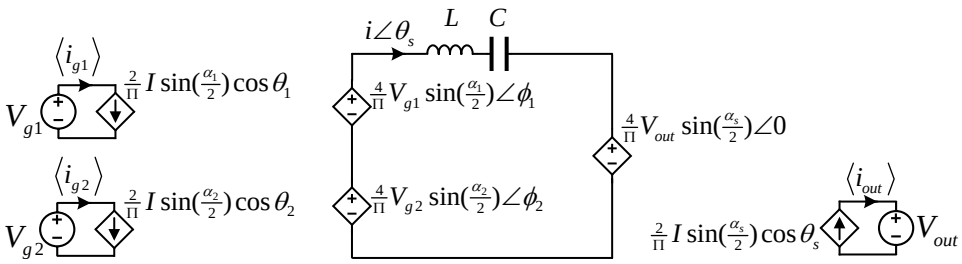


Fig. 5.5: Equivalent circuit based on the fundamental approximation

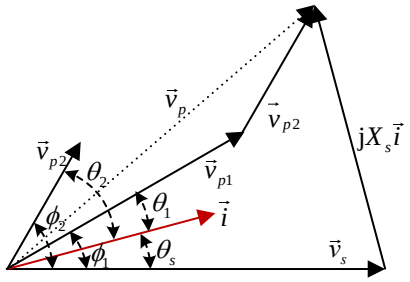


Fig. 5.6: Fundamental phasor diagram of the TABSRC

the soft DC-link voltages. V_{g1} and V_{g2} will take the values of v_{po} and v_{on} that slowly vary in time as the grid phase angle varies.

The primary bridge-P1, bridge-P2 and secondary bridge-S generate quasi-square wave voltages v_{p1}, v_{p2}, v_s respectively. The definitions for phase-shifts and duty cycle of these voltages are given in Fig. 5.4. The equivalent circuit based on the fundamental approximation is shown in Fig. 5.5. The fundamental phasor diagram of this equivalent circuit is given in Fig. 5.6. The transformer secondaries are connected in series. The equivalent circuit and phasor diagram also convey this concept. Only the fundamental component of the bridge voltages are considered to perform the analysis. This simplifies the analysis and gives reasonable accuracy. For the following analysis, the turns ratio is assumed to be unity so as to simplify the equations. The secondary bridge voltage is used as the reference for the phasor analysis. θ_1, θ_2, θ_s are the angles between tank current (i) and bridge voltages v_{p1}, v_{p2}, v_s respectively. The fundamental phasor voltages in polar and rectangular co-ordinates

are given as

$$\begin{aligned}
\vec{v}_{p1} &= \frac{4}{\pi} V_{g1} \sin(\frac{\alpha_1}{2}) \angle \phi_1 \\
&= \frac{4}{\pi} V_{g1} \sin(\frac{\alpha_1}{2}) (\cos(\phi_1) + j \sin(\phi_1)), \\
\vec{v}_{p2} &= \frac{4}{\pi} V_{g1} \sin(\frac{\alpha_2}{2}) \angle \phi_2 \\
&= \frac{4}{\pi} V_{g2} \sin(\frac{\alpha_2}{2}) (\cos(\phi_2) + j \sin(\phi_2)), \\
\vec{v}_s &= \frac{4}{\pi} V_{\text{out}} \sin(\frac{\alpha_s}{2}) \angle 0 = \frac{4}{\pi} V_{\text{out}} \sin(\frac{\alpha_s}{2}).
\end{aligned} \tag{5.1}$$

Effective primary voltage,

$$\vec{v}_p = \vec{v}_{p1} + \vec{v}_{p2}. \tag{5.2}$$

Effective tank current,

$$\vec{i}_s = \frac{\vec{v}_p - \vec{v}_s}{j X_s}. \tag{5.3}$$

Here, $Xs = \omega_s L - \frac{1}{\omega_s C}$ is the impedance of the resonant tank at angular switching frequency ω_s. Port powers P_1, P_2, P_{out} and port average currents $\langle I_{g1} \rangle$, $\langle I_{g2} \rangle$, $\langle I_{\text{out}} \rangle$ are given by

$$\begin{aligned}
P_1 &= \frac{8 V_{g1} \sin(\frac{\alpha_1}{2})}{\pi^2 X_s} [V_{out} \sin \frac{\alpha_s}{2} \sin \phi_1 + V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2 - \phi_1)] \\
P_2 &= \frac{8 V_{g2} \sin(\frac{\alpha_2}{2})}{\pi^2 X_s} [V_{out} \sin \frac{\alpha_s}{2} \sin \phi_2 + V_{g1} \sin \frac{\alpha_1}{2} \sin(\phi_1 - \phi_2)] \\
P_{\text{out}} &= \frac{8 V_{\text{out}} \sin(\frac{\alpha_s}{2})}{\pi^2 X_s} [V_{g1} \sin \frac{\alpha_1}{2} \sin \phi_1 + V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2)]
\end{aligned} \tag{5.4}$$

$$\begin{aligned}
\langle I_{g1} \rangle &= \frac{8 \sin(\frac{\alpha_1}{2})}{\pi^2 X_s} [V_{out} \sin \frac{\alpha_3}{2} \sin \phi_1 + V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2 - \phi_1)], \\
\langle I_{g2} \rangle &= \frac{8 \sin(\frac{\alpha_2}{2})}{\pi^2 X_s} [V_{out} \sin \frac{\alpha_3}{2} \sin \phi_2 + V_{g1} \sin \frac{\alpha_1}{2} \sin(\phi_1 - \phi_2)], \\
\langle I_{\text{out}} \rangle &= \frac{8 \sin(\frac{\alpha_3}{2})}{\pi^2 X_s} [V_{g1} \sin \frac{\alpha_1}{2} \sin \phi_1 + V_{g2} \sin \frac{\alpha_2}{2} \sin(\phi_2)].
\end{aligned} \tag{5.5}$$

Here, <> represents the average of a variable over a switching period, T_s.

5.2.3 Modulation Implementation

The converter has five degrees of freedom while operating at constant frequency. Since the three-port DC/DC converter must regulate the output and also achieve PFC action at input ports, at least two control variables are required. To keep the control simple for the initial implementation, the number of controlled inputs are limited to two. The additional degrees of control can be explored to minimize the overall system losses [72] or RMS tank current [73], and is left for future work.

Duty-cycle plus phase-shift control proposed in [74] for magnetically coupled multi-port converters is implemented here. The rising edge of voltages of the primary bridges are aligned to maximize the probability of ZVS for both the input bridges. A new control variable ϕ_{edge}, defined as the phase between rising edge of the primary voltages and the rising edge of the secondary voltage, is used as one control variable. The duty cycle (α) of one of the primary bridge voltages is used as the second control variable. For TABSRC, the same set of input operating conditions repeat every 60^o of the AC grid phase angle. These operating conditions can be divided into two sectors based on the relative magnitudes of the required bus currents i_p and i_n. For Sector-1 with $i_p < -i_n$, α_1 is used as control parameter and α_2 is set to π, whereas, for Sector-2 with $i_p > -i_n$, α_1 is set to π and α_2 is used as control parameter. The primary bridge with lower magnitude of current will have duty less than π, whereas the other primary bridge with higher magnitude of current will have a duty equal to π. This control approach is summarized in Table. 5.1. For example, when the converter operates in Sector-2, then $\alpha_1 = \alpha_s = \pi$, $\phi_1 = \phi_{\text{edge}}$ and $\phi_2 = \phi_{\text{edge}} + \frac{\pi-\alpha_2}{2}$. The steady state bus power and average currents with these control variables are given in (5.6) and (5.7). Similar equations can be derived for the converter operating in sector-1.

$$
\begin{aligned}
P_1 &= \frac{8V_{g1}}{\pi^2 X_s}[V_{out}\sin\phi_{\text{edge}} + V_{g2}\sin(\frac{\alpha_2}{2})\cos(\frac{\alpha_2}{2})] \\
P_2 &= \frac{8V_{g2}\sin(\frac{\alpha_2}{2})}{\pi^2 X_s}[V_{out}\cos(\phi_{\text{edge}} - \frac{\alpha_2}{2}) - V_{g1}\cos(\frac{\alpha_2}{2})] \\
P_{\text{out}} &= \frac{8V_{\text{out}}}{\pi^2 X_s}[V_{g1}\sin\phi_{\text{edge}} + V_{g2}\sin(\frac{\alpha_2}{2})\cos(\phi_{\text{edge}} - \frac{\alpha_2}{2})]
\end{aligned}
\tag{5.6}
$$

$$\begin{aligned}
\langle I_{g1}\rangle &= \frac{8}{\pi^2 X_s}[V_{out}\sin\phi_{\text{edge}} + V_{g2}\sin(\frac{\alpha_2}{2})\cos(\frac{\alpha_2}{2})] \\
\langle I_{g2}\rangle &= \frac{8\sin(\frac{\alpha_2}{2})}{\pi^2 X_s}[V_{out}\cos(\phi_{\text{edge}} - \frac{\alpha_2}{2}) - V_{g1}\cos(\frac{\alpha_2}{2})] \\
\langle I_{\text{out}}\rangle &= \frac{8}{\pi^2 X_s}[V_{g1}\sin\phi_{\text{edge}} + V_{g2}\sin(\frac{\alpha_2}{2})\cos(\phi_{\text{edge}} - \frac{\alpha_2}{2})]
\end{aligned} \tag{5.7}$$

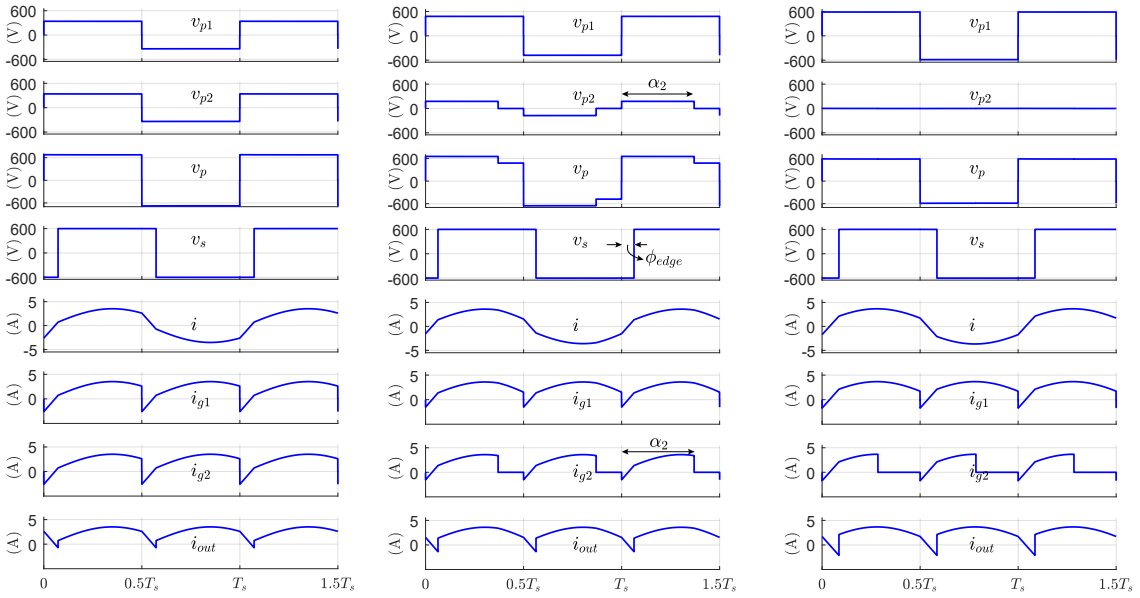
Table 5.1: Control parameters based on the input operating point

	Sector-1	**Sector-2**
Operating condition	$i_p < -i_n$	$i_p > -i_n$
Fixed parameters	$\alpha_2 = \alpha_s = \pi$	$\alpha_1 = \alpha_s = \pi$
Control parameters	α_1 and ϕ_{edge}	α_2 and ϕ_{edge}

5.3 Simulation and Hardware Results

A 2 kW TABSRC is designed to operate as a back-end converter for 480 V line to line three-phase rectifiers based on the unfolding rectification approach. The design parameters are given in Table 5.2. Simulation results are given in Fig. 5.7 for three distinct operating points (a), (b) and (c) on the soft DC-link (see v_{po} and v_{on} waveforms in Fig. 3.2) encountered in a sector of operation. These results help visualizing the evolution of DC/DC control parameters with the grid phase angle. For simulations, two DC voltage sources are used as the inputs that take the values of the soft DC-link voltages. Since the TABSRC switching frequency is significantly higher than the grid frequency, the DC simulations accurately represent the operating conditions that will be encountered with an Unfolder.

The device output capacitances (C_{oss}) and parasitic capacitances of the magnetics are not included in these simulations. All three results are for the same output voltage and power of 600 V, 1500 W. The duty cycle (α_2) and rising edge phase (ϕ_{edge}) are adjusted such that the same power is delivered at the output and PFC action is implemented at the input. The average values of input port currents match the expected soft DC-link bus



(a) TABSRC waveforms at V_{g1} = 339 V, V_{g2} = 339 V, $< i_{g1} >$ = 2.25 A, $< i_{g2} >$=2.25 A for 1.5 kW at $\omega t = \pi/3$

(b) TABSRC waveforms at V_{g1}=480 V, V_{g2}=175.7 V, $< i_{g1} >$ = 2.52 A, $< i_{g2} >$ = 1.84 A for 1.5 kW at $\omega t = 5\pi/12$

(c) TABSRC waveforms at V_{g1}=588 V, V_{g2} = 0 V, $< i_{g1} >$ = 2.6 A, $< i_{g2} >$ = 1.3 A for 1.5 kW at $\omega t = \pi/2$

Fig. 5.7: TABSRC waveforms at three distinct DC-link operating points (a) $\omega t = \pi/3$, $\omega t = 5\pi/12$, $\omega t = \pi/2$ in sector-2 at 1.5 kW. α_1 is set to π and α_2, ϕ_{edge} are used as control parameters in this sector.

currents. For all three operating points, it can be seen that the switching instant currents for the 12 devices are in the right direction to achieve soft switching. The tank current (i) RMS and peak values are relatively similar for the three operating points. This shows that the converter can work with wide variation in input voltage without having excessive tank currents.

The TABSRC hardware prototype (see Fig. 5.8) is fabricated with the parameters listed in Table 5.2. The prototype is fabricated to be modular for rapid prototyping and easy debugging. All three H-bridges are built symmetrically with the same devices and gate drives. The series resonant capacitance (10 nF) is also distributed equally across all the three bridges such that each bridge has a series resonant capacitance of 30 nF, which also serves the purpose of DC current blocking for the transformers. The resonant tank inductor is implemented as one large lumped inductor since it minimizes the overall size [75]. A

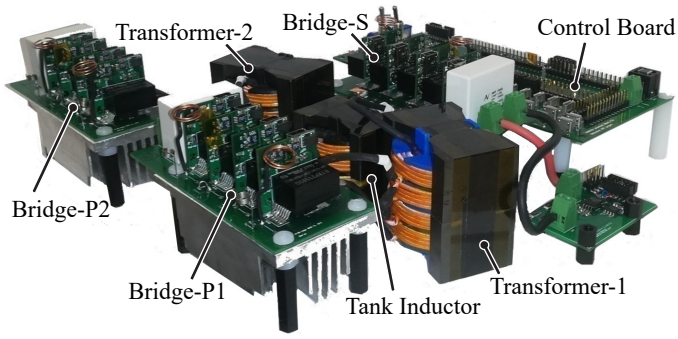


Fig. 5.8: TABSRC hardware prototype with parameters of Table 5.2 built for evaluation

deadtime of 100 ns is implemented for complementary devices.

Two programmable DC power supplies connected in series are used to emulate the input soft DC-link. A 2 kW peak rated electronic load is used to emulate load. A general-purpose control board built around the F28379D micro-controller is used to generate the PWM signals. Pre-calculated values of duty-cycles and phase-shift for each operating point are loaded on the micro-controller. The input and output DC quantities are measured using a WT1806E Power Analyzer. 1 μH inductors are used at each DC port of the converter to filter out the ripple currents to get accurate DC measurements. The measured input and output port average currents and operating conditions are summarized in Table. 5.3 and the corresponding switching waveforms are given in Fig. 5.9. Since the converter is soft switching with relatively constant tank current and output power, high efficiency of 97.7 % or higher is achieved for all three DC operating conditions.

5.4 Closed-Loop Control for Grid Connection

In the proposed topology, one DC-DC converter has to perform both the tasks of output current regulation and input PFC action. These two control objectives are strongly coupled. Similar to the grid control approach presented for 3LAFB converter, to achieve the PFC action, the grid currents are indirectly controlled by controlling the soft DC-link currents. At unity power factor operation, the ratio of i_p and i_n has a unique value for a given grid angle. The PFC loop controls the ratio of i_p and i_n. The control variable for this loop is

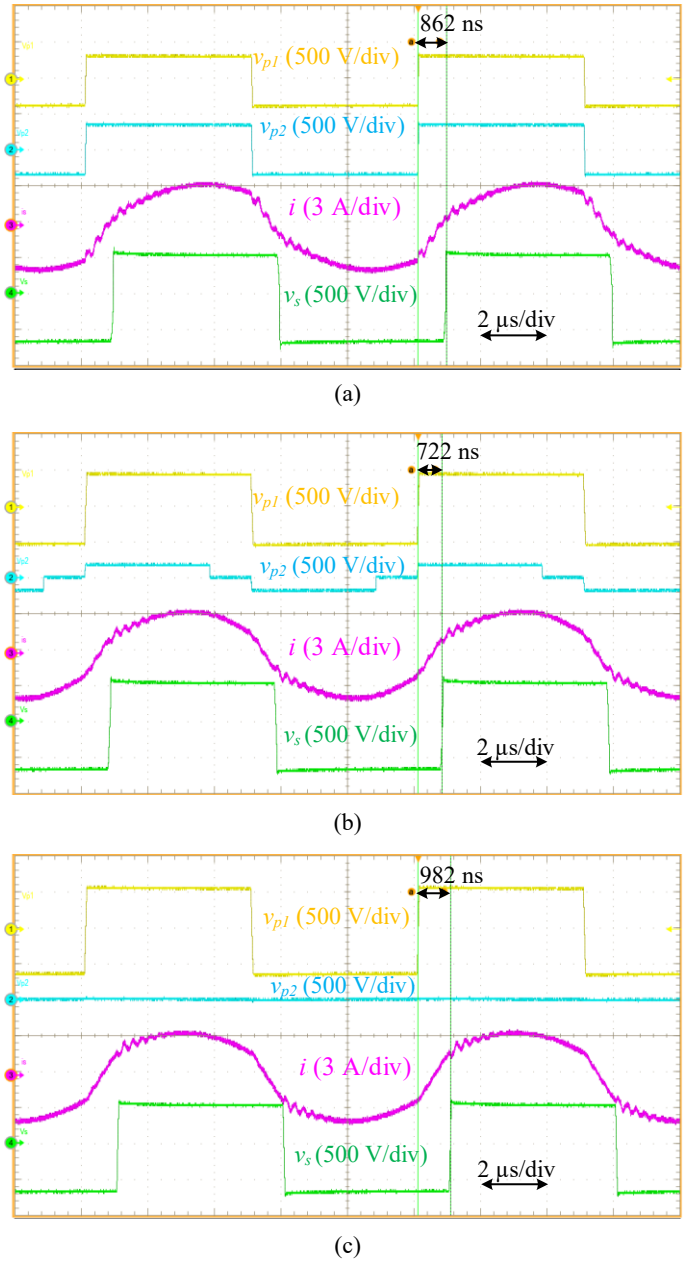


Fig. 5.9: Hardware prototype waveforms at 600 V output delivering close to 1500 W at three different input voltage operating points (a) V_{g1}= 339 V, V_{g2}= 339 V; (b) V_{g1}= 480 V, V_{g2}= 175.7 V; (c) V_{g1}= 588 V, V_{g2}= 0 V.

Table 5.2: TABSRC prototype parameters

Parameter	**Description**
Rated Power	2000 W
Nominal Input	480 V RMS Unfolded voltage
Nominal Output	600 V
Switching Frequency	100 kHz
Resonant tank	L =414 μH (includes transformer leakages), C =10 nF
Switching Devices	C3M0120100J, 1000 V, 120 mΩ
Transformers	1:1 turns ratio Core: PQ50-50, N97 material Winding: 40 turns of 420 X 42 Litz
Tank Inductor	319 μH Core: PQ40-40, N97 material Winding: 55 turns of 420 X 42 Litz
Tank Capacitor	15 nF, 1000 V, ceramic capacitor. 2 in parallel, distributed across all three bridges equally. Total six 15 nF capacitors used for capacitance

d_p/d_n. The output current is controlled by the variable ϕ_{edge}. A feedforward approach is proposed to weaken the coupling between these two control loops.

For operation in sector-1, the average output current $\langle I_{\text{out}} \rangle$ is given in 5.7. A new control variable $v_{p,q}$ is defined that captures the magnitude of quadrature component of v_p with respect to v_s. This quadrature component can be given as

$$\langle I_{\text{out}} \rangle = V_{g1} \sin \phi_{\text{edge}} + V_{g2} \sin(\frac{\alpha_2}{2}) \cos(\phi_{\text{edge}} - \frac{\alpha_2}{2}). \tag{5.8}$$

Then average output current can be simplified to

$$\langle I_{\text{out}} \rangle = \frac{8}{\pi^2 X_s} v_{p,q}. \tag{5.9}$$

Table 5.3: Hardware result summary

	Operating voltages	Modulation	Measured quantities	η %
(a)	V_{g1}= 340 V V_{g2}= 340 V V_{out}= 600 V	α_1=α_s= π α_2= π ϕ_{edge}= 0.158π	$\langle I_{g1}\rangle$= 2.26 A $\langle I_{g2}\rangle$= 2.26 A $\langle I_{out}\rangle$= 2.51 A	97.70%
(b)	V_{g1}= 480 V V_{g2}= 176 V V_{out}= 600 V	α_1=α_s= π α_2= 0.753π ϕ_{edge}= 0.146π	$\langle I_{g1}\rangle$= 2.50 A $\langle I_{g2}\rangle$= 1.80 A $\langle I_{out}\rangle$= 2.48 A	97.99%
(c)	V_{g1}= 588 V V_{g2}= 5 V V_{out}= 600 V	α_1=α_s= π α_2= 0.583π ϕ_{edge}= 0.196π	$\langle I_{g1}\rangle$= 2.60 A $\langle I_{g2}\rangle$= 1.23 A $\langle I_{out}\rangle$= 2.51 A	97.81%

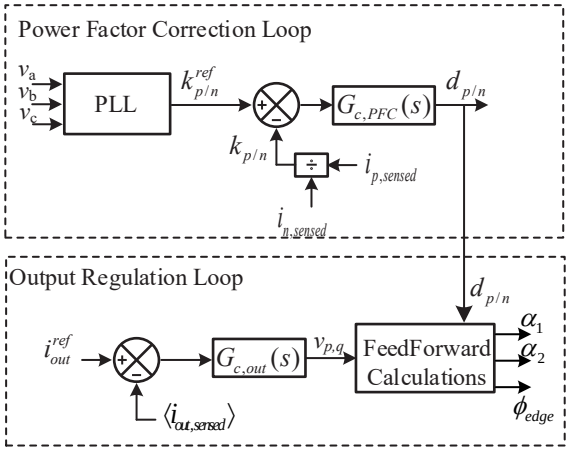


Fig. 5.10: Block diagram of the grid synchronization control implementation for TABSRC

If $v_{p,q}$ is selected as the control variable for the output loop then the outer loop can be decoupled from the PFC loop from changing duty cycle values. With this reasoning a new control approach is proposed as shown in Fig. 5.10.

The reference DC-link current ratio ($k_{p/n}^{ref}$) will be determined by the PLL block. The PLL uses the phase voltage information to determine the DC-link current ratio to achieve unity power factor. The output of this loop is used in the feedforward calculations to determine α_1, α_2 and ϕ_{edge}. The feedforward term calculations are given in Table.5.4. The

required ϕ_{edge} can be feedforward using the calculation

$$\phi_{edge} = \sin^{-1}\left(\frac{V_{p-q}}{\sqrt{K_1^2 + K_2^2}}\right) - \sin^{-1}\left(\frac{K_2}{\sqrt{K_1^2 + K_2^2}}\right), \tag{5.10}$$

where K_1 and K_2 are calculated as given in Table.5.4.

Table 5.4: Feedforward terms for TABSRC decoupled control implementation.

Parameter	$d_{p/n} < 1$	$d_{p/n} > 1$
α_1	$\pi d_{p/n}$	π
α_2	π	$\pi/d_{p/n}$
K_1	$V_{g1}\frac{1-\cos(\alpha_1)}{2} + V_{g2}$	$V_{g1} + V_{g2}\frac{1-\cos(\alpha_2)}{2}$
K_2	$V_{g1}\sin(\frac{\alpha_1}{2})$	$V_{g2}\sin(\frac{\alpha_2}{2})$

The closed-loop simulation result at rated power of 2 kW with this approach is given in Fig. 5.11. The feedforward calculations do not require any converter component information which can have high tolerances. Only the dutycyles and soft DC-link voltage information is required. This make the calculations robust.

5.5 Summary

In this chapter, the concept of three-phase medium voltage unfolding is introduced. A new three-port series input parallel output DC-DC structure is proposed for the DC-DC stage. The proposed approach results in a quasi-single stage SST. This approach reduces the implementation cost of the SST. A new three-port magnetically coupled DC-DC topology called the Triple Active Bridge converter is proposed for realizing the DC-DC module. Steady-state analysis is presented for this new topology using fundamental harmonic analysis. Modulation technique for the topology is proposed to maintain soft-switching over the entire line cycle. A 2 kW hardware prototype for this topology is fabricated. Experimental results are provided at three extreme input operating points. Soft-switch and high efficiency is maintained at all operating points, despite wide voltage swing at the input soft DC-links.

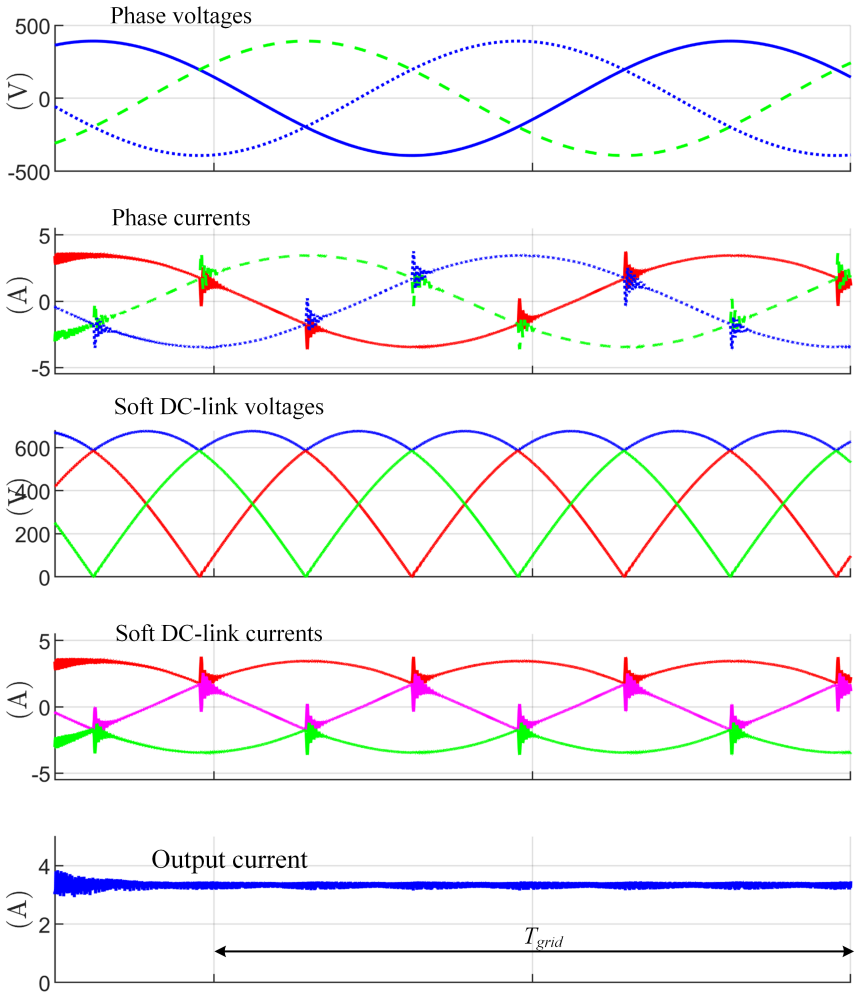


Fig. 5.11: Closed loop simulation result for 480 VAC at 2 kW output

Finally, a closed-loop control structure for grid integration for one module is presented. A unique decoupling method is used to design the control loops. Simulation results are presented that validated the control approach.

CHAPTER 6

560 kW Unfolding SST Design and Fabrication

In this chapter, a 560 kW 4.16 kV 3-phase AC to 800 VDC Solid State Transformer design is provided. First, the design of the medium voltage Unfolder is given. A novel insulation concept is proposed for the isolation transformer in the DC-DC stage. Finite element simulation results are given to validate the electric field stresses. Steady state analysis of the Triple Active Bridge with low magnetizing inductance is given. Finally, hardware results on 80 kW prototype at different soft DC-link voltage conditions are given that validate the feasibility of converter operation.

6.1 System-Level Design

The system specification of the direct medium voltage connect AC to DC converter are given in Table. 6.1. 7 modules each capable of working with a DC input voltage of up to 900 V are used. The primary bridges of the these 7 modules will be connected in series and the secondaries will be connected in parallel. The turns ratio of each transformer is selected as 1:1.

Table 6.1: Specifications for the prototype battery charger

Parameter	**Prototype specification**
Grid input voltage	4160 V_{AC} RMS voltage
Output voltage range	750 V_{DC} to 900 V_{DC}
Nominal output power	560 kW
Max. output current	750 A_{DC}
Rated power efficiency	95% or higher required

Table 6.2: Voltage and current stress on the Unfolder devices

Switch	Peak blocking voltage	Maximum RMS current	Maximum average current
d_{1-6}	V_m=5.88 kV	56.20A	31.92A
S_{abc}	0.86V_m 5.1 kV	19.66A	9.88 A

6.2 Medium Voltage Unfolder Design

Si HVIGBT that are popular for MV applications such traction, industrial drives are suitable for realization of the MV Unfolder. To limit the susceptibility to cosmic-ray induced failures of the devices (a significant failure mechanism at high DC voltages for devices with large die area) only about 50% to 60% of the devices' rated blocking voltage utilization is recommended in an application.

The system output power is 560 kW rated. The MV Unfolder has to also supply for the loss in the DC-DC stage and so to have reasonable margin, the MV Unfolder is designed for a worse-case input power of 590 kW. Ideal waveforms of the Unfolder operating with 4.16 kV grid at 590 kW are given in Fig .6.1.

In the Table. 6.2, the average and RMS current for S_{abc} are given per device (per IGBT and diode co-package). Within the co-package, the average and RMS per IGBT and per reverse diode are calculated by scaling down by 2 and 1.414 respectively to estimate losses. Each switch is realized using two 6.5 kV devices connected in series to achieve the required blocking voltage which provides more than 100% margin. Total 24 devices are used to realize the 12 switches in the Unfolder. 10 kV rated isolation power supplies are used for the IGBT gate drivers. The creepage and clearance for various components in the Unfolder are chosen to meet the recommendations in the UL2877 standard. ANSYS Icepak thermal simulations were used for the cooling design. List of selected key components is given in Table. 6.3.

The conduction losses are calculated based on the equivalent conduction representation of a series voltage drop and a resistance. The forward voltage drop and resistance of the devices are estimated based on the performance curves given in the datasheets [76,77]. The

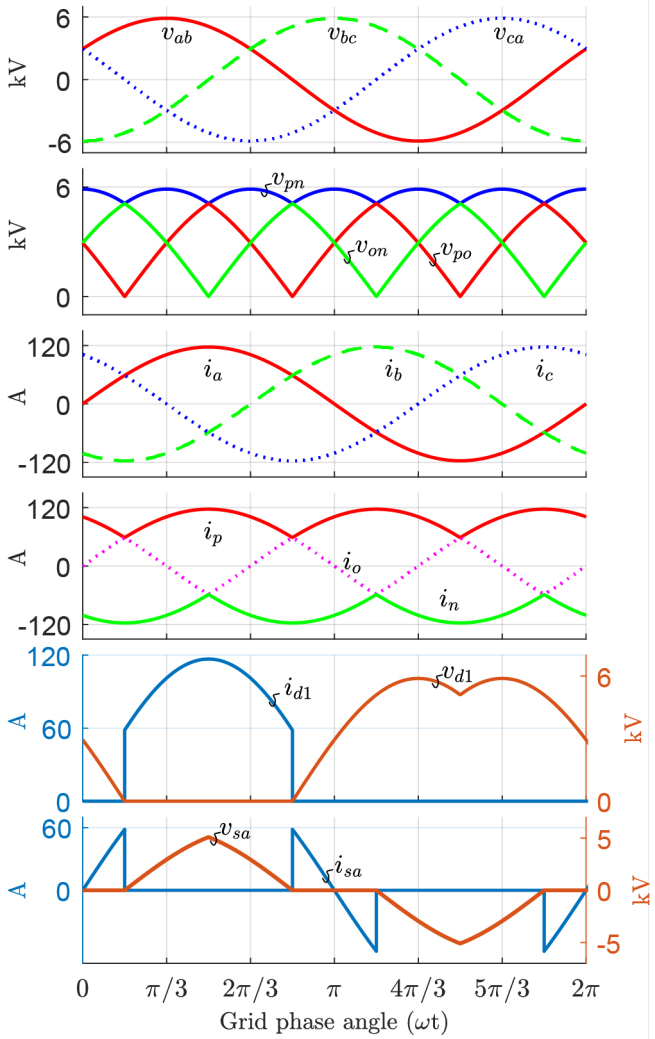


Fig. 6.1: Ideal waveforms for T-type Unfolder at 4.16 kV, 590 kW

Table 6.3: Components used in the MV Unfolder

Component	**Part Details**
Diodes, D_{1-6}	QRD6516001, 6.5 kV, 160 A
IGBT,S_{abc}	QIC6508001, 6.5 kV, 85 A
Gate driver	1SP0335V2M1-65
Gate driver supply	ISO5125I-65, 5 W, 10.2 kV isolation

Table 6.4: Loss estimation for the devices in the Unfolder

Loss per switch for D_{1-6}	111.27 W
Loss per switch for S_{abc}	70.73 W
Total conduction losses	1092 W
Unfolder efficiency at rated power	99.81%

switching losses are negligible as these devices are switching only at twice line frequency at zero voltage. Only conduction loss exists leading to high estimated efficiency of the Unfolder, see Table. 6.4.

6.3 80 kW Triple Active Bridge Design

Designing the DC-DC stage to meet the isolation requirements while simultaneously maintaining high power density is a major challenge in SST. The transformer is the key component/element in the SST. The primary challenge for the transformer is the design of reliable insulation. The isolation requirements reduce the achievable power density. The maximum temperature targets all constraint the power density increase. Minimizing the thermal impedance is one effective approach the reduced volume of the transformer.

6.3.1 Review of Insulation Concept for Medium Voltage Isolated Transformer

Various transformer structures and design guidelines are reported in literature for medium voltage isolated high frequency transformers (MVHFT) but only a few have emphasized the voltage isolation requirements. Three popular approaches to achieve the isolation

are:

1. Using high voltage cable for windings [78]
2. Potting the winding [71, 79, 80]
3. Oil immersed windings [66, 81, 82].

Using HV cable is a reliable approach. But this leads to lower power density since the insulation is present between adjacent turns not just between the two windings. This reduces the core utilization and the thermal conductivity of winding. Potting is a good option since the insulation thickness can be varied as needed in different portions of the transformer, but this approach results in higher fabrication effort that requires custom potting assemblies. For oil insulated designs, additional auxiliary equipment such as Pumps, filters, pressure vessel and heat exchanger to ambient are required. Oil dielectric can also increase the parasitic capacitance. These aspects make it not ideal for lower power designs due to increased fabrication effort..

Field strength in air will be the highest when multiple insulation materials in combination with air gap is used. This results in air being the weakest link and can potentially lead to partial discharge (PD) in the air gaps. Large airgaps are required to increase the PD inception voltage. This negatively effects the core window utilization reducing the power density of the transformer. Potting or casting smaller parts is relatively easy. Reliable void free potting can be ensured. Potting the entire winding assembly can be an elaborate process [79]. Review of the DC-DC isolation approaches:

Optimization methodology for MFT is provided in [83]. 100 kW, 10 kHz, prototype presented is an air insulated and air-cooled shell type transformer. The airgap clearance between the windings is not selected based on the isolation requirement but rather of the leakage inductance required for the topology. Critical partial discharge of 10 nC was reached at 4 kVAC. The application system voltage was not stated but 4 kVAC is a low PD value for most MV grid requirements.

A design of 350 kVA, 10 kHz, 38 kV insulation rated MFT for 15 kVrms traction drive application is presented in [78]. Coaxial medium voltage cable is used for transformer windings. Thick insulation on the MV cable restricts the bend radius. 90 mm is the radius used in [78]. Higher bend radius cannot be effectively accommodated in smaller size transformer. The excess insulation material reduces the power density due to increased volume of winding and reduced thermal conductivity. To effectively cool the windings de-ionized water is circulated through the hollow core of the inner conductor.

Design of 1.75 kHz MFT transformer for 150 kVA DC-DC module for 15 kV 16.7 Hz railway grid connected converter is given in [66]. The transformers for all the DC-DC modules are housed in a large dielectric oil tank. The high dielectric strength of oil allows for compact assembly. Oil directed forced air cooling method is used.

200 kVA, 10 kHz MFT design is presented in [80]. 35 kV and 5 kV primary and secondary short-term insulation capability to ground. A combination of polyimide film, Nomex paper, Epoxy resin and air are used to achieve the insulation. Are used for inter-turn insulation. Each winding is encapsulated, and sufficient airgap is reduce the electric field intensity. Fin array heat exchangers with forced air cooling is used.

15 kW 500 kHz DC-DC converter module for 4.16 kV utility grid application is design in [71]. The core referred to ground potential. Only the primary winding is insulated for MV to meet the isolation requirements. PTFE bobbin, dielectric tape are used to insulate the winding. 4 mm spacer between bobbin and core is used to reduce the field intensity in air. Insulation design is validated with 12 kVrms dielectric tests.

A novel insulation concept is presented in [84] for 240 kVA, 10 kHz MFT with 70 kV dielectric voltage rating. The design is good balance between cooling performance and insulation size. The airgap between the HV and LV windings is designed only to avoid PD upto 67 kVrms. Both the HV and LV windings are vacuum impregnated with resin. The thickness of the resin is chosen to handle the full voltage since the air will breakdown at impulse voltage rating of 150 kV. The winding structure allows for smoother fields and easier forced air-cooling.

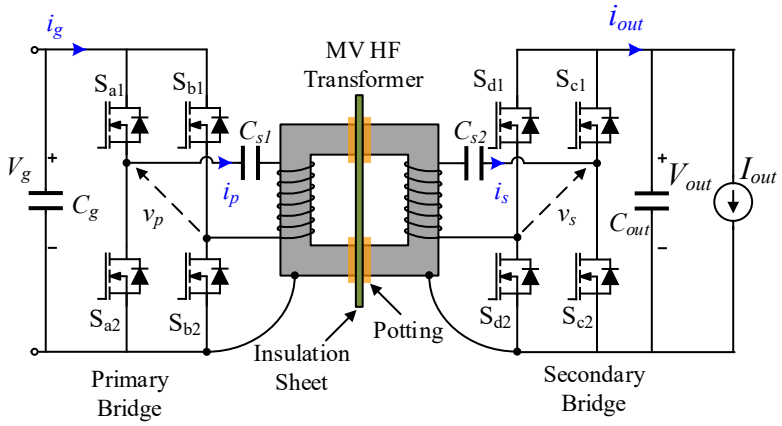


Fig. 6.2: Proposed insulation concept for medium voltage high frequency transformer

A MFT design for 166 kW, 20 kHz DC-DC converter is given in [64]. Mica tape rated for 13.8 kV is used insulation. Aluminum parts are used to thermally conduct the heat internally from core and winding to two water-cooled heat sinks. The thickness of tape is not provided. The reported design could experience PD if the electric field intensity in the air close to the breakdown voltage. Nominal system voltage or insulation test results are not provided.

6.3.2 A Simple Novel Insulation Concept

A novel insulation concept is proposed that achieves high voltage insulation without complicating the fabrication or cooling requirements for the transformer. The idea is to confine the high electric fields to a small region. Then only this small region needs to be potted with a high dielectric strength material. This is achieved by segregating the primary and secondary side of the transformer on either side of an insulation disk (see Fig. 6.2). The thickness of the insulation is selected to withstand the required breakdown voltage rating. The physical dimensions of the disk are selected to meet creepage and clearance requirements. The core on each half will be tied to the negative rail of that particular H-bridge. The peak potential between the core and its winding is just the rated voltage of one LV module. The high dielectric stress is only experienced in the region around where the two halves are close. To avoid partial discharge in air around this region, potting can be done to

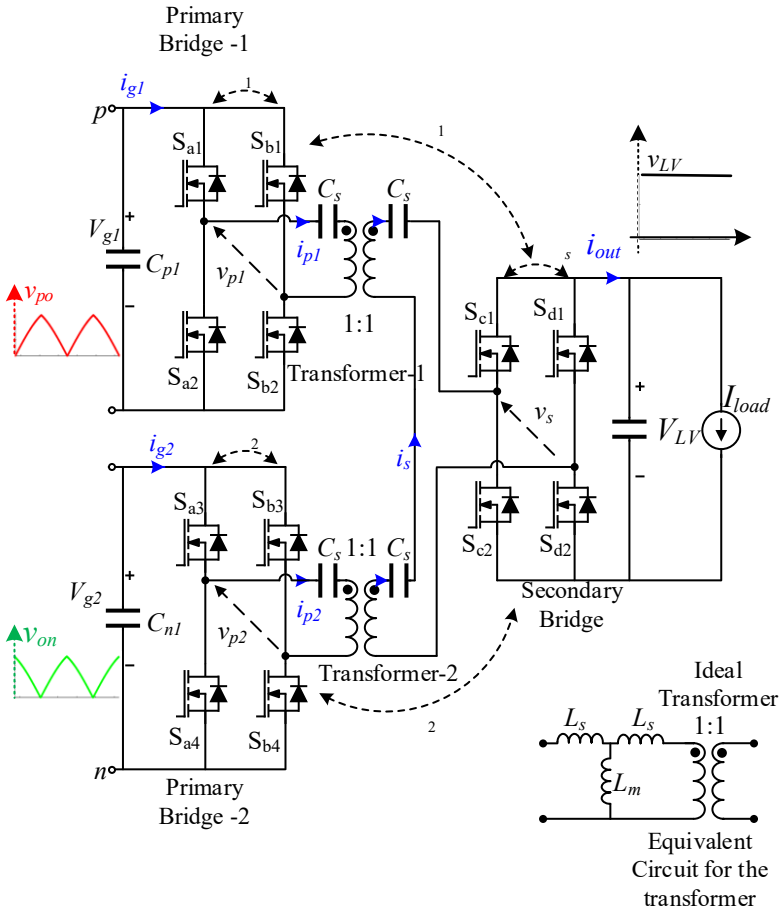


Fig. 6.3: Triple Active Bridge Schematic with Proposed Insulation Concept for Transformer

replace air with a much higher dielectric strength material. The windings and most of the ferrite volume need not be potted. This significantly simplifies the fabrication process since only small regions are potted. The thermal conductivity to ambient can also be maintained high with this approach. The proposed insulation concept can be used in conventional ISOP multi-module SST converters. The influence of this insulation approach on the Triple Active Bridge DC-DC topology proposed for MV unfolding approach is discussed in the next section.

6.3.3 Triple Active Bridge Converter Analysis with Low Magnetizing Inductance

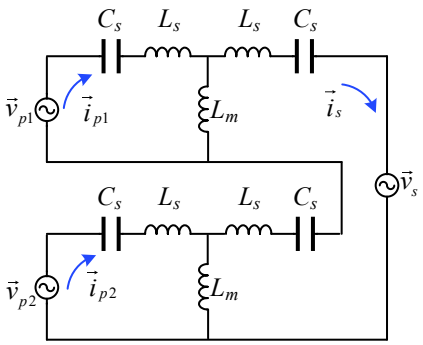


Fig. 6.4: Equivalent circuit of Triple Active Bridge CLLLC converter for fundamental harmonic analysis

With the proposed insulation approach the magnetizing inductance will not be very high due to the air-gap required for insulation between the two halves of the core. This reduced magnetizing inductance will increase the magnetizing current. If a proper switching frequency and magnetizing inductance can be designed than this magnetizing current can be advantageously used for ZVS switching of the H-bridge devices. The analysis of the triple active bridge is revisited considering magnetizing inductance of the transformers. Each winding of the transformer has a series resonance capacitor connected. This compensates for the leakage inductance of that winding. Having capacitor per winding keeps symmetry in the electrical structure of the topology. The topology proposed for the 80 kW design is shown in Fig 6.3. This topology will be referred to as the Triple Active Bridge CLLLC converter. The equivalent circuit of the resultant transformer is shown in Fig 6.3. The turns ratio of the ideal transformer is selected as physical turns ratio of the transformer.

The operation of the TAB bridges is still kept the same as discussed in chapter 5. The primary bridge-P1, bridge-P2 and secondary bridge-S generate quasi-square wave voltages v_{p1}, v_{p2}, v_s respectively. The definitions for phase-shifts and duty cycle of these voltages are given in Fig. 5.4. The equivalent circuit based on the fundamental approximation is shown in Fig. 6.4. Only the fundamental component of the bridge voltages are considered to perform the analysis.

The effective tank current on the secondary side is given by,

$$\vec{i_s} = \frac{(\vec{v_{p1}} + \vec{v_{p2}}) - (K_{sm} + 1)\vec{v_s}}{j4X_{s,w}(1 + K_{sm}/2)}. \tag{6.1}$$

Here, $X_{s,w} = \omega_s L_s - \frac{1}{\omega_s C_s}$ is the impedance of the resonant tank per winding at angular switching frequency ω_s and $K_{sm} = X_{s,w}/X_m$ where, X_m is the impedance of the magnetizing inductance.

Output power is given as,

$$P_{\text{out}} = \frac{8V_{\text{out}} \sin(\frac{\alpha_s}{2})}{\pi^2 4X_{s,w}(1 + K_{sm}/2)}[V_{g1} \sin\frac{\alpha_1}{2} \sin\phi_1 + V_{g2} \sin\frac{\alpha_2}{2} \sin(\phi_2)] \tag{6.2}$$

Examining the secondary tank current and the output power equations and comparing with the equations 5.3 and 5.4 reported in chapter 5, it can be seen that the results are very similar. The only difference in the equations is the change in effective impedance. $K_{sm}/2$ is the extra impedance that is seen other than the series resonant tank impedance. The effect of lower L_m of the transformer is slight decrease in the power transfer for the same operating conditions. The control approach and modulation technique proposed in chapter 5 are still applicable.

6.4 Fabrication Details

The transformer fabrication constraints predominantly influenced the circuit parameters used for the 80 kW DC-DC module prototype. Design iterations are carried out for the transformer along with the DC-DC converter design. The availability of ferrite cores, series capacitors to compensate for the resulting leakage inductance, and vacuum potting chamber size decided the final design. The circuit parameters for the final design for 80 kW module are given in Table. 6.5. The fabrication details of the transformer that heavily influenced the converter design is given in the next section.

Table 6.5: Circuit parameters for the TAB CLLLC 80 kW design

Circuit parameter	**Value**
Series inductance per winding, L_s	10.4 µH
Series capacitance per winding, C_s	1.5 µF
Magnetizing inductance per transformer, L_m	105.7 µH
Switching frequency, f_s	50 kHz

6.4.1 Medium Voltage Isolated High Frequency Transformer

The insulation concept proposed in section 6.3.2 is used for the transformer.The fabricated transformer picture is shown in Fig. 6.5. The blown-out CAD model of the transformer (see Fig. 6.6) shows the fine details of the transformer. The transformer is fabricated as two halves, primary on top and secondary half on the bottom. Both these halves are separated by an isolation barrier. The isolation barrier is a 1.6 mm thick sheet of G10 material. The dielectric strength of the G10 material is 20 kV/mm. The sheet can handle voltage stress of up to 31 kV. The sheet is sized to provide the creepage and clearance between the primary and secondary windings as recommended by UL2877. The ferrite plates on both sides of the G10 disc help increase the magnetizing inductance and also make the design more tolerant to misalignment of the halves of ferrite cores.

The bobbin structure is 3D printed as four individual pieces. Nylon material is used in the 3D print to withstand high temperature expected during converter operation. Each half of the bobbin has two sections, a inner-bobbin and an outer-bobbin. The bobbin structure is designed to space out the winding turns. This spacing helps to reduce the winding capacitance. The spacing also allows for better heat dissipation by letting the forced air to flow through the windings to reach the inner sections of the transformer. The winding structure is able to achieve ultra-low winding capacitance of around 50 pF.

For mechanical support, quarter-inch thick 12”X 12” G-10 sheets are used as the top and bottom base plates. Slots are grooved in the base plates to allow airflow to reach the inner sections of the transformer. Fiberglass rods and screws are used to apply the clamping pressure to hold the structure together. 5 mm thick Silicone tape is applied over each U-core

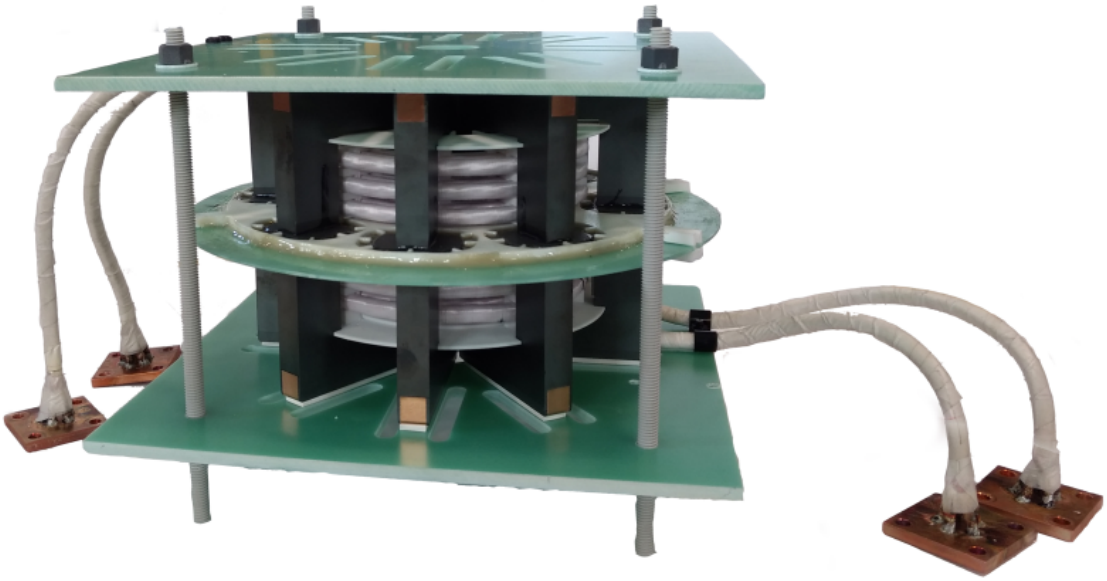


Fig. 6.5: Fabricated 80 kW transformer with 15 kV rated isolation strength

ferrite. This helps to evenly distribute the pressure applied by the base plates over all U cores. The transformers' key fabrication details are summarized in Table 6.6.

For the detailed analysis of the electric field strength in the transformer structure, 3D FEM simulation is done. The top side core and winding potential are set to 10 kV, and the bottom half is set to 0 kV. It can be seen that the high field strengths just exist in the region between the two halves of the transformer. Ferrite plates are rounded at the corners to reduce the field intensities. A close up result for the fields is shown in Fig. 6.8. The fields at the corners of the ferrite are high enough for the air around that region to break down and cause partial discharge. To prevent this, the ferrite plates are potted to displace the air with a high dielectric strength material. 3M Scotchcast Electrical Resin 280 material, which has a dielectric strength of 14.8 kV/mm, is used as the potting material. The potting is done in a thermal vacuum chamber. A picture of the vacuum potting process is given in Fig. 6.10.

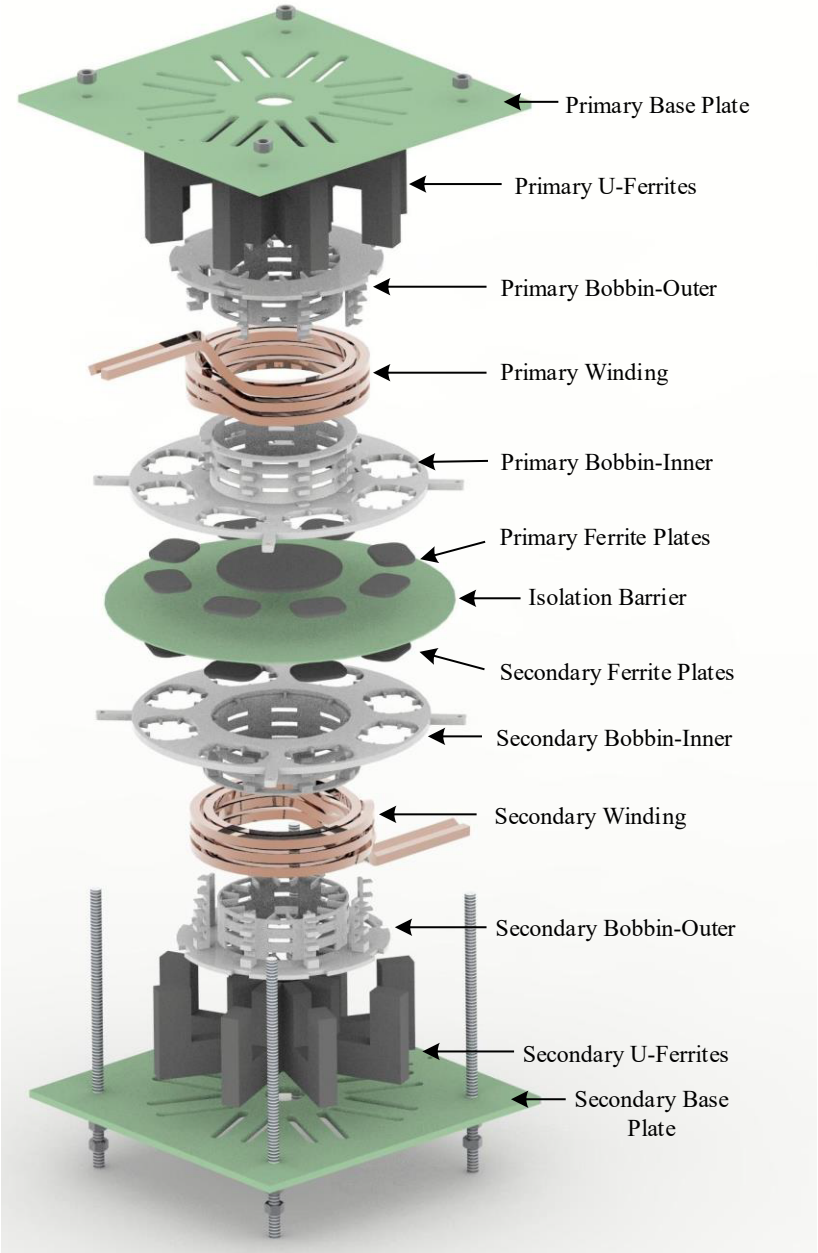


Fig. 6.6: Blown-out CAD model view of the 80 kW transformer

Table 6.6: Key fabrication details of the MV transformer

Ferrite U-core	U93/76/16 size, 3C94 material.
Ferrite plates	Custom shape fabricated using PLT64/50/5 square plates, 3C94 material
Wire	9750 strands of 42 AWG, single nylon serve. Formed to square-profile.
Insulation disk	G-10 material, 1.6 mm thick, electric strength: 20 kV/mm at 1.6 mm thickness dielectric constant: 5.20
Potting	3M^{TM} Scotchcast^{TM} Electrical Resin 280 material electric strength: 14.8 kV/mm at 3.175 mm thickness dielectric constant: 3.50
Bobbin	3D printed in Nylon material

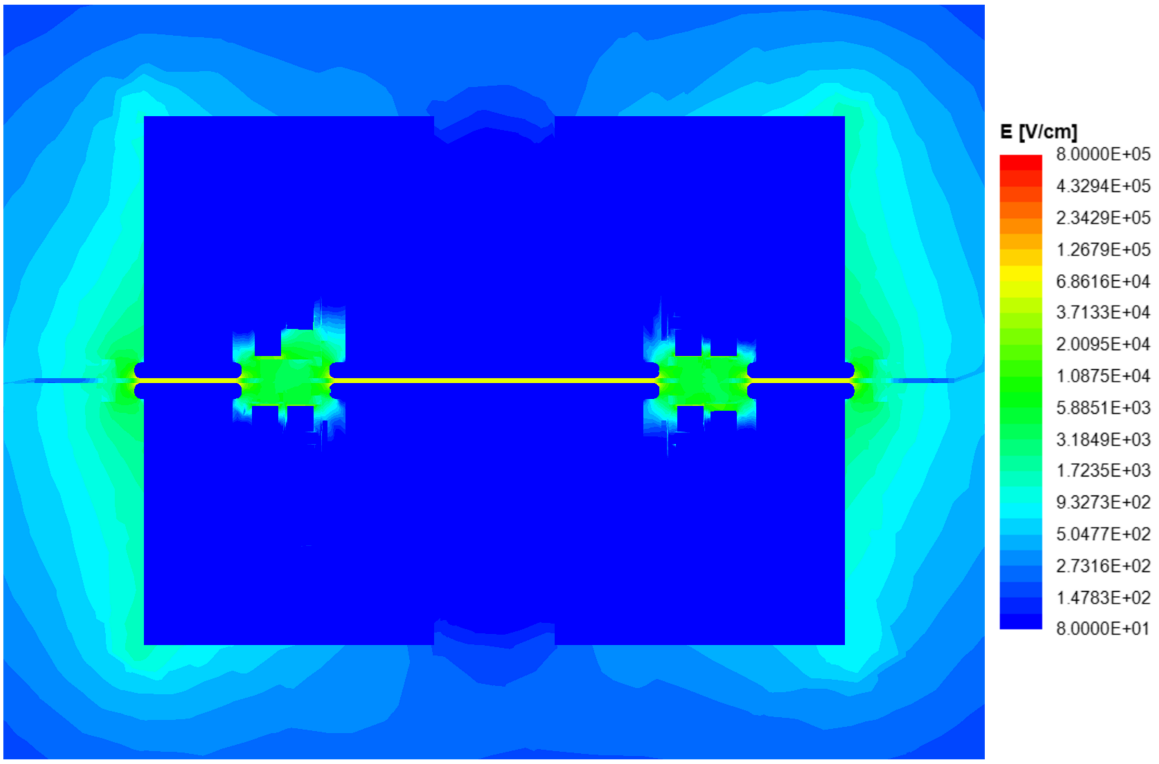
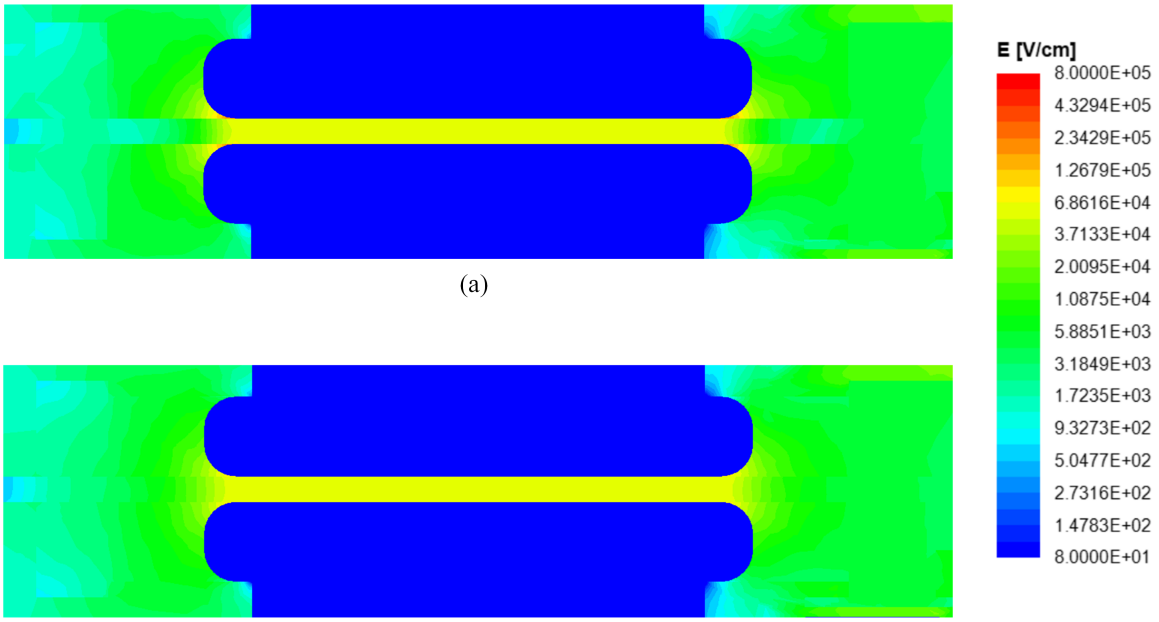


Fig. 6.7: Electrostatic FEM simulation result for the transformer under 10 kV voltage stress between the two halves.Front cross-sectional view is shown here.



(a)

(b)

Fig. 6.8: Electric field strength between the two halves of the transformer (a) before potting (b) after potting.

Fig. 6.9: Close-up picture of potted ferrite plates

Fig. 6.10: Picture of vacuum potting setup.

Table 6.7: Major components in the H-bridge assembly

Component	**Rating**	**Part number**
Switching devices	1200 V, 400 A, 4.0 mΩ SiC half-bridge module	CAB450M12XM3
DC-link film capacitor	4 X 55 µF, 1200 V, 10.5 nH ESL	CX55U1200D40, 4 in parallel
DC-link ceramic capacitor	30 X 33 nF, 1000 V, C0G	C2220X333JDGAC, 30 in parallel
Series resonant capacitor	1.5 µF, 500 Vac, 10%	155LC2500K5HM6

6.4.2 H-bridge Fabrication Details

The TAB CLLLC is designed to soft-switch all the devices at all grid angles at most loading conditions. Hence, MOSFETs with lower conduction losses are preferred since switching losses under ZVS conditions are negligible. Just a few high current SiC MOSFET module options are commercially available. CAB450M12XM3 from CREE is shortlisted for the final design due to the low resistance it offers. The XM3 package has low inductance (6.7 nH) and yet allows for a simple busbar design. Details of the major parts of the H-bridge are given in Table. 6.7.

The blown-out CAD model view (see 6.11) shows all the components in the H-bridge

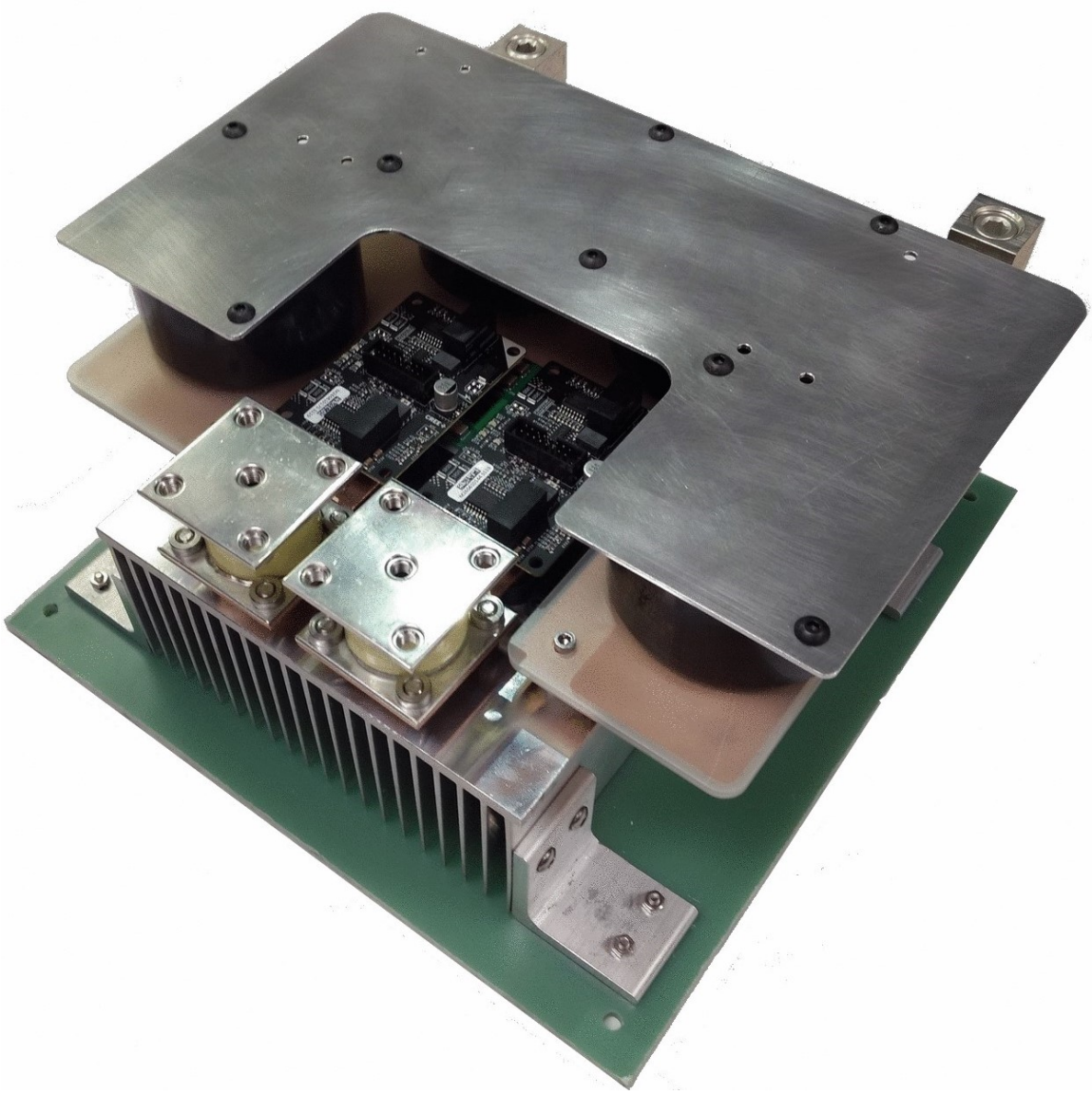


Fig. 6.11: Fabricated 80 kW H-bridge

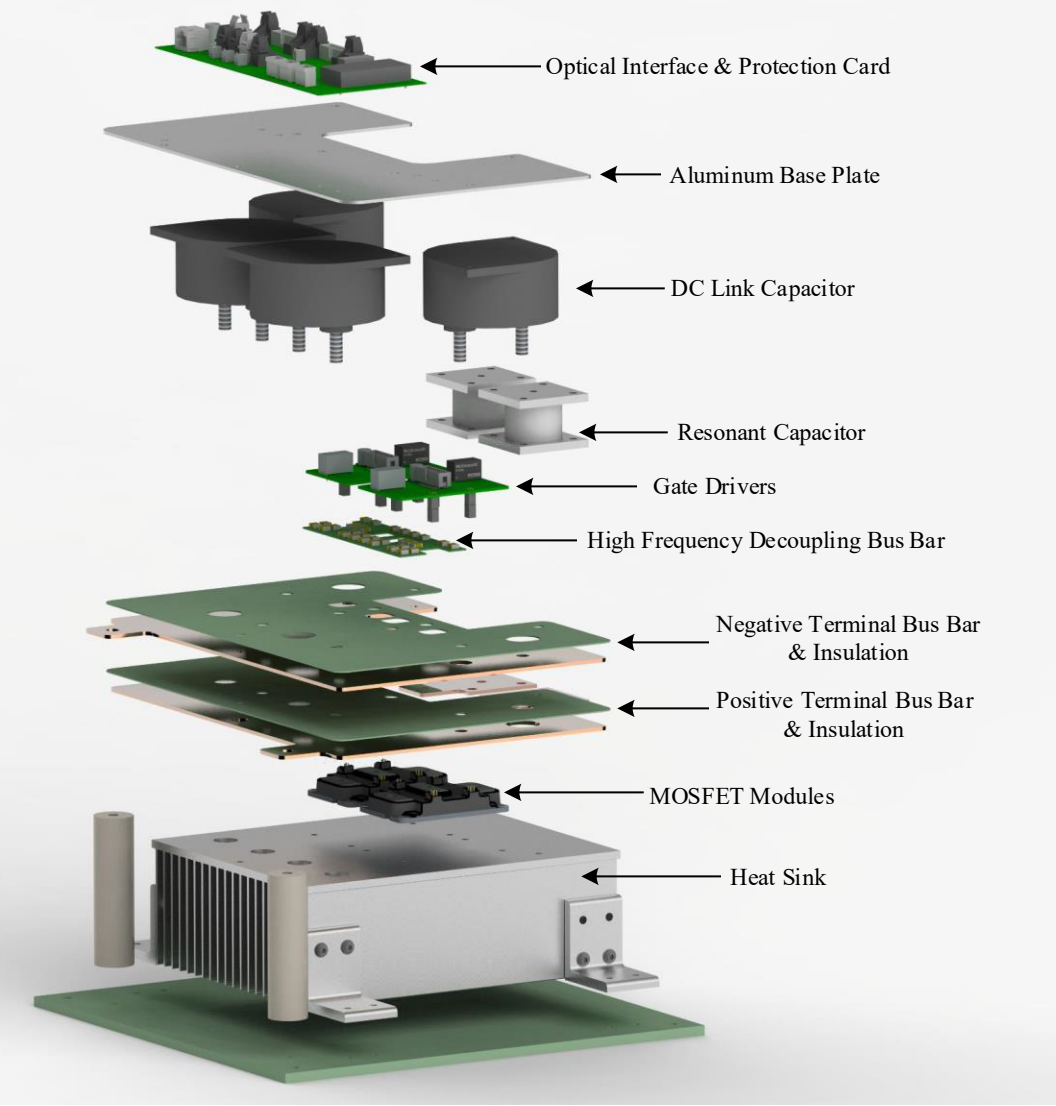


Fig. 6.12: Blown-out CAD model view of the H-bridge assembly

assembly. One of the fabricated H-bridge assemblies is shown in Fig. 6.12. The heat sink is tied to the negative rail busbar of the H-bridge. Fiber optics are used for sending the gate signals and communication signals to each H-bridge. Each bridge monitors the DC-link current, DC-link voltage and transformer winding current. Analog based protection is implemented for each H-bridge that turns off the converter if the sensed values are not within the safe limits.

Copper busbar is fabricated inhouse. The CAD design is done in SolidEdge software, and after the design verification, the copper busbar plates were machined inhouse. 2.362 mm thick copper plates are used to machine the busbar plates. A 0.8 mm thick G10 sheet is used as insulation between positive and negative busbar plates. 3 mm clearance is maintained between the positive and negative terminals in the busbar. Four were used as the DC link capacitor on each bridge. For very high-frequency decoupling capacitance, an array of 30 ceramic capacitors on PCB are directly mounted across the module terminals. The impedance plots measured using an LCR meter across the MOSFET terminals for the film capacitors with copper busbar and for ceramic capacitors on PCB are shown in Fig. 6.13. The effective series inductances estimated from the impedance data are 5.7 nH and 2.2 nH for copper busbar and PCB busbar respectively.

6.5 Experimental Test Results

One Triple Active Bridge DC-DC converter is built. The picture of this hardware prototype is shown in Fig. 6.14. The DC-DC module consists of three H-bridges and two transformers. A recirculating test setup was developed to test the converter at the rated output power of 80 kW. The block diagram of this setup is shown in Fig. 6.15. The output of the converter is fed back to the input ports which are connected in series. The power supply-1 and power supply-2 only provide for the losses in the converter. This setup allows for accurate loss measurements in the converter. For the tests, analog based protection limits are set to 120 A, 925 V and 300 A for DC-link current, voltage and transformer winding currents respectively.

The steady-state waveforms for the TAB converter operating at equal input voltages

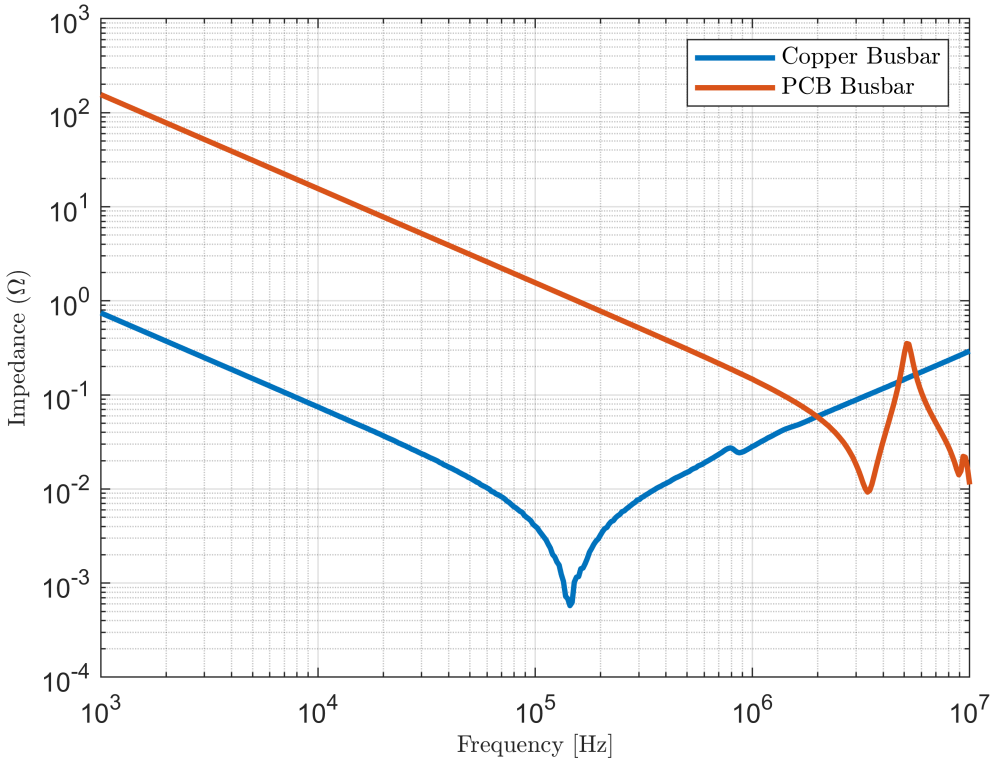


Fig. 6.13: Measured impedance of the copper busbar with film capacitors and the PCB busbar with ceramic capacitor across the MOSFET terminals.

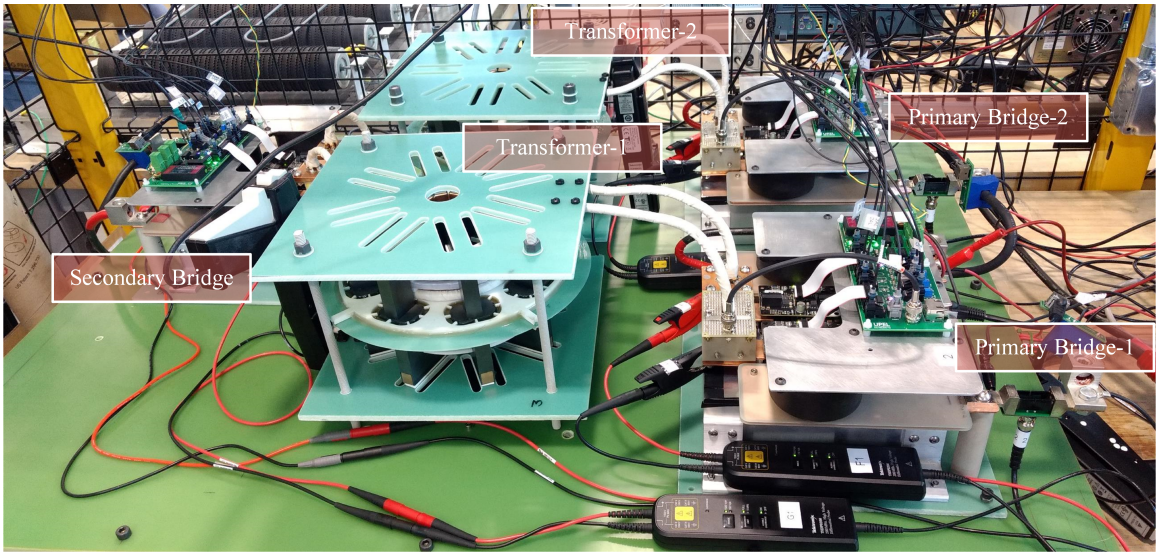


Fig. 6.14: Picture of hardware prototype of the 80 kW Triple Active Bridge.

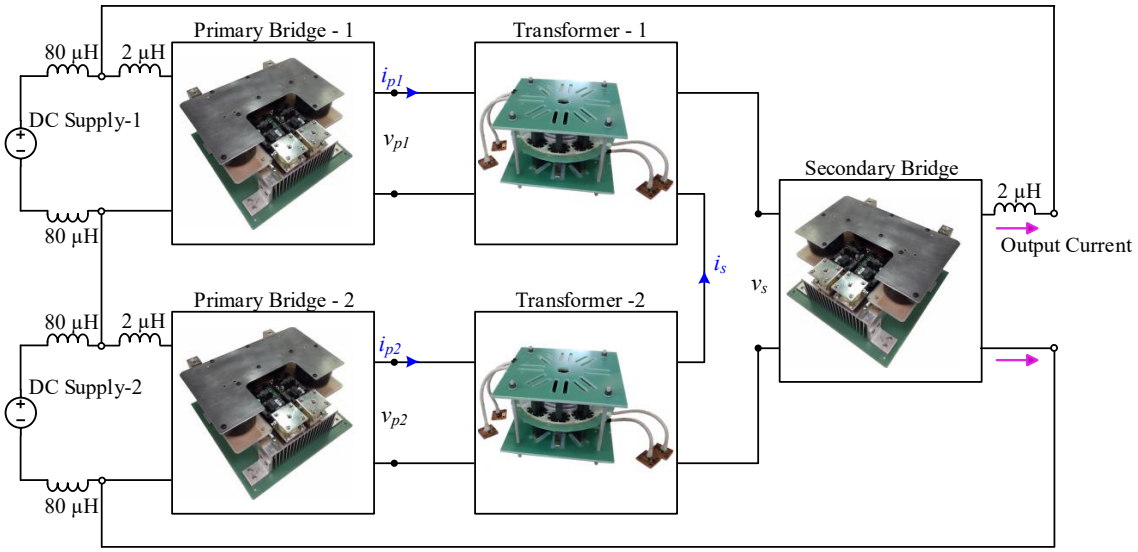


Fig. 6.15: Picture of hardware prototype of the 80 kW Triple Active Bridge.

are shown in Fig. 6.16. Each input voltage is set to 420 V. Since the output is connected to the series connection of input voltages, it is set to 840 V. These input voltage settings emulate the 60^o grid phase angle point at 4.16 kV grid. The transformer winding currents are close to sinusoidal which helps in reducing radiated EMI. The switching instant currents are in the direction to help zero-voltage switch all the semiconductor devices reducing the switching losses of the devices to be zero. Experimental result for unequal voltages is given in Fig. 6.17. DC supply-1 is set to 594 V and DC supply-2 is set to 217 V . This emulates the 75^o grid phase angle at 4.16 kV grid. The measured efficiency results from the recirculating tests at equal voltage operating point is given in Fig. 6.18. The peak efficiency of 99.14% is measured at 35% load and full load efficiency is 98.01%.

6.6 Summary

System-level design of a 560 kW, 4.16 kV 3-phase AC to 800 VDC Solid State Transformer design is given. A novel insulation concept is presented for the medium voltage isolated high-frequency transformer. The presented method achieves medium voltage insulation without complicating the fabrication or cooling requirements for the transformer.

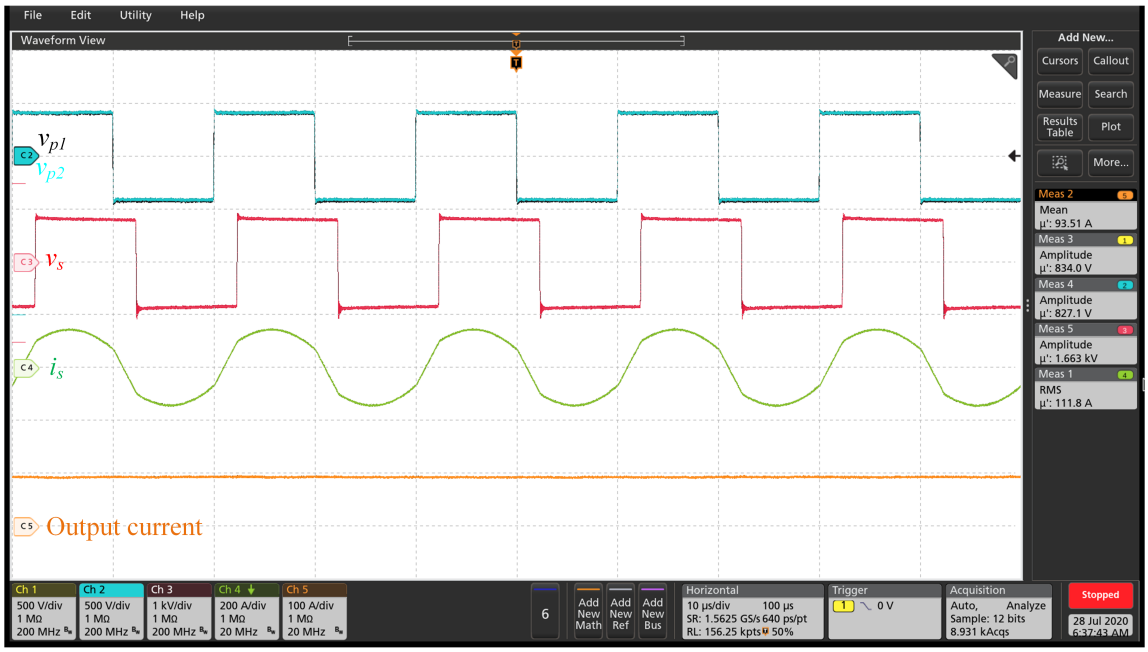


Fig. 6.16: Experimental waveforms at 80 kW for TAB converter with both the input DC supplies set to 420 V.

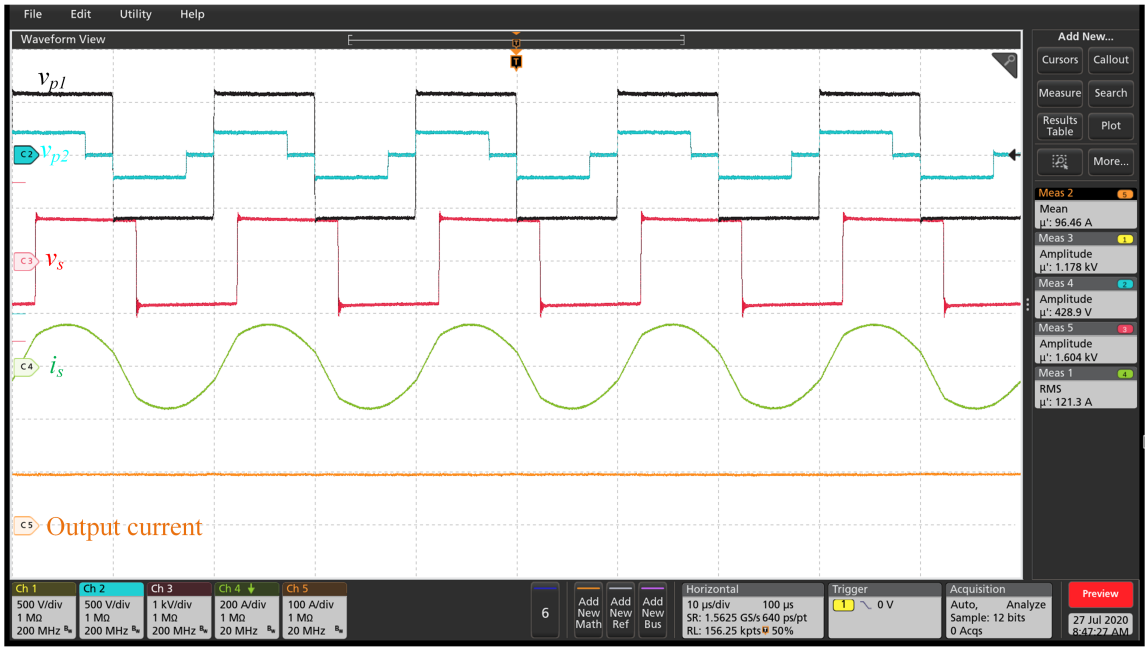


Fig. 6.17: Experimental waveforms at 80 kW for TAB converter with DC supply-1 set to 594 V and DC supply-2 set to 217 V.

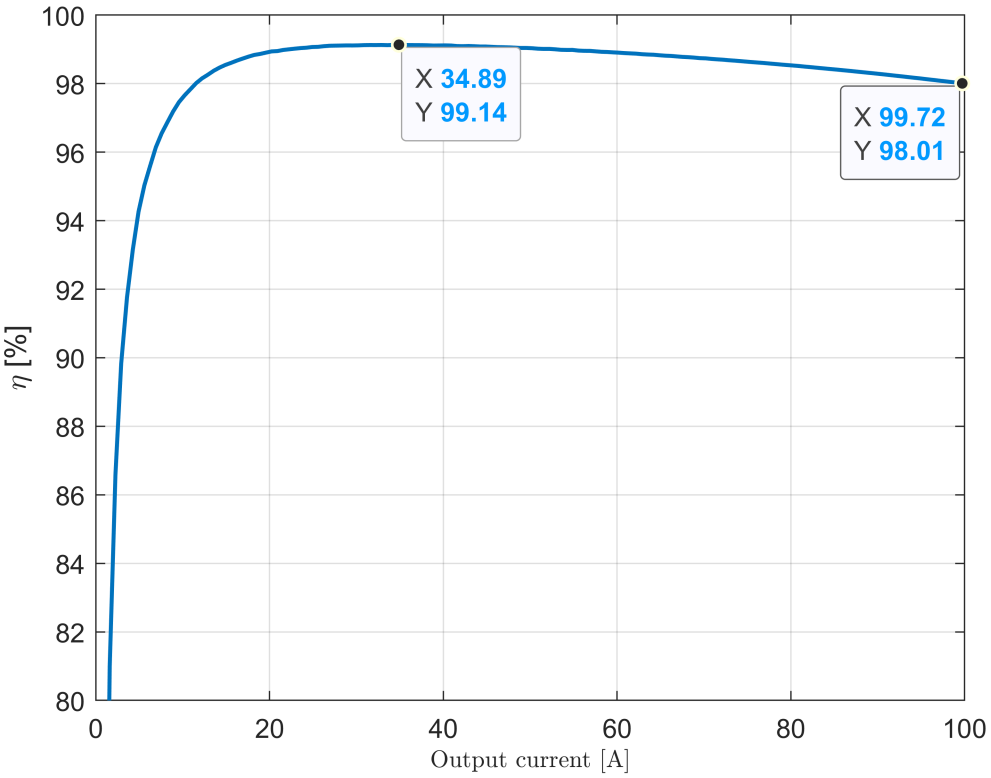


Fig. 6.18: Experimental efficiency result for TAB converter from no-load to full load for input voltages set to 420 V each. The highest efficiency point and full load efficiency points are highlighted.

The design and fabrication details of the transformer are discussed. One DC-DC converter module of the proposed topology is built. The converter operation is experimentally verified at 80 kW for different input voltage operating points. High-efficiency results measured on the prototype validated the efficient operation of the proposed DC-DC topology.

CHAPTER 7

Conclusions and Future work

Fast improvements in battery performance and the simultaneous reduction in price has increased the appeal for electric vehicles. Adoption of battery electric vehicles (BEVs) and plugin hybrid electric vehicles (PHEVs) has increased over the past few years. With the anticipated need to improve the charging infrastructure, there is renewed interest and need to develop power converter topologies that are cost-effective for battery charging applications. This dissertation has worked towards reducing the cost and volume of power converters required for electric vehicle charging applications. To achieve this objective, focus was placed predominately on reducing the number of power processing stages and also reducing the size of passive components per stage. Using high-frequency transformer for galvanic isolation; connecting directly to medium voltage grid to eliminate the need for service transformer; eliminating the need for grid-side filters were the solutions used to achieve the above objectives.

7.1 Summary of Contributions

This dissertation aimed at proposing new isolated AC to DC converter topologies for DC fast charging (DCFC) applications and grid-connected medium voltage converter for DC microgrid type applications. Both these applications have similarities that the input is three-phase utility mains voltage and output is DC. Battery chargers require efficient wide voltage range operation. SST requires efficient wide load range operation. Contributions from this dissertation are summarized here.

7.1.1 Novel Implementation for Three-Phase Unfolding Approach

Classification of three-phase AC to DC topologies reported in literature into three approaches is done identifying their key features. A new emerging approach based on soft

DC-link, referred to as three-phase unfolding approach, is identified as an ideal approach to realize battery charger topologies. This approach is typically implemented using two separate DC-DC converters in the DC-DC stage. Each DC-DC converter is processing time-varying power and has to be designed to temporarily process full power. This reduces the achievable power density and efficiency due to low utilization of the converters.

A novel three-level bridge named as Three-Level Asymmetrical Full Bridge is proposed to improve the power density and efficiency of the unfolding based converters. The proposed converter significantly improves the power density and efficiency since only one DC-DC converter is required as opposed to two converters. First-order comparison for conduction loss, switching loss, and filter size are provided for the SOA and the unfolding approach with 3LAFB. Compared to SOA, the switching losses are completely eliminated at the cost of 25% increase in conduction losses. Grid filter size is estimated to be reduced by 90% in volume.

7.1.2 New Battery Charger Topology

State-of-the-Art battery chargers are implemented using the two-stage approach. These converter designs suffer from lower power density and efficiency. A new battery charger topology is developed based on the Three-Level Asymmetrical Full Bridge (3LAFB). Ideal operation of the converter is presented, and the phenomenon of duty cycle loss is discussed. Modulation for 3LAFB converter is proposed that allows the converter to soft-switch across all grid angles. The proposed modulation also minimizes the conduction loss of the 3LAFB devices. Design procedure for a 2 kW battery charger is given. Detailed efficiency measurement results at different output voltage and output current loading conditions for three unique input soft DC-link points are given. Simple closed-loop control is proposed for grid synchronization. The proposed control approach uses two independent linear control loops to achieve the power factor correction and output current regulation. Hardware prototype is built, and experimental results are presented to validate the claims of improved power density and efficiency.

7.1.3 Three-Phase Medium Voltage Unfolding SST Topology

Using Solid State Transformer for grid interface of higher power DC loads is identified as a promising approach to eliminate the need for a line-frequency service transformer. Both space and time for service transformer installation will be saved. Literature review of this emerging topic is given. The cost of implementation of these converters is still high, and this higher cost have limited their adoption.

In this dissertation, the concept of three-phase medium voltage unfolding is introduced. The concept uses relatively low-cost silicon high voltage IGBTs to realize the AC-DC stage. A new three-port series input parallel output DC-DC structure is proposed for the DC-DC stage. The proposed approach results in a quasi-single stage SST improving the overall efficiency due to reduced number of power processing stages.

A new three-port magnetically coupled DC-DC topology called the Triple Active Bridge converter is proposed for realizing the DC-DC module for the unfolding SST. Steady-state analysis is presented for this new topology using fundamental harmonic analysis. Modulation technique for the topology is proposed to maintain soft-switching over the entire line cycle. A 2 kW hardware prototype for this topology is fabricated. Experimental results are provided at three extreme input operating points. Soft-switch and high efficiency is maintained at all operating points, despite wide voltage swing at the input soft DC-links. A closed-loop control structure for grid integration for one module is presented. A unique decoupling method is used to design the control loops. Simulation results are presented that validated the control approach.

7.1.4 Novel Insulation Concept for Medium voltage Isolated High Frequency Transformer

Designing the DC-DC stage to meet the isolation requirements while simultaneously maintaining high power density is a major challenge in SST. A review of the medium voltage insulation concepts for high-frequency transformer is done. A novel insulation concept is presented for the medium voltage isolation of the high-frequency transformer. The presented method achieves medium voltage insulation without complicating the fabrication or cooling

requirements for the transformer. The idea is to confine the high electric fields to a small region. Then only this small region needs to be potted with a high dielectric strength material. This is achieved by segregating the primary and secondary side of the transformer on either side of an insulation disk. Just a small region of the transformer required potting. This significantly reduced the fabrication efforts. Finite element analysis for electric field stress is done for the final design. The results confirm the isolation withstnd capacity of the transformer. Fabrication details of the transformer for 80 kW TAB converter are provided. Two transformers are built for realizing one TAB converter module. The converter operation is experimentally verified at 80 kW for different input voltage operating points. High-efficiency results measured on the prototype validated the efficient operation of the proposed DC-DC topology and the transformer.

7.2 Future Research Directions

This dissertation has proposed a new approach to implement unfolding based AC to DC converters. Only two new topologies are proposed and analyzed in this dissertation. Most DC-DC topologies that have H-bridge on the primary side can be easily adapted to work with Unfolder using the 3LAFB . For example, 3LAFB variant of the popular Dual Active Bridge Converter can be used for bi-directional low voltage three-phase AC to DC applications. Each new topology has to be analyzed and an appropriate control technique has to be developed explicitly to that topology. This opens up many opportunities for further research.

High power wireless power transfer (WPT) system is a second application where the proposed unfolding approach can be promising. These systems are typically realized in two stages. Potential efficiency and power density benefits can be achieved by implementing unfolding approach for WPT systems.

In this dissertation, series stacked Triple Active Bridge Converter is proposed for the DC-DC stage in the MV unfolding SST. The three-port nature of the converter makes it challenging to ensure voltage sharing across the modules. Very limited literature is available on series stacking of three-port converter. More work needs to be done here to ensure stable

operation of the unfolding SST.

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CURRICULUM VITAE

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J1 D. B. Yelaverthi, R. Hatch, M. Mansour, H. Wang and R. Zane, 3-Level Asymmetric Full-Bridge Soft-Switched PWM Converter for 3-Phase Unfolding Based Battery Charger Topology, in *IEEE Transactions on Power Electronics, under internal review.*

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