DESIGN AND CONTROL OF SERIES RESONANT CONVERTERS

FOR DC CURRENT POWER DISTRIBUTION APPLICATIONS

by

Hongjie Wang

A dissertation submitted in partial fulfillment
of the requirements for the degree

of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

Approved:

| | |
|---|---|
| Regan Zane, Ph.D. | Zeljko Pantic, Ph.D. |
| Major Professor | Committee Member |
| | |
| Rajnikant Sharma, Ph.D. | Reyhan Baktur, Ph.D. |
| Committee Member | Committee Member |
| | |
| David Geller, Ph.D. | Mark R. McLellan, Ph.D. |
| Committee Member | Vice President for Research and |
| | Dean of the School of Graduate Studies |

UTAH STATE UNIVERSITY
Logan, Utah

2018

# ABSTRACT

Design and Control of Series Resonant Converters

for DC Current Power Distribution Applications

by

Hongjie Wang, Doctor of Philosophy

Utah State University, 2018

Major Professor: Regan Zane, Ph.D.
Department: Electrical and Computer Engineering

With the growth of renewable energy usage and energy storage adoption in recent decades, people have started to reevaluate the possible roles of dc systems in current and future electrical systems. The dc voltage distribution has been applied in various applications, such as data centers, aircraft industry and dc micro-grids, for high efficiency and power density. However, for some applications such as subsea gas and oil fields, off-shore wind farms and ocean observatory systems, the dc current distribution is preferred over dc voltage distribution for its low cost, and robustness against cable impedance and faults. Design and control of dc power distribution systems for different applications is an emerging research area with complex technical challenges. This dissertation solves the technical challenges in analysis, design, modeling, control and protection of series resonant converters (SRCs) for dc current distribution applications. An optimum design that has high efficiency, high reliability, low EMI and minimum required control efforts for the SRC with constant input current has been achieved and demonstrated by applying the analysis and design procedures developed in this dissertation. The modeling and analysis presented in this dissertation represents an operating condition that has not been studied in the literature and could be easily extended to other resonant topologies. Explicit analytical expressions

have been provided for all key transfer functions, including input impedance and control-to-output, offering valuable resources to design feedback regulation and evaluate system stability. Based on the small signal model of the SRCs, with the consideration of the cable impedances, this dissertation presents an impedance based stability analysis for dc current distribution systems, and provides associated control strategies and control design for both the SRCs and the overall dc current distribution system to ensure stable operation of the entire system. The proposed analysis, design procedure, stability evaluation, control strategy and protection techniques in this dissertation can be applied to a wide range of similar scenarios as well, which greatly increases their value.

(211 pages)

PUBLIC ABSTRACT

Design and Control of Series Resonant Converters

for DC Current Power Distribution Applications

Hongjie Wang

With the growth of renewable energy usage and energy storage adoption in recent decades, people have started to reevaluate the possible roles of dc systems in current and future electrical systems. The dc voltage distribution has been applied in various applications, such as data centers and aircraft industry, for high efficiency and power density. However, for some applications such as subsea gas and oil fields, and ocean observatory systems, the dc current distribution is preferred over dc voltage distribution for its low cost and robustness against cable faults. Design and control of dc power distribution systems for different applications is an emerging research area with complex technical challenges. This dissertation solves the technical challenges in analysis, design, modeling, control and protection of series resonant converters (SRCs) for dc current distribution applications. An optimum design that has high efficiency, high reliability, and minimum required control efforts for the SRC with constant input current has been achieved and demonstrated by applying the analysis and design procedures developed in this dissertation. The modeling and analysis presented in this dissertation represents an operating condition that has not been studied in the literature and could be easily extended to other resonant converter topologies. Explicit analytical expressions have been provided for all key transfer functions, including input impedance and control-to-output, offering valuable resources to design feedback regulation and to evaluate system stability. Based on the control strategies and control design presented in this dissertation, stable and reliable operation of dc current distribution systems with long distance cable has been achieved and demonstrated. The proposed analysis, design procedure, stability evaluation, control strategy and protection techniques

in this dissertation can be applied to a wide range of similar scenarios as well, which greatly increases their value.

Dedicated to my father Guocheng Wang, my mother Chunmei Sun and my wife Siya Chen.

## ACKNOWLEDGMENTS

I would like to express my sincerest gratitude to my advisor, Prof. Regan Zane for his guidance, encouragement and support throughout my PhD program. Prof. Zane's help, trust and tolerance allowed me to freely explore the unknown, despite my ignorance and stubbornness, and develop more as a person than I could possibly have imagined.

Special thanks go to my committee members, Prof. Zeljko Pantic, Prof. Rajnikant Sharma, Prof. Reyhan Baktur and Prof. David Geller for reviewing my work and providing valuable advice and support on my research progess.

I am grateful to Utah State University Power Electronics Lab (UPEL) and the Raytheon Company for the academic and financial support which allowed me to continue my education and conduct cutting-edge research in the power electronics field. I deeply appreciate the help from my colleagues at UPEL for the collaboration and wonderful experiences in the lab. The discussions and help from them were very important and beneficial to this work. I would like thank our lab manager Ryan Bohm who provided great help and support not only to this work but also to the entire team. I would like to thank Tarak Saha who collaborated on this work, brought new ideas, and provided great help and support.

Finally, I would like to thank my family and especially my wife Siya Chen for all the unconditional love, inspiration and support throughout my graduate career. Their support and inspiration has made the completion of the PhD program possible, and I will always be grateful to them.

Hongjie Wang

CONTENTS

LIST OF TABLES

# LIST OF FIGURES

## ACRONYMS

| | |
|---|---|
| AC | Alternating current |
| DC | Direct current |
| ADC | Analog to digital convertor |
| DAC | Digital to analog converter |
| SRC | Series resonant converter |
| PRC | Parallel reonant converter |
| DABSRC | Dual active bridge series resonant converter |
| RMS | Root mean square |
| ZVS | Zero voltage switching |
| ZCS | Zero current switching |
| PI | Proportional integral |
| Verilog HDL | Verilog hardware design language |
| PLL | Phase lock loop |
| PWM | Pulse width modulation |
| SR | Synchronous rectification |
| EMI | Electromagnetic interference |

CHAPTER 1

INTRODUCTION

For more than one century, the electric energy has been the dominant energy type that is generated, transmitted and delivered to the end user in both industry and daily life in comparison to other energy types. With respect to other energy types, electric energy has better controllability, more potential to be converted to other energy types efficiently, and is easy to transport and restore. From Fig. 1.1, the total electricity disposition in the US in 2016 is 4146.428 TWh [1]. In recent years, the electricity usage has continued to grow because of the sustainability and environmental concerns from the public and government. Continued research and investigations have been spurred by the growing electricity usage in the field of power generation, power distribution and power consumption equipment, especially in power distribution.
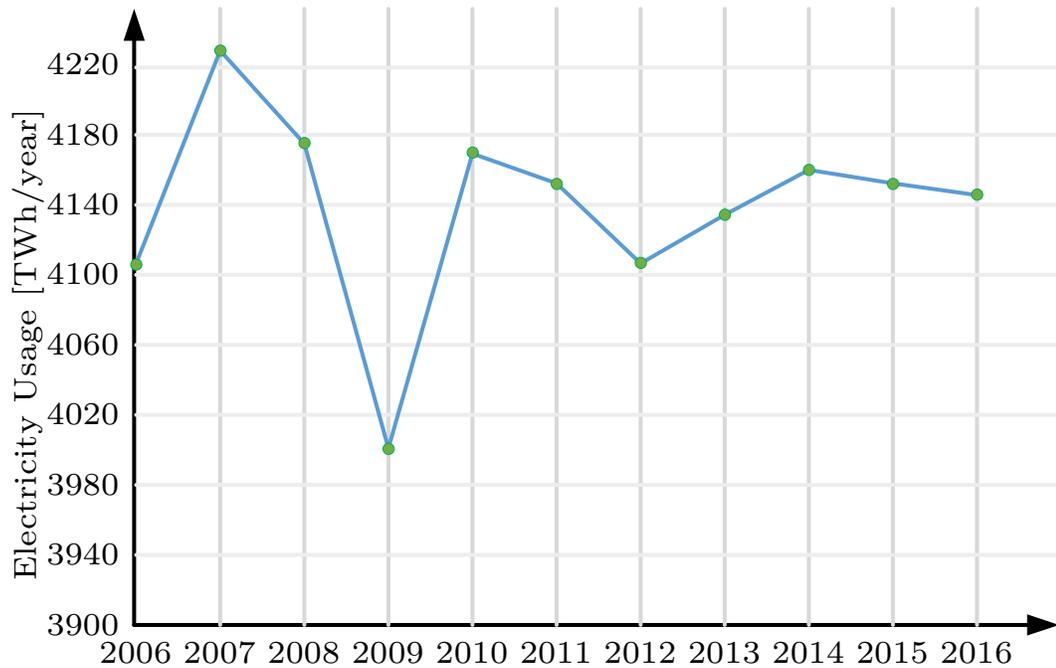


Fig. 1.1: Electricity usage in the United States.

## 1.1 Alternating Current Electricity System

The first electrical systems created by Thomas Alva Edison were completely direct current (dc) from generators to the end users [2]. However, at the early stage of electricity development, techniques for managing and controlling the dc voltages did not exist, which resulted in significant losses and voltage drops when the dc power was transmitted from generators to loads, especially for long distance power transmission and distribution. In order to overcome the serious limitations and resolve the issues, George Westinghouse proposed the development of alternating current (ac) electrical systems. The ac systems allow large amounts of power to be transmitted over long distances from one location to another through transmission lines at a convenient and efficient level by using means of transformers, which had been developed by Nikola Tesla recently at that time [3]. Therefore, the ac system won the well-known "battle of the currents", became dominant and has been considered the better solution for power generation, transmission and distribution since then.

The diagram of an ac electricity system is shown in Fig. 1.2. The ac distribution system has several advantages including easy and efficient voltage transformation, mature circuit breaker protection, and voltage stability and control [4]. One of the greatest benefits of the ac system is that the ac voltage can be easily and efficiently elevated for distribution over distance and again lowered for the end users by using different transformers, as illustrated in Fig. 1.2. The system protection techniques for ac distribution systems are much more mature than for dc distribution systems through the use of circuit breakers. The alternating nature of the ac system results in periodic zero voltage crossings, which helps the circuit breaker to extinguish a fault current arc and protect the system. For power distribution systems, system stability is always a concern. For the ac system, the advantage is that the stable voltage can be controlled independently from real power through the management of reactive power.

## 1.2 Direct Current Electricity System

Although the ac system is still the fundamental electricity type, significant technical
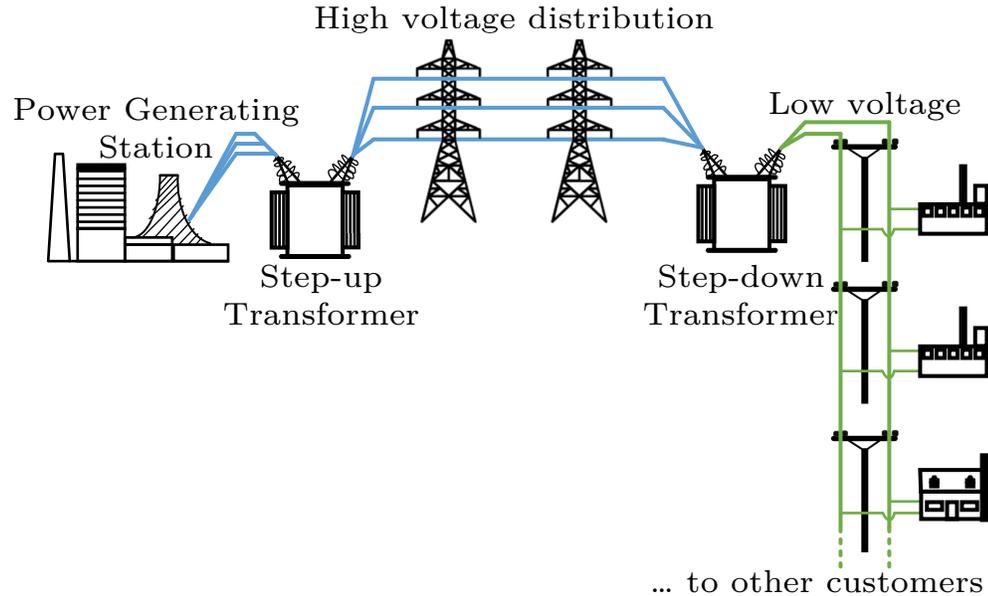
Fig. 1.2: Diagram of an ac electricity system.

developments in direct current electricity systems have been established in the electricity industry as well as power electronics over the last century [5]. The changes and developments motivate researchers and industries to reevaluate which one is the better solution, ac or dc, from the aspects of efficiency, economic and technology.

The significant changes are from loads, sources and energy storages. Nowadays, especially for the domestic and commercial users, many electrical loads inherently need dc power supply, such as advanced lighting systems including LED lighting [6] and electronic ballasts [7], televisions, monitors, communication appliances including mobile phones and modems, computers including the servers in data centers [8, 9],printers, and electric vehicles [10]. From Fig. 1.3, 70 TWh, or 1.8% of the total US electricity consumption, was consumed in data centers [11]. Presently, each electronic load generally still has its own dedicated power supply powered from ac system which requires double conversions (ac-dc and dc-dc), while the ac-dc conversion stage could be avoid if powered from a dc system.

On the other hand, new energy sources have been emerging and widely employed in recent decades. The renewable energy usage grew an average of higher than 5% per year over 2001-2017 from its most recent low in 2001, and keeps increasing. Many renewable
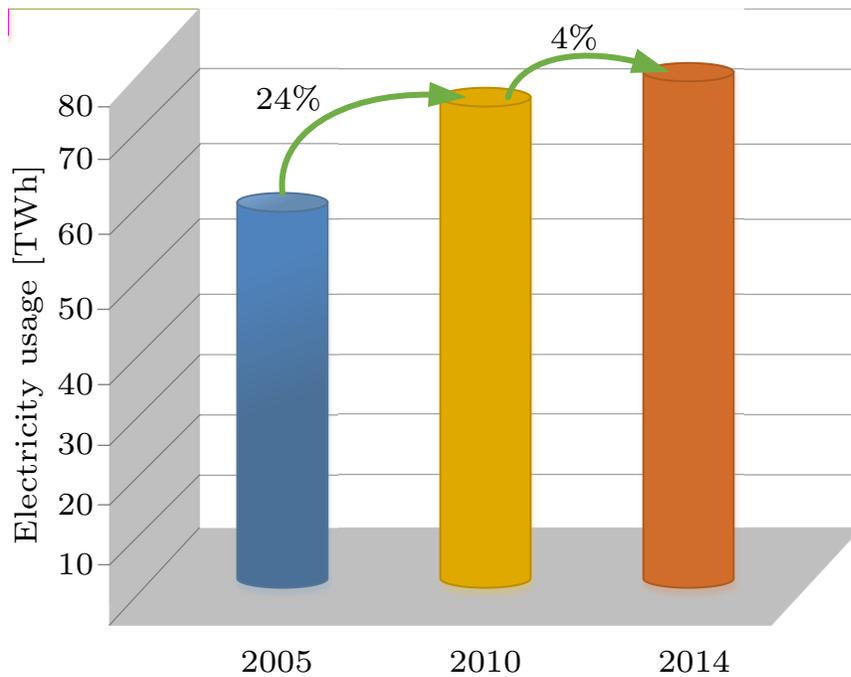
Fig. 1.3: Data center electricity usage in the US.

energy sources, including photovoltaic panels (solar energy), are dc power supplies naturally. Wind energy can also be better optimized if at least part of the wind turbine's capacity is coupled through power conversion which generally includes a dc bus [12]. The multiple conversion losses introduced by the conversion from dc to ac and later back to dc can be avoided if dc system is used.

One drawback for an ac system is that the ac electrical energy intrinsically can not be stored, which means that power generation and consumption have to happen at the same time. In order to improve the efficiency, reliability and controllability of the electrical system, a lot of effort has been made to develop different types of energy storage. Nowadays, in parallel with the renewable energy usage growth, energy storage systems have been widely used in electrical systems. Some of the most important and commonly used energy storage systems, including batteries, fuel cells, super capacitors and flywheels, have dc voltage inherently [13]. Hence, by using a dc system instead of ac system, more efficient and reliable, cheaper, simpler (for both control and manufacturing) energy storage systems can be achieved.

With the consideration of all the above points, people have started to reevaluate the better solution for electrical systems including generation, transmission and distribution, and have done a lot of research on the possible roles of dc systems in direct current electricity systems, i.e. smart grid, micro-grids, renewable energy adoption. In [2], the authors discussed the possible economic advantages that dc distribution can have over ac distribution theoretically, and revealed that using a three-line dc distribution can have considerable economic advantages over three phase ac systems. In [3], the authors presented loss comparison between ac and dc distribution systems, and concluded that ac and dc distribution systems can have the same merit when the loads are equal in ratio under the current power system infrastructure. In [4], the author concluded that the use of residential dc distribution by itself was predicted to be disadvantageous because of the inefficiency of converting bulk ac power to premise dc power. However, the author also showed that this may change when dc generations feed directly into a premise dc bus. In [14], the authors evaluated the losses in ac and dc micro-grids for residential complexes with PV system and gas engine co-generation, and showed that the total losses of the dc system are around 15% lower than that of the ac system for a year. The authors also mentioned that the dc system losses can be lower than the presented results if energy storage systems are included. For the future electronic energy network, it is anticipated that the widespread and increasing usage of new technologies in alternative, sustainable and distributed energy sources, power electronics, and energy storages will prefer dc electrical energy systems for higher efficiency, better controllability, utilization and availability of electricity [15].

## 1.3  DC Power Distribution Systems

Design and control of dc power distribution systems for different applications is an emerging research area with complex technical challenges. The diagram of a typical dc power distribution system is illustrated in Fig. 1.4. The dc power distribution system generally consists of a front-end rectifier and a dc distribution network, as shown in Fig. 1.4. The front-end rectifier is the connection between the dc distribution network and the ac transmission system, and converts the ac power to dc power. The front-end rectifier is a load

for the ac system, while it is the power source for the dc power distribution network. The front-end rectifier can either regulate its output voltage or output current, which depends on the specific application scenario. The dc distribution network consists of loads and different dc-dc converters for different purposes. The dc-dc converters are applied to implement the voltage conversion or current conversion in the dc distribution network in order to deliver desired power to loads. Depending on the architecture in the dc distribution network, the dc power distribution system can be classified as dc voltage distribution system and dc current distribution system.

### 1.3.1  DC Voltage Distribution Systems

The architecture of a typical dc voltage distribution system is illustrated in Fig. 1.5. As shown in Fig. 1.5, the source draws power from an ac transmission system or some other energy sources, and regulates the voltage on dc bus 1. The loads and dc-dc converters are connected onto the dc bus 1 in parallel. Depending on load specifications, the load may connect to the dc bus 1 directly,or connect to the dc bus 1 through a dc-dc converter. For some applications, it might be necessary to have a two-stage dc-dc conversion between dc bus 1 and the load, e.g. load 3 shown in Fig. 1.5. In a dc voltage distribution system, there might be more than one dc bus to satisfy the requirements for different voltage levels. As illustrated in Fig. 1.5, there are two dc buses. The voltage on dc bus 2 is regulated by dc-dc converter 1n. The dc-dc converter 1n draws power from dc bus 1 and deliver it to a smaller dc voltage distribution network.

The dc voltage distribution has been applied in a variety of applications, such as data centers, aircraft industry, dc micro-grids and ocean observatory systems, thanks to its high efficiency, high power density along with other benefits [16–23]. In [16–18], the authors pointed out that the overall efficiency improves from 67% to 77% by changing the ac power distribution architecture applied in the data center to a dc power distribution architecture. In [22, 23], the authors compared ac power distribution and dc power distribution for an ocean observatory system, and concluded that dc power distribution is preferred for long distance subsea power distribution.
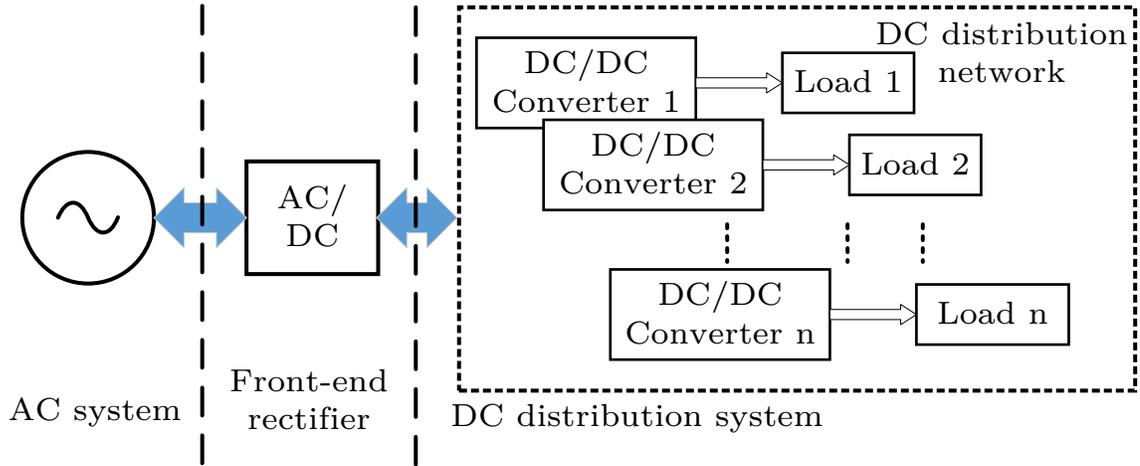
Fig. 1.4: Diagram of a typical dc power distribution system.
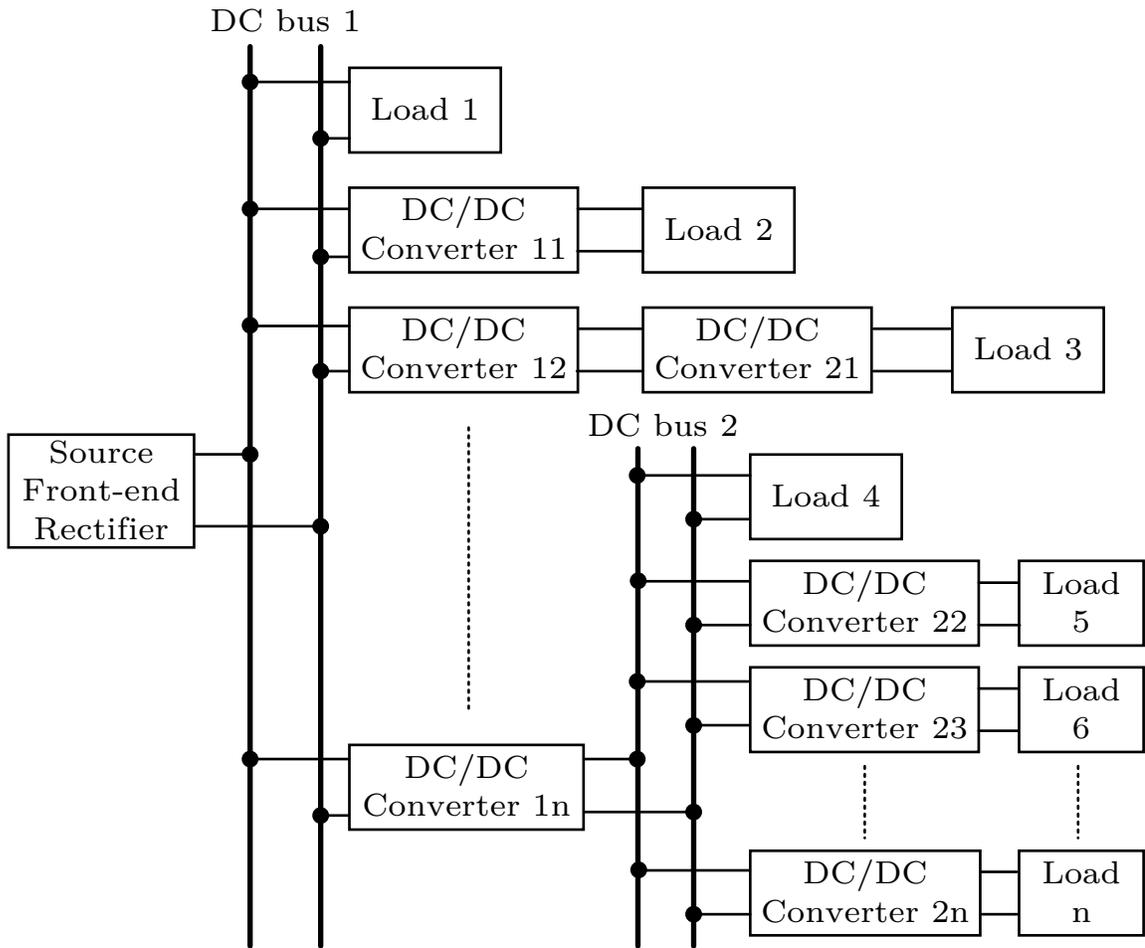


Fig. 1.5: Diagram of a typical dc voltage distribution system.

As shown in Fig. 1.5, the dc voltage distribution system is made up of smaller subsystems (dc-dc converters). Usually each subsystem (dc-dc converter) is designed based on its own stand-alone operation. As a result, after system integration, the interaction between subsystems may cause performance degradation, even system instability [24]. Based on this, a lot of research have been done regarding the stability issues of a dc voltage distribution system [19, 24–29]. In [24–27], the authors focused on the impedance based stability analysis for a dc voltage distribution system and presented impedance specifications for a stable dc voltage distribution system. In [28, 29], the authors developed local stability criterion based on impedance analysis for a dc voltage distribution system, and presented a control strategy for a dc voltage conversion system consisting of multiple converter modules based on the stability analysis.

### 1.3.2 DC Current Distribution Systems

The architecture of a typical dc current distribution system is illustrated in Fig. 1.6. For the dc current distribution system, as shown in Fig. 1.6, the shore-based source draws power from an ac transmission system or other energy sources, and regulates the current in the trunk cable #1. The loads and dc-dc converters are injected into the trunk cable in series. One should notice that the dc-dc converters distributed along the trunk cable have a constant input current instead of traditional constant input voltage. Similar with dc voltage distribution case, the load may connected to the trunk cable #1 directly, or connect through a dc-dc converter, e.g. the load 2 shown in Fig. 1.6. As shown in Fig. 1.6, it is also possible that more than one trunk cables are needed to satisfy the requirements for different current levels. The dc-dc converter 1n draws the power from trunk cable #1 and deliver it to a smaller dc current distribution network.

As shown in Fig. 1.6, the dc current distribution system is also made up of smaller subsystems (dc-dc converters). Usually each subsystem (dc-dc converter) is designed based on its own stand-alone operation. Each subsystem and dc-dc converter should be stable individually. Even though, the integrated system may have stability issues from the interactions of the feedback loops created by the input/output impedances of the interconnected
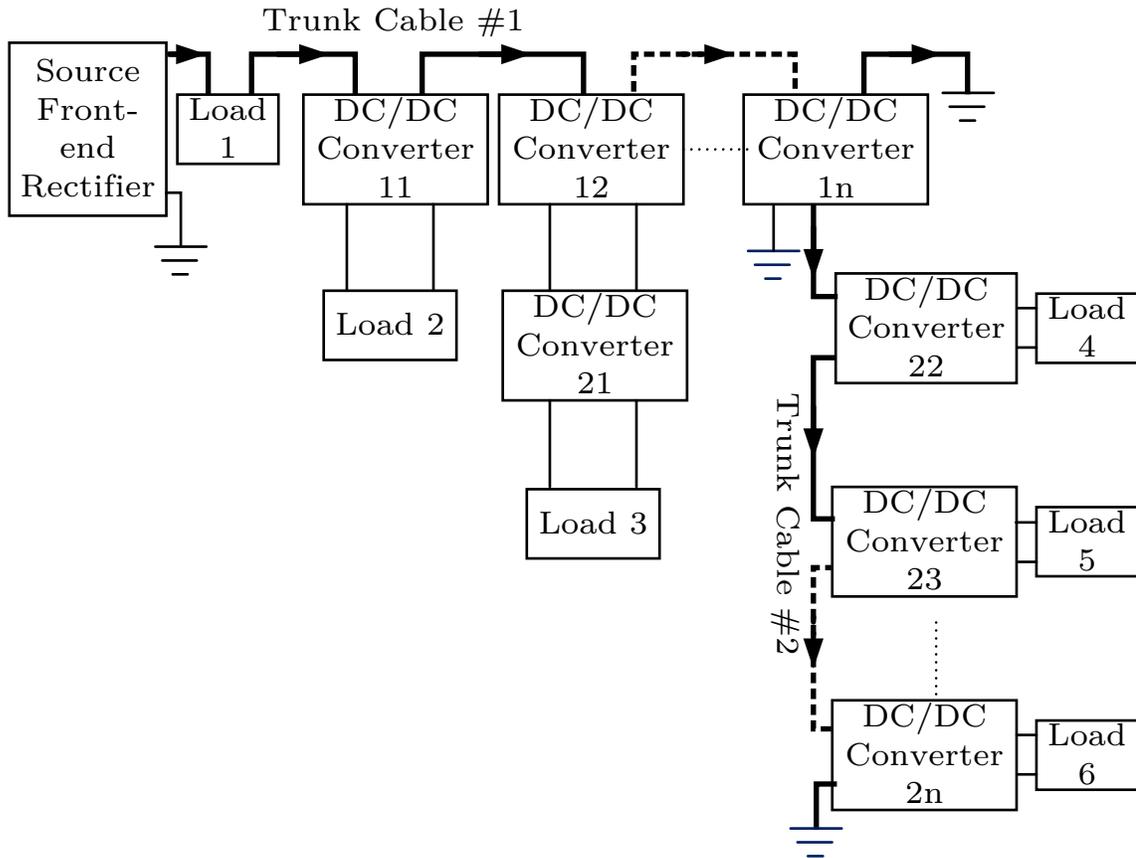
Fig. 1.6: Diagram of a typical dc current distribution system.

converters, which brings challenge to system control analysis and design.

The dc current distribution system has been applied in applications such as the underwater telecommunication systems and the ocean observatory systems [30, 31]. For the subsea applications, the dc current distribution is preferred over dc voltage distribution for its benefits of robustness against cable impedance and cable faults. For the dc current distribution system applied in subsea scenario, the constant current flows through the trunk cable, and the return current flows through sea water, which means that no cable is needed for current return. As a result, the cost of the system can be reduced significantly. In the Japanese ARENA project, supplying constant current to a mesh-like undersea cable-network for an undersea observation system is presented using current to current converters without control [32]. In both conventional underwater telecommunication systems and ocean observatory systems, as well as other dc current distribution applications, the observation
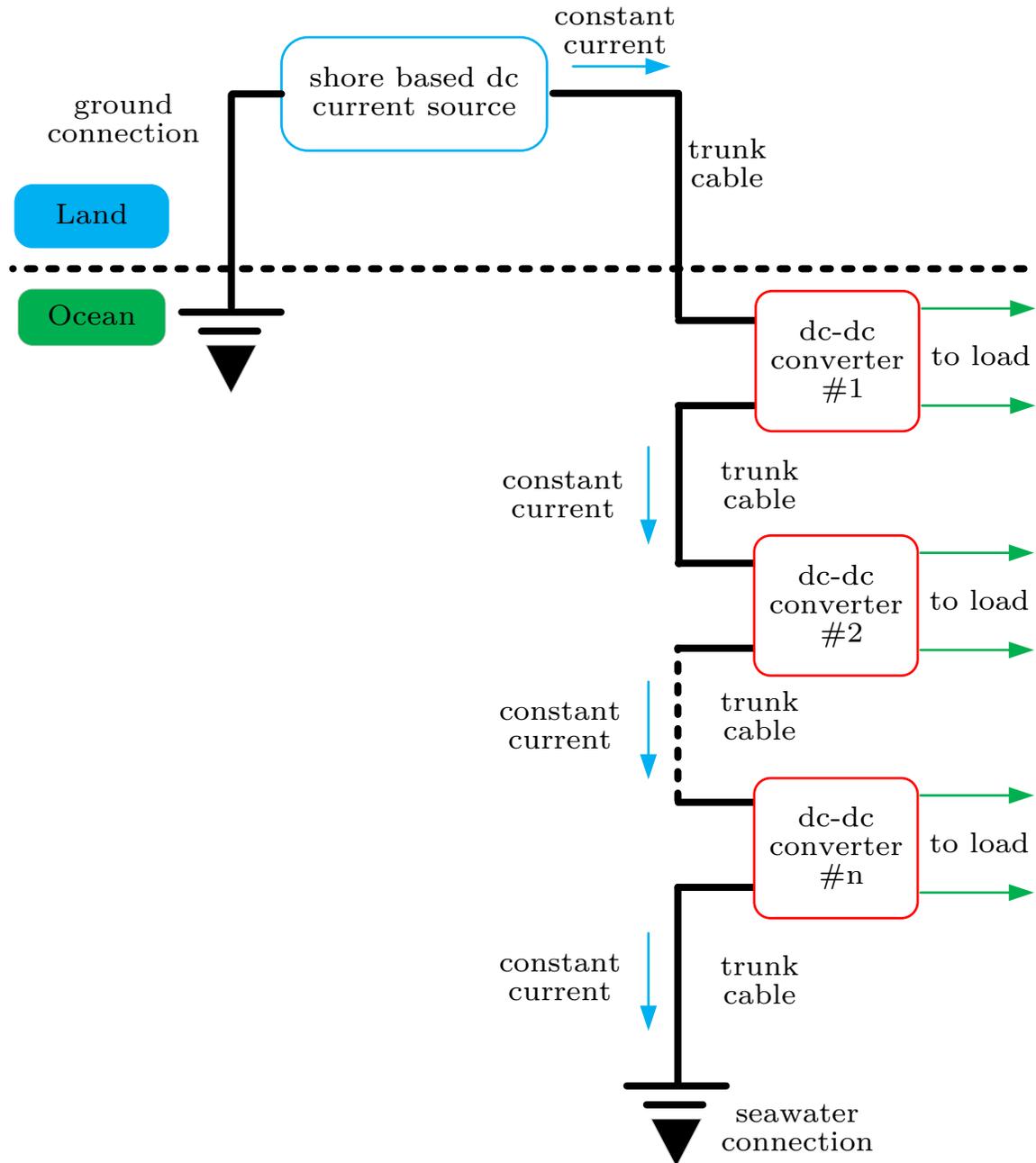
Fig. 1.7: Architecture of a single cable subsea dc current distribution system.

nodes are injected into the trunk cable, as illustrated in Fig. 1.7. In Fig. 1.7, the trunk cables generally have a length of tens of kilometers or even longer, and each dc-dc converter represents an observation node which draws the power from trunk cable and provides power to the load such as sensors.

## 1.4  Current to Current DC/DC Converters

From Fig. 1.6, it can seen that the dc-dc converters employed in a dc current distribution system have a constant input current and as a result, a variable input voltage, instead of a constant dc input voltage in conventional dc voltage distribution scenario. In a variety of industrial applications, including LED drivers [33], battery charging [34] and capacitor charging [35], output current regulated power supplies are required. Also, in the dc current distribution system itself, output current regulated dc-dc converters are required for generating different current levels in the system. So, there is a motivation to investigate current to current dc-dc converters.

Resonant converters are widely applied in various applications such as Uninterrupted Power Systems (UPSs), dc distribution systems and wireless power transfer (WPT) systems for high efficiency, high power density and low EMI [36–41]. Most of the research in the literature focuses on constant voltage input to resonant converters [36–48]. In [40], the authors showed that an LCL resonant network can be employed in a WPT system to generate a constant current running through the primary track, irresponsive to the change of the load. The authors also mentioned that the LCCL resonant network can provide a higher maximum track current compared to the LCL topology. In [49–51], the authors also mentioned that the LCL-T resonant converter behaves as a current-source under certain operating condition. Furthermore, in [52], the authors presented a detailed analysis, optimization and design guidelines of the LCL-T resonant converter for its operation as a constant current power supply. However, for the current to current converters, constant dc input current is applied instead of dc constant input voltage. The behavior of a series resonant converter (SRC) differs significantly with constant current input, a behavior that has not been studied in detail in the literature. The difference in the behavior also introduces challenges to the design, modeling, control, capability and applications of the SRC with constant input current and variable input voltage.

## 1.5  Proposed Design and Control Approaches

After comparison of several converter topologies, the SRC is selected as the current

to current dc-dc converter topology in this dissertation. This dissertation presents the unique features, develops the design procedures, derives the small signal model, performs the stability analysis and designs the controller for the SRC with constant input current used in a dc current distribution system. The system modeling, stability analysis, and control design is also developed in this dissertation, with the consideration of cable impedance. With the proposed design and control approaches, the entire dc current distribution system archives a stable operation with the output current of each converter regulated without communication among those converter modules.

A design procedure for the SRC with constant input current is developed based on the steady state analysis. This work extends previous steady state analysis technique for constant voltage input resonant converters to the constant current input resonant converters. To demonstrate the derivation of steady state solutions for resonant converters with constant input current like the SRC, the fundamental approximation is applied [53].

A frequency domain approach for the small signal model of the SRC with constant input current and variable input voltage is developed with the application of a generalized phasor transformer model. This work extends previous frequency domain small signal modeling approaches in the area, especially with regard to phasor modeling approach for switching converters. To derive the control equations and impedance equations for the controller design and stability analysis of the converters, the generalized phasor transformer is directly applied.

An in-depth analysis of the system stability including the long distance submarine cable modeling is also given in this dissertation. The impedance model of the submarine cable is developed, and the relation between closed-loop input impedance and open-loop input impedance of the converter is derived with the SRC as an example. The stability analysis of the system consists of one or more cables and one or more SRCs gives guidance on how to design the controller for the modules in a dc current distribution system to obtain a stable system behavior.

System control design including the controller design for each SRC module, control

strategy of the overall system and practical details related to system control, operation and protections are also provided. The individual local output current regulation is implemented for each SRC without communication required. The operation and protection related practical details ensure that the normal start-up and shut-down of the system are smooth and controlled, while the entire system, including the shore power supply and the SRC modules can be protected during fault scenarios.

To provide hardware verification for the analysis and design presented, a set of prototype SRCs with a 250 kHz switching frequency have been built, and a set of cable emulator for 100 km submarine cable have also been built. Each SRC module is designed to operate with a 1 A dc constant input current, and an output current of 0.33 A with the power of 1 kW. Using these prototypes, hardware results are presented for each design, and modeling and control areas developed. In addition to the hardware results conducted on the prototypes, simulation results from MATLAB, Simulink, PLECS and LTSpice are provided to demonstrate the theory and analysis throughout.

Chapter 2 of this dissertation covers the technical background materials related to the work that has been done here. A full review of efforts presented in literature on the topics discussed in this dissertation is given, as well as the challenges in the dc current distribution system. Several different candidate topologies for current to current converters are compared and discussed with the conclusion of employing the SRC. The distribution efficiency of dc voltage distribution and dc current distribution is analyzed with the roadway dynamic wireless power transfer taken as an example.

Chapter 3 presents a detailed steady state analysis of the SRC with constant input current, and as a result, variable input voltage. From the steady state analysis results, the unique features of the SRC are summarized. Based on the unique features, design challenges and constraints are given. A design procedure is developed with the consideration of resonant components variations, transformer parasitics and switching frequency optimization.

The approaches employed to drive the small signal model of the SRC are covered in

Chapter 4. Derivation of the phasor transformer are introduced first, followed by the phasor model for each of the main components in the converter, and finally explicit expressions of control to outputs, control to inputs, input and output impedances for the SRC are derived.

Using the models and results from Chapter 4, Chapter 5 discusses the stability of a dc current distribution system. The impedance model for the submarine cable is developed, and the relation between closed-loop and open-loop input impedance of a converter is derived. The results can be applied to other converter topologies, as well as systems using submarine cables. Based on these results and the stability criteria for a current cascaded system, the stability analysis of the dc current distribution system is presented.

In Chapter 6, the control design related techniques for the entire system are covered for both normal operation and fault scenarios. Using the results from Chapter 4 and analysis from Chapter 5, the control strategy and controller design for the SRC is presented. Operational study of a dc current distribution system is conducted, and the protection techniques are developed for different types of faults.

Simulation and hardware results used to validate the proposed analysis, design and approaches of previous chapters are presented and discussed in Chapter 7. Different levels of simulations and hardware experiments are discussed, ranging from a single converter level to a system level with real scenario required startup, shutdown and fault scenarios. Conclusions and future work directions are given in Chapter 8.

CHAPTER 2

REVIEW OF TECHNICAL BACKGROUND

The work presented in this dissertation builds on a wide range of previous techniques and theories. In order to put the dissertation in context with existing literature, a brief technical background of relevant fields is given in this chapter. Analysis and discussion on some general technical background for this dissertation is also presented in this chapter.

## 2.1 Converter Topologies for DC Current Distribution in Literature

A dc current to dc current converter employed in a mesh-like scientific underwater cable network is proposed in [32, 54]. The proposed topology is shown in Fig. 2.1. From Fig. 2.1, it can be seen that it is a push-pull based topology which takes a dc input current and converts it into a dc output current. The dc constant input current $I_{in}$ is switched by the switching devices *FET* 1 and *FET* 2, and fed into the transformer. The output of the transformer is rectified and filtered. The input current and number of windings of the transformer determine the output current. The proposed topology is still a voltage fed topology due to the presence of capacitor $C_1$ . However, the presented topology operates in open-loop mode without feedback controller. As a result, the output characteristics are very sensitive to any variations in the converter and system, and the loss of the core and switching loss have large influence on the output characteristics.

In [55, 56], the authors presented a current-fed dc-dc converter for a dc current power distribution system in a subsea application. The proposed topology is illustrated in Fig. 2.2. As shown in Fig. 2.2, the primary full-bridge switches need to have reverse voltage blocking capability, which is implemented by IGBT in series with diode. The proposed topology is a real current-fed topology instead of using a voltage-fed topology in a constant input current scenario, since the output current of the primary full-bridge is a phase shifted square waveform. However, the efficiency of the converter is reduced because of the series

connection of IGBT and diode, and the switching frequency of the converter is limited because the use of IGBT, which is not preferred for high power density and magnetic size reduction.

In [57], the authors presented an active clamping zero-voltage switching (ZVS) PWM current-fed half bridge converter, as shown in Fig. 2.3. The active clamping switch absorbs the voltage surge across the turned-off switch, and helps to achieve ZVS for all power switches. In [58], an active-clamped ZVS current-fed push-pull isolated dc/dc converter for renewable energy conversion applications is proposed, as illustrated in Fig. 2.4. The proposed converter conserves small input current pulsation, high-voltage conversion ratio, ZVS and zero-current-switching (ZCS) operation for primary switches and rectifier diodes, respectively, over a large load range. The additional active clamping circuit serves to suppress the voltage spike across all primary switches, as well as assists in achieving ZVS operation. In [59], the authors proposed a simple, current-fed, ac-dc, single stage, single phase, isolated, high power factor with two switches referenced to the same ground for HB-LED driver application, the circuit diagram of which is shown in Fig. 2.5. The proposed topology is based on the push-pull converter. In [60], an improved modulation scheme for a current-fed dual active bridge to reduce converter loss in battery energy storage applications is proposed by the authors. The circuit diagram of the current-fed bidirectional dc-dc converter is shown in Fig. 2.6. The proposed modulation can minimize the conduction loss by deriving the modified operation modes. All the current-fed topologies presented above in literature are PWM converters, however, for application scenarios which requires low electromagnetic interference (EMI), high power density and high efficiency, resonant converters are preferred over the PWM converters, which has not been studied in literature for dc current distribution applications.

## 2.2  Resonant Converters

Resonant converters contain resonant networks, which consist of one or more inductors and one or more capacitors. The voltage and current waveforms of the resonant tanks vary sinusoidally during one or more subintervals of each switching period [53]. A general
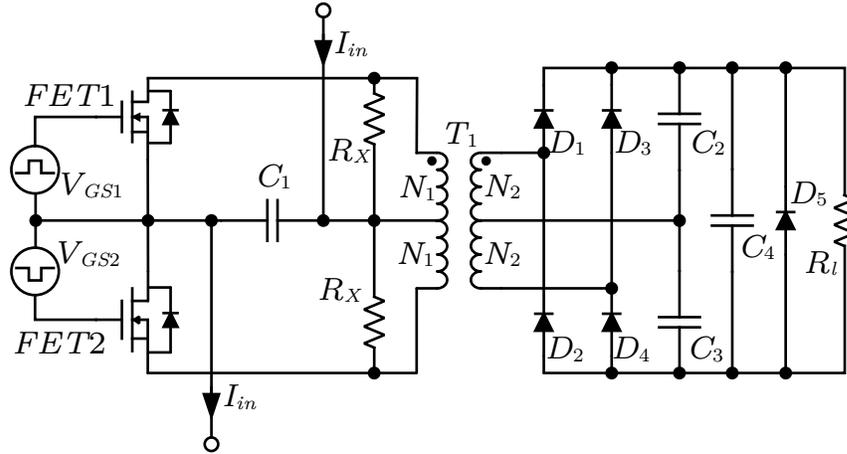
Fig. 2.1: Circuit diagram of the current to current converter topology presented in [54].
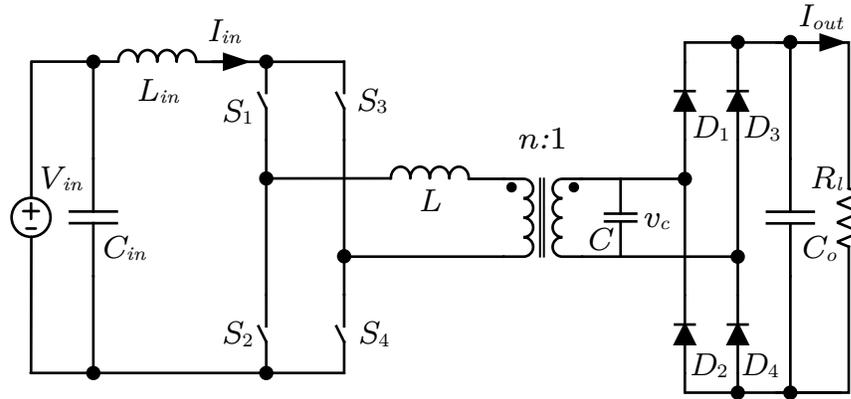


Fig. 2.2: Circuit diagram of the current to current converter topology presented in [55].

diagram of resonant converters that consist of a dc input, a switch network, a resonant network, a transformer, a rectifier network, a filter network and a dc load is illustrated in Fig. 2.7.

The switch network shown in Fig. 2.7 can be any switch networks, such as full-bridge, half-bridge and push-pull, which converts the dc input to an ac square wave at the switching frequency $f_s$. The produced ac square is applied to the resonant network which generally responds primarily to the fundamental component of the applied ac square waveforms and exhibits negligible response at the harmonics of $f_s$, as illustrated in Fig. 2.8. If it is a resonant inverter instead of a resonant dc-dc converter, the load will be connected to the resonant network output terminals instead of the transformer $T$. The transformer $T$ provides
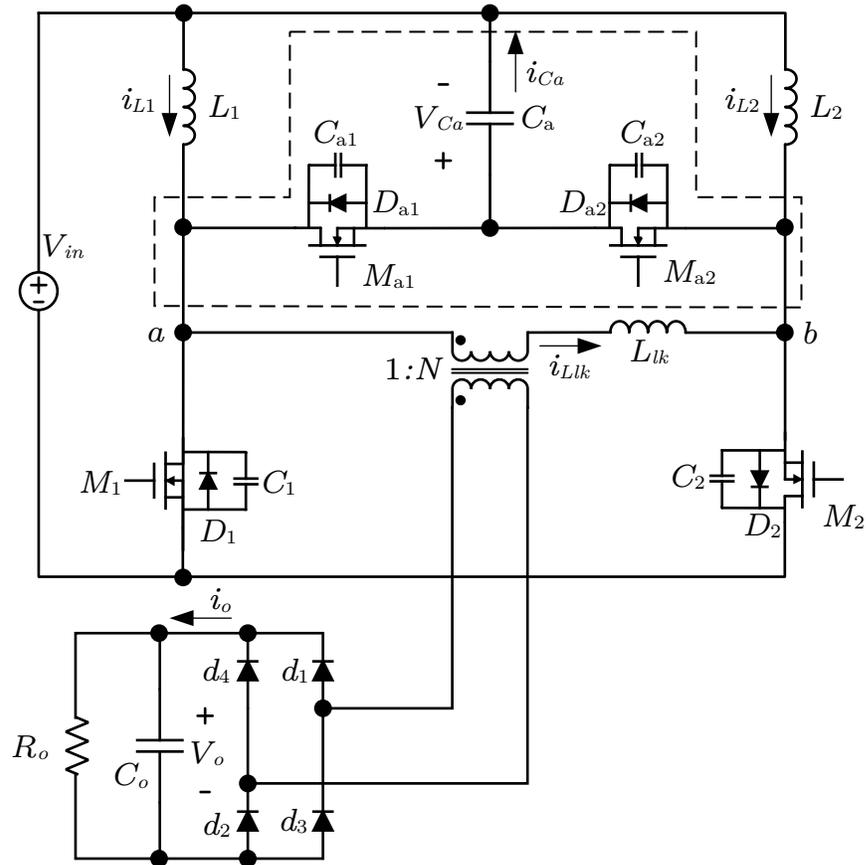
Fig. 2.3: Circuit diagram of the current-fed half-bridge converter topology presented in [57].
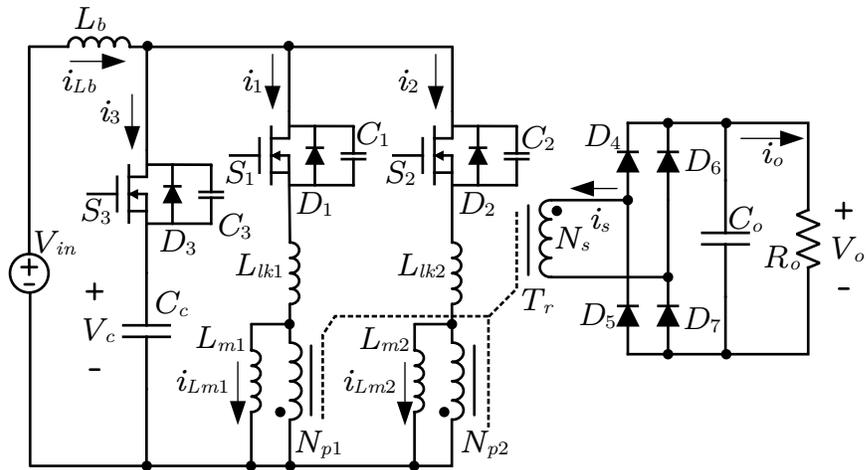


Fig. 2.4: ZVS active-clamped current-fed push-pull converter topology presented in [58].
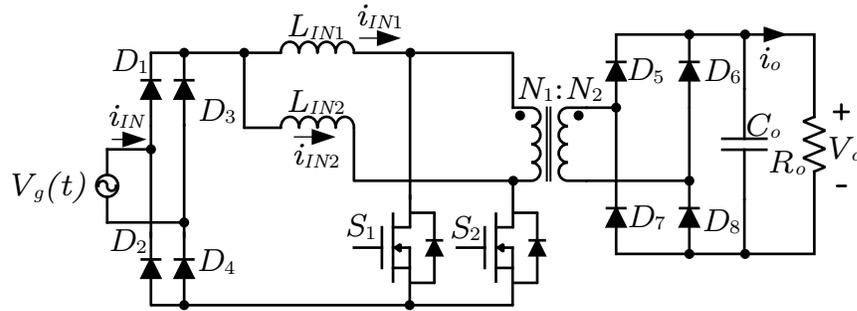
Fig. 2.5: AC-DC PFC single stage dual inductor current-fed push-pull converter topology presented in [59].
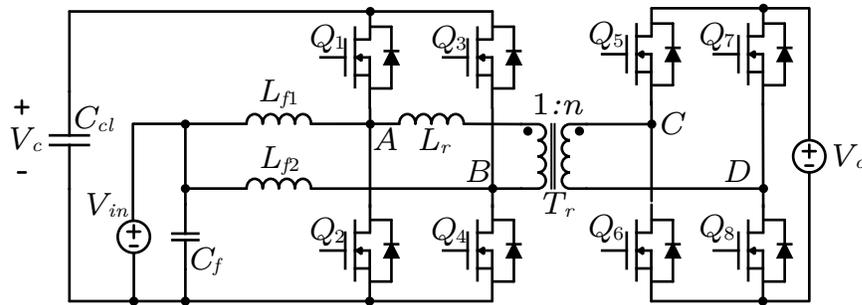


Fig. 2.6: Current-fed bidirectional dc-dc converter topology presented in [60].
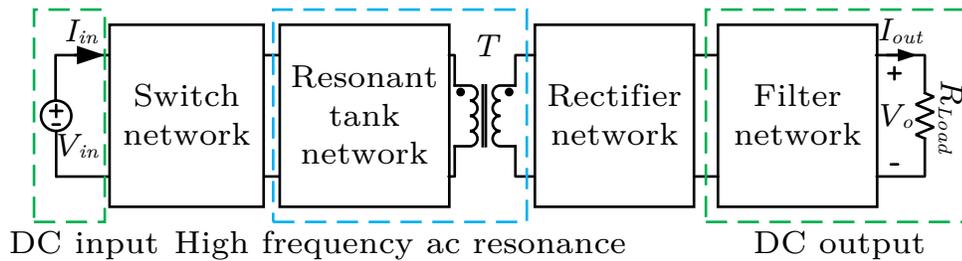


Fig. 2.7: A general diagram of resonant converters.

isolation between primary and secondary, as well as voltage step up and down functions. In applications where isolation is not required, the transformer can be avoid. Then, the sinusoidal waveform is applied to the rectifier network to converter it back to dc quantity. The rectifier can be diode full-bridge, diode half-bridge, diode voltage doubler, normal full-bridge or half-bridge with active switches. The output of the rectifier is connected to the filter network, and then to the dc load.

For the switch network, different control schemes can be employed, such as switching
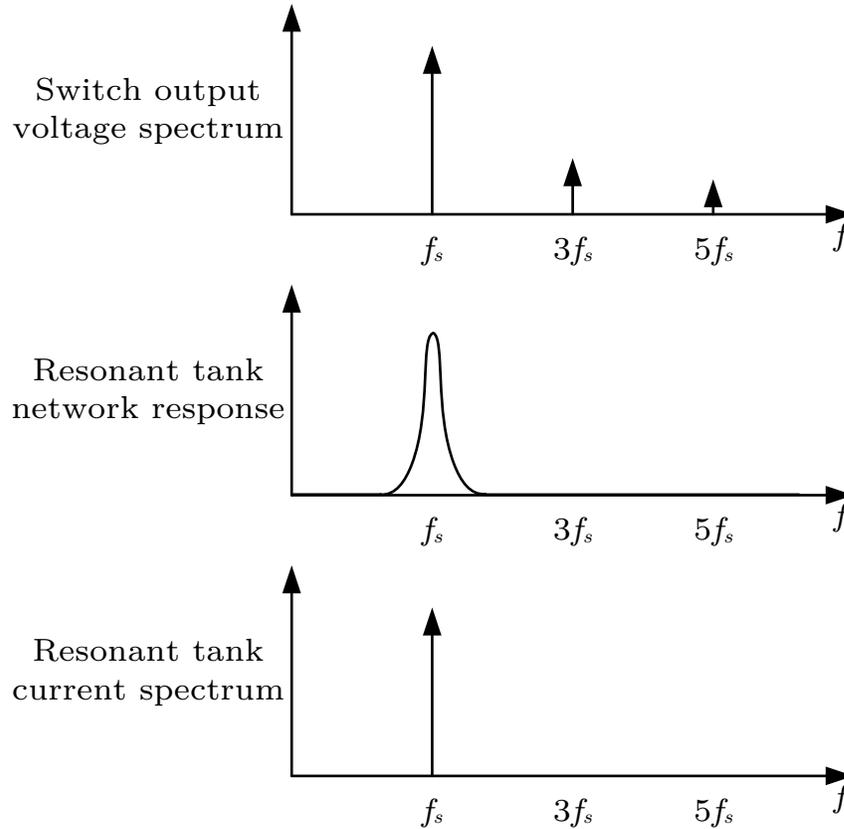
Fig. 2.8: The resonant tank network responds primarily to the fundamental component of the driving waveforms.

frequency control and phase shift control, depends on the topology that is used. For the resonant network, a variety of networks with the combinations of resonant inductors and resonant capacitors can be employed. Several basic and well-known ones, series, parallel, LCC and LCL tank networks are illustrated in Fig. 2.9.

The major advantage of resonant converters is their reduced switching loss, via mechanisms known as ZCS and ZVS. The turn-on and/or turn-off transients of the switches can occur at zero crossings of the resonant converter quasi-sinusoidal waveforms, which eliminates some of the switching loss mechanisms. Hence, resonant converters can operate at higher switching frequency because of the reduced switching loss, which results in higher power density and smaller magnetic component sizes. ZVS can also eliminate some of the sources of converter-generated EMI, which is also one of the benefits of resonant converters.
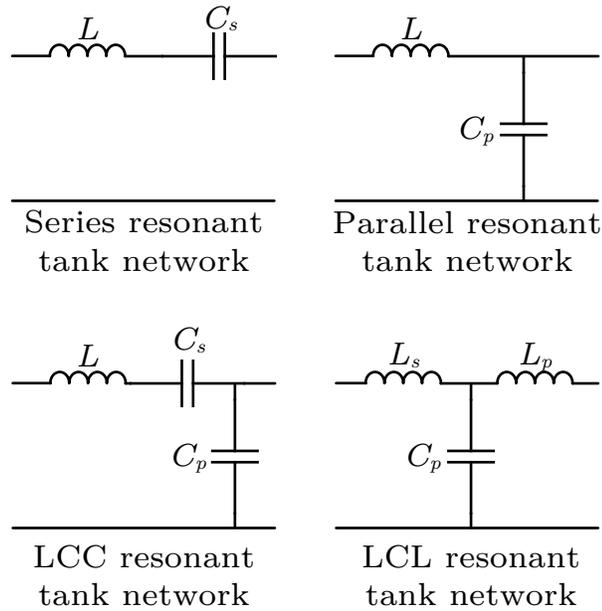
Fig. 2.9: Several basic and well-known resonant tank networks.

Although the resonant converter can be designed to obtain good performance with high efficiency at a single operating point, it is typically a challenge to have good performance over a wide range of load. Resonant currents may circulate through the tank elements, even when the load is removed, leading to poor efficiency at light load. Another disadvantage of resonant converters is that the quasi-sinusoidal waveforms exhibit greater peak values, which results in an increased conduction losses that can offset their reduced switching losses.

The resonant converters have been widely used in a variety of applications, and a lot of research efforts have been made on the analysis, design and control of the resonant converters. However, most of the research in the literature focus on constant dc voltage input resonant converters [42–48, 52]. The behavior and related analysis, design, control of resonant converters with constant dc input current have not been well studied in the literature.

## 2.3   Analysis Tools for Resonant Converters

### 2.3.1   Steady State Analysis Tools

The sinusoidal approximation, or commonly referred to as fundamental approximation as well, which assumes that the resonant tank sufficiently filters the higher order harmonics injected by the bridge and the power is primarily transferred by the fundamental component of the resonant current, is well established and widely applied to design and steady state analysis of SRCs [36–38, 53, 61]. The relation between a switch network output voltage $v_s(t)$ and its fundamental component $v_{s1}(t)$ is shown in Fig. 2.10.The sinusoidal approximation allows closed-form expressions of the steady state solution for SRCs to be derived using standard linear ac analysis. This approach is quite accurate for operation in the continuous mode with a high-Q response, but becomes less accurate when the tank is operated with a low $Q$-factor (e.g. $Q < 2.5$) or for operation of resonant converters in or near the discontinuous conduction mode [53, 61].

In [62, 63], state space approach for steady state analysis of resonant converters are presented by the authors. The state space approach requires finding all the operating modes of the resonant converter, which is difficult to determine at the initial design stage, as a result, it is not very helpful for the design of resonant converters.

In [64], the authors presented a graphical state-plane technique to perform the steady state analysis for a series resonant converter. By using inductor current and capacitor voltage of the resonant tank circuit as the two coordinates, steady-state operations of the resonant converter are graphically portrayed on a state plane. The state portrait clearly show the instantaneous resonant tank energy, output power, switching frequency and control. However, it becomes difficult for the resonant converters with more than two resonant components.

In [65], the authors presented a new analysis approach to modeling resonant converters that can be used to determine closed-form expressions for the exact resonant network waveforms based on step-superposition technique. The presented approach is good for analysis of resonant waveforms, including the start-up waveforms, but it is difficult to apply to the
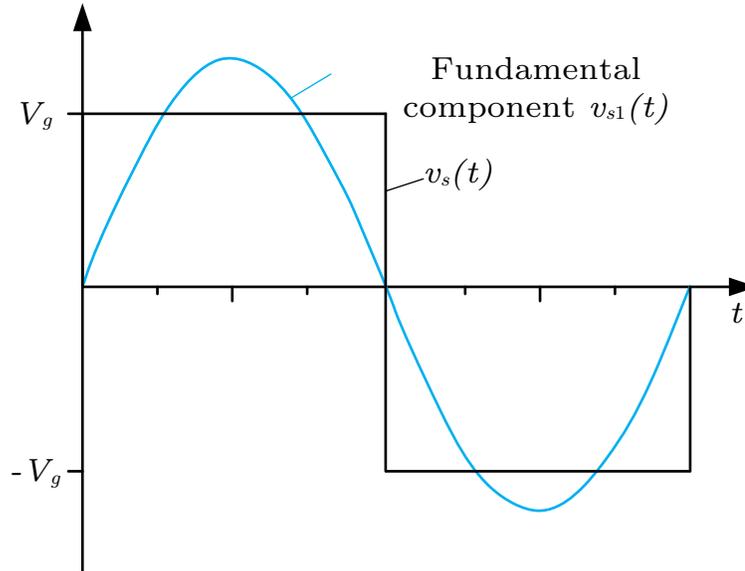
Fig. 2.10: Switch network output voltage and its fundamental component.

steady state analysis and design of the resonant converters.

After considering the aforementioned steady state analysis approaches for the resonant converter, the sinusoidal approximation analysis is employed for the calculation, analysis and design of the work presented in this dissertation.

### 2.3.2    Small Signal Modeling Tools

Several different small signal modeling approaches have been presented to model the frequency dynamics of resonant converters. In [66], the authors proposed a method from combination of state-space analysis in continuous-time and discrete-time domain, without linear ripple approximation. The proposed method is shown to be accurate by experimental results. However, because of the matrices employed in the method, it is difficult to determine the functions in expression form, and as a result, the results are computed numerically. In [67–70], the authors presented small signal modeling methods for resonant converters based on the discrete-time domain analysis or the sampled-data analysis. The discrete-time based model can predict the small-signal behavior up to the switching frequency since it captures the inherent sampling nature of the converters. However, these methods are too complex for practical use, and are very difficult to extract physical insight of the resonant

converters. In [71], the authors pointed out that the state space averaging cannot be applied to analysis and control design of resonant converters because the resonant circuits have state variables with a predominantly oscillatory behavior, and proposed a small signal modeling approach for a series-parallel resonant dc-dc converter based on the generalized averaging analysis of first harmonic. However, only the numerical solutions can be used to plot the transfer functions.

Although the small-signal models shown in [66–71] are shown accurate enough to present the beat frequency dynamics, none of the models have been widely used because all of them have complicated mathematics instead of using circuit-oriented approach. In [72], the authors proposed a low-frequency continuous time two-port y parameter equivalent circuit model based on the discrete-time result. However, the equivalent circuit model is accurate only when the perturbation is at low frequency and it cannot predict beat frequency dynamics. In [73], the authors proposed a third-order equivalent circuit for the SRC, which is simplified from the fifth-order presented in [74] based on extended describing function concept. The third-order equivalent circuit model provides analytical solutions for all the transfer functions and is shown to be accurate from the simulation and experimental results. However, it is only for the switching frequency control analysis, and does not give analysis on small signal modeling based on phase shift control.

A new modeling technique based on phasor transformation is proposed by C. T. Rim and G. H. Cho in [75]. This approach gives explicit and simple equations with fruitful physical insight. The model captures low-frequency dynamics of the SRC: in the case where the switching frequency deviates from the resonant frequency, the SRC is modeled as the first order system, and in the case of operating at resonance, the SRC is modeled as the second order system. The dynamic phasor technique has been successfully applied in small signal behavior modeling of electronic ballasts [76, 77], multi-angle phase shift modulated resonant converters [47] and uniformly sampled phase-shift modulators [78, 79].

The object of phasor transformation is to remove the rotation feature from the fundamental sinusoidal waveforms and analyze the dynamics of the static envelopes. The

transformation approach was first proposed in [75], where a sinusoidal waveform can be represented by as complex phasor:

$$x(t) \equiv Re[\overline{x}(t)e^{j\omega_s t}], \tag{2.1}$$

where $\overline{x}(t)$ is the time-varying phasor corresponding to $x(t)$. This transformation method is suitable for small-signal modeling with amplitude modulation, where the switching frequency $\omega_s$ is constant, and the small variations in the amplitude of $x(t)$ are modeled by small variations in $\overline{x}(t)$. Hence, a time-invariant small-signal model can be derived. The derivation of the phasor models for basic circuit elements have been shown in [75]. Those models are now briefly re-derived as a reference, as well as extended for use in phase modulated H-bridges and diode rectifier doubler. By applying (2.1) to the $v$-$i$ equations of the basic circuit elements, the phasor transformation for those circuit elements can be derived, as shown in Fig. 2.11.

For the inductor, the $v$-$i$ equation is

$$L\frac{di_L(t)}{dt} = v_L(t). \tag{2.2}$$

The phasor transformation of the inductor current and inductor voltage are:

$$i_L(t) \equiv Re[\overline{i}_L(t)e^{j\omega_s t}], \tag{2.3}$$

$$v_L(t) \equiv Re[\overline{v}_L(t)e^{j\omega_s t}]. \tag{2.4}$$

Substituting (2.3) and (2.4) into (2.2), the phasor equation for the inductor can be derived as

$$L\frac{d}{dt}[Re[\overline{i}_L(t)e^{j\omega_s t}]] = Re[\overline{v}_L(t)e^{j\omega_s t}], \tag{2.5}$$

$$LRe[\frac{di_L}{dt}e^{j\omega_s t} + j\omega_s i_L e^{j\omega_s t}] = Re[(L\frac{di_L}{dt} + j\omega_s Li_L)e^{j\omega_s t}] = Re[\overline{v}_L(t)e^{j\omega_s t}]. \tag{2.6}$$
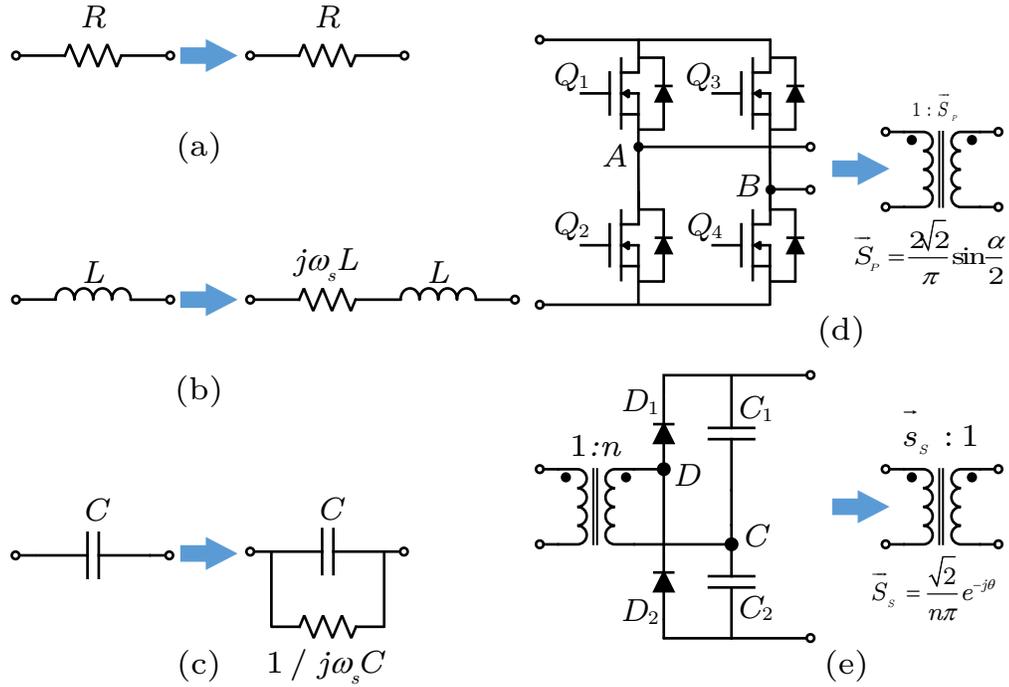
Fig. 2.11: Phasor transformations for basic elements in the SRC. Left: time domain. Right: phasor complex time domain.

From (2.6), we can get the phasor equation for the inductor as

$$L\frac{di_L(t)}{dt} + j\omega_s L i_L = v_L(t). \tag{2.7}$$

The circuit form of (2.7) can be used for the benefit of well established circuit analysis techniques, as illustrated in Fig. 2.11(b). For the capacitor, by following a similar procedure for the inductor, the the $v$-$i$ equation

$$C\frac{dv_C(t)}{dt} = i_C(t). \tag{2.8}$$

in phasor transformation domain can be expressed as

$$C\frac{dv_C(t)}{dt} + j\omega_s C v_C = i_C(t). \tag{2.9}$$

The circuit form of (2.9) is illustrated in Fig 2.11(c). Similarly, the phasor transformation

of resistor, full bridge and transformer connected with diode voltage doubler are shown in Fig. 2.11(a), Fig. 2.11(d) and Fig. 2.11(e), respectively.

In this dissertation, the dynamic phasor transformation approach is employed to develop the small-signal model for the SRC with constant dc input current. The developed small-signal model provides abundant physical insight of the SRC, and explicit expressions for all the transfer functions including control to output current and output voltage, control to input voltage, input and output impedances, which is very helpful for the control analysis and design of the SRC.

## 2.4   Stability Analysis Review

When two power converters are cascaded together, there is a stability concern even both of them are stable individually. Since most of the application scenarios around us require more than one power converters, people have put a lot of efforts to study the stability of the systems. Generally, there are two main causes of stability degradation for a dc power distribution system: 1) interactions of the feedback loop created by the input/output impedances of the interconnected converters and 2) the constant power load effects that exhibit negative incremental impedance [80]. These two causes can compromise the stability of both the converters and the complete interconnected dc power distribution system. Several approaches have been proposed for modeling the dynamics of such a system including eigenvalue based full system modeling [81–85], nonlinear modeling [86–89] and impedance-based modeling techniques. Among these, impedance-based modeling techniques have been most popular and have been shown to facilitate design specifications for sources and loads [24, 27, 90–92]. Using impedance modeling, several criteria have been proposed to analyze stability of the system. Majority of these criteria rely upon the Nyquist and/or Bode plots for analyzing the stability, where several sources and loads are grouped together with other sources and loads, respectively, and the ratio of the impedances, which is termed as the minor loop gain, of the grouped subsystems is plotted along with the region of stability. In general, the system is guaranteed to be stable if the trajectory of the minor loop does not violate the conditions defined by each criterion, provided individual converters/loads

are individually stable [90]. However, these criteria need to be reevaluated with a new set of source and load subsystems when the direction of power flow changes.

There has been research performed to analyze the stability of a dc distribution system, which is mainly found with dc microgrids [21, 93–98] and electrical ships [99–103]. An overview of the existing work is presented next for system stability analysis.

One of the most widely used stability criteria, the Middlebrook stability criterion simply restricts the minor loop gain within a circle of radius less than unity, and thus ensures stability and presents a simple procedure for designing source and load impedances with their ratios smaller than unity [104]. The criterion results in the most conservative design of passive components, which tend to be bigger in size and are usually bulky [90, 104]. With the prior knowledge of both the source and load impedances, the gain margin phase margin (GMPM) criterion relaxes the constraints imposed by the Middlebrook criterion [91]. The Nyquist diagram allows designs to go beyond the unit circle to the boundary defined by two lines at angle of $\pm$ phase margin (PM) from the negative real axis and extending from infinity to the circle defined by the Middlebrook criterion as presented graphically in Fig. 2.12. This criterion is very simple and is highly design oriented, and hence advantageous for the preliminary design of a system. However, the criterion predicts instability of a stable system when direction of power is reversed or when the operating mode of the source and load systems is swapped. In contrast to describing the stability for single lumped load and source subsystems, a more realistic scenario comprising multiple sources and load converters can be analyzed with an opposing argument criterion [24, 27, 92]. This criterion essentially imposes a condition of a vertical line, as shown in Fig. 2.12, that the Nyquist diagram is allowed to remain on the right side of the line, and its position on the axis is defined by the inverse of the gain margin (GM) [24, 92].

Energy source analysis consortium (ESAC) criterion further reduces the design conservativeness while keeping the same level of GM and PM as the opposing argument criterion [83, 84, 96, 100]. The region to the left of the indicated boundary in Fig. 2.12. is considered to be forbidden. With this approach, a 3D region with phase, frequency and
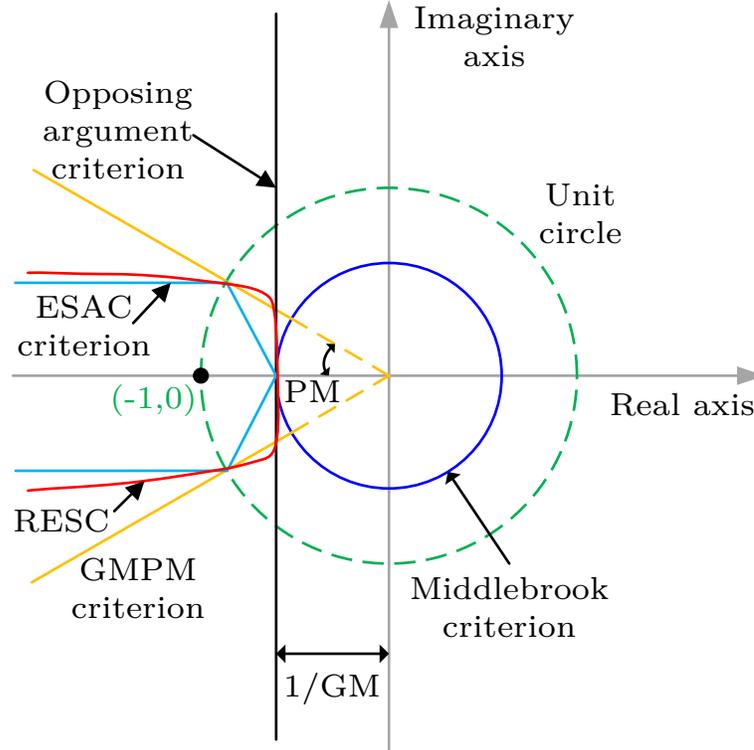
Fig. 2.12: Review of stability criteria from the literature.

magnitude of load admittance is used to formulate a forbidden volume that when not inter-sected indicates a stable system. Root exponential stability criterion (RESC) is proposed to improve the robustness of the ESAC while calculating the load admittance, where the path of the RESC in the s-plane is always well defined and is represented by a continuous function [101]. The region to avoid with the RESC is comparable to that of an ESAC. With the passivity based stability criterion [99, 105], all the sources and loads are combined as a single system that is connected to a dc bus, and the impedance of the system is measured by an external module responsible for injecting perturbation signals, deducing stability, and stabilizing the dc bus. This criterion ensures stability when bus impedance has no right-half plane poles, and the impedance has some positive resistive component at all frequencies of interest. The stability margins however are not easy to deduce with this criterion, and, furthermore, necessary and sufficient conditions for stability are not easily deduced given that the criterion cannot be related to the Nyquist criterion [105].

As presented above, most of the research on stability analysis are for dc voltage power distribution systems. However, the stability criterion for a current cascaded system is different from a voltage cascaded system, and the research results from the literature for dc voltage distribution systems can not be directly employed in dc current distribution scenario. The stability issue of dc current distribution systems has not been well studied in the literature yet. For the stability analysis of a current cascaded system, in [106], the author presented impedance-based stability criterion for grid-connected inverters, which can be used as a reference for the stability analysis and control of a dc current distribution system. The cable impedance in the system is also considered in the analysis in this dissertation.

## 2.5 System Operation and Protection

For a dc current distribution system, the operation is different from a dc voltage distribution system. The most significant difference is that the converters in a dc current distribution system are connected in series, while the converters in a dc current voltage distribution system are connected in parallel. For the dc current distribution system, the current needs a path to flow through the trunk cable even before the system is turned on, otherwise, the shore power supply which provides the dc distribution current will see a open circuit load, which should be avoid for a current source.The inherent features of the dc current distribution system bring challenge for the system operation, which have not been well studied in the literature yet. The operation of an SRC employed as a current regulated power supply in a dc current distribution system subject to startup and shutdown transient and open and short circuit fault conditions are investigated in this dissertation.

An SRC with a resonant capacitor clamping circuit to protect the SRC during fault transients was presented in [107], as illustrated in Fig. 2.13. In Fig. 2.13, the diodes $D_3$, $D_4$, $D_5$ and $D_6$ are used to clamp the voltage of the resonant capacitor $C_r$ to the input voltage $V_{in}$. However, from the resonant capacitor terminals to ground voltage analysis, the capacitor terminal voltages are expressed as $V_{in} \pm 0.5 v_{Cr}$ when $Q_1$ and $Q_3$ are on, which is a general case for phase shift modulation control [43, 44]. In this case, for phase shift modulation controlled SRC, circulating currents between the resonant tank and the input
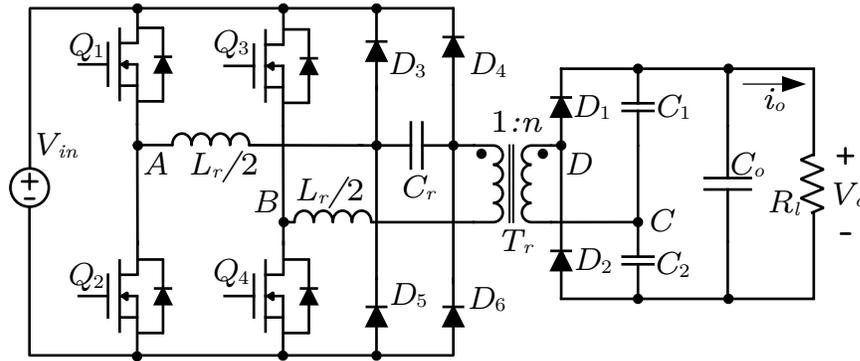
Fig. 2.13: SRC with constant voltage input and resonant capacitor voltage clamping circuit.

filter are unavoidable. On the other hand, for the SRC with constant current input, the voltage across the resonant capacitor is higher than the input voltage for certain load range as presented in [108], which means that the protection approach shown in Fig. 2.13 cannot be used since it alters the steady state operation.

CHAPTER 3

ANALYSIS AND DESIGN OF SERIES RESONANT CONVERTERS WITH
CONSTANT INPUT CURRENT

Previous analysis of resonant converters have largely focused on constant dc voltage input scenarios, while the research shown in the literature on converter topologies used in dc current distribution systems has focused on non-resonant topologies. In this chapter, the series resonant converter (SRC) with constant dc input current and variable input voltage is studied in detail. Section 3.1 presents the steady state operation of different resonant converters, including SRC, parallel resonant converter (PRC), LCL resonant converter and dual active bridge series resonant converter (DABSRC), with constant dc current input, and discussed the topology selection based on the comparison. The stress analysis for the components employed in the SRC with constant input current is performed in Section 3.2. In Section 3.3, the output characteristics of the SRC with constant input current is derived to show the different behavior of the converter with respect to the case with constant input voltage. Based on the analytical results, design considerations and procedures for the SRC with constant input current is developed in Section 3.4. In order to get an optimized design, the modeling of the high voltage transformer is presented in Section 3.5 to model the parasitics of the high voltage transformer, while design optimization is discussed in Section 3.6. Two design examples of the SRC with constant input current are shown in Section 3.7 to demonstrate the analysis, design considerations and design procedures developed in this chapter. The chapter summary is given in Section 3.8.

## 3.1  Resonant Converter Topology Comparison and Selection

The steady state analysis and output characteristics of the resonant converters with dc voltage input have been well investigated in the literature, however, the behavior of the resonant converters with constant dc current input have not been studied. In order to show

which topology should choose for a specific application scenario, the steady state solutions, output characteristics and comparison of four different commonly used resonant converter topologies are presented in this section. The fundamental approximation is employed for the calculation and analysis in the following subsections [53].

### 3.1.1 Steady State Analysis of SRC

Figure 3.1 illustrates the SRC topology with dc constant input current. The resonant tank, which consists of a capacitor $C_r$ and two inductors, each $L_r/2$, is connected to an active full bridge at the input side and a diode half-bridge voltage doubler at the output side. The input active bridge consists of devices $Q_1 \ldots Q_4$ , while the output bridge consists of diodes $D_1$ and $D_2$. A $1 : n$ power transformer, which has two primaries with the same number of turns and two secondaries with the same number of turns connected in series, provides isolation between the input and output. The input is a constant dc current source as shown in Fig. 3.1, and a phase-shift modulation strategy controls the switches of the SRC [43, 44].

The equivalent circuit of the SRC illustrated in Fig. 3.1 is shown in Fig. 3.2. For steady state analysis, the two resonant inductors shown in Fig. 3.1 are replaced by a single inductor $L_r$ and the transformer is replaced by a two winding transformer with the same turns ratio. For the active full bridge, an average approximation is applied to the input, while sinusoidal approximation is applied to the output. The input side is modeled as a controlled current source and the average value of the input current is related to the resonant tank current. The output side is modeled as a controlled voltage source and the magnitude of the fundamental component is related to the input voltage.

For the secondary side diode half-bridge, the scenario is similar. Sinusoidal approximation is applied to the input, while average approximation is applied to the output. The input side is modeled as an equivalent resistor as the input voltage is in phase with the input current. The output side is a controlled current source as the average value of the output current is related to the resonant tank current.

For the resonant inductor and capacitor, they are directly presented in the equivalent

Fig. 3.1: SRC topology with a constant input current.
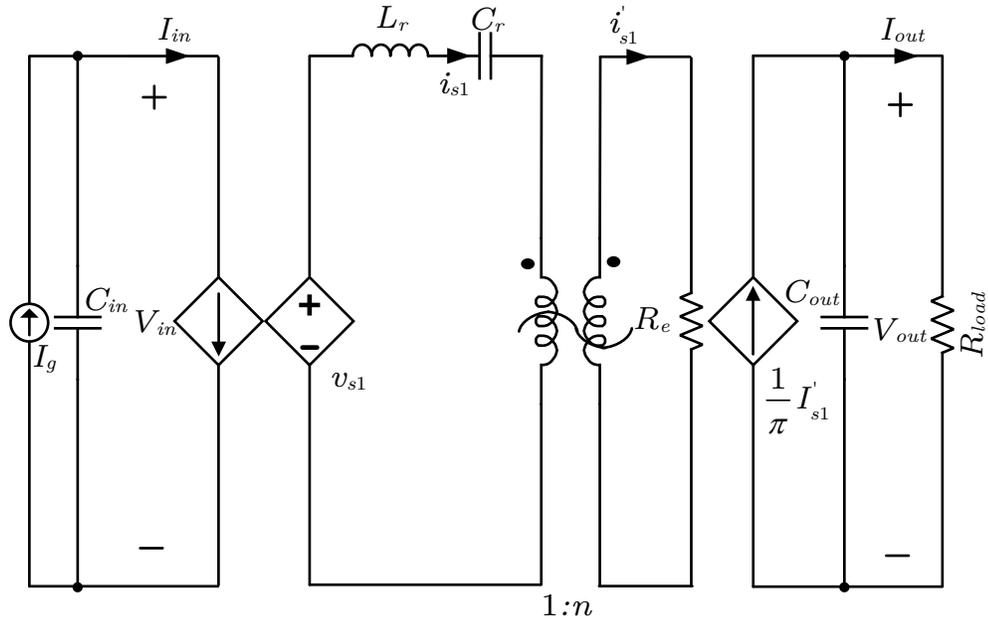


Fig. 3.2: Equivalent circuit of the SRC topology.

circuit as they are linear components. In Fig. 3.2, the equivalent resistance $R_e$, the input current $I_{in}$ and controlled voltage source $v_{s1}$ are expressed as

$$R_e = \frac{2}{\pi^2} R_{load}, \tag{3.1}$$

$$I_{in} = \frac{2I_{s1}}{\pi} \sin(\frac{\alpha}{2}) \cos(\varphi_s), \tag{3.2}$$

$$v_{s1} = \frac{4}{\pi} V_{in} \sin(\frac{\alpha}{2}) \sin(\omega_s t). \tag{3.3}$$

In (3.2) and (3.3), $\varphi_s$ is the phase shift angle of resonant tank current $i_{s1}$ with respect to $v_{s1}$, $I_{s1}$ is the peak value of resonant tank current $i_{s1}$ , $\omega_s$ is the angular switching frequency and $\alpha$ is the phase shift angle of the active full bridge, whose range is from $0°$ to $180°$. The definition of the phase shift angle $\alpha$ is illustrated in Fig. 3.3.

In Fig. 3.2, reflecting the equivalent resistance $R_e$ to the transformer primary side, the fundamental component of the resonant current $i_{s1}$ can be calculated as

$$i_{s1} = \frac{1}{A} \frac{4}{\pi} V_{in} \sin(\frac{\alpha}{2}) \sin(\omega_s t - \varphi_s) = I_{s1} \sin(\omega_s t - \varphi_s), \tag{3.4}$$

where,

$$A = \sqrt{(\frac{2}{n^2\pi^2} R_{load})^2 + (\omega_s L_r - \frac{1}{\omega_s C_r})^2}, \tag{3.5}$$

$$\varphi_s = \arctan(\frac{\omega_s L_r - \frac{1}{\omega_s C_r}}{\frac{2}{n^2\pi^2} R_{load}}), \tag{3.6}$$

$$I_{s1} = \frac{1}{A} \frac{4}{\pi} V_{in} \sin(\frac{\alpha}{2}). \tag{3.7}$$

As illustrated in Fig. 3.2, the relation between output current and the peak value of the resonant tank current $I_{s1}$ can be expressed as

$$I_{out} = \frac{1}{n\pi} I_{s1} = \frac{1}{A} \frac{4}{n\pi^2} V_{in} \sin(\frac{\alpha}{2}). \tag{3.8}$$

For a resistive load, the output voltage and output power are

$$V_{out} = I_{out} R_{load} = \frac{1}{A} \frac{4}{n\pi^2} V_{in} \sin(\frac{\alpha}{2}) R_{load}, \tag{3.9}$$
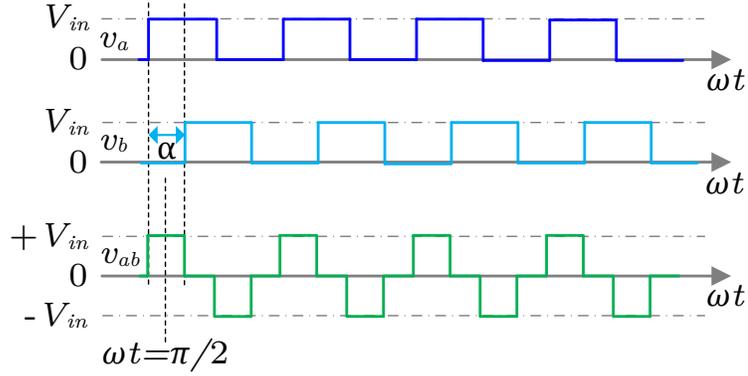
Fig. 3.3: Definition of phase shift angle $\alpha$.

$$P_{out} = V_{out}I_{out} = (\frac{1}{A}\frac{4}{n\pi^2}V_{in}\sin(\frac{\alpha}{2}))^2 R_{load}. \tag{3.10}$$

Considering the ideal case with no losses, the input power of the SRC is equal to the output power,

$$P_{in} = V_{in}I_g = P_{out} = (\frac{1}{A}\frac{4}{n\pi^2}V_{in}\sin(\frac{\alpha}{2}))^2 R_{load}. \tag{3.11}$$

From 3.11, an expression for the SRC input voltage $V_{in}$ can be obtained as

$$V_{in} = \frac{n^2\pi^4 A^2 I_g}{16\sin^2(\frac{\alpha}{2})R_{load}}. \tag{3.12}$$

Substituting (3.12) into (3.8), (3.9) and (3.10), the output current, output voltage and output power of an SRC with constant input current can be expressed as

$$I_{out} = \frac{n\pi^2 A I_g}{4\sin(\frac{\alpha}{2})R_{load}}, \tag{3.13}$$

$$V_{out} = \frac{n\pi^2 A I_g}{4\sin(\frac{\alpha}{2})}, \tag{3.14}$$

$$P_{out} = \frac{n^2\pi^4 A^2 I_g^2}{16\sin^2(\frac{\alpha}{2})R_{load}}. \tag{3.15}$$

The resonant frequency $\omega_o$ and the normalized switching frequency $F$ are defined as

$$\omega_o = \frac{1}{\sqrt{L_r C_r}}, \tag{3.16}$$

$$F = \frac{f_s}{f_o} = \frac{\omega_s}{\omega_o}. \tag{3.17}$$

The characteristic impedance $Z_o$ and loaded quality factor $Q$ of the resonant tank are

$$Z_o = \sqrt{\frac{L_r}{C_r}} = \omega_o L_r = \frac{1}{\omega_o C_r}, \tag{3.18}$$

$$Q = \frac{Z_o}{R_e'} = \frac{n^2 \pi^2 Z_o}{2R_{load}} = \frac{n^2 \pi^2 \omega_o L_r}{2R_{load}}. \tag{3.19}$$

Substituting (3.18) and (3.19) into (3.5),

$$A = \sqrt{(\frac{2}{n^2\pi^2}R_{load})^2 + (\omega_s L_r - \frac{1}{\omega_s C_r})^2} = Z_o\sqrt{\frac{1}{Q^2} + (F - \frac{1}{F})^2}. \tag{3.20}$$

Substituting (3.20) into (3.12) - (3.15), the input voltage, output current, output voltage and output power of an SRC with constant input current can be expressed in forms of normalized switching frequency $F$ and the resonant tank $Q$ as

$$V_{in} = \frac{I_g R_{load}}{4n^2 \sin^2(\alpha/2)}(1 + Q^2(F - \frac{1}{F})^2), \tag{3.21}$$

$$I_{out} = \frac{I_g}{2n\sin(\alpha/2)}\sqrt{(1 + Q^2(F - \frac{1}{F})^2)}, \tag{3.22}$$

$$V_{out} = \frac{I_g R_{load}}{2n\sin(\alpha/2)}\sqrt{(1 + Q^2(F - \frac{1}{F})^2)}, \tag{3.23}$$

$$P_{out} = \frac{I_g^2 R_{load}}{4n^2 \sin^2(\alpha/2)}(1 + Q^2(F - \frac{1}{F})^2). \tag{3.24}$$

Equations $(3.21)$ - $(3.24)$ are the steady state solutions for an SRC with constant current input. From the steady state solutions, it can be seen that the behavior of the SRC with constant current input is quite different from the constant voltage input case, and several conclusions can be drawn. 1) For a certain converter design and load resistance, the gains from phase shift angle $(\alpha)$ input to output current, output voltage and output power are all negative, which means maximum phase shift $(180°)$ results in minimum output power, while lower phase shift leads to a higher output power. 2) The SRC has a non-zero minimum output power. The minimum output power is related to the transformer turns ratio, the input current, the load resistance and the resonant tank parameters. 3) The input voltage and output power can either increase or decrease while the load resistance decreases, which depends on the relation between $R_{load}$ and resonant tank parameters. The above conclusions drawn from the steady state solutions also present challenges for designing an SRC with constant current input. For the output current regulation case, it is necessary to guarantee that the minimum output current is lower than or equal to the objective for the entire load range, which is a requirement for the output voltage regulation case as well. The challenge is that the SRC may not be able to force its input voltage down, which causes the output current or the output voltage to be higher than the control objective.

### 3.1.2 Steady State Analysis of PRC

Figure $3.4$ illustrates the PRC topology with dc constant input current. The resonant tank, which consists of a capacitor $C_p$ and two inductors, each $L_p/2$, is connected to an active full bridge at the input side and a diode rectifier at the output side. The input active bridge consists of devices $Q_1 \ldots Q_4$ , while the output bridge consists of diodes $D_1 \ldots D_4$. A $1 : n$ power transformer provides isolation between the input and output, as well as voltage step-up or step-down. The input is a constant dc current source as shown in Fig. $3.4$, and a phase-shift modulation strategy controls the switches of the PRC.

Similar with the SRC, the equivalent circuit of the PRC shown in Fig. $3.4$ can be derived as illustrated in Fig. $3.5$. For steady state analysis, the two resonant inductors shown in Fig. $3.4$ are replaced by a single inductor $L_p$ . For the active full bridge, the input side is
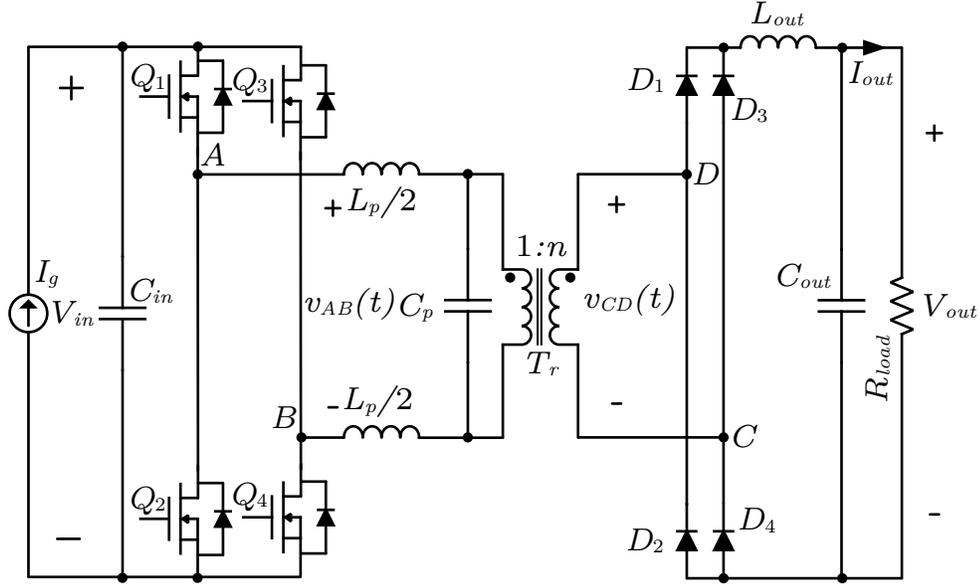
Fig. 3.4: PRC topology with a constant input current.

modeled as a controlled current source and the average value of the input current is related to the resonant tank current, while the output side is modeled as a controlled voltage source and the magnitude of the fundamental component is related to the input voltage. For the resonant inductor and capacitor, they are directly presented in the equivalent circuit as they are linear components.

In Fig. 3.5, the equivalent resistance $R_e$, the input current $I_{in}$ and controlled voltage source $v_{s1}$ are expressed as

$$R_e = \frac{\pi^2}{8} R_{load}, \tag{3.25}$$

$$I_{in} = \frac{2I_{s1}}{\pi} \sin(\frac{\alpha}{2}) \cos(\varphi_s), \tag{3.26}$$

$$v_{s1} = \frac{4}{\pi} V_{in} \sin(\frac{\alpha}{2}) \sin(\omega_s t). \tag{3.27}$$

In (3.26) and (3.27), $\varphi_s$ is the phase shift angle of resonant tank current $i_{s1}$ with respect to $v_{s1}$, $I_{s1}$ is the peak value of resonant tank current $i_{s1}$, $\omega_s$ is the angular switching frequency and $\alpha$ is the phase shift angle of the active full bridge, whose range is from $0°$ to
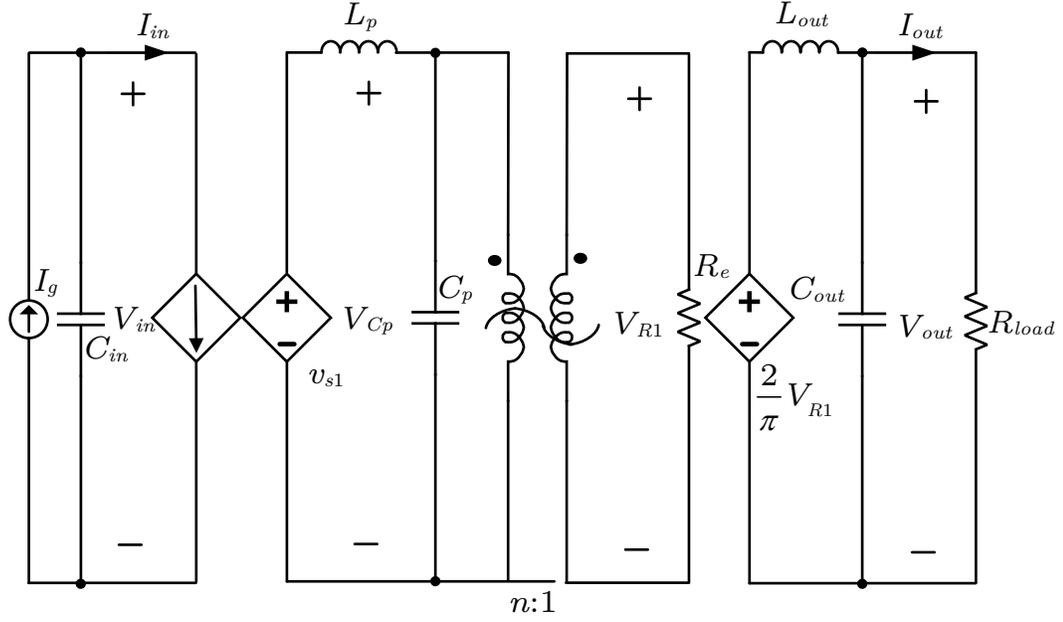
Fig. 3.5: Equivalent circuit of the PRC topology.

180°. The definition of the phase shift angle $\alpha$ is the same as that defined in SRC, which is illustrated in Fig. 3.3.

The resonant frequency $\omega_o$, normalized switching frequency $F$, characteristic impedance $Z_o$ and loaded quality factor $Q$ of the resonant tank are defined as

$$\omega_o = \frac{1}{\sqrt{L_p C_p}}, \tag{3.28}$$

$$F = \frac{f_s}{f_o} = \frac{\omega_s}{\omega_o}. \tag{3.29}$$

$$Z_o = \sqrt{\frac{L_p}{C_p}} = \omega_o L_p = \frac{1}{\omega_o C_p}, \tag{3.30}$$

$$Q = \frac{n^2 R_e}{Z_o} = \frac{n^2 \pi^2 R_{load}}{8 Z_o} = \frac{n^2 \pi^2 R_{load}}{8 \omega_o L_p} = n^2 \pi^2 R_{load} \omega_o C_p. \tag{3.31}$$

From Fig. 3.5, the resonant capacitor voltage $V_{Cp}$ and output voltage $V_{out}$ can be derived as

$$V_{Cp} = \frac{4V_{in}\sin(\frac{\alpha}{2})Q}{\pi\sqrt{F^2 + Q^2(1 - F^2)^2}}, \tag{3.32}$$

$$V_{out} = \frac{8V_{in}\sin(\frac{\alpha}{2})Q}{n\pi^2\sqrt{F^2 + Q^2(1 - F^2)^2}}. \tag{3.33}$$

Note that the input voltage is not constant in the equivalent circuit show in Fig. 3.5. The input voltage is determined by the constant input current, phase shift angle and load. For a lossless power converter, the output power should be equal to the input power, which can be used to derive the input voltage expression. The input voltage $V_{in}$ can be expressed as below in terms of $I_{in}$

$$V_{in} = \frac{I_{in}[F^2 + Q^2(1 - F^2)^2]Z_o^2}{n^2\sin^2(\frac{\alpha}{2})R_{load}}. \tag{3.34}$$

Substituting (3.34) into (3.33), we can get the equation for $V_{out}$ as

$$V_{out} = \frac{I_{in}Z_o}{n\sin(\frac{\alpha}{2})}\sqrt{F^2 + Q^2(1 - F^2)^2}. \tag{3.35}$$

Based on (3.35), the PRC output power $P_{out}$ can be given as

$$P_{out} = \frac{I_{in}^2[F^2 + Q^2(1 - F^2)^2]Z_o^2}{n^2\sin^2(\frac{\alpha}{2})R_{load}}. \tag{3.36}$$

Equations (3.34) - (3.36) are the steady state solutions for a PRC with constant current input. From the steady state solutions, similar conclusions can be drawn for the PRC with constant current input. 1) For a certain converter design and load resistance, the gains from phase shift angle ($\alpha$) input to output current, output voltage and output power are all negative, which means maximum phase shift ($180°$) results in minimum output power, while lower phase shift leads to a higher output power. 2) The PRC has a non-zero minimum output power. The minimum output power is related to the transformer turns ratio, the

input current, the load resistance and the resonant tank parameters.

### 3.1.3    Steady State Analysis of LCL Resonant Converter

The circuit diagram of the LCL resonant converter with constant dc input current is shown in Fig. 3.6. The converter includes a H-bridge, a resonant tank network, an isolation transformer and a diode voltage doubler. The input active bridge consists of devices $Q_1 \ldots Q_4$, while the resonant tank network consists of a first inductor $L$, a parallel capacitor $C$ and a second inductor $kL$. A $1 : n$ power transformer provides isolation between the input and output as well as voltage step-up or step-down. The output voltage doubler consists of diodes $D_1$ and $D_2$, and capacitors $C_1$ and $C_2$. The phase-shift modulation strategy is employed to control the LCL resonant converter.

The equivalent circuit of the LCL resonant converter illustrated in Fig. 3.6 is shown in Fig. 3.7. For the active full bridge, an average approximation is applied to the input, while sinusoidal approximation is applied to the output. The input side is modeled as a controlled current source and the average value of the input current is related to the resonant tank current. The output side is modeled as a controlled voltage source and the magnitude of the fundamental component is related to the input voltage. For the secondary side diode half-bridge, the scenario is similar. Sinusoidal approximation is applied to the input, while average approximation is applied to the output. The input side is modeled as an equivalent resistor as the input voltage is in phase with the input current. The output side is a controlled current source as the average value of the output current is related to the resonant tank current. For the resonant tank network components, they are directly presented in the equivalent circuit as they are linear components.

In Fig. 3.7, the equivalent resistance $R_e$ and controlled voltage source $v_{s1}$ are expressed as

$$R_e = \frac{2}{\pi^2} R_{load}, \tag{3.37}$$

$$v_{s1} = \frac{4}{\pi} V_{in} \sin(\frac{\alpha}{2}) \sin(\omega_s t). \tag{3.38}$$
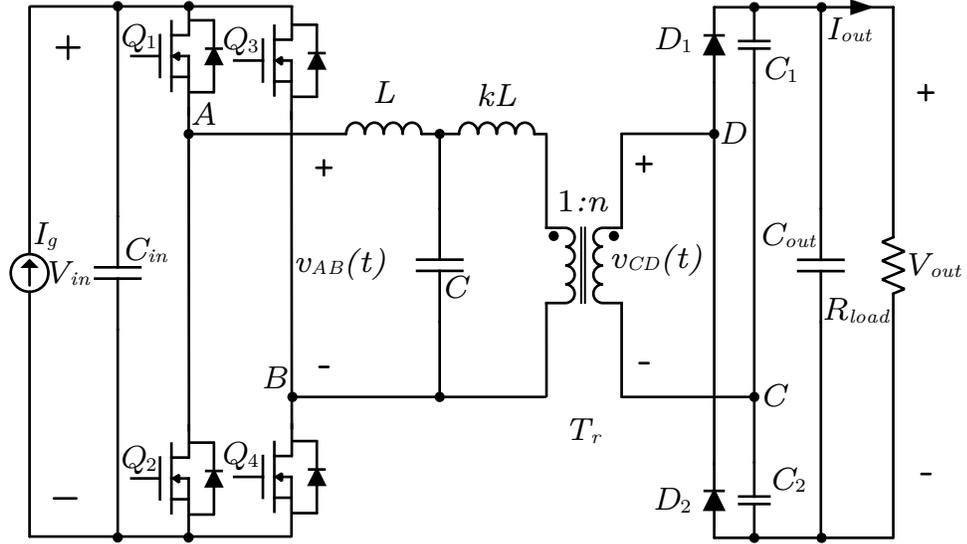
Fig. 3.6: LCL resonant topology with a constant input current.
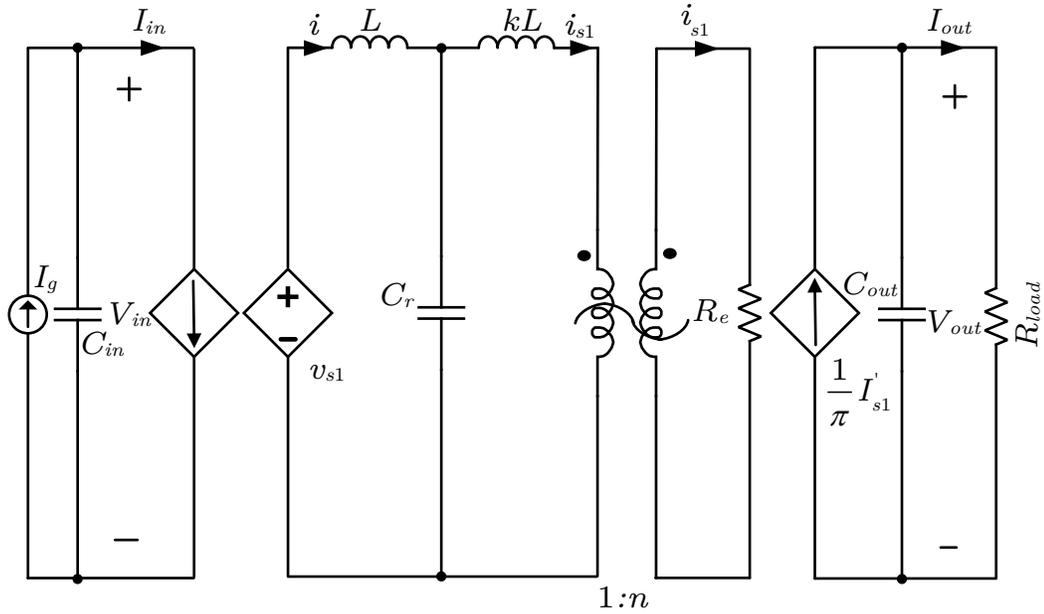


Fig. 3.7: Equivalent circuit of the LCL topology.

In (3.38), $\omega_s$ is the angular switching frequency and $\alpha$ is the phase shift angle of the active full bridge, whose range is from $0°$ to $180°$. The definition of the phase shift angle $\alpha$ is given in Fig. 3.3.

From Fig. 3.7, the relation between the output current $I_{out}$ and the peak value of resonant tank inductor current $i'_{s1}$ can be derived as

$$I_{out} = \frac{1}{n\pi} I_{s1}. \tag{3.39}$$

Reflecting the equivalent resistance $R_e$ to the transformer primary side, the fundamental component of the resonant current $i_{s1}$ can be calculated as

$$i_{s1} = \frac{1}{A}\frac{4}{\pi} V_{in} \sin(\frac{\alpha}{2}) \sin(\omega_s t - \varphi_s) = I_{s1} \sin(\omega_s t - \varphi_s), \tag{3.40}$$

where,

$$I_{s1} = \frac{1}{A}\frac{4}{\pi} V_{in} \sin(\frac{\alpha}{2}). \tag{3.41}$$

$$A = \sqrt{(\frac{2}{n^2\pi^2} R_{load})^2 (1 - \omega_s^2 LC)^2 + [(k+1)\omega_s L - kL^2 C\omega_s^3]^2}, \tag{3.42}$$

Substituting (3.41) into (3.39), we can get

$$I_{out} = \frac{1}{A}\frac{4}{n\pi^2} V_{in} \sin(\frac{\alpha}{2}). \tag{3.43}$$

Note that the input voltage is not constant in the equivalent circuit show in Fig. 3.7. The input voltage is determined by the constant input current, phase shift angle and load. For a lossless power converter, the output power should be equal to the input power, which can be used to derive the input voltage expression. The input voltage $V_{in}$ can be expressed as below in terms of $I_{in}$, phase shift angle $\alpha$ and load resistance $R_{load}$,

$$P_{in} = V_{in} I_{in} = P_{out} = I_{out}^2 R_{load}, \tag{3.44}$$

$$V_{in} = \frac{n^2\pi^4 A^2 I_{in}}{16\sin^2(\frac{\alpha}{2})R_{laod}}. \tag{3.45}$$

Substituting 3.45 into 3.43, we can get

$$I_{out} = \frac{I_{in}A}{2n\sin(\frac{\alpha}{2})R'_e},$$ (3.46)

where

$$R'_e = \frac{2R_{load}}{n^2\pi^2}.$$ (3.47)

Define the resonant frequency $\omega_o$, normalized switching frequency $F$, characteristic impedance $Z_o$ and loaded quality factor $Q$ of the resonant tank as

$$\omega_o = \frac{1}{\sqrt{LC}},$$ (3.48)

$$F = \frac{f_s}{f_o} = \frac{\omega_s}{\omega_o}.$$ (3.49)

$$Z_o = \sqrt{\frac{L}{C}} = \omega_o L = \frac{1}{\omega_o C},$$ (3.50)

$$Q = \frac{Z_o}{R'_e} = \frac{n^2\pi^2 Z_o}{2R_{load}} = \frac{n^2\pi^2\omega_o L}{2R_{load}} = \frac{n^2\pi^2}{2R_{load}\omega_o C}.$$ (3.51)

Substituting (3.48)-(3.51) into (3.42) and (3.46), the output current of LCL resonant converter with constant dc input current is expressed as

$$I_{out} = \frac{I_{in}}{2n\sin(\frac{\alpha}{2})}\sqrt{(1-F^2)^2 + Q^2[1+k(1-F^2)]^2}.$$ (3.52)

With a resistive load, the output voltage and output power are given as

$$V_{out} = \frac{I_{in}R_{load}}{2n\sin(\frac{\alpha}{2})}\sqrt{(1-F^2)^2 + Q^2[1+k(1-F^2)]^2},$$ (3.53)

$$P_{out} = \frac{I_{in}^2 R_{load}}{4n^2\sin^2(\frac{\alpha}{2})}\{(1-F^2)^2 + Q^2[1+k(1-F^2)]^2\}.$$ (3.54)

Equations (3.52) - (3.54) are the steady state solutions for an LCL resonant converter with constant dc current input. Similar with what have been discussed for other resonant converters, the behavior of the LCL resonant converter with constant dc current input is quite different from the constant voltage input case.

### 3.1.4   Steady State Analysis of DABSRC

Figure 3.8 illustrates the DABSRC topology with dc constant input current. The resonant tank, which consists of a capacitor $C_r$ and two inductors, each $L_r/2$, is connected to an active full bridge at the input side and an active full bridge at the output side. The input active bridge consists of devices $Q_1 \ldots Q_4$ , while the output bridge consists of devices $Q_5$ and $Q_8$. A $1 : n$ power transformer, which has two primaries with the same number of turns and two secondaries with the same number of turns connected in series, provides isolation between the input and output. The input is a constant dc current source as shown in Fig. 3.8, and a phase-shift modulation strategy, which controls the three phase shift angles in the converter, controls the switches of the DABSRC. The three phase shift angles are the phase shift between leg $A$ and $B$, between leg $D$ and leg $C$ and between leg $A$ and leg $D$. In order to analyze the DABSRC, the power flow of the LC series resonant tank with two ac voltages illustrated in Fig. 3.9 is analyzed. In Fig. 3.9, the phasor relation between $v_1$ and $v_2$ can be expressed as

$$\frac{v_2}{v_1} = ke^{-j\varphi}, \tag{3.55}$$

where $k > 0$ is the ratio between the magnitudes of $v_2$ and $v_1$, and $\varphi$ is the phase shift of $v_2$ with respect to $v_1$. The resonant tank network current $i$ can be derived as

$$i = \frac{v_1 - v_2}{j\omega L + \frac{1}{j\omega C}} = \frac{j\omega C}{1 - \omega^2 LC}(V_1 - V_2). \tag{3.56}$$

With the following definitions and assumption:

$$r \equiv \frac{\omega_o}{\omega} < 1, \tag{3.57}$$
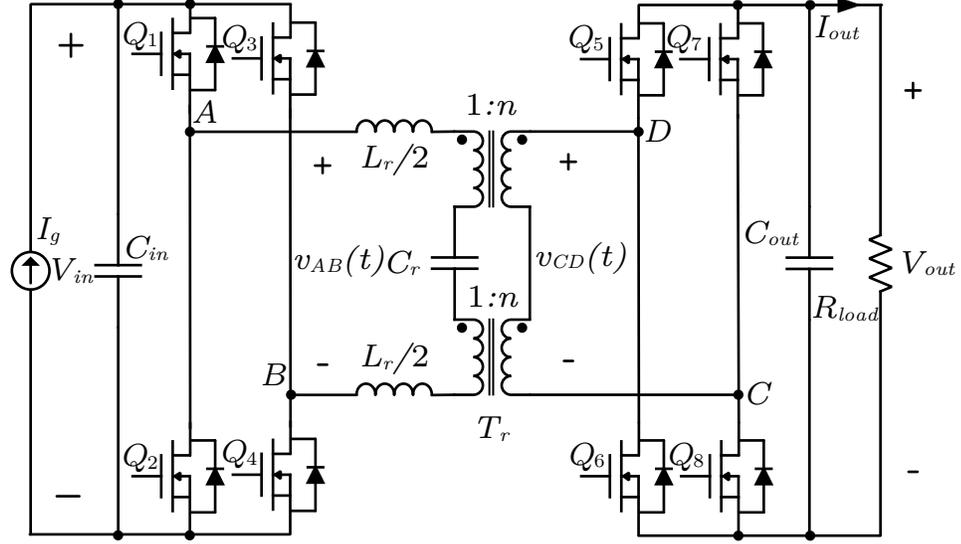
Fig. 3.8: DABSRC topology with a constant input current.
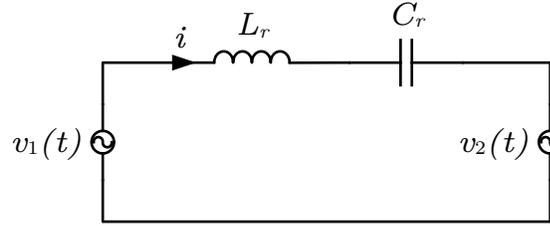


Fig. 3.9: Series L-C resonant tank operating between two sinusoidal voltage sources.

$$\omega_o \equiv \frac{1}{\sqrt{LC}}, \tag{3.58}$$

$$Z_o \equiv \sqrt{\frac{L}{C}} \equiv \omega_o L \equiv \frac{1}{\omega_o C}, \tag{3.59}$$

$$H_o(r) \equiv \frac{r}{1 - r^2}. \tag{3.60}$$

The resonant tank network current $i$ can be expressed as

$$i = \frac{jC\frac{1}{r\sqrt{LC}}}{1 - \frac{1}{r^2 LC}LC}(V_1 - V_2) = j\frac{1}{r}\sqrt{\frac{L}{C}}r^2\frac{1}{r^2 - 1}(v_1 - v2) = -j\frac{H_o(r)}{Z_o}(v_1 - v_2). \tag{3.61}$$

From (3.61), it can be seen that the tank current $i$ is orthogonal to the differential voltage $v_1 - v_2$ applied to the L-C series resonant tank. Since $H_o(r) > 0$, the tank current $i$ lags the differential voltage $v_1 - v_2$ by $90°$.

From (3.55) and (3.61), the complex power flowing from $v_1$ to $v_2$ can be calculated as

$$
\begin{aligned}
S \equiv v_2 i^* &= v_2(-j\frac{H_o(r)}{Z_o}(v_1 - v_2))^* \\
&= v_2(j\frac{H_o(r)}{Z_o}(v_1 - v_2)^*) \\
&= v_2 v_1^*(j\frac{H_o(r)}{Z_o}(1 - \frac{v_2}{v_1})^*) \\
&= j|v_1|\cdot|v_2|(e^{-j\varphi} - k)\frac{H_o(r)}{Z_o}.
\end{aligned}
\tag{3.62}
$$

The active power flowing from $v_1$ to $v_2$ can be derived from (3.62) as the real part of the complex power $S$

$$
P_{out} \equiv \Re[S] = \frac{|v_1|\cdot|v_2|}{Z_o}H_o(r)\sin(\varphi).
\tag{3.63}
$$

From (3.63), it can be seen that the $\varphi$ between $v_2$ and $v_1$ controls the active power flow through the series $LC$ resonant tank. The power always flows from the leading voltage source to the lagging voltage source.

The equivalent circuit of the DABSRC illustrated in Fig. 3.8 is shown in Fig. 3.10. For steady state analysis, the two resonant inductors shown in Fig. 3.8 are replaced by a single inductor $L_r$ and the transformer is replaced by a two winding transformer with the same turns ratio. For the input active full bridge, an average approximation is applied to the input, while sinusoidal approximation is applied to the output. The input side is modeled as a controlled current source and the average value of the input current is related to the resonant tank current. The output side is modeled as a controlled voltage source and the magnitude of the fundamental component is related to the input voltage. For the secondary active full bridge, the scenario is similar. For the resonant inductor and capacitor, they are directly presented in the equivalent circuit as they are linear components.
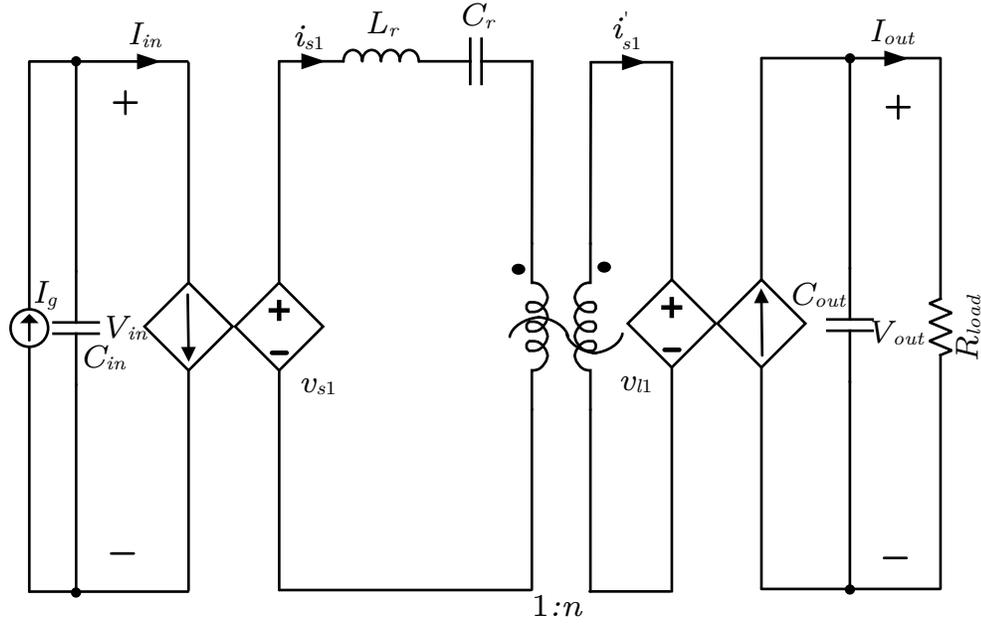
Fig. 3.10: Equivalent circuit of the DABSRC topology.

In Fig. 3.10, the controlled voltage source $v_{s1}$ , and controlled voltage source $v_{l1}$ are expressed as

$$v_{s1} = j\frac{4}{\pi}V_{in}\sin(\frac{\varphi_{AB}}{2})e^{-j\varphi_{AB}}, \tag{3.64}$$

$$v_{l1} = j\frac{4}{\pi}V_{out}\sin(\frac{\varphi_{DC}}{2})e^{-j(\varphi_{AD}+\frac{\varphi_{AB}}{2})}. \tag{3.65}$$

In (3.64) and (3.65), $\varphi_{AB}$ is the phase shift angle between leg $A$ and leg $B$, $\varphi_{AD}$ is the phase shift angle between leg $A$ and leg $D$, and $\varphi_{DC}$ is the phase shift angle between leg $D$ and leg $C$.

Referring Fig. 3.10 back to Fig. 3.9, $v_1$ and $v_2$ can be expressed as

$$v_1 = v_{s1} = j\frac{4}{\pi}V_{in}\sin(\frac{\varphi_{AB}}{2})e^{-j\varphi_{AB}}, \tag{3.66}$$

$$v_2 = \frac{1}{n}v_{l1} = j\frac{4}{n\pi}V_{out}\sin(\frac{\varphi_{DC}}{2})e^{-j(\varphi_{AD}+\frac{\varphi_{AB}}{2})}. \tag{3.67}$$

From (3.63) and (3.64)-(3.67), the output power flow through the DABSRC is

$$P_{out} = \frac{8V_{in}V_{out}H_o(r)}{n\pi^2 Z_o} \sin(\frac{\varphi_{AB}}{2}) \sin(\frac{\varphi_{DC}}{2}) \sin(\varphi_{AD} + \frac{\varphi_{DC} - \varphi_{AB}}{2}). \tag{3.68}$$

Note that the input voltage is not constant in the equivalent circuit show in Fig. 3.8. The input voltage is determined by the constant input current, the three phase shift angles and load. For a lossless power converter, the output power should be equal to the input power, which can be used to derive the output voltage expression. The output voltage $V_{out}$ and output current $I_{out}$ can be expressed as

$$V_{out} = \frac{n\pi^2 Z_o I_{in}}{8H_o(r) \sin(\frac{\varphi_{AB}}{2}) \sin(\frac{\varphi_{DC}}{2}) \sin(\varphi_{AD} + \frac{\varphi_{DC} - \varphi_{AB}}{2})}, \tag{3.69}$$

$$I_{out} = \frac{n\pi^2 Z_o I_{in}}{8R_{load}H_o(r) \sin(\frac{\varphi_{AB}}{2}) \sin(\frac{\varphi_{DC}}{2}) \sin(\varphi_{AD} + \frac{\varphi_{DC} - \varphi_{AB}}{2})}. \tag{3.70}$$

Equations (3.69) and (3.70) are the steady state solutions for a DABSRC with constant current input. From the steady state solutions, it can be seen that the outputs of the DABSRC with constant current input can be controlled by the three phase shift angles, as well as the power flow.

### 3.1.5 Converter Topology Selection

From the steady state analysis of the commonly employed resonant converters with constant dc input current, which are series resonant converter, parallel resonant converter, LCL resonant converter and dual active bridge series resonant converter, several general features can be given. First, for a certain converter design and load resistance, the gains from phase shift angle inputs to output current, output voltage and output power are all negative, which means maximum phase shift (180°) results in minimum output power, while lower phase shift leads to a higher output power. Second, the resonant converters have a non-zero minimum output power. The minimum output power is related to the transformer turns ratio, the input current, the load resistance and the resonant tank parameters.

On the other hand, different resonant converter has different characteristics. For the SRC, the converter has a load independent output current behavior if it operates at resonance. For the PRC, the output behaves as a load independent natural voltage source when operates at resonance. For the LCL resonant converter, it can be design to have a load independent current or load independent voltage behavior at its output. For the DABSRC, the converter has a load independent output voltage controlled by the three phase shift angles.

Depending on the application scenario, the resonant converter topology should be selected properly. For the work presented in this dissertation, the converter draws power from the dc constant current input, and provides power to the load with a regulated output current. Among the four different resonant converters, the SRC and LCL resonant converter are capable of providing a load independent output current, and have a nature current source behavior. However, the LCL resonant converter has more components, and does not operate at resonance in order to achieve the aforementioned properties. Based on the steady state solutions and the above analysis, the SRC is selected to be the dc current to dc current converter in this work.

## 3.2   Component Stress Analysis of the SRC

It is important to understand the component stress in a converter in order to have optimized converter design. The component stress in the converter determines the selection of devices, helps the converter loss analysis, and provides guideline for PCB layout.

### 3.2.1   Resonant Inductor Current Analysis

The conduction loss of the converter is directly related to the resonant inductor RMS current. With the fundamental approximation, from (3.7), (3.20) and (3.21), the resonant inductor rms current can be expressed as

$$I_{L_r,rms} = \frac{\pi I_g}{2\sqrt{2}\sin(\frac{\alpha}{2})}\sqrt{1 + Q^2(F - \frac{1}{F})^2}. \tag{3.71}$$

For the output current regulated case, sine of half of the phase shift angle $\hat{I}\acute{s}$ can be calculated from (3.22) as

$$\sin(\frac{\alpha}{2}) = \frac{I_g}{2nI_{out}}\sqrt{1 + Q^2(F - \frac{1}{F})^2}. \tag{3.72}$$

Substituting (3.72) into (3.71), the resonant inductor rms current can be expressed as

$$I_{L_r,rms} = \frac{n\pi I_{out}}{\sqrt{2}}. \tag{3.73}$$

From (3.73), it can be seen that the resonant inductor rms current is directly determined by the transformer turns ratio n and output current, and independent from the normalized switching frequency $F$, as well as $Q$ (load). This can be justified since the output current is the resonant inductor current rectified by the secondary diode half-bridge voltage doubler.

### 3.2.2 Resonant Capacitor Differential Voltage Analysis

The differential voltage across the resonant capacitor governs its rating and size. From (3.4), (3.20) and (3.21), the fundamental component of the resonant tank current $i_{s1}$ can be derived. Based on that, the peak value of the differential voltage across the resonant capacitor can be derived as

$$V_{C_r} = \frac{\pi I_g Z_o}{2F \sin(\frac{\alpha}{2})}\sqrt{1 + Q^2(F - \frac{1}{F})^2}. \tag{3.74}$$

Substituting (3.72) into (3.74), with output current regulated, the peak value of the resonant capacitor differential voltage can be expressed as

$$V_{C_r} = \frac{n\pi I_{out} Z_o}{F}. \tag{3.75}$$

From (3.75), the peak value of the resonant capacitor differential voltage is determined by the transformer turns ratio, the output current, the resonant tank characteristic impedance and the normalized switching frequency, and independent from the $Q$ (load).

From (3.75), $V_{C_r}$ can be further expressed in terms of $F$, $Q$ and $R_{load}$ by replacing $Z_o$ with $Q$ and $R_{load}$, resulting in

$$V_{C_r} = \frac{2I_{out}QR_{load}}{n\pi F}. \tag{3.76}$$

From (3.76), it can be seen that the relation between the normalized switching frequency $F$ and the maximum $Q$ can be obtained for a certain design with requirements for $V_{C_r}$, $I_{out}$ and minimum $R_{load}$. As an example, the relation between $F$ and the constraint (3.76) for $Q$ of the resonant tank is illustrated in Fig. 3.11. In this example, $V_{C_r}$ is 600 V, $I_{out}$ is 330 mA, transformer turns ratio $n$ is 2 and minimum $R_{load}$ is 450 $\Omega$. In Fig. 3.11, the designed operating point should be in the region below the curve in order to have $V_{C_r}$ lower than desired value.

### 3.2.3  Resonant Capacitor Terminal to Ground Voltage Analysis

The resonant capacitor terminal to ground voltage analysis can guide the PCB layout to guarantee that the voltage isolation level from terminals of the resonant capacitor to ground is high enough to handle the potential between them. The one-cycle operation of the SRC topology is composed of a sequence of linear circuits, each of which corresponds to a specific switching interval. As shown in Fig. 3.12, there are six equivalent circuit topologies based on the switching states. The resonant capacitor terminal to ground voltages for each switching interval can be derived by solving the circuits illustrated in Fig. 3.12.

In Fig. 3.12, $V_E$ is the reflected output voltage on each of the transformer primary sides, $V_{in}$ is the input voltage at a particular operating point. For different circuit topologies in Fig. 3.12 (a) to Fig. 3.12 (f), the circuit behavior can be described by the following equations,

$$L_r \frac{di_{L_r}}{dt} = V - v_{C_r}, \tag{3.77}$$

$$v_{C_r 2} = V' + \frac{L_r}{2} \frac{di_{L_r}}{dt} = V - v_{C_r}, \tag{3.78}$$

Fig. 3.11: Maximum $Q$ versus normalized switching frequency $F$ according to (3.76) under the condition of $V_{C_r} = 600$ V, $I_{out} = 330$ mA, $n = 2$ and minimum load resistance is 450 $\Omega$.

$$v_{C_r 1} = v_{C_r 2} + v_{C_r},  \tag{3.79}$$

where the value of $V$ and $V'$ for different circuit topologies are listed in TABLE 3.1.

From (3.77) - (3.79) and the values in TABLE 3.1, the capacitor terminal to ground voltages $V_{C_r 1}$ and $V_{C_r 2}$ in different switching intervals can be calculated as tabulated in TABLE 3.2. From TABLE 3.2, the equations for $V_{C_r 1}$ and $V_{C_r 2}$ are related to the switching status of the SRC, while the polarity of $V_{C_r}$ in the equations is determined by the direction of the resonant inductor current. When $Q_1$ and $Q_3$ are on (c and d), $V_{C_r 1}$ and $V_{C_r 2}$ are expressed as $V_{in} + 0.5 v_{C_r}$ and $V_{in} - 0.5 v_{C_r}$, respectively, which means that one of the two terminal voltages is higher than $V_{in}$ by half of $|v_{C_r}|$.

For a conventional SRC with constant voltage input and using phase shift modulation control, 180° phase shift angle results in maximum output power for a given load. For an SRC with constant current input using phase shift modulation control, 180° phase shift angle results in the minimum output power for a given load. In general, for both cases, the
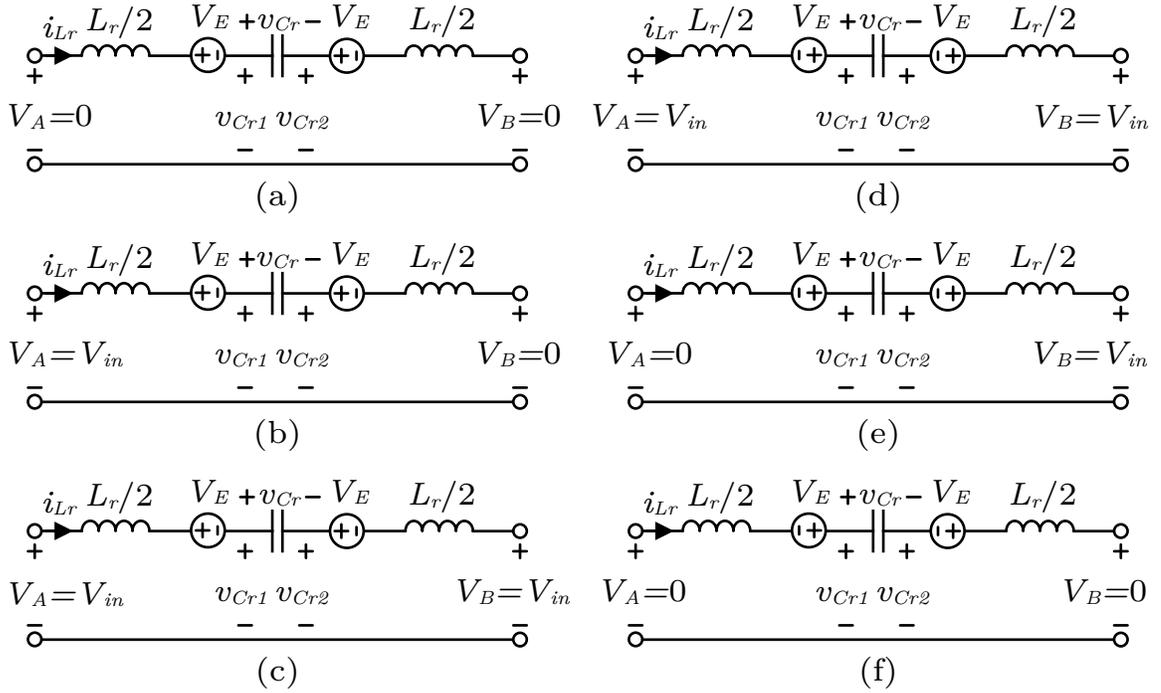
Fig. 3.12: Circuit topologies of SRC. (a) $Q_2$, $Q_4$ on ($i_{L_r} > 0$). (b) $Q_1$, $Q_4$ on ($i_{L_r} > 0$). (c) $Q_1$, $Q_3$ on ($i_{L_r} > 0$). (d) $Q_1$, $Q_3$ on ($i_{L_r} < 0$). (e) $Q_2$, $Q_3$ on ($i_{L_r} < 0$). (f) $Q_2$, $Q_4$ on ($i_{L_r} < 0$).

Table 3.1: VALUE OF $V$ AND $V'$ FOR
DIFFERENT CIRCUIT TOPOLOGIES OF
THE SRC

| Circuit Topologies | $V$ | $V'$ |
|:---:|:---:|:---:|
| a | $-2V_E$ | $V_E$ |
| b | $V_{in} - 2V_E$ | $V_E$ |
| c | $-2V_E$ | $V_{in} + V_E$ |
| d | $2V_E$ | $V_{in} - V_E$ |
| e | $2V_E - V_{in}$ | $V_{in} - V_E$ |
| f | $2V_E$ | $-V_E$ |

phase shift angle range is designed to be less than 180° for the desired load range in order to keep some margin. As a result, there is always a switching interval when $Q_1$ and $Q_3$ are on and the capacitor terminal voltages are expressed as $V_{in} \pm 0.5v_{C_r}$.

Table 3.2: RESONANT CAPACITOR TERMINAL TO GROUND VOLTAGES
FOR DIFFERENT CIRCUIT TOPOLOGIES OF THE SRC

| Circuit Topologies | $v_{Cr1}$ | $v_{Cr2}$ |
|:---:|:---:|:---:|
| a | $0.5 v_{C_r}$ | $-0.5 v_{C_r}$ |
| b | $0.5 V_{in} + 0.5 v_{C_r}$ | $0.5 V_{in} - 0.5 v_{C_r}$ |
| c | $V_{in} + 0.5 v_{C_r}$ | $V_{in} - 0.5 v_{C_r}$ |
| d | $V_{in} + 0.5 v_{C_r}$ | $V_{in} - 0.5 v_{C_r}$ |
| e | $0.5 V_{in} + 0.5 v_{C_r}$ | $0.5 V_{in} - 0.5 v_{C_r}$ |
| f | $0.5 v_{C_r}$ | $-0.5 v_{C_r}$ |

### 3.2.4 Power Loss Analysis

Based on the resonant inductor rms current analysis presented in Section 3.2.1, the conduction losses can be analyzed. The conduction losses in the individual components are expressed as

$$P_{Q1} = P_{Q2} = P_{Q3} = P_{Q4} = I_{Lr,rms}^2 R_{onQ} D = \frac{n^2 \pi^2 I_{out}^2 R_{onQ} D}{2}, \qquad (3.80)$$

$$P_{tank} = I_{Lr,rms}^2 (R_{ESR\_L_r} + R_{ESR\_C_r}) = \frac{n^2 \pi^2 I_{out}^2 (R_{ESR\_L_r} + R_{ESR\_C_r})}{2}, \qquad (3.81)$$

$$P_{transformer} = I_{Lr,rms}^2 \left(R_{TFR\_Pri} + \frac{R_{TFR\_Sec}}{n^2}\right) = \pi^2 I_{out}^2 \frac{(n^2 R_{TFR\_Pri} + R_{TFR\_Sec})}{2}, \qquad (3.82)$$

where $R_{onQ}$ is the on state resistance of the MOSFETs, $D$ is the switch conducting duty cycle that is 0.5 for the applied phase shift modulation control, $R_{ESR\_Lr}$ and $R_{ESR\_Cr}$ are the ESRs of the resonant inductor and resonant capacitor respectively, $R_{TFR\_Pri}$ and $R_{TFR\_Sec}$ are the winding resistances of transformer primary and secondary respectively.

The total conduction loss in the converter expressed in terms of $I_{out}$ and transformer turns ratio $n$ is given by

$$P_{Loss} = \frac{n^2 \pi^2 I_{out}^2}{2}(R_{onQ} D + R_{ESR\_L_r} + R_{ESR\_C_r} + R_{TFR\_Pri}) + \frac{\pi^2 I_{out}^2 R_{TFR\_Sec}}{2}. \qquad (3.83)$$

From (3.83), it can be seen that the conduction loss is higher with higher transformer turns ratio $n$ for the same output current.

## 3.3  Output Characteristics Analysis of the SRC

From the steady state analysis presented in Section 3.1.1, it has been seen that the behavior of the SRC with constant input current differs from the constant input voltage case. Different design considerations and constrains are required because of the new behaviors found in this work. In order to develop the design constrains, the output characteristics are further analyzed in this section based on the steady state analysis results.

### 3.3.1  Output Power Analysis

For output current regulation, it is desirable that as the load resistance decreases the output power decrease monotonically as well over the full load range. These conditions can be derived by further analysis of the steady state solutions.

In order to do further analysis, the output power equation (3.24) is rewritten in a form as

$$P_{out} = \frac{I_g^2}{4n^2 \sin^2(\frac{\alpha}{2})}[R_{load} + \frac{n^4\pi^4 Z_o^2}{4R_{load}}(F - \frac{1}{F})^2] = KZ, \tag{3.84}$$

where

$$K = \frac{I_g^2}{4n^2 \sin^2(\frac{\alpha}{2})}, \tag{3.85}$$

$$Z = R_{load} + \frac{n^4\pi^4 Z_o^2}{4R_{load}}(F - \frac{1}{F})^2. \tag{3.86}$$

In (3.84), $K$ can be considered as a constant for a given input current, phase shift angle and transformer turns ratio. The output power is then directly proportional to $Z$. The condition mentioned above requires that $Z$ should decrease with the load resistance. The derivative of $Z$ with respect to $R_{load}$ is employed to solve the condition, which is

$$\frac{\partial Z}{\partial R_{load}} = 1 - \frac{n^4\pi^4 Z_o^2}{4R_{load}^2}(F - \frac{1}{F})^2. \tag{3.87}$$

If $\partial Z/\partial R_{load}$ is not negative, the condition is satisfied, which can be expressed as

$$1 - \frac{n^4\pi^4 Z_o^2}{4R_{load}^2}(F - \frac{1}{F})^2 \geq 0, \tag{3.88}$$

$$R_{load} \geq \frac{n^2\pi^2 Z_o}{2}|F - \frac{1}{F}| \Rightarrow Q \leq \frac{1}{|F - \frac{1}{F}|}. \tag{3.89}$$

From (3.89), the relation between output power and load resistance is determined by the resonant tank parameters, switching frequency, and the transformer turns ratio. The relation between the normalized switching frequency $F$ and the constraint (3.89) for $Q$ of the resonant tank is illustrated in Fig. 3.13. The output power decreases while the load resistance decreases only if $Q$ is less than $1/|F-1/F|$, which is the gray shaded region shown in Fig. 3.13. The output power reaches its minimum value when $Q$ is equal to $1/|F-1/F|$, which is the solid line in Fig. 3.13. The output power increases while the load resistance decreases if $Q$ is greater than $1/|F-1/F|$, as indicated by the white region in Fig. 3.13. For a system with output current regulation, the resonant tank parameters and normalized switching frequency should be designed properly so that the SRC operating point lies in the gray shaded region as shown in Fig. 3.13, for the entire load range.

### 3.3.2 Current Gain Analysis

For output current regulation, the current gain for maximum phase shift ($180°$) must be designed to be lower than or equal to the objective for the entire load range so that phase shift modulation can be employed to control the output current and meet the control objective. The current gain is defined as

$$M_I = \frac{I_{out}}{I_g}. \tag{3.90}$$
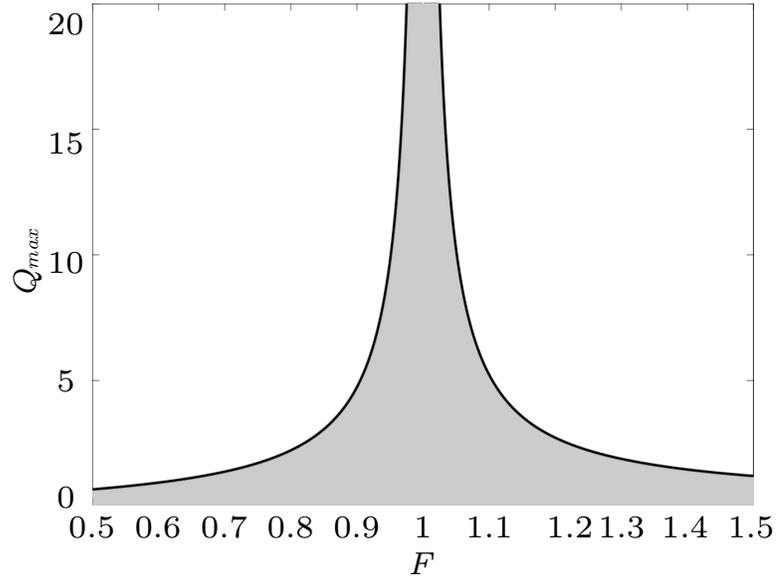
Fig. 3.13: Maximum $Q$ versus normalized switching frequency according to ((3.89).

Based on the analysis presented in Section 3.1.1, the current gain can be derived as

$$M_I = \frac{\sqrt{1 + Q^2(F - \frac{1}{F})^2}}{2n\sin(\frac{\alpha}{2})}. \tag{3.91}$$

Defining $m$ as the desired current gain gives the constraint,

$$\frac{\sqrt{1 + Q^2(F - \frac{1}{F})^2}}{2n\sin(\frac{\alpha}{2})} \leq m \Rightarrow Q \leq \frac{\sqrt{(2mn\sin(\frac{\alpha}{2}))^2 - 1}}{|F - \frac{1}{F}|}. \tag{3.92}$$

In (3.91), the current gain increases as the load resistance decreases for a given converter design, so the lightest load (lowest load resistance) operating point should be considered while designing the converter. In other words, (3.92) needs to be satisfied for the lightest load in order to obtain desired behavior for the entire load range.

The transformer turns ratio requirement can also be derived from (3.92). In (3.92), since $Q$ of the resonant tank should be a positive real value, the constraint becomes

$$(2mn\sin(\frac{\alpha}{2}))^2 > 1 \Rightarrow n > \frac{1}{2m\sin(\frac{\alpha}{2})}. \tag{3.93}$$

So, the minimum transformer turns ratio can be expressed as

$$n_{min} = \frac{1}{2m}. \tag{3.94}$$

The transformer turns ratio needs to be higher than the minimum value shown in (3.94). As an example, the constraints presented in (3.92) with current gain $m = 1/3$ for different transformer turns ratios are illustrated in Fig. 3.14. With $m = 1/3$, the minimum transformer turns ratio $n_{min}$ is 1.5. In Fig. 3.14, the constraints for $n$ equal to 2, 3 and 4 are presented. From Fig. 3.14, it can be seen that higher $Q$ is allowed for the same normalized switching frequency $F$ with higher transformer turns ratio $n$. On the other hand, higher transformer turns ratio means higher resonant inductor rms current and higher conduction loss from (3.73) and (3.83).

### 3.3.3  Current Source Behavior Analysis

From (3.91), the current gain $M_I$ is a function of quality factor $Q$, normalized switching frequency $F$, transfer turns ratio $n$ and the phase shift angle $\alpha$. By close examination of (3.91), it can be seen that the current gain $M_I$ becomes independent of $Q$ (load) if the normalized switching $F$ is equal to 1. Furthermore, when $F$ is equal to 1, $M_I$ can be expressed as

$$M_I = \frac{I_{out}}{I_{in}} = \frac{1}{2n\sin(\frac{\alpha}{2})}. \tag{3.95}$$

From (3.95), the current gain of the SRC with constant current input only depends on the transformer turns ratio $n$ and the SRC input bridge phase shift angle $\alpha$, and is independent of the load resistance $R_{load}$, which means the SRC has a current source output behavior. From (3.95), it can be seen that, for the SRC with constant current input, maximum phase shift (180°) results in minimum current gain, while lower phase shift angle leads to a higher current gain. When the phase shift angle $\alpha$ equals to 180°, the minimum
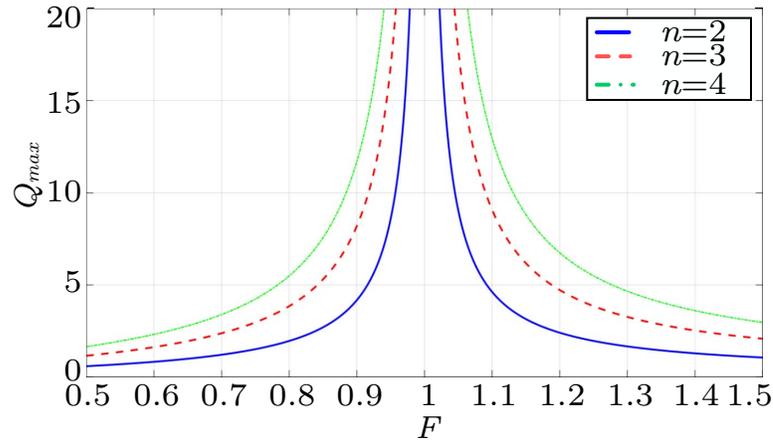
Fig. 3.14: Maximum $Q$ versus normalized switching frequency according to (3.92) for different transformer turns ratios; green dash-dotted line is for $n=4$, red dashed line is for $n=3$ and blue solid line is for $n=2$.
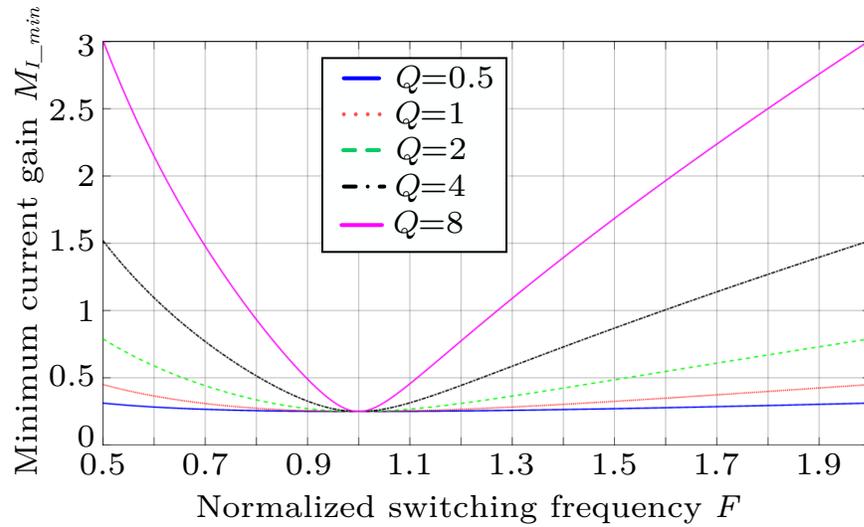


Fig. 3.15: Minimum converter current gain $M_{I\_min}$ versus normalized switching frequency $F$ for different $Q$ values with $n = 2$.

current gain can be expressed as

$$M_{I\_min} = \frac{I_{out}}{I_{in}} = \frac{1}{2n}. \tag{3.96}$$

From (3.96), it can be clearly seen that the minimum current gain of the SRC with constant current input is determined by the transformer turns ratio $n$. As a result, the transformer turns ratio $n$ must be properly designed so that the minimum current gain is

lower than the objective, considering the input current variation. As an example, the plots of minimum current gain $M_{I\_min}$ versus the normalized switching frequency $F$ are illustrated in Fig. 3.15 for different $Q$ values with transformer turns ratio $n = 2$.

## 3.4    Design Considerations and Procedures

Because of the different behavior of the SRC with constant dc input current found in this work, the conventional design considerations and procedures for SRC with constant dc input voltage presented in the literature can not be applied. In this section, two application scenarios are considered. The first one is a design with non-zero minimum output power, and the other one is a design with current source behavior. For the design with non-zero minimum output power, the converter needs less assistance for ZVS operation. For the design with current source behavior, the converter can work with short-circuit output while regulating the output current. Based on the practical application, one can choose the proper design that satisfies the objectives.

### 3.4.1    Considerations and Procedures of Design with Non-Zero Minimum Output Power

The converter can be designed by combining the constrains from input voltage analysis, current gain analysis and resonant capacitor differential voltage analysis. The designed operating point should be within the gray shaded region in Fig. 3.13 and the region under the solid curve in Fig. 3.11 and Fig. 3.14. Also, lower $Q$ means lower harmonic rejection for a certain normalized switching frequency. As an example, the designed operating point and the constraints from earlier analysis in terms of relation between $Q_{max}$ and $F$ are illustrated in Fig. 3.16. In Fig. 3.16, the red cross marks the designed operating point, the solid line is $Q_{max}$ versus normalized switching frequency $F$ according to (3.89), the dashed line is $Q_{max}$ versus $F$ according to (3.76) and the dash-dot line is $Q_{max}$ versus $F$ according to (3.92). From Fig. 3.16, one can notice that the designed operating point gives the maximum $Q$ for this design scenario.

In practice, the values of resonant components may vary with manufacturing and with
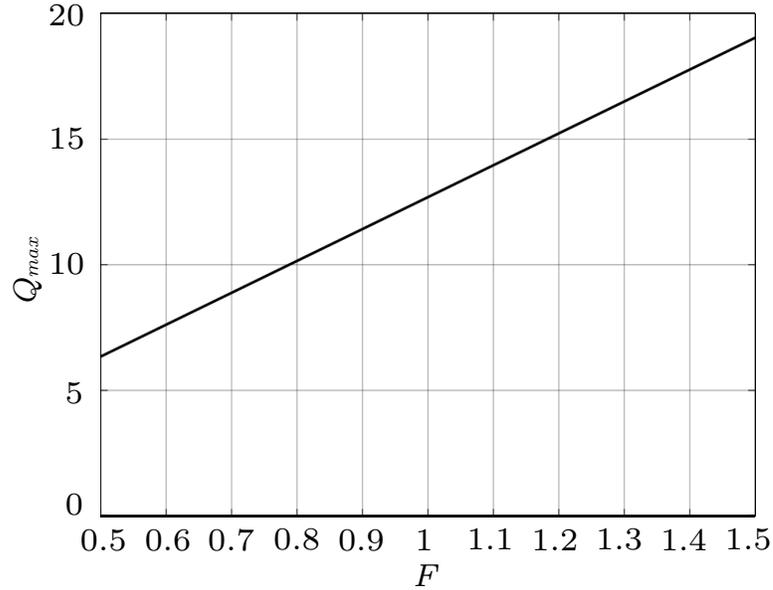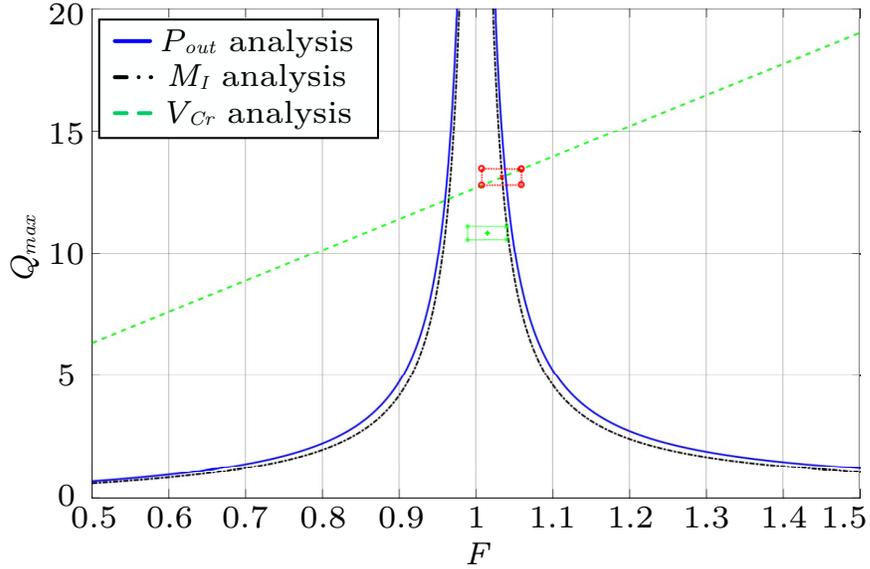
Fig. 3.16: Maximum $Q$ versus normalized switching frequency according to (3.89), (3.76) and (3.92) under the condition of $V_{C_r} = 600$ V, $I_{out} = 330$ mA, $n = 2$ and minimum load resistance is 450 $\Omega$. Red cross: ideal operating point. Red dotted rectangular area: possible operating region of the ideal operating point with variation of resonant components. Green plus sign: designed operating point. Green solid rectangular area: possible operating region of the designed operating point with variation of resonant components.

time. In this case, the operation changes from a single point to a possible region. The area of the possible operating region depends on how much variation the components have. As illustrated in Fig. 3.16, while considering $\pm 5\%$ variation in the values of resonant compo-nents, the designed operation changes from the red cross point to the red dotted rectangular area. From Fig. 3.16, it can be seen that half of the rectangular area is beyond the con-straints derived earlier, which means that the steady state solution may not always exist for the entire desired load range. So, it is important to consider the variation of the res-onant components while designing an SRC with constant current input. In this case, the whole possible operating region instead of just a single operating point should satisfy the constraints derived earlier.

### 3.4.2 Considerations and Procedures of Design with Current Source Behavior

As analyzed in Section 3.3.3, the normalized switching frequency is chosen to be one in order to obtain current source behavior at the output of the SRC with constant current

input. As a result, according to (3.71) and (3.74) the resonant inductor rms current and resonant capacitor voltage are independent from the load as well, which can be written as

$$I_{L_r,rms} = \frac{\pi I_g}{2\sqrt{2}\sin(\frac{\alpha}{2})}, \tag{3.97}$$

$$V_{C_r,rms} = \frac{\pi Z_o I_g}{2\sqrt{2}\sin(\frac{\alpha}{2})}. \tag{3.98}$$

From (3.97), it can be seen that the rms current of the resonant inductor only depends on dc input current and phase shift angle $\alpha$. From (3.95), for a given current gain, the required phase shift angle $\alpha$ is determined by the transformer turns ratio $n$. So, the rms current of the resonant inductor is actually determined by the dc input current and transformer turns ratio $n$ for a given current gain. Since the resonant inductor rms current is independent from the load as well, it should be constant for the entire load range for a given design and dc input current.

Equation (3.98) shows that the rms voltage of the resonant capacitor depends on the characteristic impedance $Z_o$ of the resonant tank, the input current and the phase shift angle $\alpha$. By looking at (3.97) and (3.98) carefully, one can notice that the rms voltage of the resonant capacitor is the rms current of the resonant inductor $I_{L_r,rms}$ multiplied by the characteristic impedance $Z_o$. Similar to $I_{L_r,rms}$ , the resonant capacitor rms voltage should be constant for the entire load range for a given design.

For a given application scenario, the SRC with constant current input and regulated output current can be designed by applying (3.95), (3.97) and (3.98). The design procedure is summarized as follows.

1) Calculate the possible current gain range based on the given input current range and desired output current.

2) Determine the transformer turns ratio based on the minimum current gain and (3.96) with the considerations of design margin and losses. One should notice that lower phase shift angle $\alpha$ means higher rms resonant inductor current, which means higher losses, so it

is important to keep a proper margin in order to obtain higher efficiency.

3) Substituting (3.96) into (3.97) and (3.98), the rms values of the resonant inductor current and the resonant capacitor voltage are expressed as

$$I_{L_r,rms} = \frac{n\pi I_{out}}{\sqrt{2}}, \tag{3.99}$$

$$V_{C_r,rms} = \frac{n\pi Z_o I_{out}}{\sqrt{2}}. \tag{3.100}$$

4) From (3.99), it can be seen that the resonant inductor rms current is determined once the transformer turns ratio $n$ is selected.

5) Based on the desired voltage stress on the resonant capacitor, the designed transformer turns ratio n, the desired output current and (3.100), the characteristic impedance $Z_o$ of the resonant tank can be calculated.

6) The desired operating frequency of the SRC generally is a known parameter for a design scenario. Based on the calculated characteristic impedance $Z_o$, the desired switching frequency and (3.18), the value of either resonant inductor or resonant capacitor can be determined.

7) Based on the result from last step and (3.16), value of the other resonant component can be calculated.

For the design of an SRC with constant current input and regulated output current, one should notice that the minimum quality factor $Q$ of the resonant tank is at full load. Lower voltage stress on the resonant capacitor means lower characteristic impedance $Z_o$, which results in lower quality factor $Q$ at full load. Lower quality factor $Q$ means higher harmonic components in the SRC, which is not desired. However, on the other hand, higher quality factor $Q$ means lower resonant capacitance for a given switching frequency. In practice, the transformer used in the SRC has a parasitic capacitance, especially for a high frequency, high isolation voltage transformer. In this case, high quality factor $Q$ at full load may result in a condition that the transformer parasitic capacitance is comparable to the

resonant capacitance, which is also not desirable. So, an SRC with constant current input and regulated output current should be designed according to the analysis and procedure presented in this paper along with other considerations such as load range and parasitic parameters of the employed transformer.

## 3.5   High Voltage Transformer Modeling

The isolation feature of the SRC is achieved through an isolation transformer. The parasitic components in a high voltage transformer need to be taken into account in transformer and power converter design and analysis for their significant effects on overall performance. The parasitic components of transformers used in resonant converters have significant impact on their overall performance, including waveform distortion and reduced efficiency [109].

References [110–115] provide several approaches for modeling, calculation, and determination of parasitic parameters in high frequency transformers based upon the magnetic and electric field analysis. However, those approaches need either a large amount of information about the geometry and electrostatic behavior of the transformer or sophisticated field analysis. In [116] and [117], the authors presented a two-port network and step response approach to experimentally determine the stray capacitances in high frequency transformers. The two-port network approach requires significant computational power and requires that the transformer windings be separated from the magnetic core for measurement, which can be difficult or destructive once the core is set in a planar design. The step response approach requires a non-linear magnetic core model and can be difficult and inaccurate for high frequency designs due to oscillations in the excitation current and strong sensitivity to small deviations in the time duration measurement.

This section presents simple but accurate techniques for experimental determination of parasitic parameters in high frequency two-winding transformers. The proposed approach does not require a magnetic core model, information about the geometry and electrostatic behavior of the transformer, or complex field analysis.

### 3.5.1 Model of a High Voltage Transformer

Figure 3.17 shows the typical equivalent circuit model of a two-winding transformer including parasitic effects, where $V_P$ and $V_S$ are the primary and secondary terminal voltages, $R_{lp}$ and $R_{ls}$ are the resistances of the primary and secondary windings, $L_{lp}$ and $L_{ls}$ are the leakage inductances of the primary and secondary, $L_m$ is the magnetizing inductance, $R_C$RC is the equivalent core loss resistance, and $C_P$, $C_S$ and $C_{PS}$ are used to account for the self-capacitance of the primary and secondary windings and the mutual capacitance between the primary and secondary windings, respectively.

The leakage inductances in a high frequency transformer are small compared to the magnetizing inductance in general. For example, a 400 kHz, 500 W planar PCB transformer with 10 kV voltage isolation ($N_P$=8, $N_S$=32) has leakage inductances of 25.77 $\mu$H for primary winding and 15.77 $\mu$H for secondary winding (referred to the primary side) while the magnetizing inductance is about 1.5 mH. The voltage drop across the leakage inductances is insignificant, and hence the effect of $C_{PS}$ is insignificant [117].

For a high frequency transformer, shields enclosing the windings are generally applied to limit common-mode currents and reduce electromagnetic noise. For the high voltage, high frequency planar PCB transformer, each winding is enclosed by a copper foil. In addition, the separation between primary and secondary windings is over 2 cm in order to provide high voltage isolation, as illustrated in Fig. 3.19. The dielectric effect of the shields plus the large separation of the windings significantly reduce the mutual capacitance between primary and secondary windings.

Based on the above analysis, the equivalent circuit model for a high frequency transformer shown in Fig. 3.17 can be simplified as the equivalent circuit model shown in Fig. 3.18, where the mutual capacitance between primary and secondary is ignored.

### 3.5.2 Measurements of the Parameters

The measurements of the transformer model parameters has two parts: one is the magnetizing inductance, leakage inductance and winding resistances, which does not require energizing of the transformer; the other one is the parasitic capacitances.
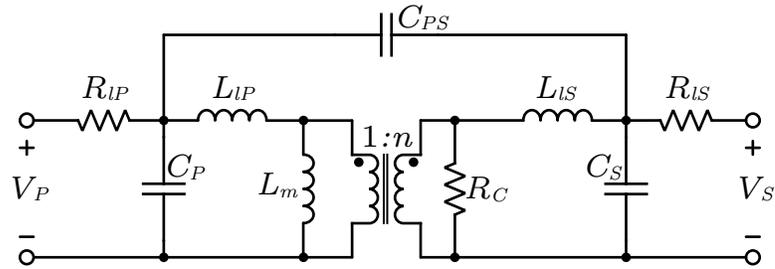
Fig. 3.17: Equivalent circuit model of a two-winding high voltage transformer with parasitic components included.
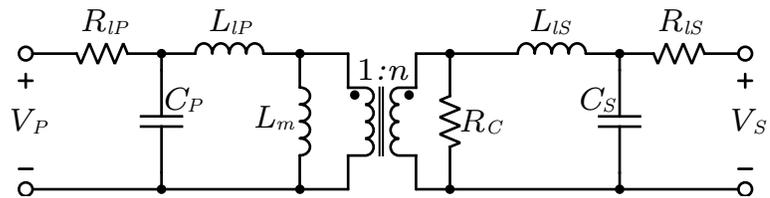


Fig. 3.18: Simplified equivalent circuit model of a two-winding high voltage transformer.
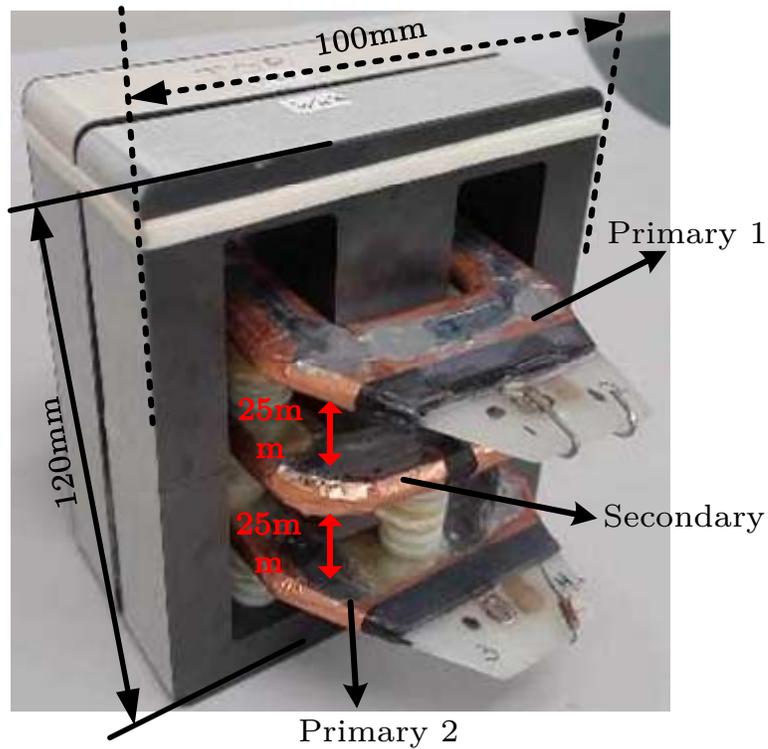


Fig. 3.19: Photo of the PCB based 13 kV isolation transformer.

For measuring the magnetizing inductance, leakage inductance and winding resistances, since the transformer is not energized during the measurements, the parasitic capacitances and equivalent core loss resistance in Fig. 3.18 can be removed and the equivalent circuit becomes the one shown in Fig. 3.20. The magnetizing inductance and leakage inductances can be calculated from a set of open circuit and short circuit measurements by using an RLC meter at operating frequency, while the winding resistance can be measured directly from a multi-meter.

In Fig. 3.20, the measured inductance on the primary side, with secondary side open circuit is

$$L_{P\_O} = L_{lP} + L_m, \tag{3.101}$$

and the measured inductance on the secondary side, with primary side open circuit is

$$L_{S\_O} = L_{lS} + n^2 L_m, \tag{3.102}$$

while the measured inductance on secondary side with primary side short circuit is

$$L_{S\_S} = L_{lS} + n^2 (L_{lP} \parallel L_m). \tag{3.103}$$

In (3.103), since $L_m$ is much larger than $L_{lP}$, (3.103) can be simplified as

$$L_{S\_S} = L_{lS} + n^2 L_{lP}. \tag{3.104}$$

From (3.101), (3.102) and (3.104), the magnetizing inductance and leakage inductances can be calculated by using the equations

$$L_{lP} = \frac{n^2 L_{P\_O} - L_{S\_O} + L_{S\_S}}{2n^2}, \tag{3.105}$$

$$L_{lS} = \frac{L_{S\_O} + L_{S\_S} - n^2 L_{P\_O}}{2}, \tag{3.106}$$
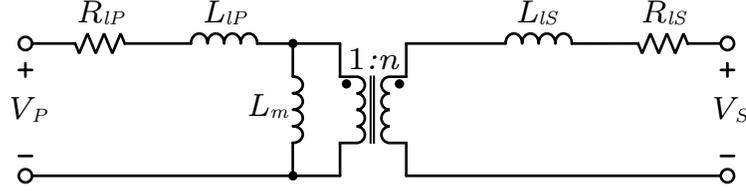
Fig. 3.20: Equivalent circuit model for static measurement of a two-winding transformer.

$$L_m = \frac{n^2 L_{P\_O} - L_{S\_S} + L_{S\_S}}{2n^2}. \tag{3.107}$$

For the equivalent circuit model shown in Fig. 3.18, if the transformer is excited from the primary side by a square wave voltage with the secondary side open circuit, all the components can be referred to secondary side as illustrated in Fig. 3.21, where $nV_P$ is the excitation voltage referred to the secondary side, $V_{S_O}$ is the open circuit voltage measured on the secondary side. At this point, since the resistive components do not change the resonant frequency in a RLC circuit, the resistive components are not included.

The transformer is excited by a square wave voltage $V_P$ and the secondary side open circuit voltage $V_{S_O}$, voltage across the secondary parasitic capacitor $C_S$, is measured, as shown in Fig. 3.21. Since the equivalent circuit shown in Fig. 3.21 is an RLC circuit, the measured $V_{S_O}$ has a resonant behavior caused by the leakage inductances (referred to the secondary side) and the secondary side parasitic capacitance, as illustrated in Fig. 3.22. By measuring the resonant period of $V_{S_O}$, the secondary side parasitic capacitance can be calculated through

$$C_S = \frac{1}{(2\pi/T)^2 (n^2 L_{lP} + LlS)}, \tag{3.108}$$

where $T$ is the measured resonant period as shown in Fig. 3.22, $L_{lP}$ and $L_{lS}$ are the measured leakage inductances calculated from (3.105) and (3.106).

The determination technique for the primary side parasitic capacitance $C_P$ is similar, the details and analysis of which is not presented. The measured and experimentally determined parasitic parameters of the high voltage transformer are tabulated in TABLE 3.3.
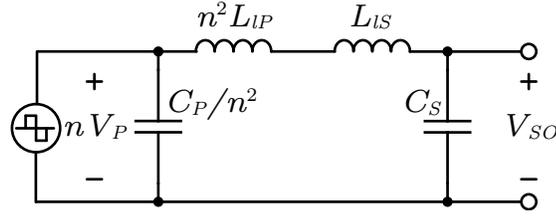
Fig. 3.21: Equivalent circuit model for determination of secondary side parasitic capacitance.
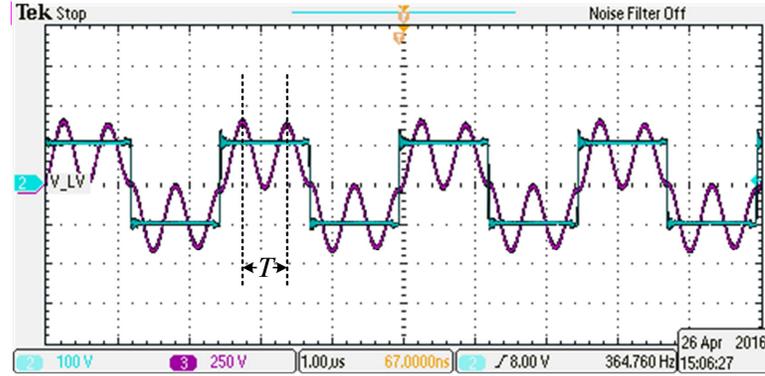


Fig. 3.22: Excitation voltage on primary side and measured secondary side open circuit voltage. Light blue (CH2): primary voltage; Purple (CH3): secondary voltage.

Table 3.3: DETERMINED PARASITICS
OF THE TRANSFORMER

| Parasitic Parameters | Value |
|:---:|:---:|
| $R_{lP}(\Omega)$ | 0.62 |
| $R_{lS}(\Omega)$ | 3.34 |
| $L_{lP}(\mu\mathrm{H})$ | 25.8 |
| $L_{lS}(\mu\mathrm{H})$ | 63.2 |
| $L_m(\mathrm{mH})$ | 1.5 |
| $C_S(\mathrm{pF})$ | 59.4 |
| $C_P(\mathrm{pF})$ | 36.5 |

## 3.6 Design Optimization of the SRC

The design procedure of an output current regulated SRC with constant current input presented in Section 3.4. However, the design was not fully optimized to account for the parasitics associated with the high voltage isolation transformer modeled in Section 3.5. This section develops a new design optimization procedure to account for transformer para-

sitics in the design of SRCs used in dc current distribution systems. The design optimization guarantees that the steady state solution of the output current regulated SRC with constant input current exists for the entire expected load range, maintains the minimum circulating current in the resonant tank across the entire load range without active control techniques, and provides help in meeting ZVS requirements and reduces component stresses.

As presented in Section 3.4.2, the output current regulated SRC with constant current input is designed to operate at normalized switching frequency $F$ equals to 1 in order to obtain a natural current source behavior. The resonant tank quality factor $Q$ is determined by load. Hence, the only parameter left for design optimization is the switching frequency. For an SRC, with the transformer being a part of the tank network, the equivalent circuit seen by the primary-side H-bridge is shown in Fig. 3.23. In Fig. 3.23, $Z_{in}$ is the input impedance of the modified tank network, $L_r$ is the resonant inductor, $C_r$ is the resonant capacitor, $R_e$ is the ac equivalent load resistance reflected to transformer primary side, and other components are the transformer parasitics reflected to primary side. From Fig. 3.23, it can be noticed that the original resonant inductance is increased due to the presence of $L_{lP}$ and $L_{lS}$, which can be easily accommodated by changing $L_r$. Based on Fig. 3.23, $Z_{in}$ can be expressed as,

$$Z_{in} = sL_r + \frac{1}{sC_r} + \frac{1}{sC_p} \parallel (sL_{lP} + sL_m \parallel (sL_{lS} + R_e \parallel \frac{1}{sC_s})), \qquad (3.109)$$

where, $x \parallel y$ denotes parallel combination of impedances $x$ and $y$.

For the analysis, a SRC design is taken as an example. The SRC has a load range of 50 W to 500 W with 0.33 A output current. The SRC is designed to operate at resonance with a minimum quality factor $Q$ of 1.2. The desired switching frequency range for the SRC is 100 kHz to 500 kHz with EMI and other considerations. With the knowledge of switching frequency (resonant frequency), desired load range and minimum quality factor, the resonant inductance and resonant capacitance can be calculated for each switching frequency.

Substituting the $L_r$ and $C_r$ values into (3.109), the phase angle of $Z_{in}$ ($\varphi_{Z_{in}}$) for each
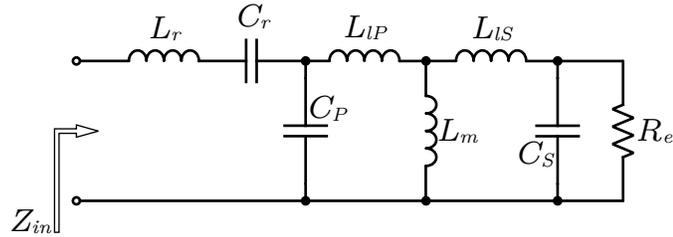
Fig. 3.23: Equivalent impedance network seen by the primary H-bridge.
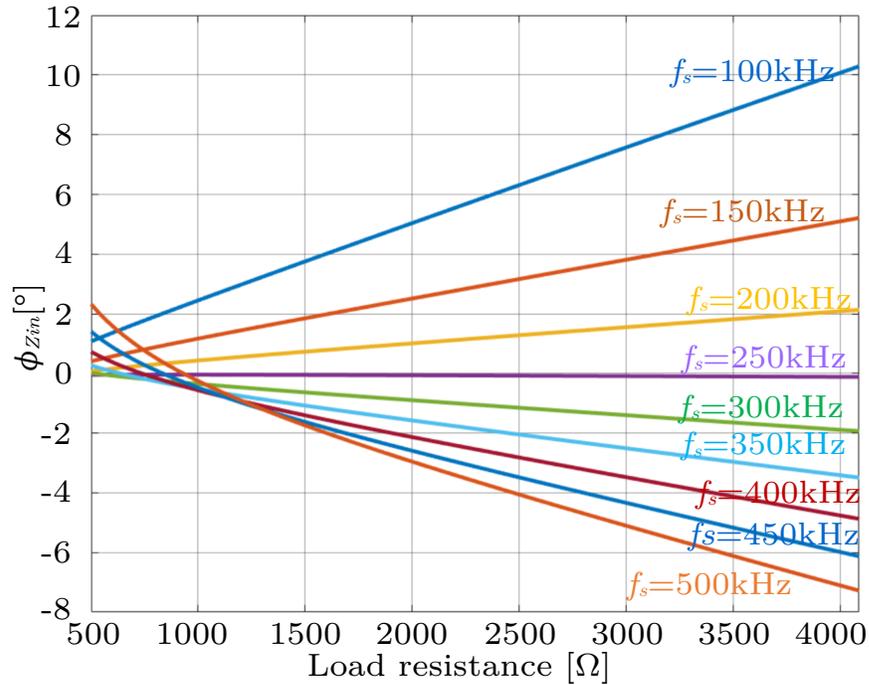


Fig. 3.24: Phase angle of $Z_{in}$ ($\varphi_{Z_{in}}$) vs $R_{load}$ at different $f_s$.

load resistance can be derived. By sweeping the switching frequency, a set of $\varphi_{Z_{in}}$ versus load resistance curves can be obtained, as shown in Fig. 3.24. It can be observed here that tank current lags tank input voltage at low $f_s$ and leads at high $f_s$. In Fig. 3.25, a plot is shown for the summed power factor across the load range, for different $f_s$. From Fig. 3.24 and Fig. 3.25, it can be seen that 250 kHz is the optimum choice of the switching frequency for the given transformer, since $\varphi_{Z_{in}}$ is about 0° for the entire load range with negligible variation.
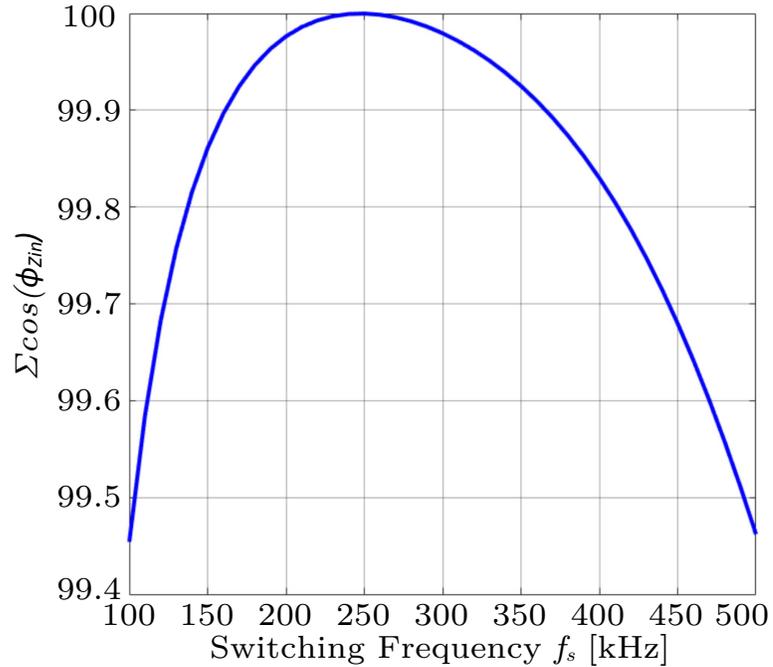
Fig. 3.25: Summation of power factor across load variation vs $f_s$.

## 3.7  Design Examples

### 3.7.1  Design with Non-Zero Minimum Output Power

Design for a 400 kHz, 450 W SRC with 1 A constant input current, 330 mA regulated output current and 600 V resonant capacitor peak voltage based on the above analysis, is presented as an example.

For this design, the current gain $m$ is 1/3, so the minimum transformer turns ratio is 1 : 1.5 according to (3.94). The transformer turns ratio is selected to be 1 : 2 considering the design margin and lower component stresses and losses.

As shown in Fig. 3.16, by applying the constraints from (3.89), (3.76) and (3.92), the designed operating point should be the red cross point while the variation of the resonant components is not considered, which has $F = 1.04$ and $Q_{max} = 13$. However, the variation of the resonant components has to be considered based on the above analysis. In this

design scenario, $\pm 5\%$ variation of the resonant components is considered. As illustrated in Fig. 3.16, the green plus sign marks the designed operating point, while the red solid rectangular area shows the possible operating region. From Fig. 3.16, it can be seen that the whole possible operating region (green solid rectangular area) satisfies the constraints derived from earlier analysis, which means that the proposed design can tolerate $\pm 5\%$ variation of the resonant components.

The designed operating point has $Q_{max} = 11$ and $F = 1.02$, which means that the resonant frequency is 392 kHz with 400 kHz switching frequency. The desired load range for the SRC is 450 W to 50 W. Since the output current is regulated, the $Q$ is minimum at full load and maximum at minimum load, which means that $Q = 11$ for minimum load and $Q = 1.2$ for full load.

The values of the resonant inductor and capacitor can be calculated from the designed $Q$, $F$ and the load resistance for the minimum load according to (3.16),(3.17) and (3.18), which are tabulated in TABLE 3.4 along with other parameters for this design example. In practice, the actual resonant frequency may deviate from the designed value because the values of the components may not be exactly the same as the designed values. Thus manual or automated tuning of the switching frequency may be needed in order to obtain the designed normalized switching frequency $F$.

### 3.7.2 Current Source Behavior Design

Design of a 1 kW SRC with 1 A constant input current, 330 mA regulated output current and 400 V resonant capacitor rms voltage is presented as an example to demonstrate the analysis and design procedure developed in this chapter. For this design, the current gain $m$ is 1/3, so the minimum transformer turns ratio is 1 : 1.5 according to (3.96). The transformer turns ratio is selected to be 1 : 2 considering the design margin and lower component stresses and losses.

From (3.99), it can be seen that the resonant inductor rms current is a function of output current and transformer turns ratio $n$, which is 1.47 A according to (3.99) and the designed transformer turns ratio $n$. From (3.100), it can be seen that the resonant capacitor

Table 3.4: PARAMETERS OF THE DESIGN EXAMPLE

| | |
|---|---|
| **Input current [A]** | 1 |
| **Output current [mA]** | 330 |
| **Load range [W]** | 450 - 50 |
| **Switching frequency [kHz]** | 400 |
| **Transformer turns ratio** | 1 : 2 |
| **Normalized switching frequency $F$** | 1.02 |
| $Q$ | 1.2 - 11 |
| **Resonant inductor [$\mu$H]** | 102 |
| **Resonant capacitor [nF]** | 1.6 |
| **MOSFETS (SiC)** | C2M1000170D |
| **Gate driver** | IXDN609YI |

rms voltage is determined by the transformer turns ratio $n$, the resonant tank characteristic impedance $Z_o$ and output current $I_{out}$. For this design, based on the desired voltage stress on the resonant capacitor, the designed transformer turns ratio n, the desired output current and (3.100), the characteristic impedance $Z_o$ of the resonant tank then can be calculated. According to the analysis presented in Section 3.6, the switching frequency is selected to be 250 kHz. The designed operating point has $Q_{min} = 0.6$ and $F = 1$, which means that the resonant frequency equals to the switching frequency 250 kHz. The desired load range for the SRC is 0 W to 1 kW. Since the output current is regulated, the $Q$ is minimum at full load, which means that $Q = 0.6$ for full load.

The values of the resonant inductor and capacitor can be calculated from the designed $Q$, $F$ and the load resistance for the maximum load according to (3.16),(3.17) and (3.18), which are tabulated in TABLE 3.5 along with other parameters for this design example. In practice, the actual resonant frequency may deviate from the designed value. From Fig. 3.15, it can be seen that the current gain is minimum when the switching frequency is equal to the resonant frequency, thus tuning of the switching frequency can be applied based on this fact to obtain a current source behavior. Tuning can be applied manually or adaptively using techniques such as an adaptive step-size controller [118].

Table 3.5: PARAMETERS OF THE CURRENT SOURCE
BEHAVIOR DESIGN EXAMPLE

| | |
|---|---|
| **Input current [A]** | 1 |
| **Output current [mA]** | 330 |
| **Load range [W]** | 1000 - 0 |
| **Switching frequency [kHz]** | 250 |
| **Transformer turns ratio** | 1 : 2 |
| **Normalized switching frequency $F$** | 1 |
| $\boldsymbol{Q_{min}}$ | 0.6 |
| **Resonant inductor [$\mu$H]** | 174 |
| **Resonant capacitor [nF]** | 2.33 |
| **MOSFETS (SiC)** | C2M1000170D |
| **Gate drive** | +18V/-5V pulses with 100 ns dead-band |
| **Gate driver** | IXDN609YI |

## 3.8   Summary

This chapter studies the steady-state operations of resonant converters with constant dc input voltage instead of conventional constant dc input voltage, and develops design procedures for the design of SRCs with constant dc input current. Based on the steady state operation analysis of the resonant converters, this work found that all four commonly used resonant converters, SRC, PRC, LCL resonant converter and DABSRC, when used with a constant input current, behave differently in comparison to the case with constant input voltage. From the comparison, the SRC is selected as the converter topology for the dc current to current converter used in a dc current distribution system because of the natural current source behavior at its output while operating at resonance along with other benefits. For the SRC with constant dc input current, the component stress, loss distribution and output characteristics are analyzed in detail for developing the proposed design considerations and procedures. A design optimization is presented to eliminate the parasitics of the high-voltage transformer by optimizing the switching frequency. Two design examples, one with non-zero minimum output power and the other one with current source behavior, are given to demonstrate the presented analysis and design procedures.

CHAPTER 4

SMALL SIGNAL ANALYSIS OF THE SERIES RESONANT CONVERTER WITH

CONSTANT DC INPUT CURRENT

As regulated output is required for most of applications, the control-to-output transfer function is needed to design the feedback loop. For applications that involve multiple SRCs, such as dc voltage distribution and dc current distribution, input impedance is required to evaluate system stability. For either of these purposes, small-signal modeling is indispensable.

The small signal model for an SRC aims to generate transfer functions for the average output current and independent input (voltage or current) as functions of the control angle and dependent input (current or voltage). This chapter develops and validates small signal models using dynamic phasor modeling techniques for phase-shift modulated SRCs with constant input current and derives explicit analytical expressions for all key transfer functions, including input impedance and control-to-output. The small signal models and transfer functions are suitable for feedback loop design, system stability evaluation and related design oriented analysis. Section 4.1 derives the phasor transformed equivalent circuit of SRC with constant current input using the phasor transformation technique presented in Section 2.3.2. The small signal expression of the resonant tank current is derived in Section 4.2 based on the simplified phasor transformed equivalent circuit. In Section 4.3, the key transfer functions of the SRC with constant input voltage are derived. Based on the small signal model of the SRC with constant input voltage, Section 4.4 presents the small signal input voltage and small signal output current for the SRC with constant current input. The chapter summary is given in Section 4.5.

## 4.1 Derivation of the Phasor Transformer Model

In Section 2.3.2, the phasor models of the basic circuit elements, including resistor,

inductor, capacitor, H-bridge and diode voltage doubler, are presented in Fig. 2.11. For the purpose of deriving explicit expressions for all transfer functions, the phasor domain model of the series resonant tank, which is an inductor in series with a capacitor, is still too complex to utilize, as shown in Fig. 4.1(b). When the switching frequency is within a narrow range around the resonant frequency, the series resonant tank is a second order model, while it is a first order model when the switching frequency is beyond that range [75], as illustrated in Fig. 4.1(c). For the two scenarios where the resonant tank is represented as a first order model and a second order model, the small signal derivation process is similar. Since the SRC design in this work operates at resonance, which means that the resonant tank can be simplified as an inductor in the phasor domain as shown in Fig. 4.1(c), derivation and analysis for the series resonant tank represented as a second order model is presented in this chapter.

For the SRC topology illustrated in Fig. 3.1, the phasor transformed equivalent circuit can be derived based on the phasor models for basic elements in the circuit presented in Fig. 2.11. The derived phasor transformed equivalent circuit of the SRC with constant input current is illustrated in Fig. 4.2.

In Fig. 4.2, $I_g$ is the constant input current, $C_{in}$ is the input capacitor, $C_o$ is the equivalent output capacitor which is $C_{out}$ in parallel with the series connection of $C_1$ and $C_2$ in Fig. 3.1, $R_{load}$ is the load resistance, $\vec{s}_P$ is the primary phasor transformer, $2sL$ is the model for the resonant tank, and $\vec{s}_S$ is the secondary phasor transformer combined with the physical power transformer. From Fig. 4.2, it can be seen that in the equivalent circuit, the dc quantities are represented in their original format, the ac quantities are represented in phasor format, and the phasor transformer realizes the conversion between them.

As shown in Fig. 2.11 and Fig. 4.2, the primary phasor transformer $\vec{s}_P$ is

$$\vec{s}_P = \frac{2\sqrt{2}}{\pi} sin(\frac{\alpha}{2}), \tag{4.1}$$
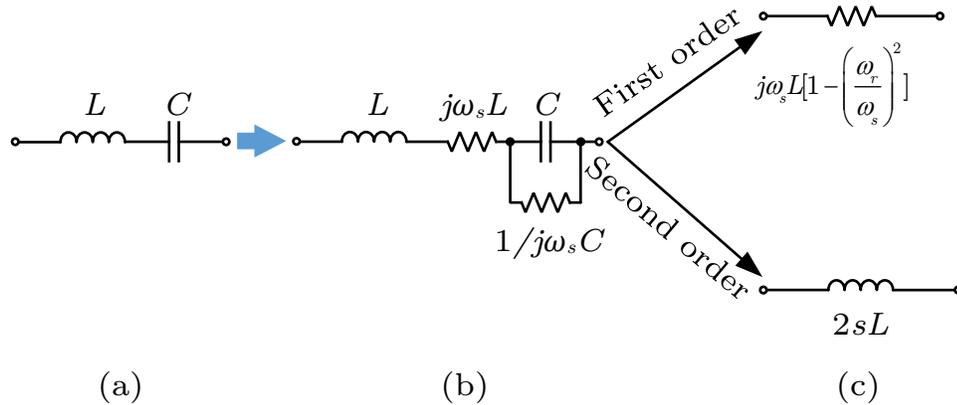
Fig. 4.1: Simplified phasor models for the series resonant tank.
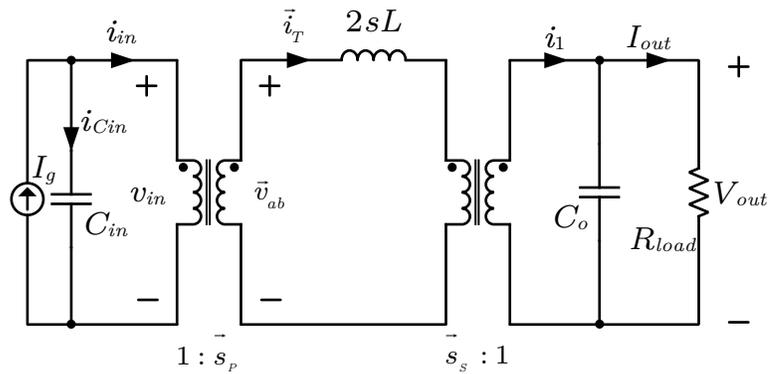


Fig. 4.2: Second order phasor transformed equivalent circuit of the SRC with constant current input.

where $\alpha$ is the phase shift between the primary H-bridge legs. The secondary phasor transformer $\vec{s}_S$ is

$$\vec{s}_S = \frac{\sqrt{2}}{n\pi}e^{-j\theta}, \tag{4.2}$$

where $n$ is the power transformer turns ratio, and $\theta$ is the phase shift between the secondary voltage and current.

## 4.2 Small Signal Tank Current

As the first step, or for an SRC with constant input voltage, the input voltage is assumed to be an independent input variable to the converter. Applying the primary phasor

transformer shown in (4.1), the primary H-bridge output voltage in the phasor domain is

$$\vec{v}_{ab} = V_{in}\vec{s}_P = V_{in}\frac{2\sqrt{2}}{\pi}sin(\frac{\alpha}{2}). \tag{4.3}$$

Taking the partial derivative of (4.3) with respect to $\alpha$ and $V_{in}$, the small signal response of $\vec{v}_{ab}$ with respect to perturbations in $\alpha$ and $v_{in}$ can be expressed as

$$\hat{\vec{v}}_{ab} = \frac{2\sqrt{2}}{\pi}sin(\frac{\alpha}{2})\hat{v}_{in} + V_{in}\frac{\sqrt{2}}{\pi}\cos(\frac{\alpha}{2})\hat{\alpha}. \tag{4.4}$$

Hence, the small signal equivalent circuit seen from the output of the primary H-bridge can be derived as shown in Fig.4.3.

Since the secondary side is a diode rectifier doubler as shown in Fig. 3.1, the angle $\theta$ in the phasor equation (4.2) is zero, which means the phasor is real instead of complex as shown in (4.5). With a real phasor transformer, the components and variables on one side can be reflected to the other side, which is similar with a normal transformer. By reflecting the equivalent output capacitor $C_o$ and load resistor $R_{load}$ to the primary side of phasor transformer $\vec{s}_S$ using (4.5), the equivalent small signal circuit can be derived as illustrated in Fig. 4.4.

$$\vec{s}_S = \frac{\sqrt{2}}{n\pi}. \tag{4.5}$$

From Fig. 4.4, by applying (4.4), the small signal expression for the envelope of the resonant current $\hat{\vec{i}}_T$ can be derived as

$$\hat{\vec{i}}_T = \frac{n\pi}{\sqrt{2}}\frac{1 + sR_{load}C_o}{R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o}(2\sin(\frac{\alpha}{2})\hat{v}_{in} + nV_{in}\cos(\frac{\alpha}{2})\hat{\alpha}). \tag{4.6}$$

## 4.3   Small Signal Model Derivation of SRC with Constant Input Voltage

For the small signal modeling of SRC with constant input voltage, the small signal input voltage $\hat{v}_{in}$ and the small signal phase shift angle input $\hat{\alpha}$ are the two independent inputs, while the input current $\hat{i}_{in}$ and output current $\hat{i}_{out}$ are the two small signal responses.
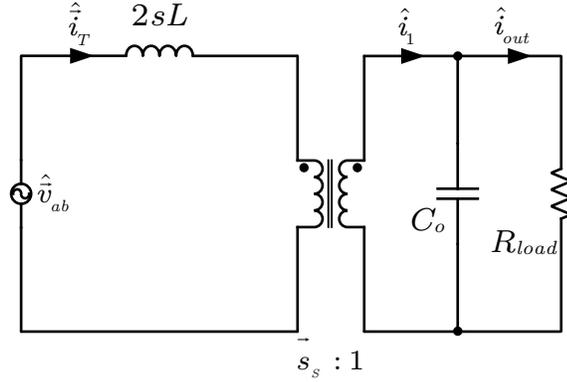
Fig. 4.3: Small signal equivalent circuit of an SRC with constant current input seen from the primary H-bridge output in phasor domain.
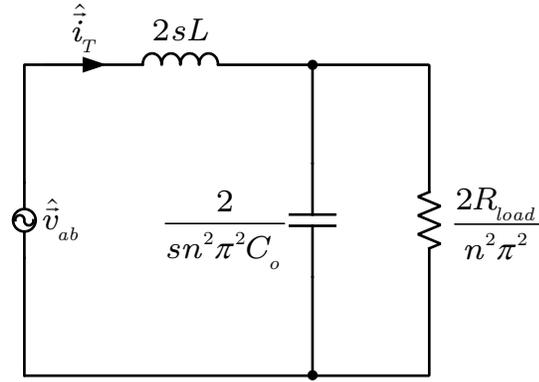


Fig. 4.4: Small signal equivalent circuit of an SRC tank current in phasor domain.

### 4.3.1 Small Signal Input Current

According to phasor transformer $\vec{s}_P$, the average input current can be expressed as

$$I_{in} = Re[\vec{i}_T \cdot \vec{s}_P] = \vec{i}_T \frac{2\sqrt{2}}{\pi} \sin(\frac{\alpha}{2}). \tag{4.7}$$

By taking the partial derivative of (4.7) with respect to $\alpha$ and $\vec{i}_T$, the small signal response of input current with respect to the perturbations in $\alpha$ and $\vec{i}_T$ can be derived as

$$\hat{i}_{in} = \frac{2\sqrt{2}}{\pi} \sin(\frac{\alpha}{2})\hat{\vec{i}}_T + \vec{i}_T \frac{\sqrt{2}}{\pi} \cos(\frac{\alpha}{2})\hat{\alpha}. \tag{4.8}$$

From Fig. 4.2, the steady state phasor $\vec{i}_T$ can be derived as

$$\vec{i}_T = \frac{I_{out}}{\vec{s}_S} = \frac{n\pi I_{out}}{\sqrt{2}}.$$ 

(4.9)

Substituting (4.6) and (4.9) into (4.8), the small signal response of input current can be expressed as

$$\hat{i}_{in} = 2n\sin(\frac{\alpha}{2})(2n\sin(\frac{\alpha}{2})\hat{v}_{in} + nV_{in}\cos(\frac{\alpha}{2})\hat{\alpha})G_o + nI_{out}\cos(\frac{\alpha}{2})\hat{\alpha},$$ 

(4.10)

where

$$G_o = \frac{1 + sR_{load}C_o}{R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o}.$$ 

(4.11)

From (4.10), the transfer function from the phase shift control input to the input current of the conventional SRC with constant input voltage is

$$G_{i_{in}-\alpha} = \frac{\hat{i}_{in}}{\hat{\alpha}} = \frac{2n^2 V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})(1 + sR_{load}C_o)}{R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o} + nI_{out}\cos(\frac{\alpha}{2}),$$ 

(4.12)

and the input admittance is

$$Y_{in} = \frac{\hat{i}_{in}}{\hat{v}_{in}} = \frac{4n^2\sin^2(\frac{\alpha}{2})(1 + sR_{load}C_o)}{R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o}.$$ 

(4.13)

### 4.3.2   Small Signal Output Current

From Fig. 4.3, the small signal current $\hat{i}_1$ can be expressed as

$$\hat{i}_1 = \hat{\vec{i}}_T \vec{s}_S.$$ 

(4.14)

The small signal output current $\hat{i}_{out}$ can be expressed in terms of $\hat{i}_1$ as

$$\hat{i}_{out} = (1 + sR_{load}C_o)\hat{i}_1.$$ 

(4.15)

Substituting (4.6) and (4.14) into (4.15), the small signal output current of the SRC with constant input voltage can be derived as

$$\hat{i}_{out} = \frac{2\sin(\frac{\alpha}{2})\hat{v}_{in} + nV_{in}\cos(\frac{\alpha}{2})\hat{\alpha}}{R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o}. \tag{4.16}$$

From (4.16), the transfer function from the phase shift control input to the output current of the conventional SRC with constant input voltage is

$$G_{i_{out}\_\alpha} = \frac{\hat{i}_{out}}{\hat{\alpha}} = \frac{nV_{in}\cos(\frac{\alpha}{2})}{R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o}, \tag{4.17}$$

and the transfer function from the input voltage to the output current of the conventional SRC with constant input voltage is

$$G_{i_{out}\_v_{in}} = \frac{\hat{i}_{out}}{\hat{v}_{in}} = \frac{2\sin(\frac{\alpha}{2})}{R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o}. \tag{4.18}$$

### 4.4   Small Signal Model Derivation of the SRC with Constant Input Current

For the SRC with constant input current, however, the challenge is that the small signal input voltage $\hat{v}_{in}$ becomes a variable which depends on $\hat{\alpha}$ and $\hat{i}_g$ , instead of an independent input. The two independent inputs are the small signal input current $\hat{i}_g$ and the small signal phase shift angle input $\hat{\alpha}$, and the two small signal output responses are the input voltage $\hat{v}_{in}$ and output current $\hat{i}_{out}$.

#### 4.4.1   Small Signal Input Voltage

According to Fig. 4.2, the relation between $\hat{v}_{in}$ and $\hat{i}_{in}$ is expressed as

$$\hat{v}_{in} = \frac{1}{sC_{in}}(\hat{i}_g - \hat{i}_{in}). \tag{4.19}$$

Substituting (4.10) into (4.19), the small signal input voltage of the SRC with constant input current can be expressed as

$$\hat{v}_{in} = \frac{1}{sC_{in}}\{\hat{i}_g - 2n\sin(\frac{\alpha}{2})[2n\sin(\frac{\alpha}{2})\hat{v}_{in} + nV_{in}\cos(\frac{\alpha}{2})\hat{\alpha}]$$
$$\frac{1 + sR_{load}C_o}{R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o} + nI_{out}\cos(\frac{\alpha}{2})\hat{\alpha}\}, \quad (4.20)$$

which can be rewritten as

$$\hat{v}_{in} = \frac{1}{sC_{in}}\{\hat{i}_g - 2n\sin(\frac{\alpha}{2})[2n\sin(\frac{\alpha}{2})\hat{v}_{in} + nV_{in}\cos(\frac{\alpha}{2})\hat{\alpha}]\frac{N}{D} + nI_{out}\cos(\frac{\alpha}{2})\hat{\alpha}\}, \quad (4.21)$$

where, $N$ and $D$ are defined as

$$N = 1 + sR_{load}C_o, \quad (4.22)$$

$$D = R_{load} + n^2\pi^2 sL + n^2\pi^2 s^2 R_{load}LC_o. \quad (4.23)$$

The small signal input voltage equation (4.21) can be simplified as

$$\hat{v}_{in} = \frac{1}{sC_{in}}\hat{i}_g - \frac{1}{sC_{in}}\frac{N}{D}4n^2\sin^2(\frac{\alpha}{2})\hat{v}_{in} - \frac{1}{sC_{in}}2n^2 V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})\frac{N}{D}\hat{\alpha}$$
$$- \frac{1}{sC_{in}}nI_{out}\cos(\frac{\alpha}{2})\hat{\alpha}, \quad (4.24)$$

$$[1 + \frac{1}{sC_{in}}\frac{N}{D}4n^2\sin^2(\frac{\alpha}{2})]\hat{v}_{in} = \frac{1}{sC_{in}}\hat{i}_g - \frac{2n^2 V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})N + nI_{out}\cos(\frac{\alpha}{2})D}{sC_{in}D}\hat{\alpha}, \quad (4.25)$$

$$\frac{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}{sC_{in}D}\hat{v}_{in} = \frac{1}{sC_{in}}\hat{i}_g - \frac{2n^2 V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})N + nI_{out}\cos(\frac{\alpha}{2})D}{sC_{in}D}\hat{\alpha}, \quad (4.26)$$

$$\hat{v}_{in} = \frac{D}{sC_{in}D + 4n^2\sin^2(\frac{\alpha}{2})N}\hat{i}_g - \frac{2n^2V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})N + nI_{out}\cos(\frac{\alpha}{2})D}{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}\hat{\alpha}. \qquad (4.27)$$

Equation (4.27) is the explicit expression of the small signal input voltage for the SRC with constant input current in terms of the small signal input current and small signal phase shift control input.

From (4.27), the transfer function from the phase shift control input to the input voltage is

$$G_{v_{in}\_\alpha} = \frac{\hat{v}_{in}}{\hat{\alpha}} = -\frac{2n^2V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})N + nI_{out}\cos(\frac{\alpha}{2})D}{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}, \qquad (4.28)$$

and the input impedance is

$$Z_{in} = \frac{\hat{v}_{in}}{\hat{i}_g} = \frac{D}{sC_{in}D + 4n^2\sin^2(\frac{\alpha}{2})N}. \qquad (4.29)$$

From (5.36), it can be seen that the gain from phase shift angle $\hat{\alpha}$ to the input voltage $v_{in}$ is negative, which means that the increasing of phase shift angle $\alpha$ results in the decreasing of input voltage $V_{in}$. The input impedance expression (4.29) is the open loop input impedance of the SRC with constant dc input current, which can be used to evaluate the stability of the dc current distribution system.

### 4.4.2   Small Signal Output Current

With the expression of the small signal input voltage for the SRC with constant input current derived above, the small signal tank current can be derived as below by substituting (4.27) into (4.6).

$$\hat{i}_T = \frac{2n\pi\sin(\frac{\alpha}{2})}{\sqrt{2}}\frac{N}{D}\{\frac{D}{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}\hat{i}_g - \frac{2n^2V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})N + nI_{out}\cos(\frac{\alpha}{2})D}{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}\hat{\alpha}\}$$
$$+ \frac{n^2\pi V_{in}}{\sqrt{2}}\frac{N}{D}\cos(\frac{\alpha}{2})\hat{\alpha}. \quad (4.30)$$

$$\hat{\tilde{i}}_T = \frac{\sqrt{2}n\pi\sin(\frac{\alpha}{2})N}{sC_{in}D + 4n^2\sin^2(\frac{\alpha}{2})N}\hat{i}_g +$$
$$\{\frac{n^2\pi V_{in}N\cos(\frac{\alpha}{2})}{\sqrt{2}D} - \frac{\sqrt{2}n\pi\sin(\frac{\alpha}{2})N(2n^2V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})N + nI_{out}\cos(\frac{\alpha}{2})D)}{D(sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2}))}\}\hat{\alpha}. \quad (4.31)$$

For the small signal output current $\hat{i}_{out}$ of the SRC with constant input current, the expression can be derived by substituting (4.27) into (4.16) as

$$\hat{i}_{out} = \frac{1}{D}\{2\sin(\frac{\alpha}{2})[\frac{D}{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}\hat{i}_g - \frac{2n^2V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})N + nI_{out}\cos(\frac{\alpha}{2})D}{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}\hat{\alpha}]$$
$$+ nV_{in}\cos(\frac{\alpha}{2})\hat{\alpha}\}, \quad (4.32)$$

$$\hat{i}_{out} = \frac{1}{D}\frac{2\sin(\frac{\alpha}{2})D}{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}\hat{i}_g$$
$$- \frac{2n\sin(\frac{\alpha}{2})}{D}\frac{2n^2V_{in}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})N + nI_{out}\cos(\frac{\alpha}{2})D}{sC_{in}D + N4n^2\sin^2(\frac{\alpha}{2})}\hat{\alpha} + \frac{nV_{in}\cos(\frac{\alpha}{2})}{D}\hat{\alpha}, \quad (4.33)$$

By simplifying (4.33), the explicit expression for the small signal output current $\hat{i}_{out}$ of the SRC with constant input current can be given as

$$\hat{i}_{out} = \frac{2n\sin(\frac{\alpha}{2})}{sC_{in}D + 4n^2\sin^2(\frac{\alpha}{2})N}\hat{i}_g + \frac{nV_{in}\cos(\frac{\alpha}{2})sC_{in} - 2n^2I_{out}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})}{sC_{in}D + 4n^2\sin^2(\frac{\alpha}{2})N}\hat{\alpha}. \quad (4.34)$$

From (4.34), the transfer function from the phase shift control input to the output current is

$$G_{i_{out\_\alpha}} = \frac{\hat{i}_{out}}{\hat{\alpha}} = \frac{nV_{in}\cos(\frac{\alpha}{2})sC_{in} - 2n^2I_{out}\sin(\frac{\alpha}{2})\cos(\frac{\alpha}{2})}{sC_{in}D + 4n^2\sin^2(\frac{\alpha}{2})N}, \quad (4.35)$$

and the transfer function from input current to the output current is

$$G_{i_{out\_i_{in}}} = \frac{\hat{i}_{out}}{\hat{i}_{in}} = \frac{2n\sin(\frac{\alpha}{2})}{sC_{in}D + 4n^2\sin^2(\frac{\alpha}{2})N}. \quad (4.36)$$

From (4.35), it can be seen that the gain from phase shift angle $\hat{\alpha}$ to the output current $\hat{i}_{out}$ is negative, which means that the increasing of phase shift angle $\alpha$ results in the decreasing of output current $i_{out}$.

## 4.5   Summary

This chapter derives the small signal models and explicit analytical expressions for all transfer functions of an SRC with both constant input voltage and constant input current to help researchers and engineers to implement the feedback loop design and stability evaluation. This chapter also solves challenges in both the steady state operation and small signal analysis of the SRC with constant input current introduced by the variable input voltage. The models allow both steady state and small signal quantities to be derived without undue complexity.

CHAPTER 5

STABILITY ANALYSIS OF DC CURRENT DISTRIBUTION SYSTEMS

The integrated dc distribution system may become unstable even if the converters are stable individually. There are two main causes of stability degradation for a dc power distribution system: 1) interactions of the feedback loop created by the input/output impedances of the interconnected converters and 2) the constant power load effects that exhibit negative incremental impedance [80]. Hence, it is necessary to evaluate the stability of a dc power distribution system during the analysis and design process to guarantee a stable system behavior.

In this chapter, the stability analysis of dc current distribution systems is presented with the considerations of the two main causes of stability degradation and the cable impedance in the system. The stability analysis criterion of a constant current cascaded system and the general control strategy are developed in Section 5.1. The impedance model of a long distance cable is derived in Section 5.2 by taking the submarine cable as an example. The relation between closed-loop and open-loop input impedance of power converters is found in Section 5.3, where the SRC with constant input current is taken as an example. Based on the developed cable impedance model and closed-loop input impedance of the converter, the stability of a dc current distribution system consists of one cable and one converter is analyzed in Section 5.4, while the stability of a dc current distribution system consists of multi-cables and multi-converters is studied in Section 5.5. The summary of this chapter is given in Section 5.6.

## 5.1 Stability Analysis Criterion of a Constant Current Cascaded System

It is well known that stability is a major concern for dc distribution systems because the integrated system may become unstable even though the subsystems are stable individually. Significant analysis and design has been applied to dc voltage distribution systems, while

stability and related control strategy are not well studied for dc current distribution systems, especially for the scenarios with long transmission cables. In this section, the stability analysis and related control strategy of a dc current distribution system are presented followed by discussions.

The block diagram of a dc current cascaded system with two power converters is shown in Fig. 5.1. In Fig. 5.1, the two power converters, which are source subsystem and load subsystem, are connected in series. $V_s$ is the input voltage of the source subsystem, while $I_{out}$ is the output current of the load subsystem. The $G_{source}$ is the input-to-output transfer function of the source subsystem, and the $G_{load}$ is the input-to-output transfer function of the load subsystem. The currents $I_s$ and $I_{in}$ are the same, which is the dc link current regulated by the source subsystem. The impedance $Z_o$ represents the output impedance of the source subsystem and the impedance $Z_{in}$ is the input impedance of the load subsystem.

The two subsystems are assumed to be stable individually, which means that

$$I_s = G_{source}V_s \Rightarrow G_{source} = \frac{I_s}{V_s}, \tag{5.1}$$

$$I_{out} = G_{load}I_{in} \Rightarrow G_{load} = \frac{I_{out}}{I_{in}}. \tag{5.2}$$

For the cascaded system, the overall input-to-output transfer function can be expressed as

$$G_{overall} = \frac{I_{out}}{V_s} = \frac{I_{out}}{I_{in}}\frac{I_{in}}{I_s}\frac{I_s}{V_s}. \tag{5.3}$$

Substituting (5.1) and (5.2) into (5.3), we can get

$$G_{overall} = G_{load}\frac{I_{in}}{I_s}G_{source}. \tag{5.4}$$

Since the subsystems are stable individually, the stability of the cascaded system is then determined by $I_{in}/I_s$. For the dc current cascaded system, the circuit diagram of the block diagram shown in Fig. 5.1 can be plotted as illustrated in Fig. 5.2.
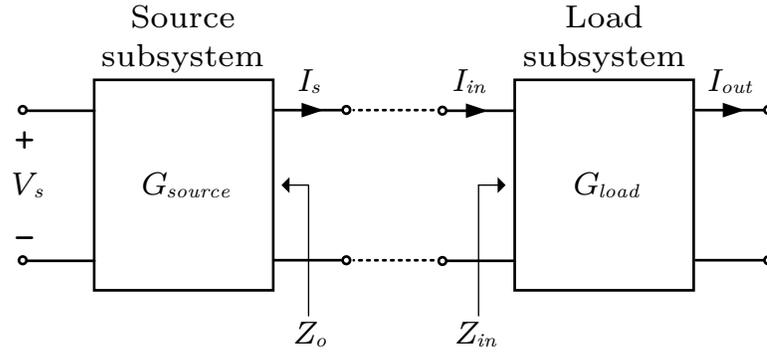
Fig. 5.1: Block diagram of a dc current cascaded system.
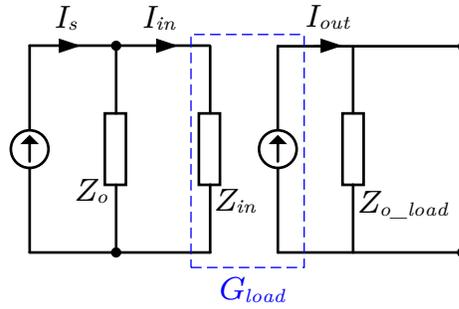


Fig. 5.2: Circuit diagram of a dc current cascaded system.

From Fig. 5.2, the transfer function from $I_s$ to $I_{in}$ can be derived as

$$\frac{I_{in}}{I_s} = \frac{Z_o \parallel Z_{in}}{Z_{in}} = \frac{Z_o}{Z_{in} + Z_o}. \tag{5.5}$$

Substituting (5.5) into (5.4), we can get

$$G_{overall} = G_{load}G_{source}\frac{Z_o}{Z_{in} + Z_o}, \tag{5.6}$$

$$G_{overall} = G_{load}G_{source}\frac{1}{\frac{Z_{in}}{Z_o} + 1} = G_{load}G_{source}\frac{1}{T_m + 1}, \tag{5.7}$$

with

$$T_m = \frac{Z_{in}}{Z_o}. \tag{5.8}$$

From (5.7), it can be seen that the term $T_m$ can be used to evaluate the stability of the

dc current cascaded system. Similar to the minor loop gain defined in a voltage cascaded system [104], $T_m = Z_{in}/Z_o$ is defined as the minor loop gain for a constant current cascaded system, which is employed to determine the stability of a dc constant current distribution system.

If multiple load subsystems are distributed along the constant current trunk, the overall $Z_{in}$ will be the sum of each load subsystem's input impedance plus the impedance of the entire trunk cable, since they are connected in series. If $|Z_o| >> |Z_{in}|$ for all frequencies, the whole dc constant current power distribution system is stable, assuming that the load subsystems are individually stable.

## 5.2    Modeling of Long Distance Cables

The architecture of the undersea dc current distribution system including a shore based power supply, a submarine dc transmission cable with multiple sections and multiple SRC modules is illustrated in Fig. 5.3. The submarine/trunk cable shown in Fig. 5.3 generally has a length of tens of kilometers or even longer. For stability analysis in dc distribution systems, the transmission line is often ignored or modeled as an equivalent inductor or inductor in series with a resistor [27, 119, 120]. However, for the dc current distribution, as aforementioned, it is generally employed in relatively long distance applications, where the distributed high capacitance of the transmission cable is too significant to be neglected, especially for submarine dc transmission cables. In this section, models of the long transmission cables are developed with cable impedance expressions derived for better understanding of the cable dynamic behavior.

As aforementioned, the transmission line is usually equivalent as an inductor or an inductor in series with a resistor. However, because of the relatively long distance from the shore power supply to the SRCs, and according to the cable parameters listed in TABLE 5.1, the distributed capacitance of the submarine transmission cable can no longer be ignored during the system design and stability analysis. In other words, the lumped inductor approach and the lumped inductor in series with the lumped resistor approach are not accurate enough to model the submarine transmission cable for stability analysis because of
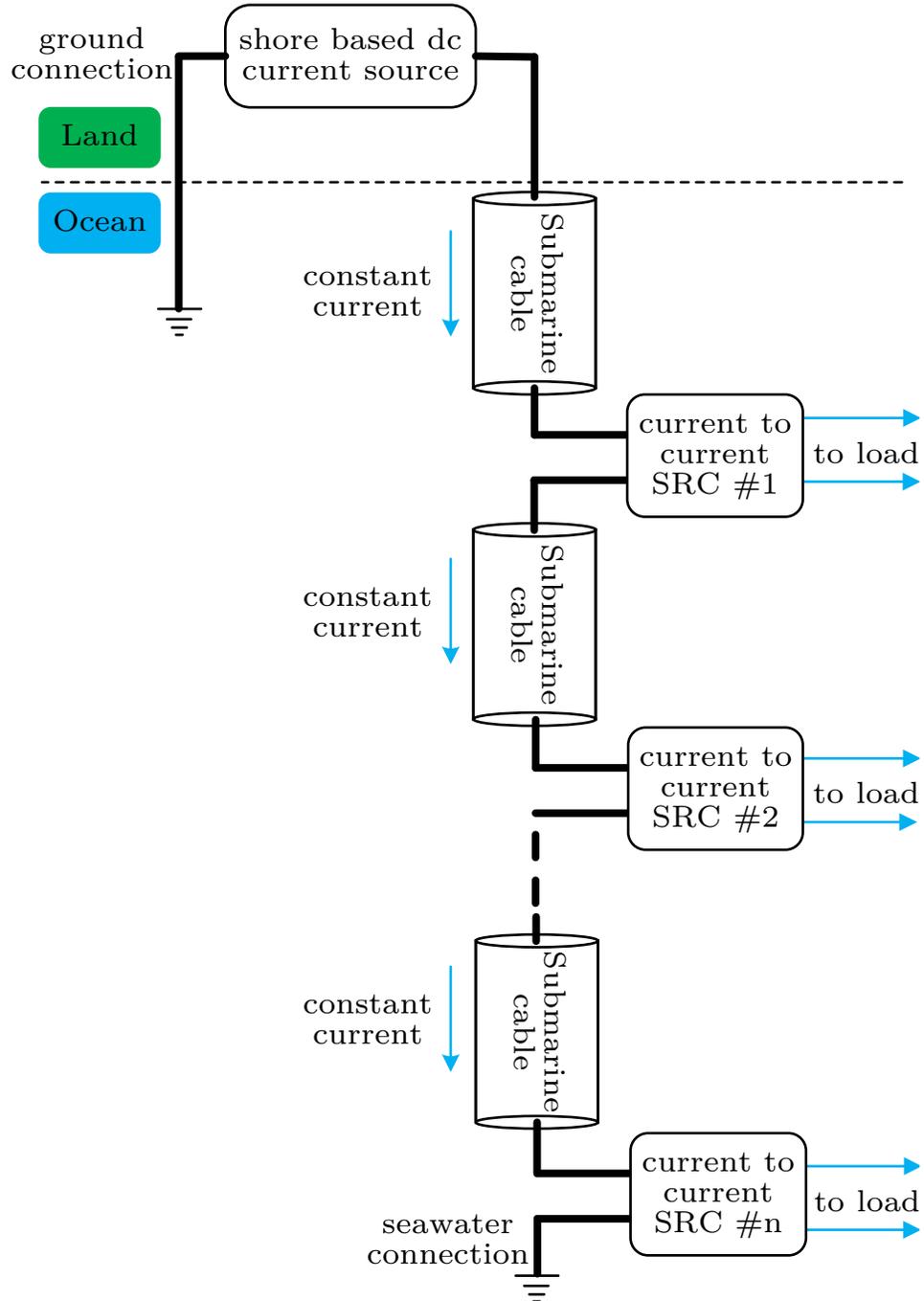
Fig. 5.3: Architecture of an undersea dc current distribution system consists of a shore power supply, a long submarine cable with multiple sections and multiple SRCs.

the considerable distributed capacitance along the cable. Hence, in this work, the cascaded

$\pi$-section approach is adapted to model the submarine cable for exploring the dynamic

performance [121, 122].

The schematic diagram of a single-phase transmission cable of length $l$ is shown in Fig. 5.4. In Fig. 5.4, $l$ is the length of the cable, $n$ is the number of $\pi$-sections used to model the cable, and $R$, $L$ and $C$ are the lumped resistance, inductance and capacitance of each $\pi$-section, respectively. From Fig. 5.4, it can be seen that the cascaded $\pi$-section model for the transmission cable essentially is a lumped model of the distributed cable parameters, which means that the model will be more accurate with more $\pi$-sections employed. However, on the other hand, the model will have higher complexity with more $\pi$-sections, which is also not preferred for analysis and hardware evaluation. So, one has to make a balance between the accuracy of the model and the complexity of the model based on the interested frequency range.

The bode plots of a transmission cable impedance modeled with different number of $\pi$-sections are illustrated in Fig. 5.5 and Fig. 5.6. The cable parameters used for Fig. 5.5 and Fig. 5.6 are listed in TABLE 5.1. The input impedance of the cable with the other terminal open is shown in Fig. 5.5, while Fig. 5.6 shows the input impedance of the cable with the other terminal shorted to ground. From Fig. 5.5 and Fig. 5.6, it can be seen that the 5 $\pi$-sections model has a good match with higher order models for the frequency range up to 1 kHz, which is much higher than the interested frequency range of the application scenario studied in this paper. The 5 $\pi$-sections model is then employed for the analysis shown in this paper, as well as developing the cable emulator for experimental demonstration in this work, since the 5 $\pi$-sections model provides a good balance between accuracy and complexity.

In order to obtain a better understanding of the cable dynamic behavior, and provide analytical expressions for system design and stability analysis, the cable input impedance expressions for different scenarios are derived in this section based on the 5 $\pi$-sections model. The circuit diagrams, based on the 5 $\pi$-sections model, for the cable input impedance calculation are shown in Fig. 5.7, Fig. 5.8 and Fig. 5.9. Fig. 5.7 is the circuit diagram for the scenario where the other terminal of the cable is open, Fig. 5.8 is the circuit diagram for the scenario where the other terminal of the cable is short to ground, and Fig. 5.9 is the

Table 5.1: PARAMETERS OF THE CABLE

| | |
|---|---|
| **Length [km]** | 100 |
| **Unit resistance [$\Omega$/km]** | 1 |
| **Unit inductance [mH/km]** | 0.128 |
| **Unit capacitance [$\mu$F/km]** | 0.2 |
| **Number of $\pi$-sections** | 1, 5, 10, 20, 40 |
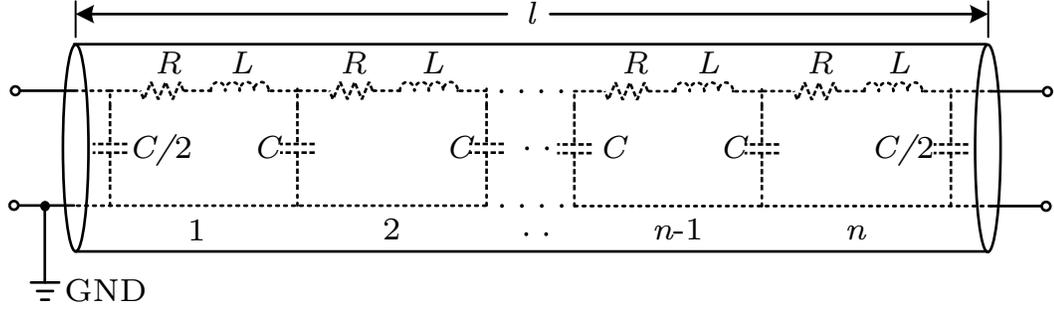


Fig. 5.4: Schematic diagram of a single-phase transmission cable of length $l$.

circuit diagram for the scenario where the other terminal of the cable has an impedance $Z$.

The circuit diagrams shown in Fig. 5.7, Fig. 5.8 and Fig. 5.9 are basic circuits comprising resistors, inductors and capacitors. The input impedance can be solved according to the circuits by applying circuit analysis knowledge. In Fig. 5.7, $Z_1$ is expressed as

$$Z_1 = R + sL + \frac{2}{sC} = \frac{2 + sRC + s^2LC}{sC} = \frac{Z_0}{sC}, \tag{5.9}$$

where $Z_0$ is defined as

$$Z_0 \equiv 2 + sRC + s^2LC. \tag{5.10}$$

Based on (5.9), from Fig. 5.7, the cable impedance with one terminal open can be derived as

$$Z_2 = \frac{1}{sC + \frac{1}{Z_1}} = \frac{Z_0}{sC(1 + Z_0)}, \tag{5.11}$$

$$Z_3 = R + sL + Z_2 = \frac{Z_0 + (Z_0 + 1)(Z_0 - 2)}{sC(1 + 2Z_0 + (Z_0 + 1)(Z_0 - 2))}, \tag{5.12}$$
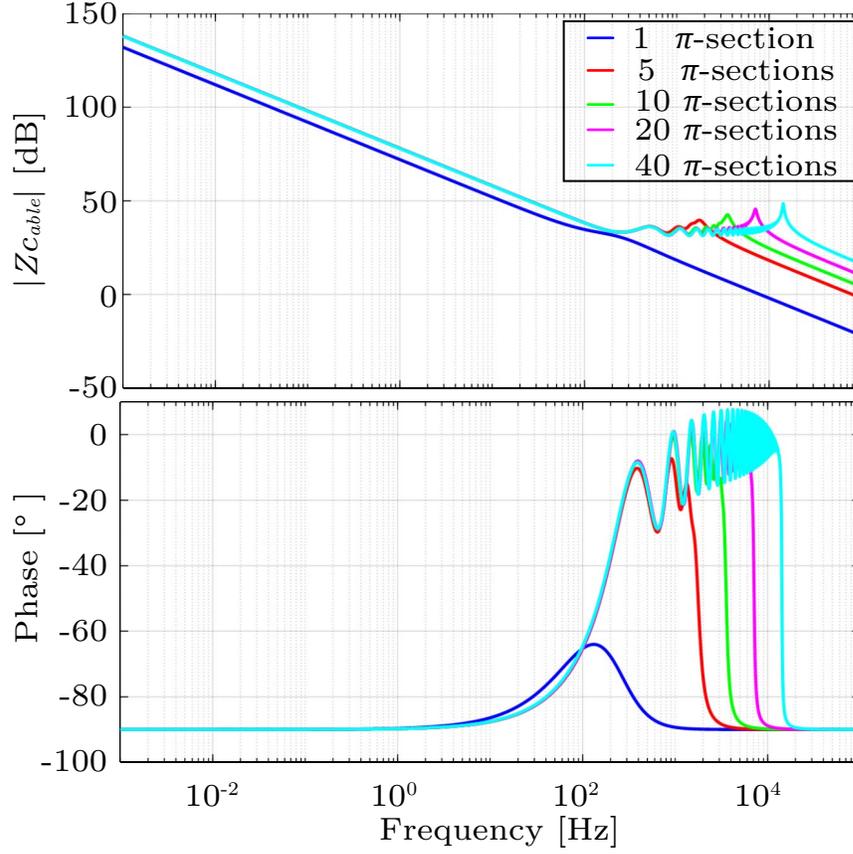
Fig. 5.5: Input impedance of the transmission cable when the cable is open.

$$Z_4 = \frac{1}{sC + \frac{1}{Z_3}} = \frac{Z_0^2 - 2}{sC(Z_0^2 + Z_0 - 1)}, \tag{5.13}$$

$$Z_5 = R + sL + Z_4 = \frac{Z_0^3 - 3Z_0}{sC(Z_0^2 + Z_0 - 1)}, \tag{5.14}$$

$$Z_6 = \frac{1}{sC + \frac{1}{Z_5}} = \frac{Z_0^3 - 3Z_0}{sC(Z_0^3 + Z_0^2 - 2Z_0 - 1)}, \tag{5.15}$$

$$Z_7 = R + sL + Z_6 = \frac{Z_0^4 - 4Z_0^2 + 2}{sC(Z_0^3 + Z_0^2 - 2Z_0 - 1)}, \tag{5.16}$$
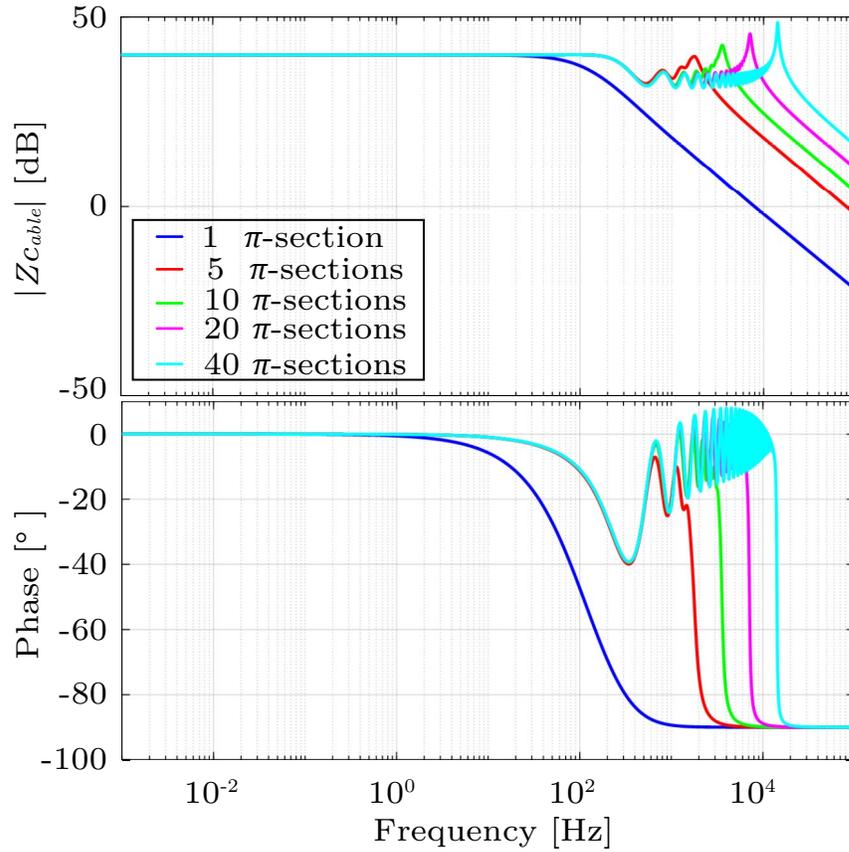
Fig. 5.6: Input impedance of the transmission cable when the cable is terminated in a short circuit.
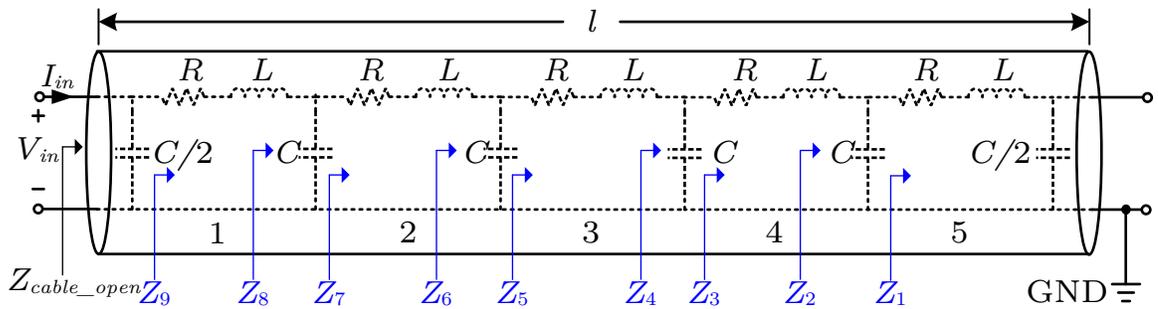


Fig. 5.7: Circuit diagrams for input impedance calculation of the transmission cable with a length of $l$ and open terminal modeled by 5 $\pi$-sections model.

$$Z_8 = \frac{1}{sC + \frac{1}{Z_7}} = \frac{Z_0^4 - 4Z_0^2 + 2}{sC(Z_0^4 + Z_0^3 - 3Z_0^2 - 2Z_0 + 1)}, \tag{5.17}$$
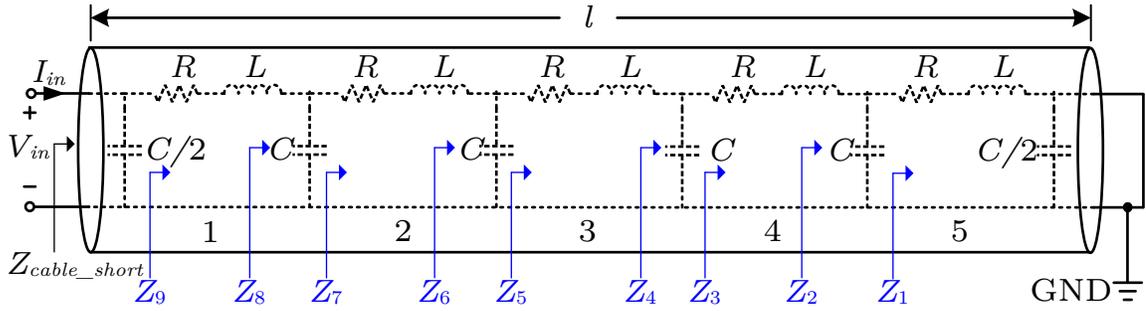
Fig. 5.8: Circuit diagrams for input impedance calculation of the transmission cable with a length of $l$ and short terminal modeled by 5 $\pi$-sections model.
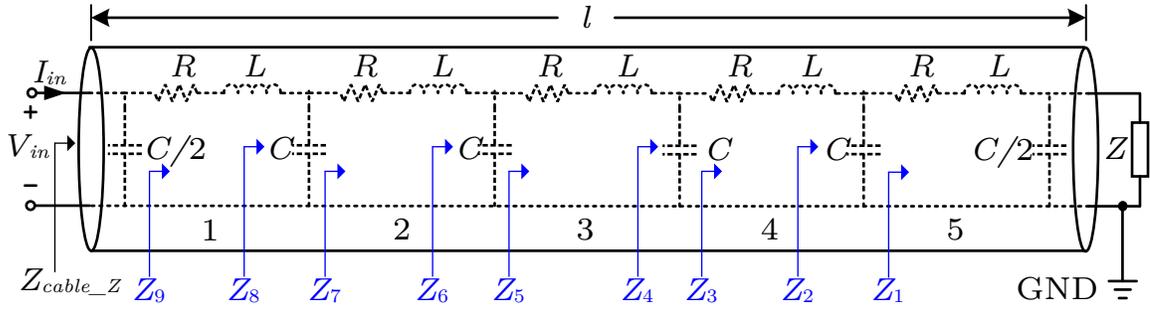


Fig. 5.9: Circuit diagrams for input impedance calculation of the transmission cable with a length of $l$ and impedance of $Z$ at the other terminal modeled by 5 $\pi$-sections model.

$$Z_9 = R + sL + Z_8 = \frac{Z_0^5 - 5Z_0^3 + 5Z_0}{sC(Z_0^4 + Z_0^3 - 3Z_0^2 - 2Z_0 + 1)}, \tag{5.18}$$

$$Z_{cable\_open} = \frac{1}{\frac{sC}{2} + \frac{1}{Z_9}} = \frac{2(Z_0^5 - 5Z_0^3 + 5Z_0)}{sC(Z_0^5 + 2Z_0^4 - 3Z_0^3 - 6Z_0^2 + Z_0 + 2)}. \tag{5.19}$$

Equation (5.19) is the expression for the input impedance of the cable with the other terminal open. In Fig. 5.8, $Z_1$ and $Z_2$ are expressed as

$$Z_1 = R + sL, \tag{5.20}$$

$$Z_2 = sC + \frac{1}{R + sL} = \frac{R + sL}{1 + sRC + s^2LC} = \frac{R + sL}{Z_0}, \tag{5.21}$$

where $Z_0$ is defined as

$$Z_0 \equiv 1 + sRC + s^2LC. \tag{5.22}$$

Based on (5.21), from Fig. 5.8, the input impedance of the cable with the other terminal short to ground can be derived as below. Since the calculation procedure is similar with the terminal open case, the final expression is provided below without showing the detailed derivations.

$$Z_{cable\_short} = \frac{2(R + sL)(Z_0^4 + 4Z_0^3 + 3Z_0^2 - 2Z_0 - 1)}{Z_0^5 + 5Z_0^4 + 5Z_0^3 - 5Z_0^2 - 5Z_0 + 1)}. \tag{5.23}$$

For the scenario that the other terminal of the cable is connected to an impedance $Z$, the input impedance of the cable can be calculated from Fig. 5.9. The final expression can be expressed as

$$Z_{cable\_Z} = \frac{2(Z_c Z_d^4 - 5Z_c Z_d^2 + 4Z_c + (4Z_d^2 - 6)Z_e + Z_d Z)}{sC[(Z_d + 2)(Z_c Z_d^3 - 3Z_c Z_d + Z) + (4Z_d^2 + 8Z_d - 6)Z_e] + 8Z_d - 12}, \tag{5.24}$$

where

$$Z_c \equiv 2(R + Z) + s(2L + RCZ) + s^2LCZ, \tag{5.25}$$

$$Z_d \equiv 2 + sRC + s^2LC, \tag{5.26}$$

$$Z_e \equiv R + sL. \tag{5.27}$$

In (5.19), (5.23) and (5.24), $R$, $L$ and $C$ are the lumped resistance, inductance and capacitance of each $\pi$-section, respectively. $Z$ is the impedance connected between cable terminal and ground. When a certain length cable is modeled by a 5 $\pi$-sections based model, the $R$, $L$ and $C$ of each cell can be calculated, which can be used to build the per-unit scale laboratory emulator. From Fig.5.4, it can be seen that the $\pi$-section model has a lumped capacitor at the cable terminals. However, the real transmission cable is generally inductive at its terminals. To improve that, a model with the combination of $\pi$-section and T-section
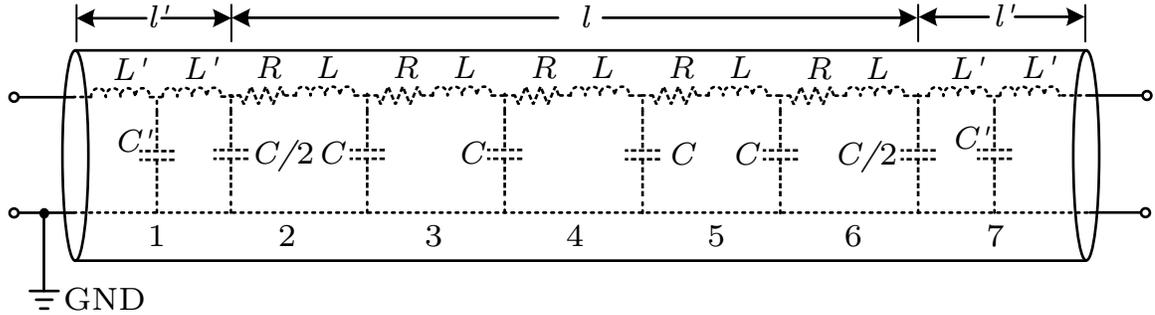
Fig. 5.10: Schematic diagram of the 5 $\pi$-section combined with 2 T-section model.

are used in this work, as shown in Fig.5.10. In Fig.5.10, the 5 $\pi$-sections at the center model the major length of the cable while the two T-sections at two ends model a short length to improve the model accuracy. When a certain length cable is modeled by the 5 $\pi$-sections plus 2 T-sections model, the $R$, $L$, $C$, $L^{'}$ and $C^{'}$ of each cell can be calculated based on the parameters of the cable, which is used to build the per-unit scale cable emulator that is used in laboratory tests. As a result, the laboratory emulator has the same impedance as the real cable in the case of the same per-unit length parameters and the same cable length. Since the cable length modeled by the T-section is quite short compared with the length modeled by the $\pi$-section model, for the system stability analysis, the 5 $\pi$-sections model is used. For the laboratory cable emulator, the 5 $\pi$-sections plus 2 T-sections model is used to simulate the inductive behavior at the terminals of the cable.

## 5.3 Relation between Closed-loop and Open-loop Input Impedance of Converters

The open-loop input impedance of a converter can be derived from its small signal model. However, the closed-loop input impedance of the converter is needed for the system stability analysis since the output of the converter is required to be regulated for most of the applications. The closed-loop input impedance of a converter is complex and can not be derived from the small signal model directly. In this section, the SRC with constant current input and regulated output current is taken as an example to analyze the relation between closed-loop and open-loop input impedances, the small-signal control diagram of

which is illustrated in Fig.5.11. The analysis can be applied to other converters easily.

In Fig.5.11, for the closed-loop operation, $\hat{i}_{ref} = 0$. From Fig.5.11, we can get

$$\hat{\alpha} = H(s)G_c(s)K(s)\hat{i}_{out}, \tag{5.28}$$

$$\hat{i}_{out} = \hat{\alpha}G_{i\alpha}(s) + \hat{i}_{in}G_{i\_i_{in}}(s). \tag{5.29}$$

Substituting (5.29) into (5.28), $\hat{\alpha}$ can be expressed as

$$\hat{\alpha} = H(s)G_c(s)K(s)\hat{i}_{out}[\hat{\alpha}G_{i\alpha}(s) + \hat{i}_{in}G_{i\_i_{in}}(s)]. \tag{5.30}$$

From (5.30), in terms of $\hat{i}_{in}$, $\hat{\alpha}$ can be expressed as

$$\hat{\alpha} = \frac{H(s)G_c(s)K(s)G_{i\_i_{in}}(s)}{1 - H(s)G_c(s)K(s)G_{i\alpha}(s)}\hat{i}_{in}. \tag{5.31}$$

For a closed-loop converter, the small signal input voltage $\hat{v}_{in}$ is expressed as

$$\hat{v}_{in} = Z_{in}\hat{i}_{in} + G_{v_{in}\_\alpha}(s)\hat{\alpha}, \tag{5.32}$$

where $Z_{in}$ is the open-loop input impedance of the converter.

Substituting (5.31) into (5.32), we can get

$$\hat{v}_{in} = (Z_{in} + \frac{H(s)G_c(s)K(s)G_{i\_i_{in}}(s)G_{v_{in}\_\alpha}(s)}{1 - H(s)G_c(s)K(s)G_{i\alpha}(s)})\hat{i}_{in}. \tag{5.33}$$

From (5.33), the closed-loop input impedance of the converter can be derived as

$$Z_{in\_cl} = Z_{in} + \frac{H(s)G_c(s)K(s)G_{i\_i_{in}}(s)G_{v_{in}\_\alpha}(s)}{1 - H(s)G_c(s)K(s)G_{i\alpha}(s)}. \tag{5.34}$$
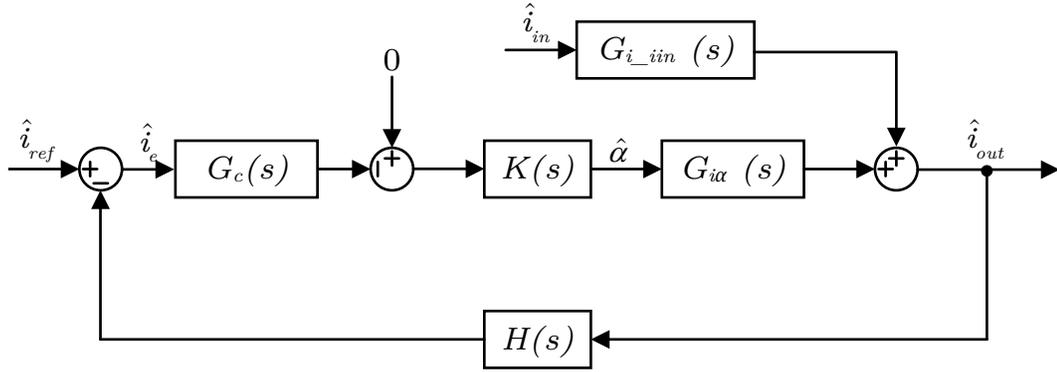
Fig. 5.11: Small signal control diagram of an SRC with constant current input and regulated output current.

In (5.29) to (5.34), $Z_{in}$ is the open-loop input impedance of the converter, and

$$G_{i\_i_{in}}(s) \equiv \left. \frac{\hat{i}_{out}}{\hat{i}_{in}} \right|_{\hat{\alpha}=0}, \tag{5.35}$$

$$G_{v_{in}\_\alpha}(s) \equiv \left. \frac{\hat{v}_{in}}{\hat{\alpha}} \right|_{\hat{i}_{in}=0}, \tag{5.36}$$

$$G_{i\alpha}(s) \equiv \left. \frac{\hat{i}_{out}}{\hat{\alpha}} \right|_{\hat{i}_{in}=0}. \tag{5.37}$$

For the frequency range around the crossover frequency, (5.34) is more accurate than the approximation that the closed-loop input impedance is a negative resistor below crossover frequency and is the open-loop input impedance above crossover frequency.

## 5.4  Stability Analysis of a System Consists of One Cable and One SRC

As presented in Section 5.1, the minor loop gain of a constant current cascaded system, which is defined as $T_m = Z_{in}/Z_o$, can be employed to evaluate the stability of a dc current distribution system. For a current cascaded system with long transmission cable, as illustrated in Fig.5.12, $Z_{in}$ is the closed-loop input impedance of the load converter, while $Z_o$ is the output impedance of the system seen by the load converter. The closed-loop input impedance of the load converter can be calculated from (5.34). Instead of the output impedance of

the current source, $Z_o$ becomes the input impedance of the cable with the other terminal connected to an impedance $Z$, where $Z$ is the output impedance of the current source. If the output impedance of the current source is available, the $Z_o$ can be calculated from (5.24). However, in some practical applications, the output impedance of the source may not be available a priori. In this case, for the current source, the output impedance can be assumed to be infinite within its bandwidth, which means the current source is assumed to be an ideal current source within its bandwidth. In this case, the impedance seen by the load converter $Z_o$ becomes the cable impedance with the other terminal open, which is given by (5.19).

In order to demonstrate the analysis proposed in this section, a system consists of a 1 A dc current source, a 100 km submarine cable and an SRC with 0.33 A regulated output current operating at 500 W output power is taken as an example. The circuit diagram of the system is illustrated in Fig.5.12. In this example, a simple integrator is employed to control the SRC. The 100 km submarine cable is modeled by the 5 $\pi$-sections model with the parameters tabulated in TABLE 5.1. According to the above analysis, $Z_o$ of the system can be derived according to (5.19), the bode plot of which is shown in Fig.5.13.

For the SRC with 1 A input current, 0.33 A output current and 500 W output power, the closed-loop input impedance can be assumed to be the negative resistor, which is 53.7 dB, within the controller bandwidth for the initial design. From Fig.5.13, it can be seen that $Z_o$ has a magnitude of less than 53.8 dB for frequency range higher than 16.3 Hz, which means the controller bandwidth of the SRC should be lower than 16.3 dB in order to obtain stable behavior. Based on this, the SRC controller can be initially designed. Then, based on (5.19) and (5.34), the Nyquist plot of the resulted minor loop gain $T_m$ can be easily plotted to verify the design and check the stability margins.

The Nyquist plots of the minor loop gain $T_m$ for three controller designs are illustrated in Fig.5.14, Fig.5.15 and Fig.5.16, to check the stability of the designs. In Fig.5.14, the controller is $500/s$, which results in a controller bandwidth of 9.65 Hz. In Fig.5.15, the controller is $1000/s$, which results in a controller bandwidth of 18.8 Hz. In Fig.5.16, the
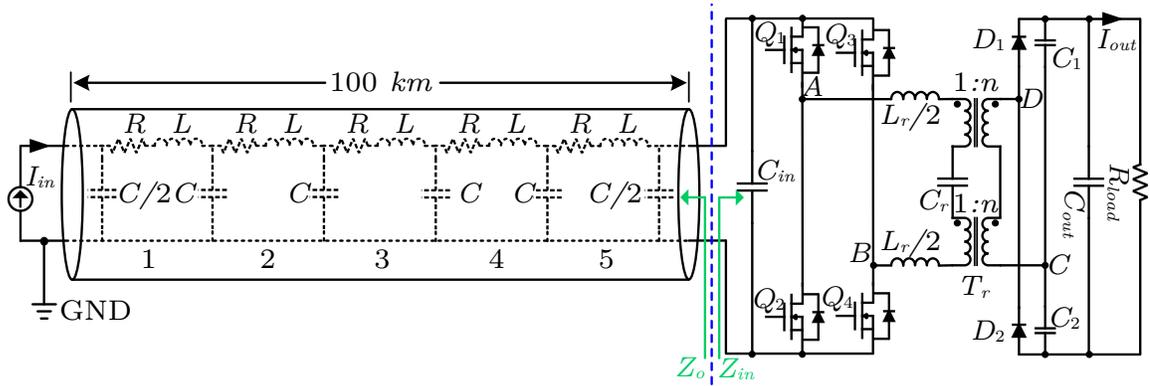
Fig. 5.12: A current cascaded system with long transmission cable.
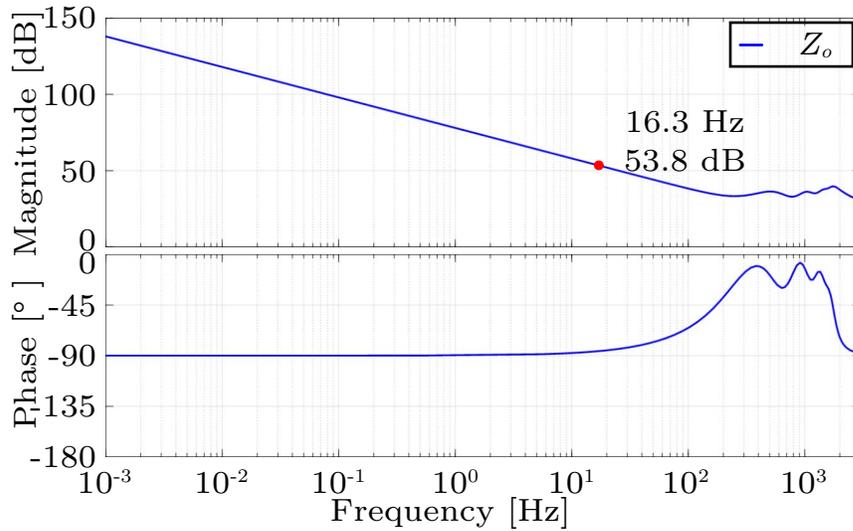


Fig. 5.13: The bode plot of the $Z_o$ of the system under study.

controller is $1033/s$, which results in a controller bandwidth of 19.4 Hz. According to the above analysis based on the negative resistor assumption, 9.65 Hz controller bandwidth is stable, and the other two controller designs are unstable. However, from Fig.5.14, Fig.5.15 and Fig.5.16, all three controller designs are stable with different margins. The disagreement comes from the assumption that the closed-loop input impedance is a negative resistor within controller bandwidth and is the open-loop input impedance beyond the controller bandwidth. Hence, the assumption can be used as a start point for the design, while Nyquist plot of the system minor loop gain $T_m$ based on (5.19) and (5.34) should be employed to verify the stability, and check the stability margin.
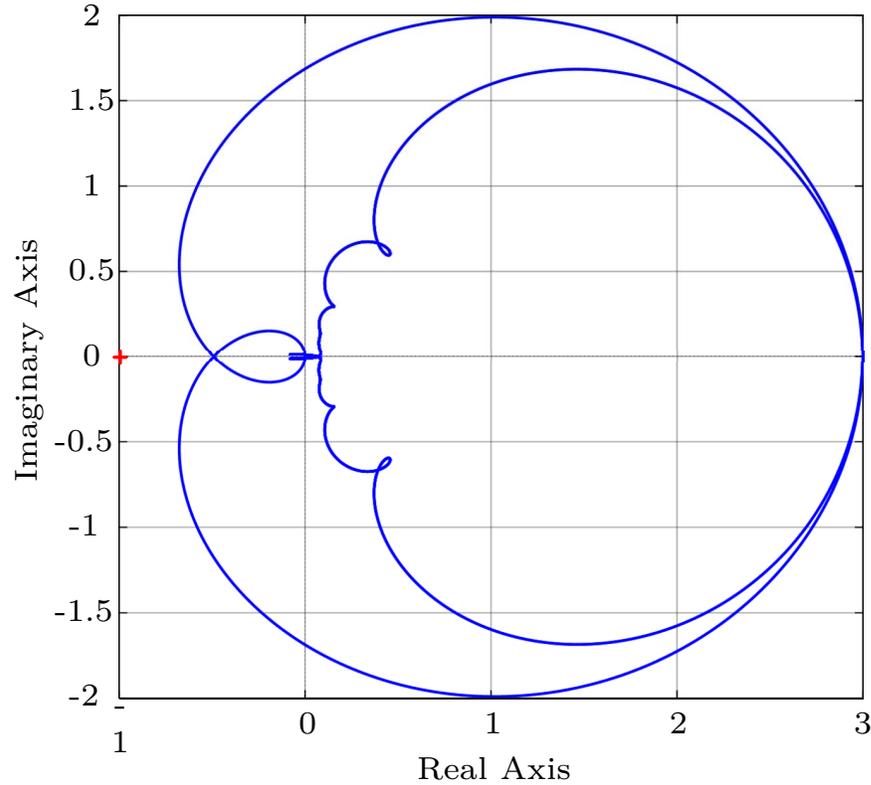
Fig. 5.14: Nyquist plot of $T_m$ for the controller $500/s$.

The three controllers shown in Fig.5.14, Fig.5.15 and Fig.5.16 are all stable from the Nyquist plot. However, they are not the same. The controller design shown in Fig.5.14 has a lot of margin, which means that the system can maintain stable even with a big disturbance. The controller design shown in Fig.5.15 has a little bit of margin, which means that the system may become marginally stable with a disturbance. The controller design shown in Fig.5.16 barely has stable margin, which means that the system may become unstable even with a small disturbance.

## 5.5   Stability Analysis of a System Consists of Multi-cables and Multi-SRCs

Generally, a dc current distribution system includes more than one cable sections and more than one dc-dc power converter modules. A system which has two 100 km and two SRCs is illustrated in Fig. 5.17 as a case study. For the stability analysis, the SRC shown in Fig. 5.17 can be modeled by its closed-loop input impedance, as illustrated in Fig. 5.18.
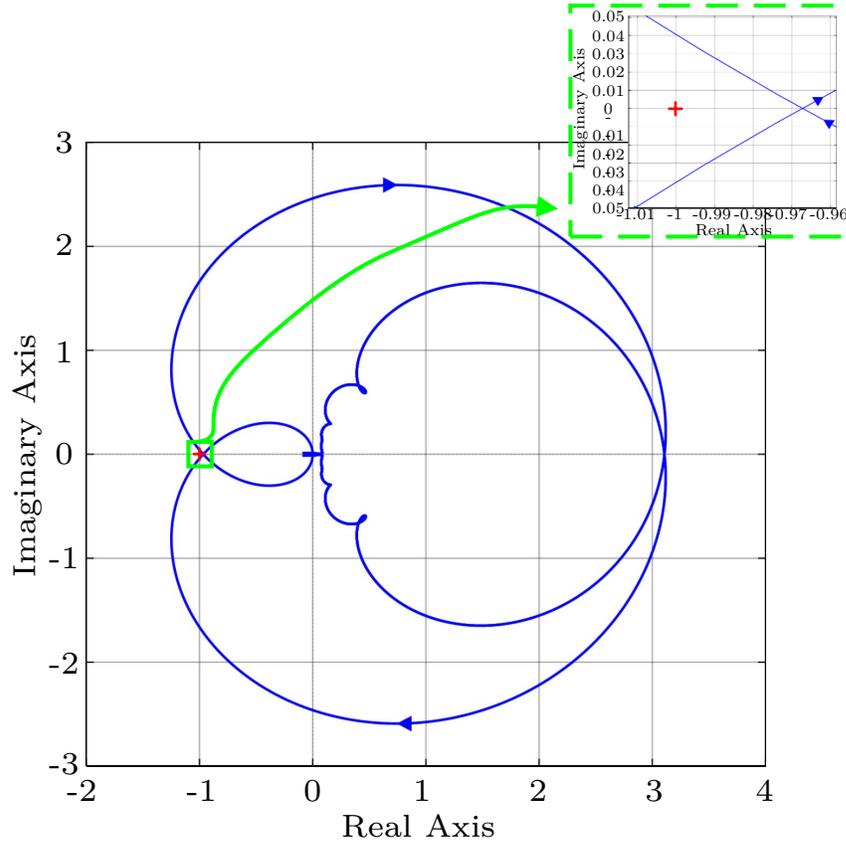
Fig. 5.15: Nyquist plot of $T_m$ for the controller $1000/s$.

In Fig. 5.18, the closed-loop input impedance can be calculated from (5.34) based on the operating point. $Z_2$ in Fig. 5.18 can be calculated from (5.24) by having $Z_1$ ($Z_{in\_cl}$) as the impedance connected to the other terminal, as shown in Fig. 5.18. As an example, the bode plots of $Z_1$ and $Z_2$ shown in Fig. 5.18 are presented in Fig. 5.19. The cable parameters used in this example is tabulated in TABLE 5.1, and the SRC operates at 1 A input current, 0.33 A output current with 1 kW output power.

From Fig. 5.19, it can be seen that the impedance $Z_1$, which is the closed-loop input impedance of the SRC, can be employed to represent the impedance $Z_2$ in Fig. 5.18 for the system stability evaluation during the system design stage. Also, it can be seen that $|Z_1|$ is higher than $|Z_2|$ from Fig. 5.19, which means that the system has a little bit more stability margin by using $Z_1$ to represent $Z_2$ for the system stability analysis. On the other hand, the sub-system in the green dashed box should be stable individually, which means
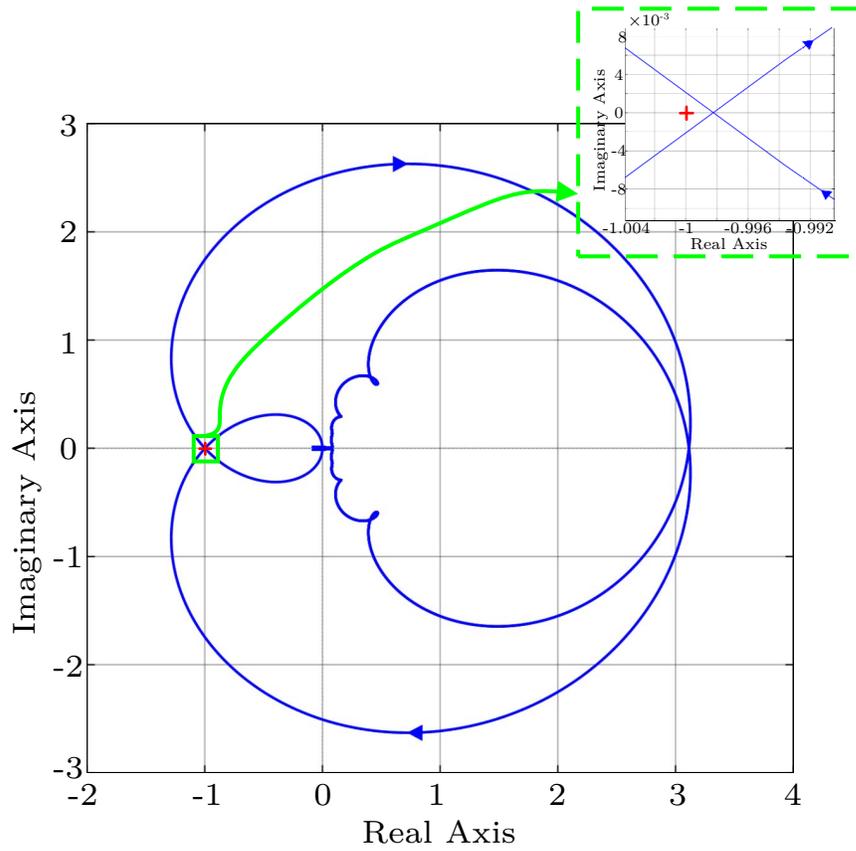
Fig. 5.16: Nyquist plot of $T_m$ for the controller $1033/s$.
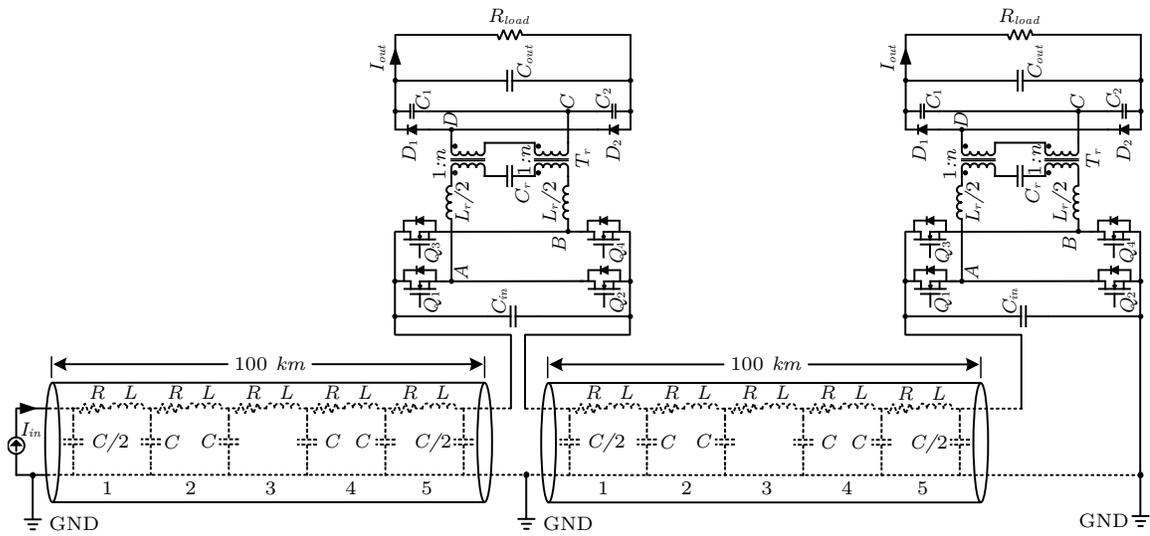


Fig. 5.17: A dc current distribution system with two 100 km cables and two SRCs.
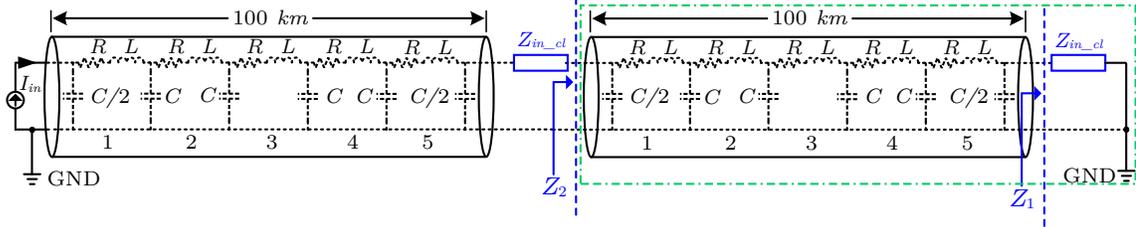
Fig. 5.18: Impedance model of a dc current distribution system with two 100 km cables and two SRCs.
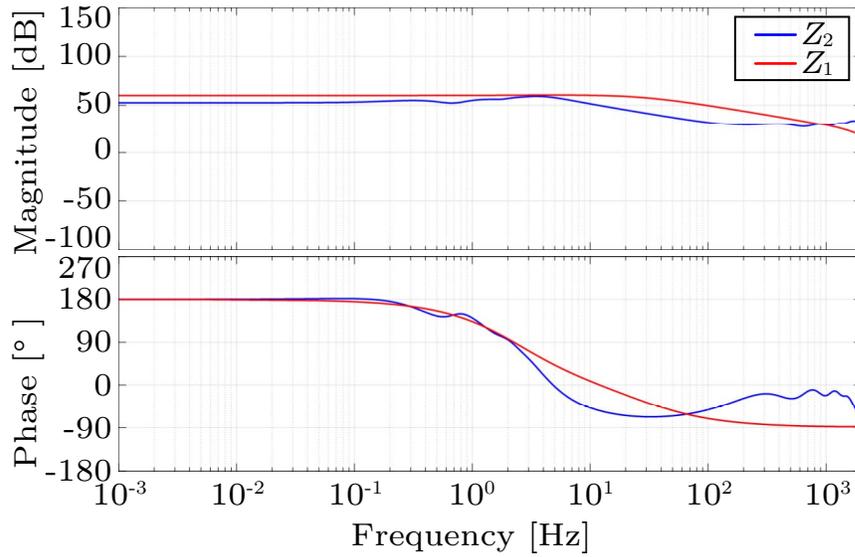


Fig. 5.19: The bode plots of $Z_1$ and $Z_2$ in Fig. 5.18.
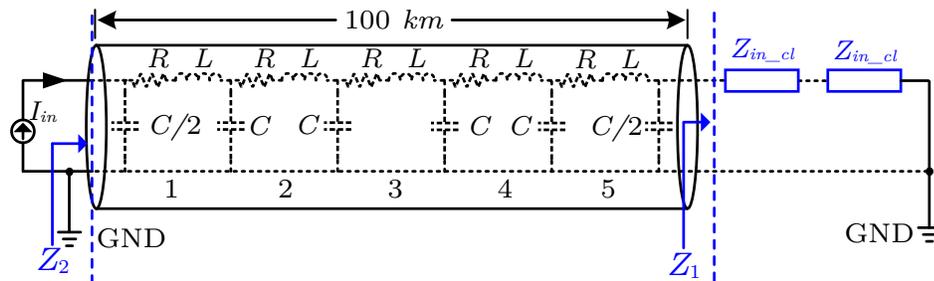


Fig. 5.20: Simplified impedance model of a dc current distribution system with two 100 km cables and two SRCs.

that $|Z_{cable\_open}|$ should be higher than $|Z_1|$ with some margin. In Fig. 5.18, the impedance $Z_2$ can be approximated as the parallel combination of $Z_{cable\_open}$ and $Z_1$. In hence, the impedance $Z_2$ can be approximated as the impedance $Z_1$ for system stability analysis.
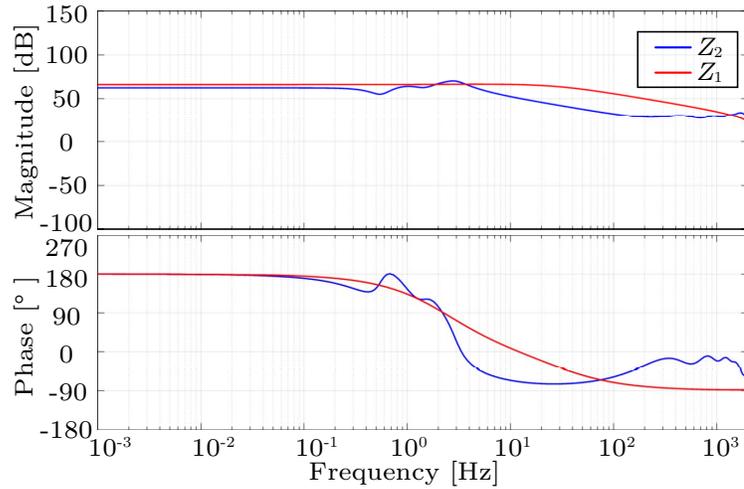
Fig. 5.21: The bode plots of $Z_1$ and $Z_2$ in Fig. 5.20.
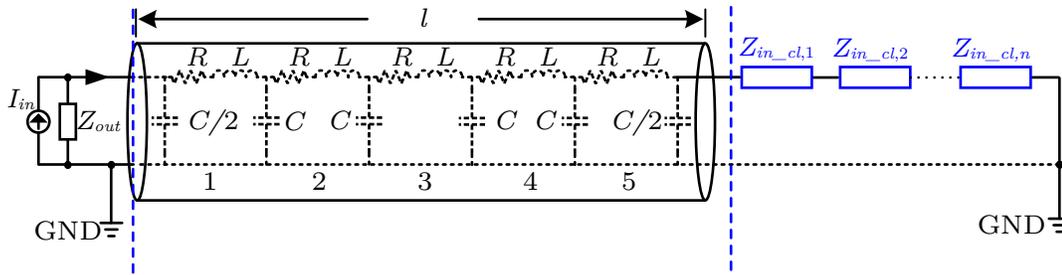


Fig. 5.22: Simplified impedance model of a dc current distribution system.

Based on the above analysis, the impedance model shown in Fig. 5.18 can be simplified as illustrated in Fig. 5.20. In a similar approach, the bodes plots of $Z_1$ and $Z_2$ shown in Fig. 5.20 are presented in Fig. 5.21. Here, the two SRCs are assumed to be identical to simplify the math. From Fig. 5.21, it can be seen that $Z_1$ can be used to represent $Z_2$ in Fig. 5.20, where $Z_1$ is the sum of input impedances of the two SRCs.

For a general dc current distribution system contains multiple cables and multiple SRCs, by applying the above analysis, the system can be simplified as illustrated in Fig. 5.22. For the simplified impedance model presented in Fig. 5.22, the $l$ km cable is the trunk cable that connects the shore-based power supply and the first SRC module. Then, the analysis proposed in SECTION 5.4 can be employed to evaluate the stability of the entire system

since the simplified impedance model .

## 5.6   Summary

This chapter studies the stability of dc current distribution systems with the consideration of cable impedances. First, the impedance based stability analysis criterion for dc current distribution systems is derived, where $T_m = Z_{in}/Z_o$ is defined as the minor loop gain to evaluate the stability of dc constant current distribution systems. Second, the long distance cable used in a dc current distribution system is modeled by taking submarine cable as an example, in which case the cable capacitance can no longer be ignored, and the cable is modeled by a number of $\pi$-sections or T-sections instead of inductors in series with resistor or simple inductors. The explicit expressions of the cable impedance under different conditions are derived. Third, the relation between closed-loop and open-loop input impedances of power converters is derived by using the SRC with constant dc input current as an example, which is more accurate than simply assume that the closed-loop input impedance is a negative resistor below crossover frequency and is the open-loop input impedance above crossover frequency. Based on the aforementioned analysis, stability evaluation of a system consists of one cable and one SRC is presented to demonstrate the proposed stability analysis. On top of that, the stability analysis for a dc current distribution system includes multi-cables and multi-SRCs is discussed.

CHAPTER 6

SYSTEM CONTROL DESIGN

The unique features, different steady state and dynamic behaviors of dc current distribution systems and the SRCs with constant input current used in the dc current distribution systems introduces challenges to the control of the entire system, including protection of the SRCs. This chapter proposes solutions to solve the challenges related to control, operation and protection of the dc current distribution systems.

In this chapter, based on the stability analysis presented in CHAPTER 5, the control strategy and controller design for the SRC with constant dc input current in a dc current cascaded system is presented in Section 6.1, while Section 6.3 discusses the output impedance requirements and control design of the shore-based output current regulated power supply. The operational techniques of dc current distribution systems are studied in Section 6.4, including the startup and normal shutdown strategies, and discussions on hardware requirements related to system operation. The possible fault scenarios and corresponding protection techniques for the SRCs with constant dc input current are analyzed in Section 6.5. The FPGA implementations, including normal operation, integral controller, synchronous rectification and protections, are presented in Section 6.6. The summary of this chapter is given in Section 6.7.

## 6.1 Control Strategy and Controller Design for the SRC without Cable Impedance

### 6.1.1 Control Strategy

If the output impedance of the source is known, the impedance specifications presented in [27, 28] can be used to develop a control strategy that guarantees the stable operation of the dc power distribution system. However, in some practical applications, the output impedance of the source may not be available a priori. In these cases, the impedance

specifications mentioned in the literatures become difficult to implement. For the undersea constant current dc power distribution system investigated in this work, the shore based current source is a commercial product without an output impedance description, while the controller bandwidth is known.

For an output current or output voltage regulated converter, the closed loop input impedance is a negative resistance over a frequency range lower than the crossover frequency, while it is the open loop input impedance over the frequency range higher than the crossover frequency. If the shore based current source has a crossover frequency higher than the load SRC module, the load impedance seen by the source at higher frequencies is the open loop input impedance of the SRC module. In this case, the high output impedance of the constant current source covers the stability condition up to its crossover frequency, and overall stability is guaranteed if the SRC modules operate stable in open loop mode with the source for the entire load range and all operating points.

For each SRC module, a single loop current control can be employed with a crossover frequency lower than the shore based current source crossover frequency. A simple PI controller or integrator can be used to implement the control as shown in Fig. 6.1. In Fig. 6.1, a $180°$ inversion is included in the feedback loop due to the negative gain of the SRC from phase input to current output, as seen in (3.22). The saturation block in Fig. 6.1 is employed to limit the minimum phase shift due to the resulting high input voltage discussed in the steady state analysis. Each SRC module in the system is controlled by its own controller independently.

For a dc current distribution system with significant cable impedances, the above proposed control strategy needs to be improved. The stability analysis presented in Section 5.4 and 5.5 are employed to help designing the controller for the SRCs in the system. In order to obtain a stable system behavior, the assumption that the closed-loop input impedance is a negative resistor within controller bandwidth and is the open-loop input impedance beyond the controller bandwidth can be used as a start point for the controller design, while Nyquist plot of the system minor loop gain $T_m$ based on (5.19) and (5.34) should be
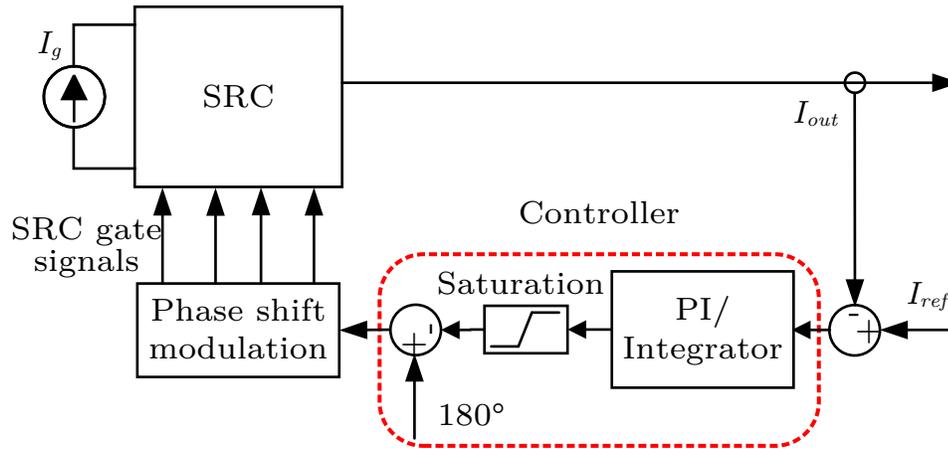
Fig. 6.1: Controller architecture.

employed to verify the stability, and check the stability margin.

### 6.1.2 Discussion

For a cascaded system which contains output regulated power converters, the regulated converter presents a constant load to the source subsystem because all load is on the regulated side of the converter. For example, if the input current drops, the power converter compensates and the input voltage increases. This means that the source subsystem will see a negative load resistance, and the system may become unstable.

In the design of RF integrated circuits (IC), a resistor in parallel with the input to the IC or in series with the output (as appropriate) is employed as a solution to avoid oscillation caused by the negative resistance [23]. The power loss associated with this technique is acceptable in RF work, but not in a power system. For a power system, especially for a constant voltage cascaded power system, the general approach is to design an input filter for the load power converter accordingly. However, for a dc constant current power distribution system, the approach applied in RF work may be acceptable as well because of the different structure it has.

For the undersea constant current power distribution system investigated in this dissertation, the entire trunk cable generally has a length of tens of kilometers or even longer. The conventional underwater telecommunication cable is generally used as the trunk cable

for its high quality, high reliability and relatively low cost. The underwater telecommunication cable has a typical resistance of around 1 $\Omega$/km, which means that the total resistance of the trunk cable in an undersea constant current power distribution system is several hundred ohms. Since the regulated power converters are distributed along the trunk cable, the trunk cable resistance is in series with the input impedance of those power converters. In other words, the load impedance seen by the source subsystem is the sum of the negative resistances from the regulated power converters and the positive resistance from the trunk cable. Since the trunk cable resistance is unavoidable in such a scenario, the trunk cable is able to assist the system to be stable and avoid oscillation.

The control strategy presented in this section is robust against cable faults and converter faults as well. When the trunk cable is broken at any point, the trunk cable current shunts to sea water, the output voltage of the shore based current source on the land will automatically vary so that the voltage at the fault point becomes ground voltage and the current from the source to the fault point remains constant. The SRC modules in the series chain are controlled independently, so the energized modules can still operate as normal. The fault point can also be located by measuring the dc resistance between the source output and the ocean. When there is a converter fault in the system, such as the SRC module's output open circuit fault, the controller will short the input of that module to bypass the trunk current to the rest of the system. The shore based current source on the land will automatically maintain the trunk current to be constant, and the rest of the system can operate without disturbances. In addition, shorting the input of an SRC module will reduce the total input impedance of the load subsystem while the output impedance of the source subsystem remains the same, so the whole system will be still stable as analyzed in Section 5.1.

## 6.2 Controller Design for the SRC Considering the Cable Impedance

In general, the controller design of a power converter is based on the loop gain analysis to archive expected individual stability and dynamic behavior. However, for a dc current distribution system, the controller design of the SRC also depends on the system stability

analysis in order to ensure the system wide stable operation. As presented in Section 5.4, the closed loop input impedance of the SRC $Z_{in\_cl}$ is a function of the controller $G_c(s)$. In this work, the SRC controller is designed based on the system stability analysis, and double checked in the loop gain analysis to make sure that the SRC is stable individually.

The controller bandwidth from the stability analysis presented in this work is in the 10 Hz range, which is low enough to ensure the individual stability. The loop gain analysis is not presented in this work because of that. The dc current distribution scenario investigated in this work does not have high dynamic performance requirements, since it is a slow system because of the long distance, and the loads are almost constant in the system. Since a very low bandwidth controller is needed, a simple controller structure can be employed to implement the controller, such as PI controller or integrator. The controller structure used in this work is an integrator. For the applications that needs wide bandwidth control, additional research is needed based on the stability analysis, which is discussed in Chapter 8 as one of the future research directions.

## 6.3 Shore-based DC Current Power Supply Design

In a dc current distribution system for undersea application, the shore-based dc current power supply provides a regulated current to the trunk cable and the SRC modules deployed in the system. The shore power supply needs to be capable of regulating the distribution current with no load but trunk cable in the system, and with full load in the system. As a result, the output voltage of the shore power supply needs to vary within a wide range from no load to full load.

One candidate topology for the shore power supply is the grid-tied three-phase ac-dc converter using DABSRC and a three-phase unfolder presented in [123]. The topology presented in [123] has smaller dc-link capacitance, negligible unfolder switching losses, reduced line filter sizes, and faster dynamic response. In [124], the authors presented multimode control techniques of series and parallel connected DABSRC modules, which means that the shore power supply can be designed in a modularized way by using the Unfolder-DABSRC topology. The inputs of the unfolders can be either in parallel or series depending

on the grid that the shore power supply is tied to. The outputs of the DABSRCs can be designed in series and controlled by using the techniques presented in [124] to implement a relatively low output current regulation with a wide range of output voltage variation.

The integrated dc distribution system may become unstable even if the shore-based dc current power supply is stable individually, because of the interactions of shore power supply output impedances and the rest of the system, as analyzed in Chapter 5. As illustrated in Fig. 6.2, the shore-based dc current power supply can be modeled as an ideal current source in parallel with its output impedance, the cable can be modeled by the $\pi$-section model, and the SRCs can be modeled by their closed-loop input impedances.

As shown in Fig. 6.2, the minor loop gain $T_m = Z_{rest}/Z_{out}$ can be used to evaluate the system stability, as well as to derive the output impedance specification for a stable dc current distribution system design. The impedance $Z_{rest}$ is a combination of cable impedances and closed-loop input impedances of the SRCs. The input impedances of the SRCs can be calculated from (5.34) based on the small-signal model derived in Chapter 4. The impedance $Z_{rest}$ can then be calculated from (5.24) and input impedances of the SRCs with necessary iterations. With the calculated impedance $Z_{rest}$, according to the stability criterion, the output impedance specification of the shore-based dc current power supply can be developed to guide the control design. The system stability can then be evaluated accurately by plotting the Nyquist plot of the minor loop gain $T_m = Z_{rest}/Z_{out}$, as demonstrated in Section 5.4.

Based on the analysis presented in Section 5.5 for a system with multiple cables and multiple SRCs, the system impedance model shown in Fig. 6.2 can be simplified as shown in Fig. 6.3, where the shore-based dc current power supply is modeled by an ideal current source and its output impedance, and the rest of the system is modeled by the series combination of the closed-loop input impedances of the SRCs in the system.

In Fig. 6.3, the impedance $Z_{out}$ is the output impedance of the shore-based dc current power supply, and the impedance $Z_{rest}$ is the series combination of the closed-loop input impedances of the SRCs. By applying the stability analysis shown in Section 5.1 and 5.4, the
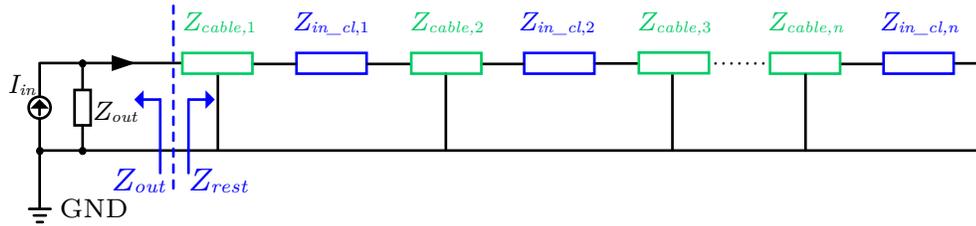
Fig. 6.2: Impedance model of the dc current distribution system for shore power supply stability evaluation.

output impedance specification of the shore-based dc current power supply can be derived for a stable dc current distribution system.

## 6.4 Operational Study of a Current Distribution System

In a dc current distribution system for subsea applications, as illustrated in Fig. 5.3, the shore-based power supply is controlled as a current source converter with a variable output voltage. The overall link voltage is controlled by the shore-based power supply to maintain a continuous link current at a desired value. The SRC modules in the system are connected in series through the trunk cables, which is different from the dc voltage distribution architecture. The difference in the system architecture also introduces challenges to the operation of the entire system.

If the circuit of SRC with constant current input shown in Fig. 3.1 is directly employed as the SRC module in Fig. 5.3, the entire system cannot operate because the MOSFETs in the primary bridge are enhancement type MOSFETs which are normally open. Since the SRC modules are connected in series, as shown in Fig. 5.3, open state of the MOSFETs means that the main trunk cable is open. One possible solution would be to provide an auxiliary supply separate from the trunk cable to supply power to the auxiliary circuits of the SRC modules. However, in such a long distance dc current distribution system for undersea applications, it is impractical with the consideration of cost, voltage drop and system reliability. Hence, the auxiliary power for the SRC module is provided by the trunk cable, which requires a continuous current flow through the trunk cable in order to deliver auxiliary power to the SRCs. In this case, a closed circuit path for the trunk cable current
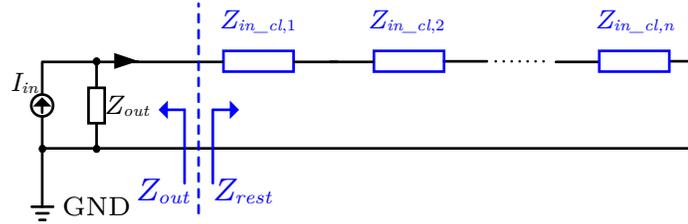
Fig. 6.3: Simplified impedance model of the dc current distribution system for shore power supply stability evaluation.

is required at startup.

The proposed circuit diagram in this work is illustrated in Fig. 6.4. In Fig. 6.4, the MOSFET $Q_5$ is a depletion type MOSFET and $r$ is the current sensing resistor in that branch. This bypass branch in the SRC modules, which is $Q_5$ in series with $r$ in the solid green box in Fig. 6.4, and the submarine cable in the system provide a continuous path for the main trunk current even before any SRC module in the system is energized. The depletion type MOSFET $Q_5$ needs to be selected to be capable of handling the power dissipation during startup and shutdown of SRC modules.

### 6.4.1 Startup Sequence

Based on the above analysis, a three-step startup technique for system operation is proposed in this section, as shown in Fig. 6.5.

For the startup, the first step is to turn on the shore power supply and provide the desired distribution current to the rest of the system, which is used to power all the auxiliary power supplies of each SRC. When the auxiliary power supply is on, a certain amount of time delay is required before taking the next action in order to ensure that all the auxiliary power supplies in the system are turned on.

The second step is to pass the trunk current from the bypass branch to the SRC input. In this step, the SRC operates at 180° phase shift in open loop mode, which provides minimum output current to the load. The bypass branch current controller ramps down the current flow through the bypass branch from full trunk current to 0. The ramp time and the load of the SRC at 180° phase shift determines how much energy is dissipated in
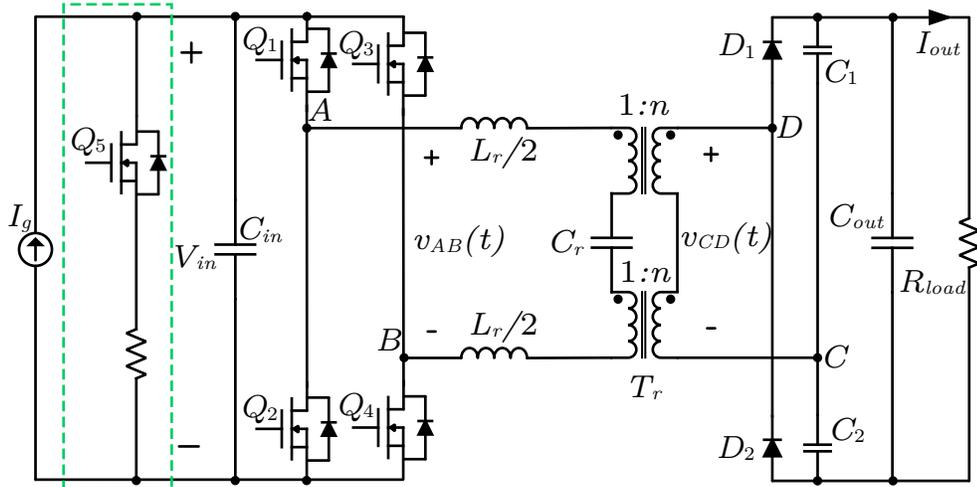
Fig. 6.4: Proposed circuit for the SRC with constant input current employed in a dc current distribution system.
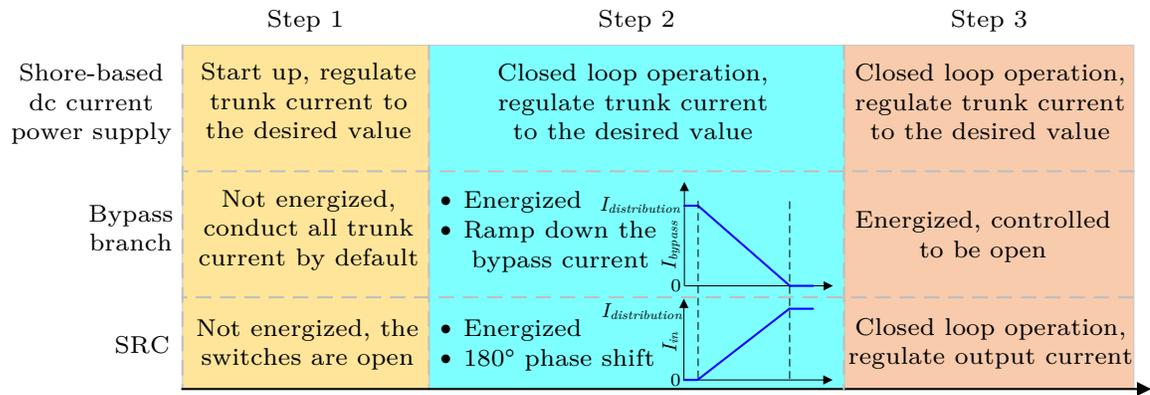


Fig. 6.5: The block diagram of the three-step startup technique for a dc current distribution system.

the bypass branch during the startup. The SRC modules in the system can do this at the same time or in a sequence. The second step is completed once the full trunk current flows through the SRC instead of the bypass branch.

The third step is to enable the SRC to start regulating its output current and to close the feedback control loop. In this step, the shore power supply is regulating the distribution current, and the bypass branch is controlled to behave as an open circuit switch. When the third step is finished, the system goes into normal operation mode.

### 6.4.2 Shutdown Sequence

For the shutdown, the scenario is similar. The block diagram of the proposed three-step shutdown technique is illustrated in Fig. 6.6.

As shown in Fig. 6.6, the first step is to open the feedback loop of the SRC, and have it operates in open loop mode. The phase shift angle $\alpha$ is then ramped up to $180°$ from the value it has. The shore power supply and the bypass branch are working normally in this step.

The second step is to bypass the trunk current from the SRC input to the bypass branch. In this step, the SRC operates at $180°$ phase shift in open loop mode, which provides minimum output current to the load. The bypass branch current controller ramps up the current flow through the bypass branch from 0 to full trunk current. The ramp time and the load of the SRC at $180°$ phase shift determines how much energy is dissipated in the bypass branch during the shutdown. The SRC modules in the system can do this at the same time or in a sequence. For the shutdown, the phase shift ramp up in step one and the bypass branch current ramp up can be done simultaneously or in a sequence. The second step is completed once the full trunk current flows through the bypass branch instead of the SRC.

The third step is to turn off the shore power supply, which will also turn off the auxiliary power supplies of each SRC. The entire system is powered off when the third step is completed.

### 6.5 Protection of the SRC

For a dc current power distribution system for subsea application, the maintenance and the replacement of the SRC modules in the system are quite challenging after the system is installed. As a result, the requirements on reliability and life time of the system and the SRC modules used in the system are high. The protection techniques presented in this section are suitable for practical implementation to improve reliability and life of both dc current distribution systems and SRCs with constant input current. The two major fault
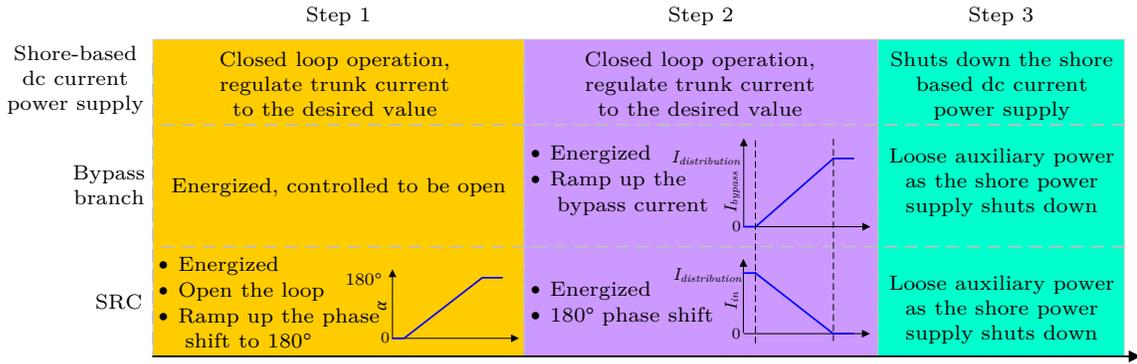
Fig. 6.6: The block diagram of the three-step shutdown technique for a dc current distribution system.

scenarios investigated in this section are output open circuit fault and output short circuit fault.

### 6.5.1 Series Resonant Capacitor Voltage Clamping Technique

As discussed in Section 2.5, the resonant capacitor clamping circuit presented in [107], as illustrated in Fig. 2.13, causes unavoidable circulating currents between the resonant tank and the input filter for phase shift modulation controlled SRC, as analyzed in Section 3.2.3. On the other hand, for the SRC with constant current input, the voltage across the resonant capacitor is higher than the input voltage for certain load range as presented in Section 3.2.2, which means that the protection approach shown in Fig. 2.13 cannot be used since it alters the steady state operation.

The proposed protection circuit is illustrated in the dashed blue box in Fig. 6.7. As shown in Fig. 6.7, the resonant capacitor voltage is clamped to the voltage of a floating capacitor $C$, which holds the peak voltage across the resonant capacitor regardless of the relation between the resonant capacitor voltage and the input voltage. In Fig. 6.7, $R$ is a bleed resistor in parallel with the floating capacitor $C$. During steady state, since the floating capacitor holds the resonant capacitor peak voltage, no current flows through the clamping diodes $(D_3 - D_6)$ expect for a small current to feed the bleed resistor $R$.

For the SRC without a protection circuit, the energy stored in the input capacitor $C_{in}$
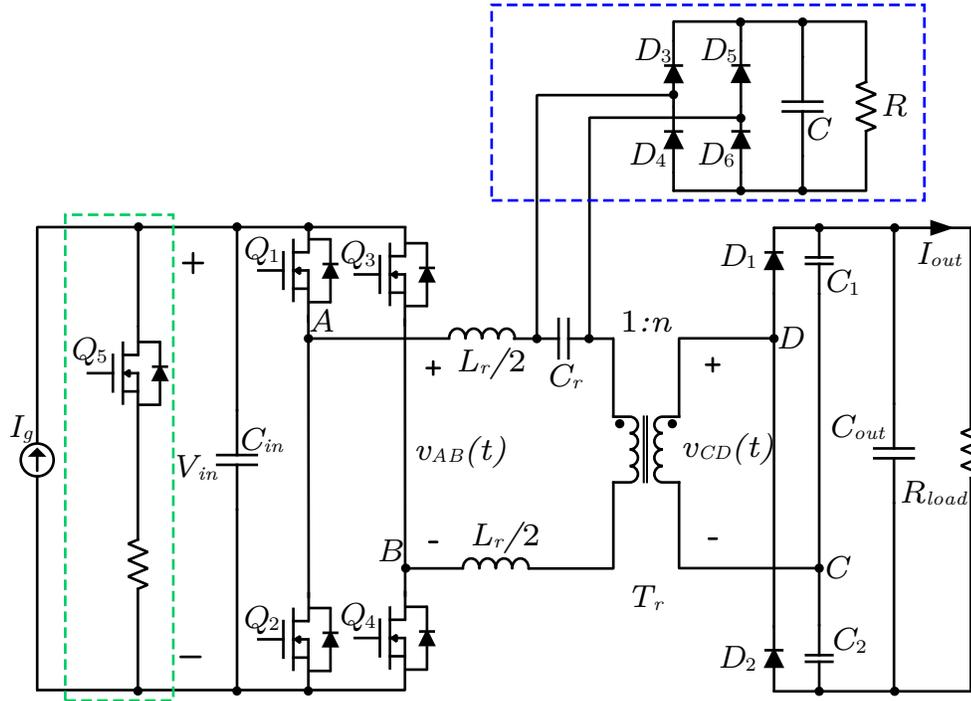
Fig. 6.7: The proposed protection circuit for clamping the resonant capacitor voltage of the SRC with constant input current.

is transferred to the resonant tank during an output short circuit fault transient. With the protection circuit shown in Fig. 6.7, the energy stored in the input capacitor $C_{in}$ is transferred to the resonant tank and the floating capacitor $C$. In this case, during fault transients, the voltage across the resonant capacitor can be well limited to protect the converter.

The energy stored on a capacitor is calculated from

$$E = \frac{1}{2}CV^2. \tag{6.1}$$

Hence the energy stored in those three capacitors before the fault happens can be expressed as

$$E_{C_{in}} = \frac{1}{2}C_{in}V_{in}^2, \tag{6.2}$$

$$E_{C_r} = \frac{1}{2}C_r V_r^2, \tag{6.3}$$

$$E_C = \frac{1}{2}CV_C^2, \tag{6.4}$$

where $V_{in}$ is the dc input voltage, $V_{C_r}$ is the peak voltage of the resonant capacitor $C_r$, and $V_C$ is the peak voltage of the floating capacitor $C$, which equals to $V_{C_r}$.

From (6.3)-(6.4), the total energy stored on resonant capacitor $C_r$ and the floating capacitor $C$ is

$$E_{C_r} + E_C = \frac{1}{2}(C_r + C)V_r^2. \tag{6.5}$$

During an output short circuit fault transient, the energy stored in the input capacitor $C_{in}$ is transferred to the resonant tank and the floating capacitor $C$. Hence, the total energy $E_{total}$ stored on $C_r$ and $C$ becomes

$$E_{total} = E_{C_r} + E_C + E_{C_{in}} = \frac{1}{2}(C_r + C)V_r^2 + \frac{1}{2}C_{in}V_{in}^2. \tag{6.6}$$

With the energy transferred from the input capacitor $C_{in}$, the voltage across the resonant capacitor and floating capacitor increases by

$$\Delta V = \sqrt{V_{C_r}^2 + \frac{C_{in}V_{in}^2}{C_r + C}} - V_{C_r}. \tag{6.7}$$

From (6.7), the floating capacitor required for limiting the voltage across the resonant capacitor to a certain voltage increment $\Delta V$ can be derived as

$$C = \frac{C_{in}V_{in}^2}{(V_{C_r} + \Delta V)^2 - V_{C_r}^2} - C_r. \tag{6.8}$$

### 6.5.2 Additional Techniques

For output short-circuit fault, the resulting large surge output current may damage the current sensing circuit if resistive current sensing is employed. From reliability aspect, it is
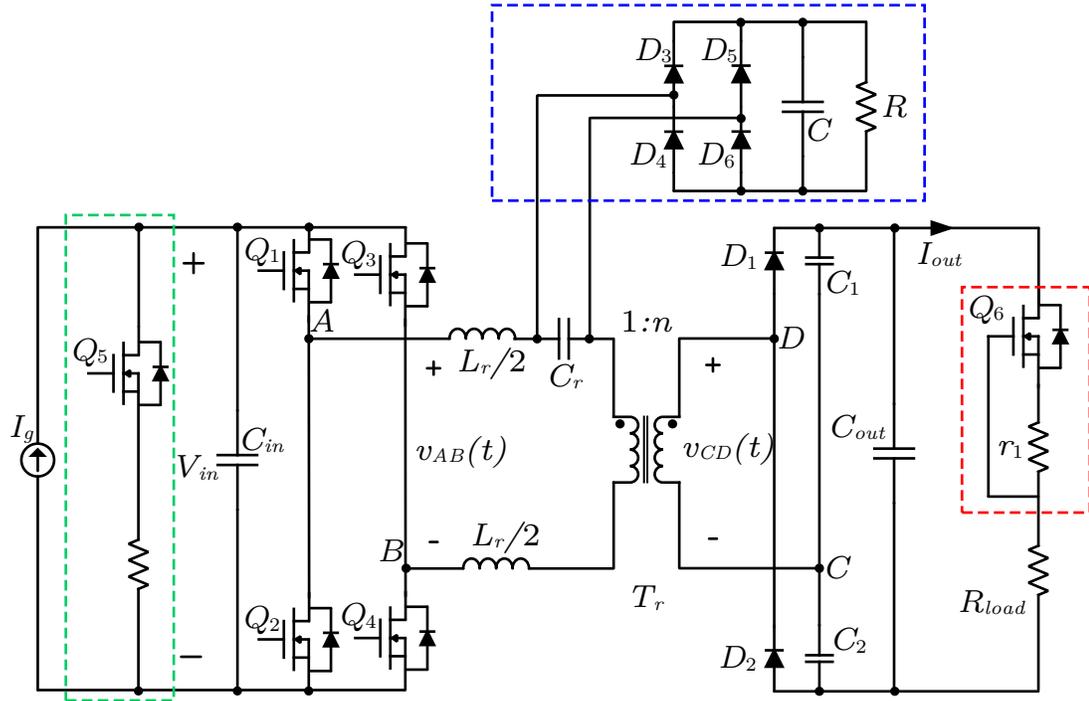
Fig. 6.8: The proposed protection circuit for output current limiting of the SRC with constant input current.

preferred to have an output current limiting circuit for protection, especially for low output current, high output voltage applications. The proposed output current limiting circuit is illustrated in the dotted red box in Fig. 6.8. In Fig. 6.8, $Q_6$ is a depletion type MOSFET and $r_1$ is the feedback resistor. As shown in Fig. 6.8, the negative voltage from $r_1$ is applied to the gate terminal of $Q_6$ to control the equivalent resistance presented by $Q_6$, since $Q_6$ operates in the linear region. The proposed current limiting circuit does not require any active drive or auxiliary circuits. The current limiting circuit does introduce additional power loss during the normal operation because of the low output current that flows the high on-resistance of the depletion type MOSFET. In this work, the current limiting circuit introduces an additional 20 $\Omega$ resistance that consumes 2 W during normal operation, which is negligible compared with 1 kW output power.

For the dc current distribution system, the module that has fault needs to be bypassed in order to keep the rest of the system operating. As discussed earlier, the capacitance of the

submarine cable is significantly high due to its parameters and length. Since the modules are connected in series, bypass of one module means discharging the cable capacitance in its forward current path. In this case, uncontrolled cable discharging may result in large current through other SRC modules in the system, and finally cause the entire system shutdown. To guarantee the normal operation of the complete system, a two-level fault response strategy is proposed in this work. The first level is to disable the gate signals of the primary switches, and the second level is to use the bypass branch to control the discharging of the cable to make sure that the distribution current stay within the range.

## 6.6  FPGA Implementation

An FPGA based controller for the SRC with constant input current has been developed based on the control analysis and design from previous sections. Implemented on a Xilinx SPARTAN-6 FPGA device and coded in Verilog Hardware Design Language (Verilog HDL), the controller implements a number of control functions to achieve a stable and reliable behavior. The FPGA used has a 100 MHz system clock which is increased to 300 MHz using a clock manager PLL. The converter switching frequency is set by stepping down the 300 MHz clock to 250 kHz, and allows for 11 bit resolution for the phase shift modulation. The 3.3 ns timing resolution when using the 300 MHz clock with 11 bit phase shift resolution means that a maximum error of 0.083% is introduced into phase control angles by the phase shift modulator. All sensing are done with 12 bits of precision and internal computations on sensed variables are performed with 12 bit resolution.

### 6.6.1  System Startup and Shutdown

The block diagram of the startup and shutdown module implemented in the FPGA is illustrated in Fig. 6.9. In Fig. 6.9, the blue signals are the input signals to the module, the green signals are the output signals to other modules, and the light blue ones are the internal signals and registers. The module is driven by a ramp clock generated from the 300 MHz clock. The ramping speed is determined by both the ramp clock and the ramp step.
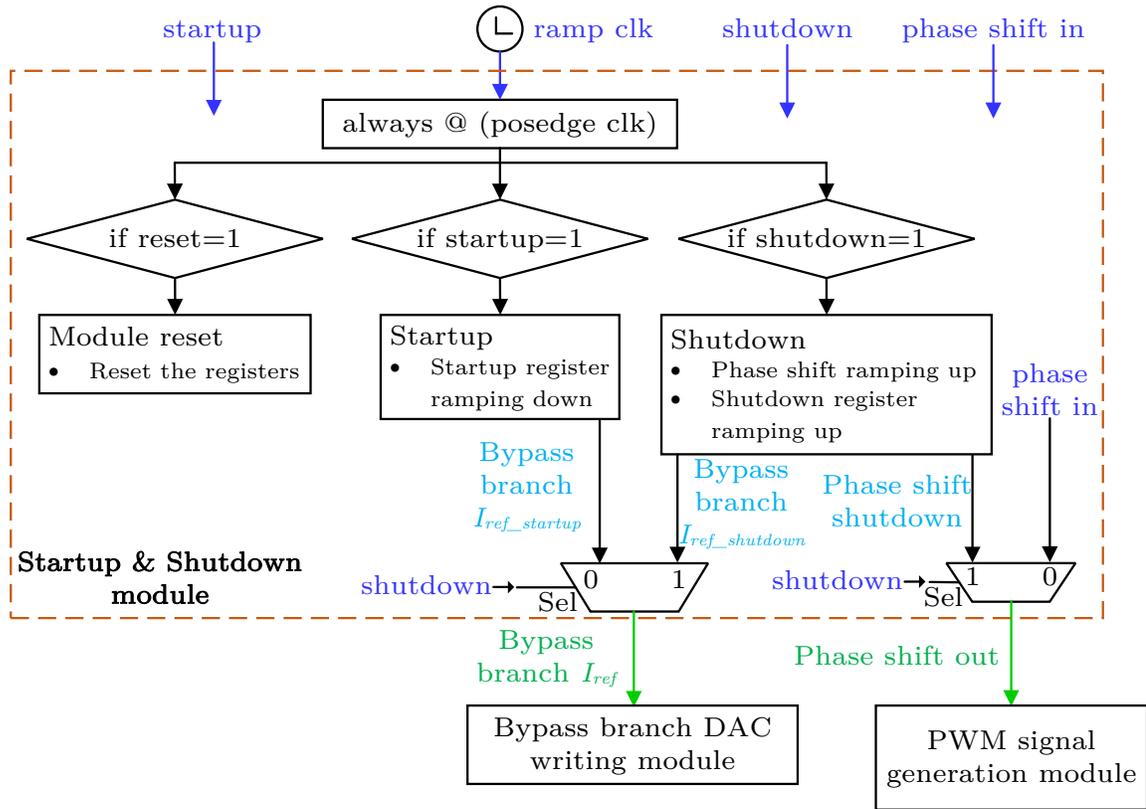
Fig. 6.9: Block diagram of startup and shutdown module implementation.

### 6.6.2 Integral Controller Design

The digital integral controller used for output current regulation of the SRC with constant dc input current is implemented as a direct form I controller as shown in Fig. 6.10. The sensed output current is subtracted from the reference current to get the signed error signal. A signed multiplier with two twelve bit inputs is used ot multiply the controller error signal by gain $K_a$. The resulting 24 bit number is extended with 12 bits of zeros and then shifted by $K_b$ bits in order to complete the full gain multiplication. This result is then downsized with saturation to 24 bits before summed with the previous state. This summation is done by extending each input by a single bit, and saturating the result back down to 24 bits. This result is stored as the previous state every switching clock cycle, and is threshold limited to 367. The upper 12 bits of this result is then subtracted from 599, which means 180° phase shift. The result is then used as the new command variable which

is connected to the PWM generation module in order to generate new phase shift angles for the SRC.

### 6.6.3   Implementation of Synchronous Rectification

For the secondary bridge in the SRC, diodes are generally used as the switching devices to reduce the control complexity and obtain unity power factor operation. However, diodes gives higher conduction loss in most of the applications compared with the scenario with MOSFETs, because of the forward voltage drop. In order to have lower loss and keep the unity power factor operation feature, MOSFETs are generally used in the secondary H-bridge and synchronous rectification (SR) technique is applied. The first step of the SR is to generate a square waveform signal from the transformer secondary current based on its polarity. The generated square waveform is sent to FPGA, where the SR module generates the gate signals with certain deadtime based on the input square waveform signal.

This section presents the implementation of the synchronous rectification in the FPGA by using case statements. The SR signal has two states, 0 and 1, which means that 1 bit is required to represent its state. In order to generate deadtime, timers are needed for the on-time and off-time duration timing. The different states of the on-timer and off-timer for 250 kHz operation with 300 MHz clock signal and maximum 100 ns deadtime are tabulated in TABLE 6.1. From TABLE 6.1, it can be seen that the on-timer and off-timer has 4 states, respectively. In hence, 2 bits are required to represent the on-timer states, and 2 bits are required to represent the off-timer states. As a result, a 5 bits register is required to represent all the possible combinations of the SR signal, on-timer and off-timer state for the SR implementation.

With the 5 bits register, 32 possible states are there. For the SR implementation in the FPGA, the next step is to list out the actions for each state. Several different states may end up with the same actions. A set of if statements are used to generate the state for case statement based on status of the SR signal, and value of the on-timer and off-timer as illustrated in Fig. 6.11. Based on the generated state, case statements are employed to implement the SR function as shown in Fig 6.12.
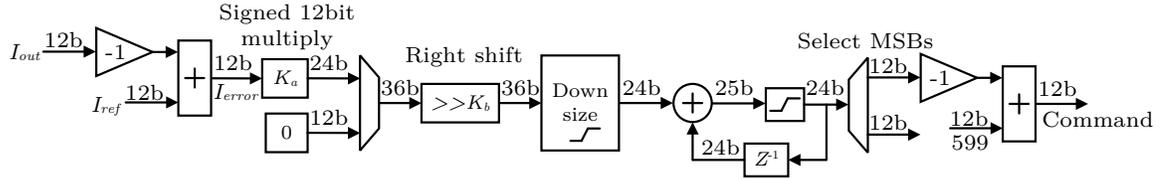
Fig. 6.10: Direct Form I implementation of the output current feedback controller in FPGA.

Table 6.1: STATES OF THE ON-TIMER AND OFF-TIMER FOR SR

| States | On-timer | Off-timer |
|:------:|:--------:|:---------:|
| 1 | On-timer=0 | Off-timer=0 |
| 2 | 0<On-timer<540 | 0<Off-timer<540 |
| 3 | 540≤On-timer≤660 | 540≤Off-timer≤660 |
| 4 | On-timer>660 | Off-timer>660 |

State[4] <= SR_In;
if (off_timer == 10'd0) State[3:2] <= 2'b00;
if ((off_timer > 10'd0) && (off_timer < 10'd540)) State[3:2] <= 2'b01;
if ((off_timer >= 10'd540) && (off_timer <= 10'd660)) State[3:2] <= 2'b10;
if (off_timer > 10'd660) State[3:2] <= 2'b11;
if (on_timer == 10'd0) State[1:0] <= 2'b00;
if ((on_timer > 10'd0) && (on_timer < 10'd540)) State[1:0] <= 2'b01;
if ((on_timer >= 10'd540) && (on_timer <= 10'd660)) State[1:0] <= 2'b10;
if (on_timer > 10'd660) State[1:0] <= 2'b11;

Fig. 6.11: If statements used to generate the state for case statements based on status of the SR signal, and value of the on-timer and off-timer.

### 6.6.4 Protection Implementation

The SRC has two levels of protections, which are hardware protection and software protection. For the hardware protection, the fault signals are generated by the comparators on the PCB board. The fault signals include input over-voltage, input over-current, output over-voltage and output over-current. The two input fault signals are used to generate one primary fault signal using AND logic gate, as well as the two output fault signals. The primary and secondary fault signals are then taken to the FPGA. In the FPGA, the fault signals are filtered and then latched. Only the fault signals that last longer than 2 $\mu$s are considered as a real fault. The software protection is implemented in the FPGA based on

```verilog
always @ (posedge clk)  begin
case (State)
    5'b00000,5'b00001,5'b01000,5'b01001: begin
            on_timer <= on_timer +1;
            out_HI <= 1'b1;
            off_timer <= 10'd0;
            end
    5'b00010,5'b01010: begin
            on_timer <= on_timer +1;
            out_HI <= 1'b0;
            off_timer <= 10'd0;
            end
    5'b00011,5'b01011: begin
            out_HI <= 1'b0;
            off_timer <= 10'd0;
            end
    5'b00100,5'b00101,5'b00110,5'b01101,5'b01110: begin
            on_timer <= on_timer +1;
            out_HI <= 1'b0;
            off_timer <= 10'd1;
            end
    5'b00111,5'b01111: begin
            out_HI <= 1'b0;
            off_timer <= 10'd1;
            end
    5'b10000,5'b10100,5'b10010,5'b10110: begin
            off_timer <= off_timer +1;
            out_LO <= 1'b1;
            on_timer <= 10'd0;
            end
    5'b11000,5'b11010: begin
            off_timer <= off_timer +1;
            out_LO <= 1'b0;
            on_timer <= 10'd0;
            end
    5'b11100,5'b11110: begin
            out_LO <= 1'b0;
            on_timer <= 10'd0;
            end
    5'b10001,5'b10101,5'b11001,5'b10011,5'b10111,5'b11011: begin
            off_timer <= off_timer +1;
            out_LO <= 1'b0;
            on_timer <= 10'd1;
            end
    5'b11100,5'b11110: begin
            out_LO <= 1'b0;
            on_timer <= 10'd1;
            end
endcase
```

Fig. 6.12: Case statements coded to implement the SR function.

the ADC readings. The fault response is only triggered when ten continuous ADC readings are higher than the protection threshold.

After a fault is detected, the gate signals to the four switches in the primary H-bridge are disabled, and the current reference of the bypass branch is set to control the discharging of the cable to make sure that the distribution current stay within the range to maintain normal operation of the entire system. The fault response part is implemented in the FPGA through hardwired networks, which means that it barely have delay, and can have very quick response to the faults.

## 6.7    Summary

This chapter investigates the design and implementation of control and protection for both the SRCs with constant input current and the entire system. The control strategy and controller design for the SRC are presented based on the analysis shown in Section 5.1 and 5.4, with a focus on the stability of the dc current distribution system. On top of that, the design and output impedance requirements of the shore-based dc current power supply are discussed based on the analysis presented in Section 5.5. The operation of a dc current distribution system, including startup and normal shutdown sequences, is studied and discussed for normal operation of the system. Different protection techniques are presented and implemented to protect the SRCs, and to increase the reliability of the SRCs. All the control and protection presented in this work are implemented on a Xilinx SPARTAN-6 FPGA device, the implementation of which are described in detail in this chapter.

CHAPTER 7

SIMULATION AND EXPERIMENTAL RESULTS

This chapter presents simulation results, prototype hardware designs and experimental results to validate the proposed analysis, design, modeling, control and protection of the SRCs with dc constant input current for dc current power distribution applications.

Section 7.1 presents the hardware prototypes and experimental results to verify the analysis and design of an SRC with dc constant niput current. A 400 kHz, 500 W hardware prototype of the SRC with non-zero minimum output power has been built and tested to validate the output characteristics of the converter. A 250 kHz, 1 kW SRC prototype with 1 A input current, 0.33 A output current and natural current source behavior has been developed to demonstrate the proposed design and analysis. In addition, LTSpice simulation results have been used to validate the experimental measurements based high voltage transformer model. Hardware experiments have also been conducted on the prototype to verify the proposed design optimization of the SRC. In Section 7.2, simulation results based on the Matlab/PLECS full switching level simulation by using white noise injection technique are provided to verify the expressions derived from the small signal modeling of the SRC, for both constant voltage input and constant scenarios. Section 7.3 presents the developed cable emulator and hardware results to demonstrate the proposed stability analysis and control design for the dc current distribution system. The cable emulator that has been built is used to emulate a 100 km submarine cable. Section 2.5 provides the experimental results conducted on a scaled down version of the dc current distribution system that has been developed with the cable emulators and the SRC prototypes to show the proposed system operation and SRC protection techniques. The chapter summary is given in Section 7.5.

## 7.1 Design of the SRC with Constant Input Current

### 7.1.1 The SRC with Non-Zero Minimum Output Power

A 400 kHz, 450 W SRC with a 1 A constant input current and 330 mA output current has been built with the parameters listed in TABLE 3.4. Phase-shift modulation is employed as the driving scheme for the SRC. The SiC MOSFETs are driven by transformer isolated gate drivers with +18V/-5V pulses and 100 ns dead-band between top and bottom gate pulses of the same leg.

The hardware setup of the SRC is shown in Fig. 7.1. With 1 A input current, $85°$ phase shift and 4120 $\Omega$ load resistance (full load), the SRC provides an output power of 450 W at 330 mA output current with an efficiency of 95%. The oscilloscope waveforms of the signals in the converter at this operating point are shown in Fig. 7.2. The loss distribution in the converter under this operating condition is plotted in Fig. 7.3. Zero voltage switching (ZVS) of the MOSFETs in the primary bridge is implemented through passive ZVS assistance with an inductor of 40 $\mu$H. The detailed analysis on ZVS can be found in [125]. In Fig. 7.3, the MOSFETs are the primary bridge MOSFETs, while the diodes are the secondary voltage doubler diodes.

In order to demonstrate the feasibility of the designed converter, hardware experiments are conducted on the designed SRC with 1 A input current and 4120 $\Omega$ load resistance to regulate the output current. The theoretical and experimental results of output current versus phase shift angle with 1 A input current and 4120 $\Omega$ load resistance are illustrated in Fig. 7.4. From Fig. 7.4, the experimental results verify the theoretical results and the steady state analysis presented in Section 3.1.1.

Hardware experiments are also conducted for load resistance variation with 1 A input current and fixed phase shift angle of $180°$ in order to validate that the output power decreases while the load resistance decreases if the load resistance $R_{load}$ is greater than $\frac{n^2\pi^2 Z_o}{2}|F - \frac{1}{F}|$, and output power increases while the load resistance decreases if $R_{load}$ is less than $\frac{n^2\pi^2 Z_o}{2}|F - \frac{1}{F}|$. The comparison of analytical and experimental results of output power versus load resistance with 1 A input current and $180°$ phase shift are shown in Fig. 7.5.
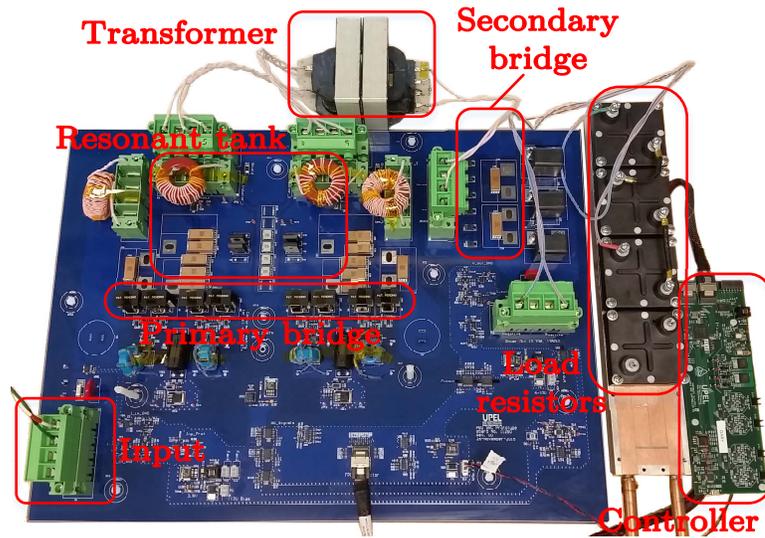
Fig. 7.1: Photograph of the hardware.
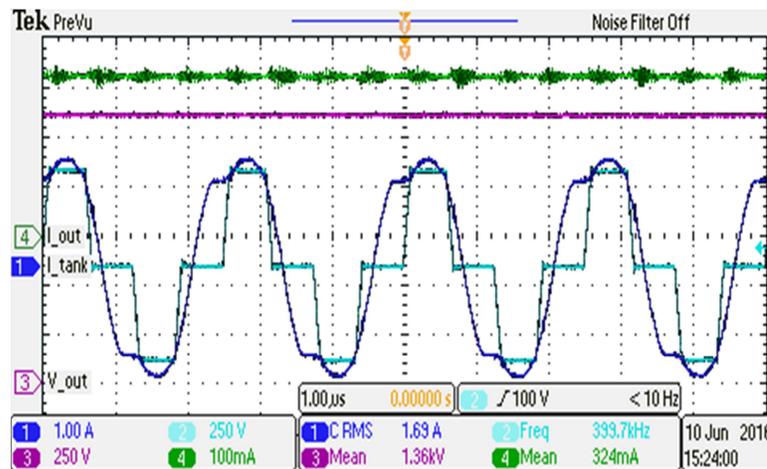


Fig. 7.2: Oscilloscope waveforms of the signals in the converter at nominal operating point. The green trace (CH4) is the output current, the purple trace (CH3) is the output voltage, the light blue trace (CH2) is the active full bridge output voltage, and the blue trace (CH1) is the resonant inductor current.

The experimental efficiency of the SRC with 1 A input current and 330 mA regulated output current at different loads is presented in Fig. 7.6, where it has an efficiency of 95% at full load and an efficiency of 83% at 50 W load (11% load).

In order to validate the green solid rectangular region of the design depicted in Fig. 3.16, experiments were conducted at each of the design corners. The oscilloscope waveforms of the
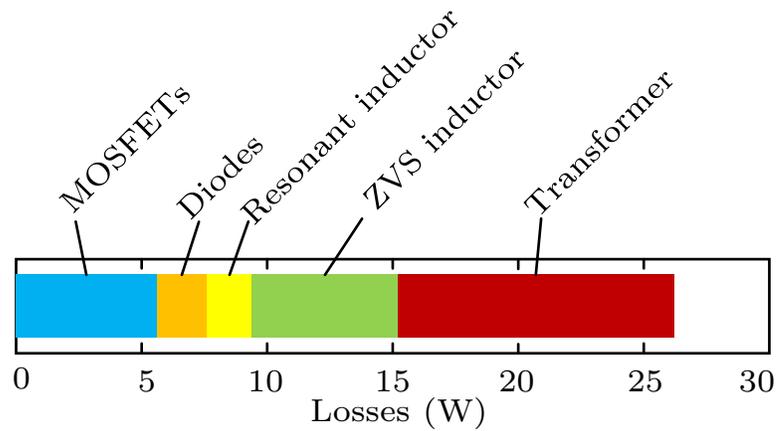
Fig. 7.3: Distribution of the losses within the SRC.
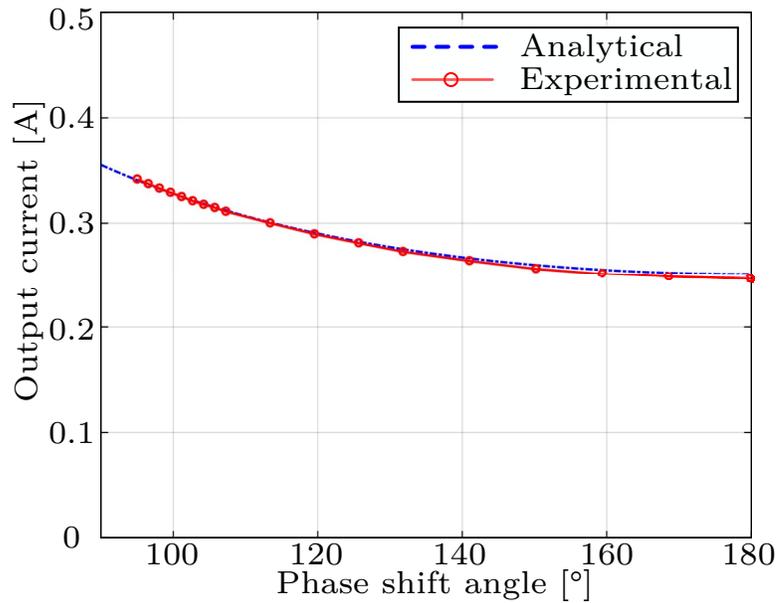


Fig. 7.4: Analytical and experimental results of output current versus phase shift angle with 1 A input current and 4120 Ω load resistance (full load).

signals in the converter at the corners are shown in Fig. 7.7. From Fig. 7.7, it can be seen that the minimum output current of the SRC is lower than 0.33 A, and the resonant capacitor voltage is lower than 600 V, with 450 Ω minimum load resistance and ±5% variation in the values of resonant components, which matches the design goals from Fig. 3.16.
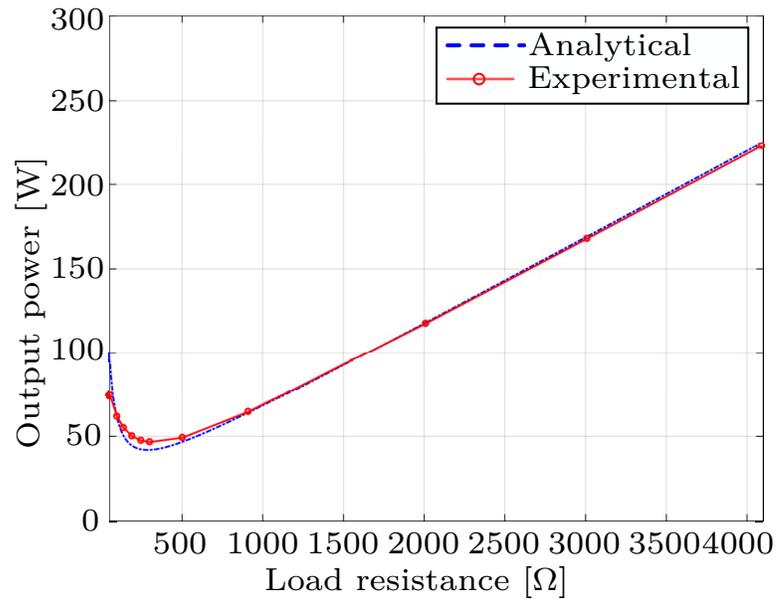
Fig. 7.5: Analytical and experimental results of output power versus load resistance with 1 A input current and 180° phase shift.
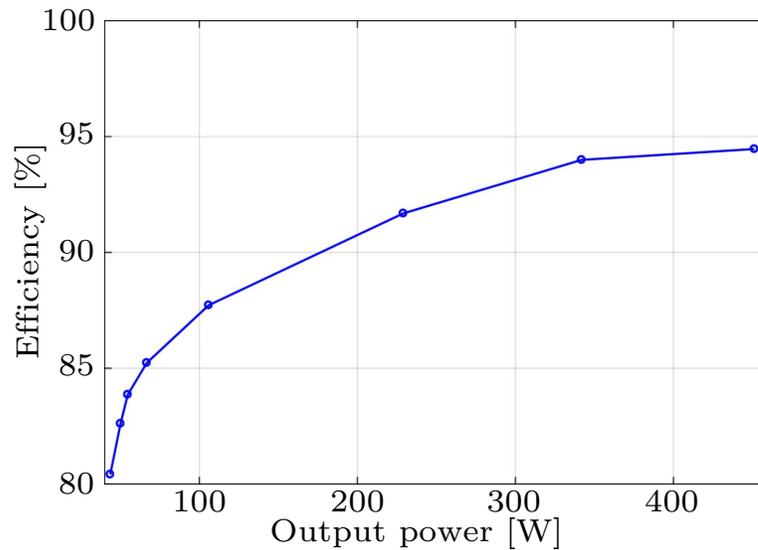


Fig. 7.6: Experimental results of converter efficiency versus output power with 330 mA regulated output current.

### 7.1.2 Validation of the High Voltage Transformer Model

To verify the high voltage transformer model presented in Section 3.5, LTSpice is employed to run simulations with the parameters listed in TABLE 3.3. The comparison
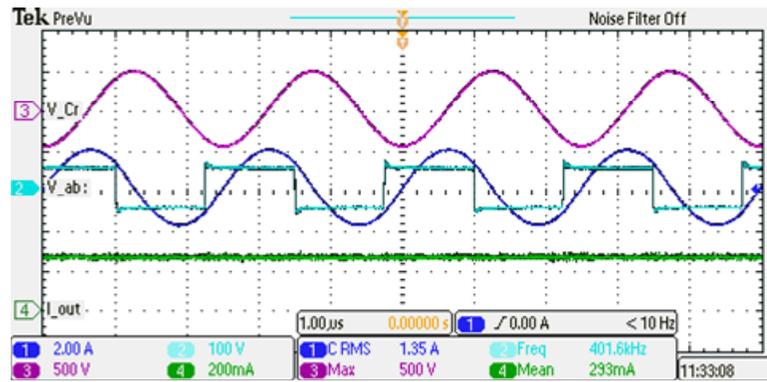
(a)
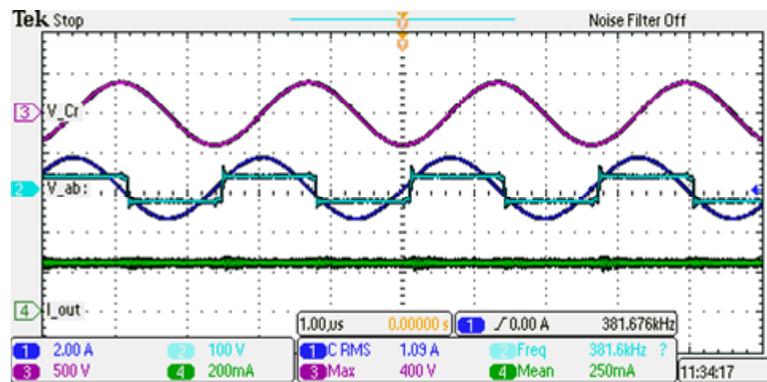


(b)

Fig. 7.7: Oscilloscope waveforms of the signals in the converter at the corners of Fig. 3.16 design. (a) Operating at the right corner, (b) operating at the left corner. The green trace (CH4) is the output current, the purple trace (CH3) is the resonant capacitor voltage, the light blue trace (CH2) is the active full bridge output voltage, and the blue trace (CH1) is the resonant inductor current.

between the hardware results and simulation results are illustrated in Fig. 7.8. In these experiments, the transformer is driven by a 100 V, 400 kHz square waveform on the primary side, or equivalently by a 200 V, 400 kHz square waveform on the secondary side.

In Fig. 7.8, (a) presents the comparison between the hardware results and simulation results of driving from primary side, while (b) illustrates the comparison of driving from secondary side. From Fig. 7.8, it can be seen that the simulation results match the hardware result pretty well, which validates the high voltage transformer model.

In order to verify the model, LTSpice simulations are run for the whole SRC system with the transformer model included. The primary bridge output voltage and resonant current
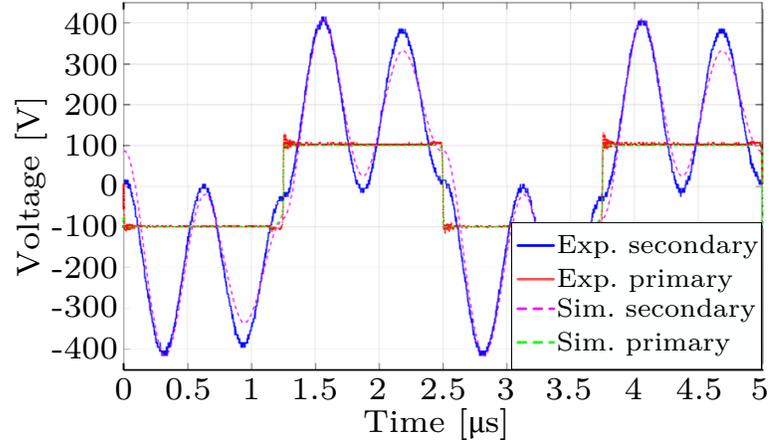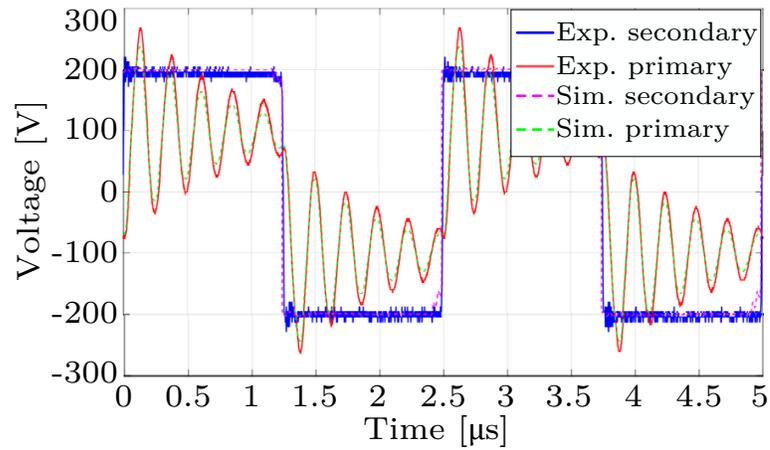
Fig. 7.8: Comparison between the hardware results and simulation results of the high voltage transformer model. (a) The transformer is driven by a 100 V, 400 kHz square waveform on the primary side. (b) The transformer is driven by a 200 V, 400 kHz square waveform on the secondary side.

waveforms are compared between hardware and simulation results. For the comparison, the conditions are: $L_r$ is 60 $\mu$H, $C_r$ is 1.6 nF, $f_s$ is 400 kHz, phase angle is 85°, output current is 0.33 A, load resistance is 4125 $\Omega$, output power is 500 W, the ZVS inductor for leg A is 38 $\mu$H, and without ZVS inductor for leg B. The comparison between hardware and simulation results are illustrated in Fig. 7.9.

In Fig. 7.9, the top figure is the primary bridge output voltage, while the bottom figure is the resonant inductor current. The deviation in the bridge output voltage is introduced
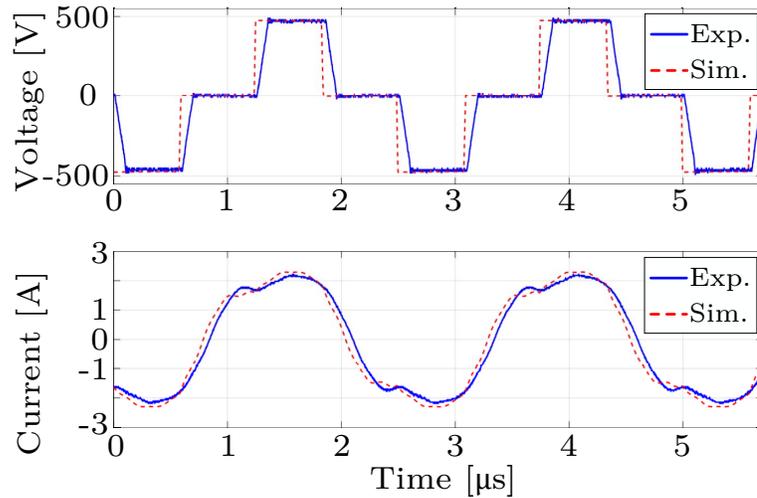
Fig. 7.9: Comparison of simulation and hardware results of the SRC operating at 400 kHz, 1 A input current, 0.33 A output current, and 500 W output power.

by different ZVS behaviors in the hardware and simulation. In the simulation, the model of switching devices are not for the ones used in the hardware. From the bottom figure, it can be seen that the resonant inductor current simulated from the model matches the hardware result well.

### 7.1.3  Design Optimization of the SRC

The waveforms of the converter operating at $f_s$=$f_o$=380 kHz is shown in Fig. 7.10. It can be seen that the resonant tank current leads the H-bridge output voltage, as predicted in Fig. 3.24. The waveforms of the converter operating at $f_s$=$f_o$=250 kHz are shown in Fig. 7.11, where it can be seen that the resonant tank current is almost in phase with the H-bridge output voltage, as designed.

The experimental measured ratio between resonant tank rms current and input dc current versus load resistance for 380 kHz and 250 kHz switching frequency are illustrated in Fig. 7.12. From Fig. 7.12, it can be seen that the ratio is approximately constant over the entire load range for 250 kHz operation, while there is a large variation for 380 kHz operation. Compared with 380 kHz operation, 250 kHz operation has lower tank rms current for the same input and output operating conditions.
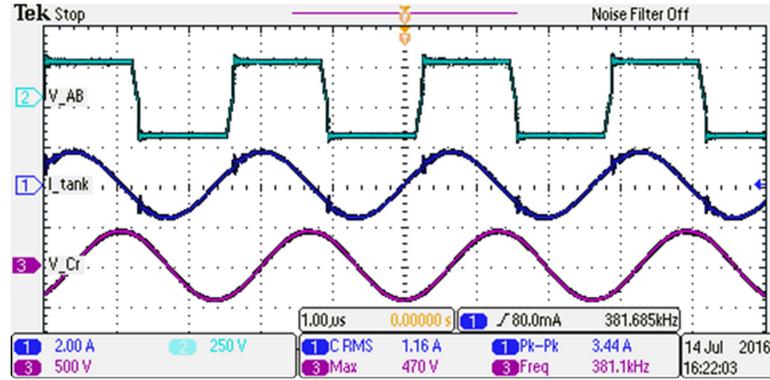
Fig. 7.10: Experimental waveform at $f_s=f_o=380$ kHz. From top to bottom: H-bridge output voltage, resonant tank current and resonant capacitor voltage.
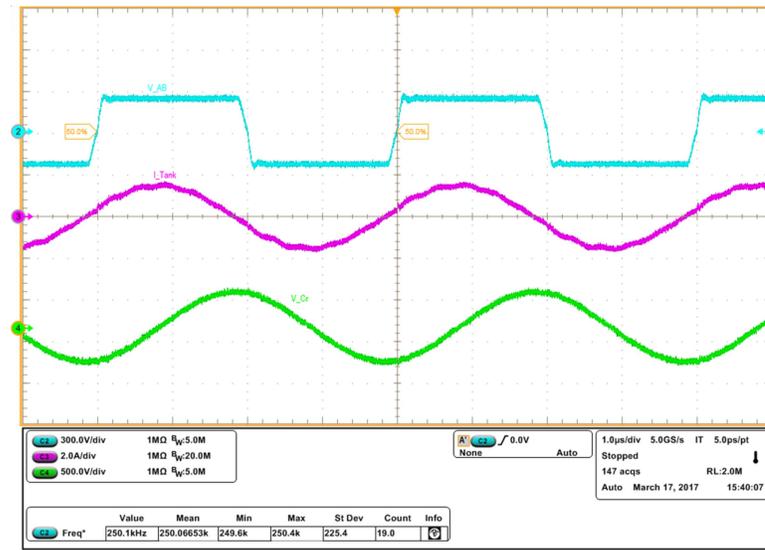


Fig. 7.11: Experimental waveform at $f_s=f_o=250$ kHz. From top to bottom: H-bridge output voltage, resonant tank current and resonant capacitor voltage.

### 7.1.4   The SRC with Natural Current Source Behavior

A laboratory prototype of the SRC with 1 A constant input current, regulated 0.33 A output current, 1 kW full output power and the parameters listed in TABLE 3.5 has been built and tested. The photograph of the hardware prototype is illustrated in Fig. 7.13. Passive ZVS assistance technique with a 120 $\mu$H inductor is employed to archive ZVS operation for the SRC. The SRC has an efficiency of 94% at 1 kW output power and 0.33 A regulated output current.
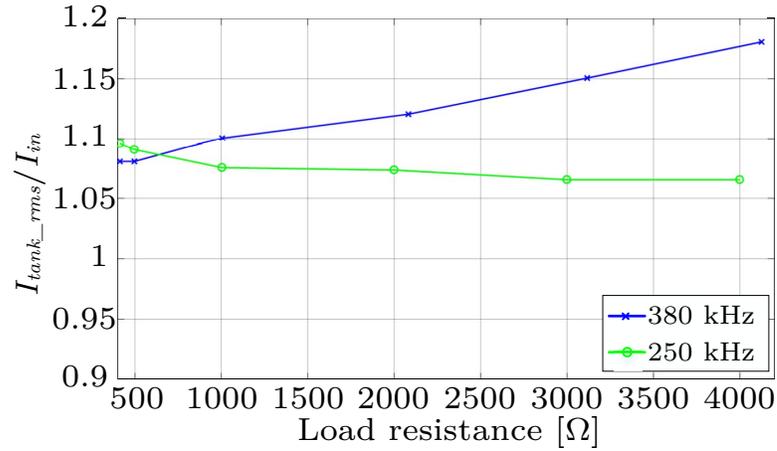
Fig. 7.12: Measured resonant tank rms current to input dc current ratio for 10% to 100% $R_{load}$ variation at different frequencies. Blue:380 kHz operation; Green:250 kHz operation.
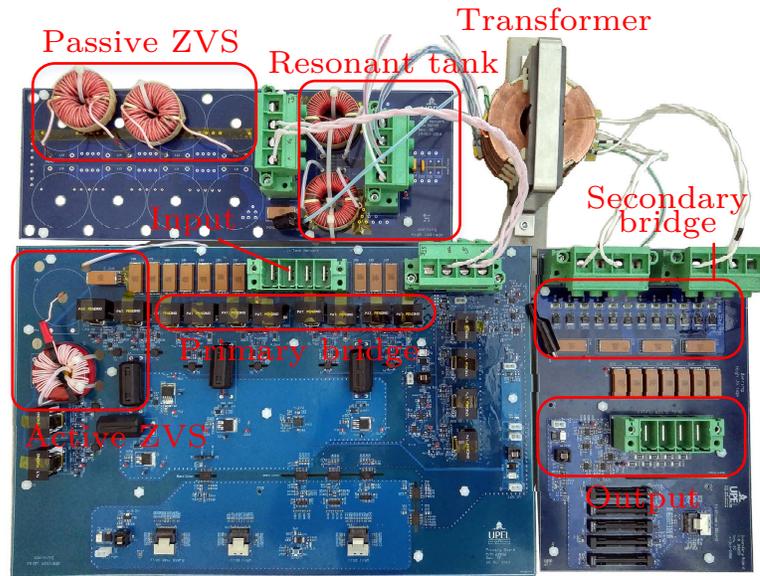


Fig. 7.13: Photograph of the 1 kW SRC prototype.

With 1 A input current, 180° phase shift and short circuit output, the SRC provides an output current of 0.258 A with 1.5 A resonant inductor peak current and 430 V resonant capacitor peak voltage. The oscilloscope waveforms of the signals in the converter are shown in Fig. 7.14(a). With 1 A input current, 180° phase shift and half load resistance, the SRC provides an output current of 0.242 A with 1.6 A resonant inductor peak current and 470 V resonant capacitor peak voltage. The oscilloscope waveforms of the signals in the converter are shown in Fig. 7.14(b). Under the above operating conditions, according to (3.97) and
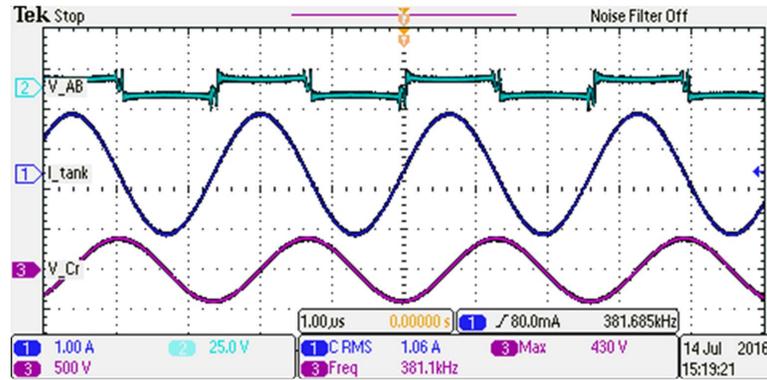
(a)
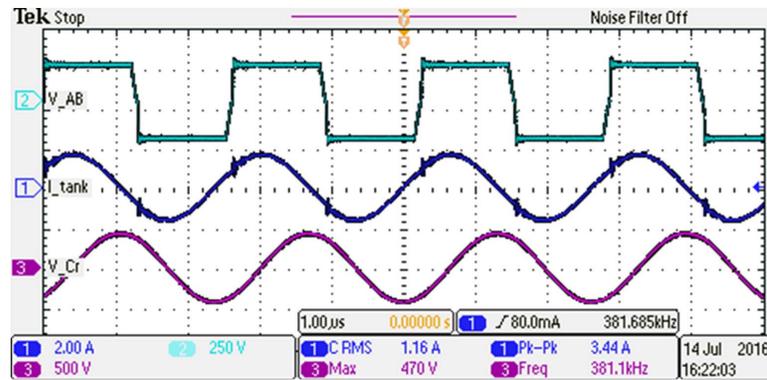


(b)

Fig. 7.14: Oscilloscope waveforms of the signals in the converter. (a) 1 A input current, 180°
phase shift, short circuit load. (b) 1 A input current, 180° phase shift, half load resistance
load. The blue trace (CH1) is the resonant current, the light blue trace (CH2) is the primary
side bridge output voltage, and the purple trace (CH3) is the resonant capacitor voltage.

(3.98), the theoretical resonant inductor peak current is constant 1.57 A and the resonant
capacitor peak voltage is constant at 397 V. From Fig. 7.14, the resonant inductor current
and resonant capacitor voltage amplitudes are seen to be approximately constant over the
full load range, in agreement with the theoretical results. The slight increase is due to the
decrease of the quality factor $Q$ while the load increases from short circuit to full load, which
results in higher harmonic components in the resonant tank waveforms. The oscilloscope
waveforms of the signals in the converter at full load operating point (0.33 A output current,
1 kW output power) are illustrated in Fig. 7.15.

The open-loop output characteristics of the SRC with 180° phase shift and regulated
output characteristics are illustrated in Fig. 7.16. The load is varied from short circuit
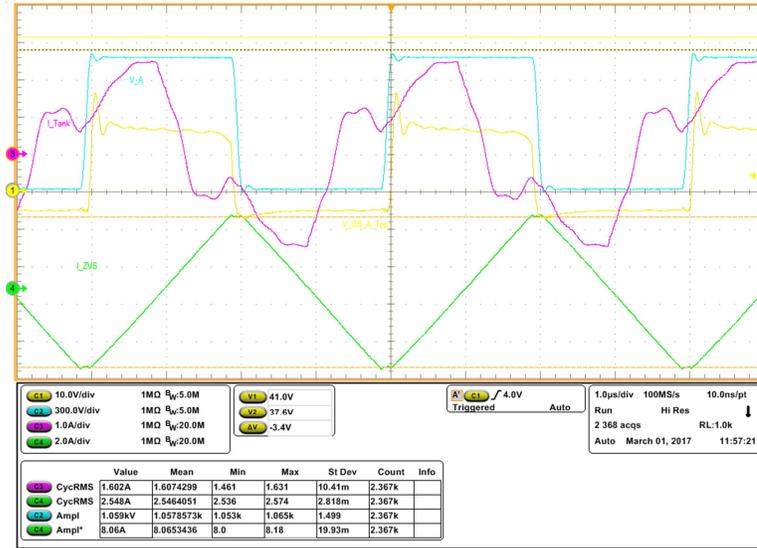
Fig. 7.15: Oscilloscope waveforms of the signals in the converter at full load. The yellow trace (CH1) is the gate to source voltage of Leg A top MOSFET, the light blue trace (CH2) is the switch node voltage of Leg A, the purple trace (CH3) is the resonant inductor current, and the green trace (CH4) is the ZVS inductor current.
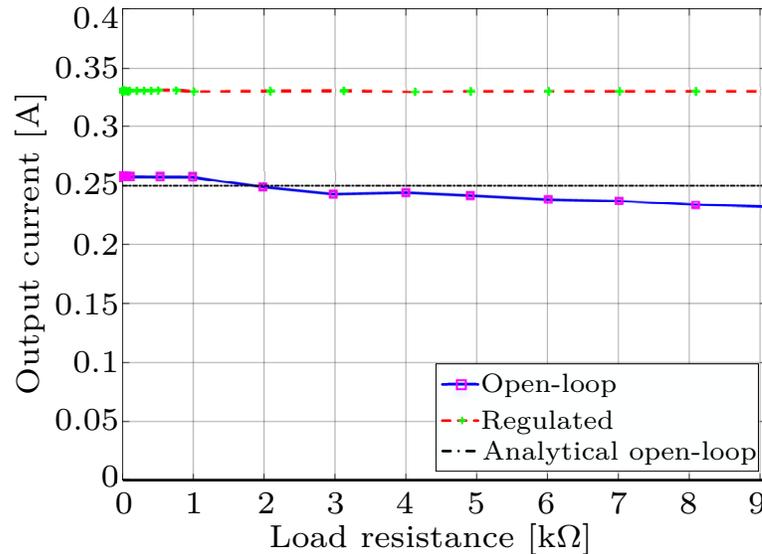


Fig. 7.16: Output characteristics of the SRC prototype. Open-loop: $180°$ phase shift. Regulated: phase shift angle ranges from $109°$ (short circuit) to $79°$ (full load).

to full load. In open-loop operation, compared with analytical results 0.25 A, the output current is seen to be approximately constant at 0.25 A. From Fig. 7.16, it can be seen that the output current is independent from the load resistance, which validates the analysis
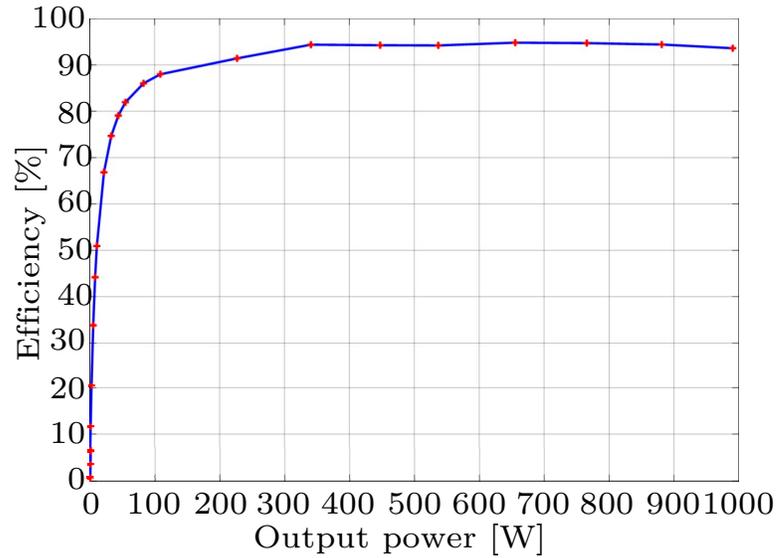
Fig. 7.17: Efficiency of the SRC prototype with 1 A input current and 0.33 A regulated output current from short circuit to full load (1 kW).

and design proposed in Section 3.4.2 and 3.7.2. The slight droop in the characteristics is due to the increase in losses in the input bridge, resonant tank and transformer. For the regulated operation, phase shift modulation control is applied, and the output current can be regulated to 0.33 A with 109° to 79° range of phase shift angle for the load varying from short circuit to full load.

The measured experimental efficiency versus output power for the load varies from short circuit (0 W) to full load (1 kW) is shown in Fig. 7.17. From Fig. 7.17, one can see that the SRC has an efficiency of 94% at full load, an efficiency of over 90% for the load range of 5:1 and an efficiency of over 80% for the load range of 20:1.

## 7.2 Modeling of the SRC

In order to verify the small signal models and transfer functions derived in Chapter 4, simulations are run for an SRC with constant voltage input and an SRC with constant current input. For the simulations, the white noise injection technique combined with Matlab/PLECS switching level simulation are used to generate the transfer functions.

In the simulation, the Band-Limited White Noise block is used for the white noise

injection. The sample time of the block is set to be 4 $\mu$s. The To Workspace block is used to sample the injection and the output response in the simulations. The sample time of the To Workspace block is 4 $\mu$s. The sampled input and output data is then analyzed in Matlab to generate the transfer functions.

First, a Matlab function "iddata($y$,$u$,$T_s$)" is used to combine the sampled input and output data together and generates an iddata object. The "iddata($y$,$u$,$T_s$)" function creates an iddata object containing a time-domain output signal $y$ and input signal $u$, respectively. $T_s$ specifies the sample time of the experimental data. Then, the generated iddata object is sent to Matlab function "ssest(data)" to estimate the state-space model. The "ssest(data)" function estimates a state-space model using time- or frequency- domain data, "data". Finally, the estimated state-space model is sent to "tf(sys)" function to get its transfer function form. The "tf(sys)" function creates transfer function model, or converts the state-space models to transfer function form. The generated transfer function is then compared with the theoretical result.

### 7.2.1 Small Signal Model of SRC with Constant Input Voltage

For the SRC with constant voltage input, it operates at a steady state with 250 kHz switching frequency, 500 V input voltage, 120° phase shift angle and 1000 $\Omega$ load resistance. The white noise was injected to the input voltage and phase shift angle, respectively, to verify the derived transfer functions.

Based on the injection to the control phase shift angle $\alpha$, the transfer functions from control to output current and input current can be measured. The analytical and simulated results of control to output current transfer functions are shown in Fig. 7.18, while the results of control to input current transfer functions are shown in Fig. 7.19. With the injection to the input voltage, the transfer function from input voltage to output current and input current for the SRC with constant voltage input can be measured. The analytical and simulated results of input voltage to output current transfer functions are shown in Fig. 7.20, while the results of input voltage to input current transfer functions are presented in Fig. 7.21.

From Fig. 7.18, Fig. 7.19, Fig. 7.20 and Fig. 7.21, it can be seen that the theoretical
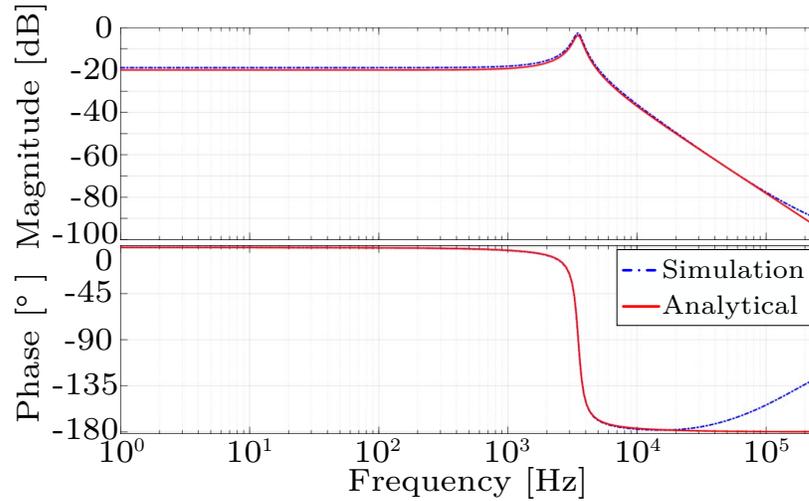
Fig. 7.18: Theoretical and simulated control to output current transfer function of SRC with constant voltage input and $\alpha=120°$.
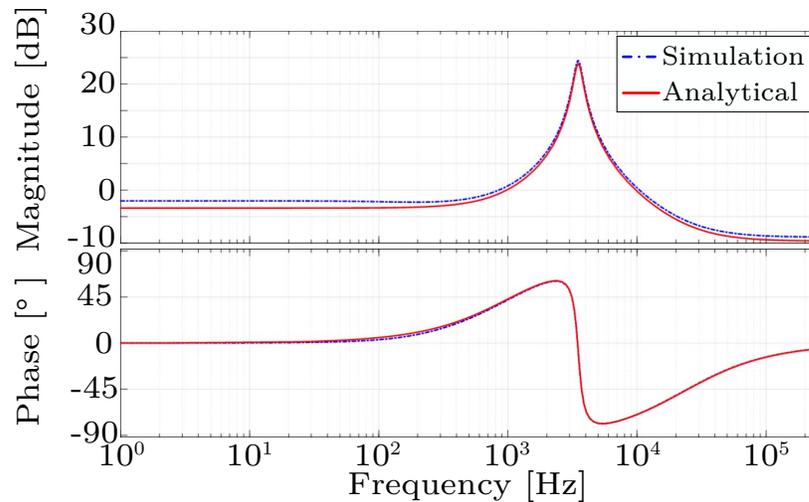


Fig. 7.19: Theoretical and simulated control to input current transfer function of SRC with constant voltage input and $\alpha=120°$.

transfer functions match the measured transfer functions through simulation pretty well, for the SRC with constant voltage input.

### 7.2.2   Small Signal Model of SRC with Constant Input Current

For the SRC with constant current input, the SRC operates at a steady state with 1 A input current, $107°$ phase shift angle and 0.33 A output current.

Based on the injection to the control phase shift angle $\alpha$, the transfer functions from
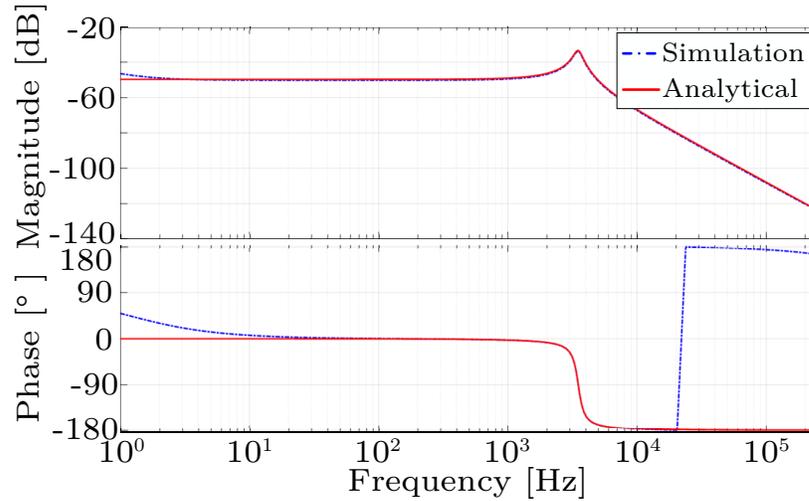
Fig. 7.20: Theoretical and simulated input voltage to output current transfer function of SRC with constant voltage input and $\alpha=120°$.
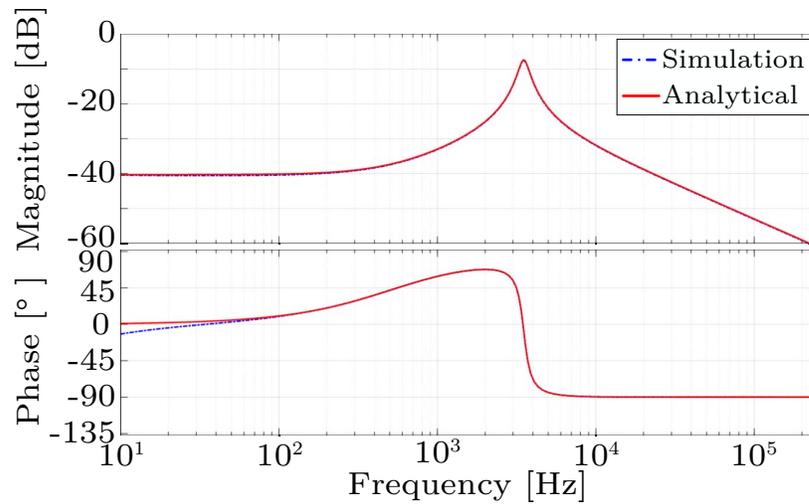


Fig. 7.21: Theoretical and simulated input voltage to input current transfer function of SRC with constant voltage input and $\alpha=120°$.

control to output current and input voltage can be measured for the SRC with constant input current. The analytical and simulated results of control to output current transfer functions are shown in Fig. 7.22, while the results of control to input voltage transfer functions are shown in Fig. 7.23.

With the injection to the input current, the transfer function from input current to output current and the input impedance for the SRC with constant current input can
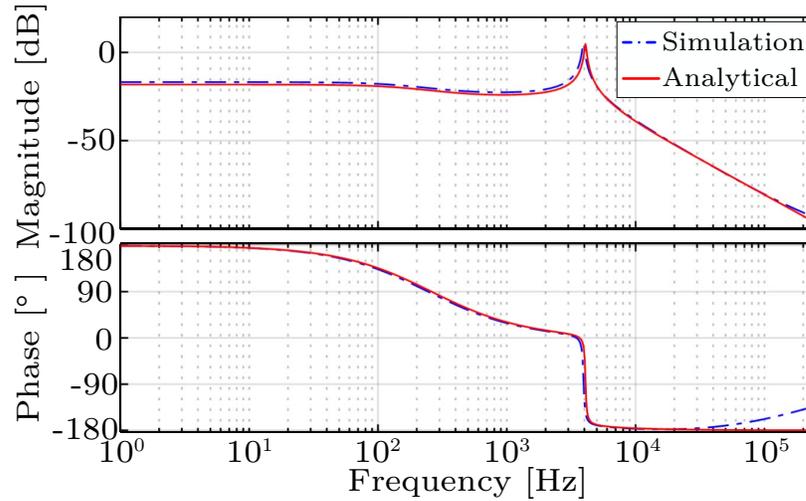
Fig. 7.22: Theoretical and simulated control to output current transfer function of SRC with 1 A constant current input, $\alpha=107°$ and 0.33 A output current.
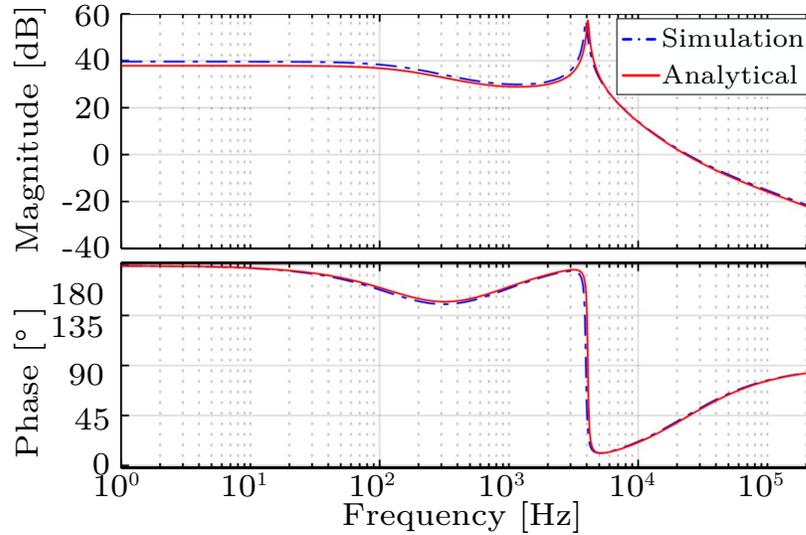


Fig. 7.23: Theoretical and simulated control to input voltage transfer function of SRC with 1 A constant current input, $\alpha=107°$ and 0.33 A output current.

be measured. The analytical and simulated results of control to output current transfer functions are shown in Fig. 7.24, while the results of input impedances are illustrated in Fig. 7.25.

From Fig. 7.22, Fig. 7.23, Fig. 7.24 and Fig. 7.25, it can be seen that the theoretical transfer functions and input impedance expression have a good match with the measured transfer functions and input impedance through simulation, for the SRC with constant
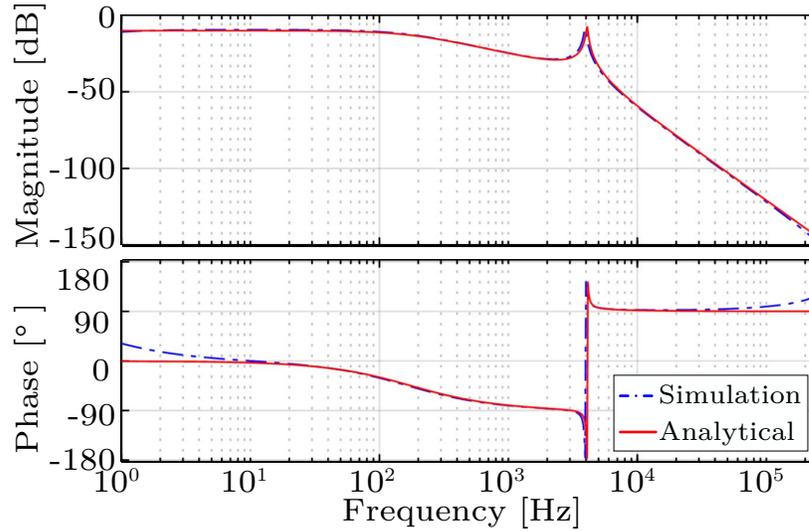
Fig. 7.24: Theoretical and simulated input current to output current transfer function of SRC with 1 A constant current input, $\alpha$=107° and 0.33 A output current.
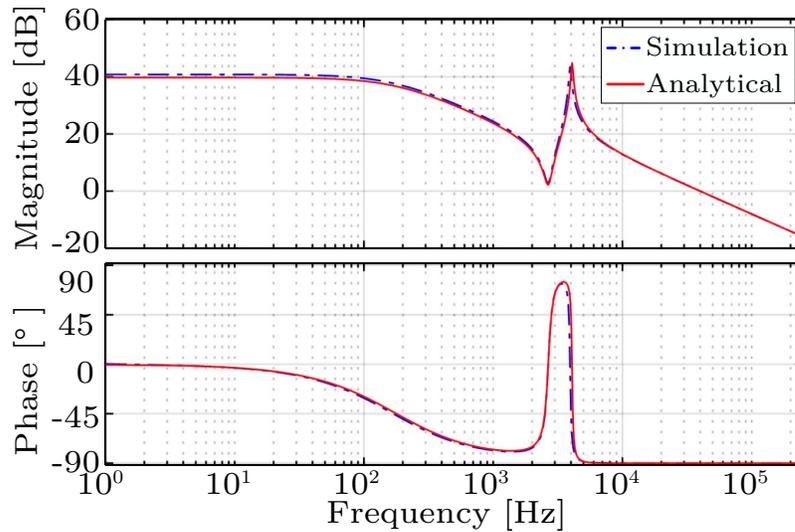


Fig. 7.25: Theoretical and simulated input impedance of SRC with 1 A constant current input, $\alpha$=107° and 0.33 A output current.

current input.

## 7.3  System Stability Analysis and Control

In order to validate the stability analysis and controller design considerations proposed in this dissertation, a 5 $\pi$-sections based cable emulator has been built to emulate the 100 km

submarine cable, and a 500 W SRC hardware prototype with 1 A input current and 0.33 A regulated output current has been built for the system demonstration.

### 7.3.1  Cable Modeling

The hardware photo of the developed cable emulator is shown in Fig. 7.26. The parameters of the cable are listed in TABLE 5.1. The impedance of the cable emulator is measured by the LCR meter Hioki IM3536. The measured and simulated impedance of the 100 km cable are illustrated in Fig. 7.27 and Fig. 7.28, where Fig. 7.27 is the cable impedance with the other terminal open, and Fig. 7.28 is the cable impedance with the other terminal short to ground. From Fig. 7.27 and Fig. 7.28, it can be seen that the developed cable emulator match the simulation results pretty well.

### 7.3.2  System with Two SRCs

As the first step, experiments are conducted in order to validate that the SRC module is stable individually. The SRC module is a 100 kHz, 500 W SRC with 1:1 transformer turns ratio, 200 $\mu$H resonant inductor, 34 nF resonant capacitor, 1 A input current and regulated output current. An integral type controller is employed to control the output current of the SRC, as illustrated in Fig. 6.1. The controller has been designed to have a bandwidth of 10 Hz, and digitally implemented using a Xilinx VIRTEX 5 FPGA.

Figure 7.29 shows the waveforms for the reference step down from 0.33 A to 0.2 A, where the blue trace (CH1) is the output current of the SRC module, the pink trace (CH3) is the input voltage and the green trace (CH4) is the output voltage. The load resistance used in this experiment is 1 k$\Omega$.

Figure 7.30 illustrates the hardware results for the load resistance step up from 700 $\Omega$ to 1 k$\Omega$, where the blue trace (CH1) is the output current of the SRC module, the pink trace (CH3) is the input voltage and the green trace (CH4) is the output voltage. The output current reference used in this test is 0.33 A.

From Fig. 7.29 and Fig. 7.30, the hardware results validate that the SRC module is stable individually by using the controller which has a crossover frequency lower than the
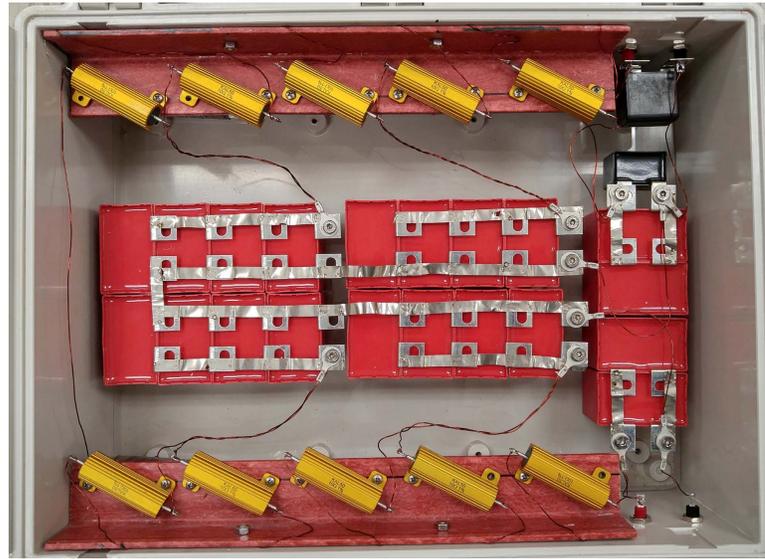
Fig. 7.26: Photograph of the cable emulator for a 100 km submarine cable.
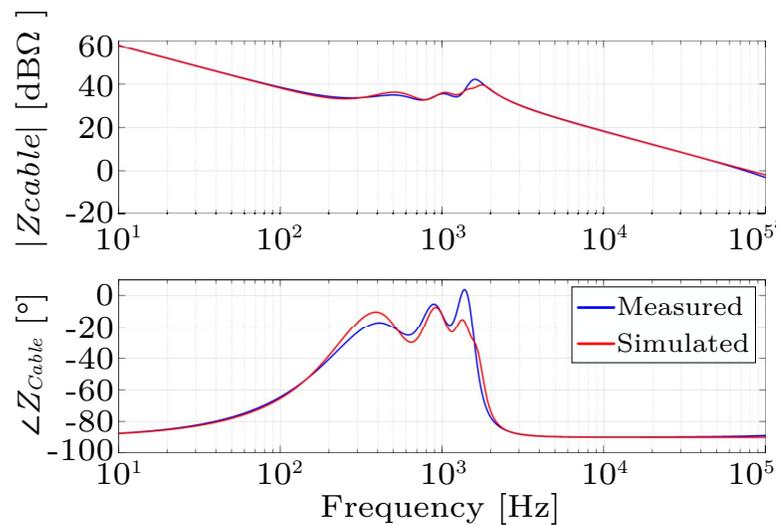


Fig. 7.27: The measured and simulated impedance of the 100 km cable emulator with the other terminal open.

source controller bandwidth.

The scenario investigated in this dissertation is constant current dc distribution in undersea applications with a single shore-based source and multiple loads distributed along the cable, as illustrated in Fig. 1.7. The hardware experiments are conducted to validate the proposed control approach on a system consisting of two 500 W SRC modules connected
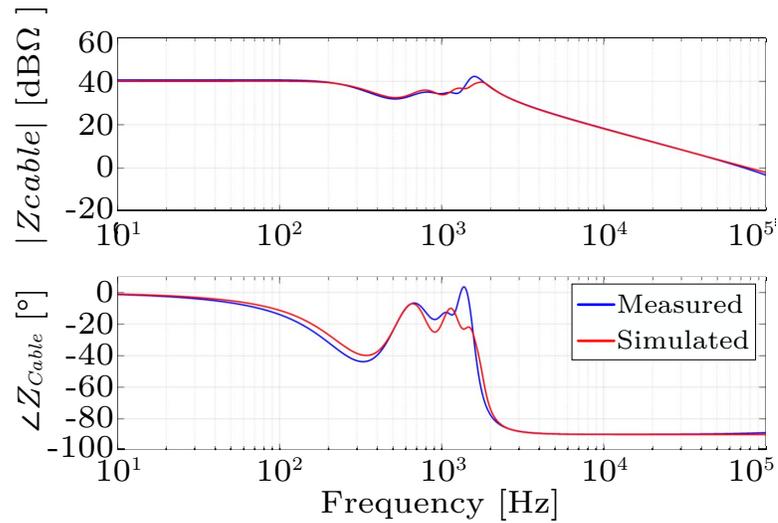
Fig. 7.28: The measured and simulated impedance of the 100 km cable emulator with the other terminal short to ground.
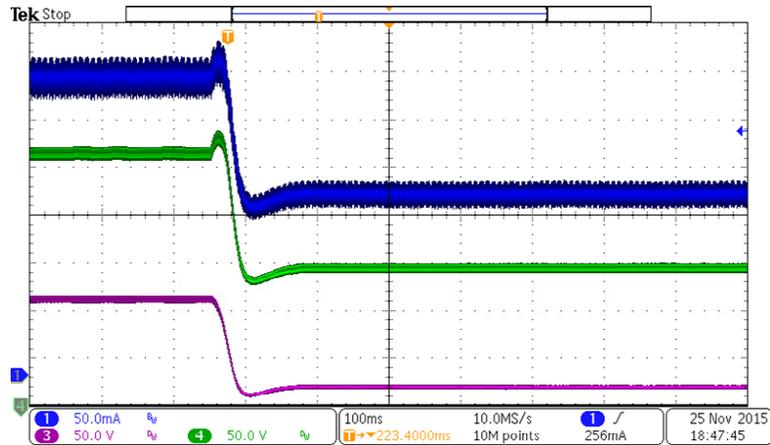


Fig. 7.29: Reference step down transition. From top to bottom are output current, output voltage and input voltage of the SRC module.

in series and fed with 1 A constant input current. The parameters of the SRC modules and details of the controller are listed above.

The experimental results are shown in Figs. 7.31-7.34, where the blue trace (CH1) is output current of SRC #1, the light blue trace (CH2) is input voltage of SRC #1, the pink trace (CH3) is output current of SRC #2 and the green trace (CH4) is input voltage of SRC #2.
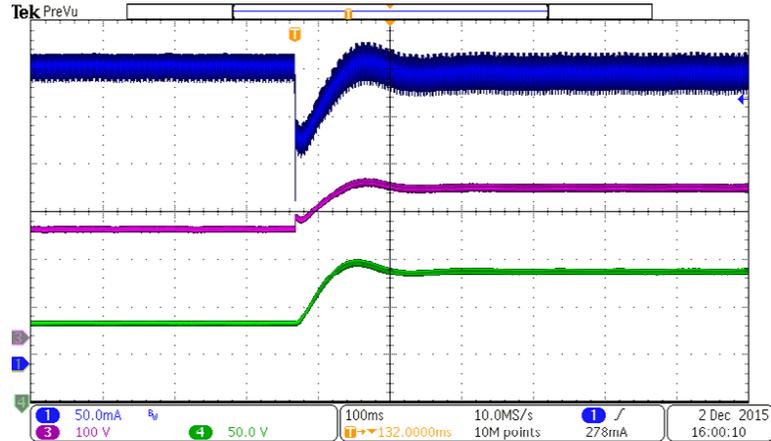
Fig. 7.30: Load step up transition. From top to bottom are output current, output voltage and input voltage of the SRC module.
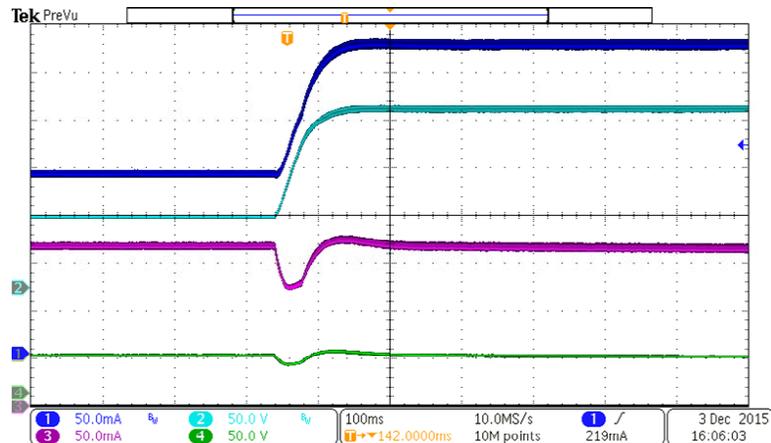


Fig. 7.31: Reference step up transients on SRC #1. From top to bottom are output current of SRC #1, input voltage of SRC #1, output current of SRC #2, and input voltage of SRC #2.

First, the system response for output current reference step change on SRC #1 is demonstrated. Fig. 7.31 shows the results for current reference of SRC #1 stepped up from 0.2 A to 0.33 A, while Fig. 7.32 shows the system response for current reference of SRC #1 stepped down from 0.33 A to 0.2 A. The load resistance for both SRC modules is 1 kΩ during this experiment. The output current reference of SRC #2 is set to be 0.2 A in order to show the capability of regulating the output current to different values for different modules.
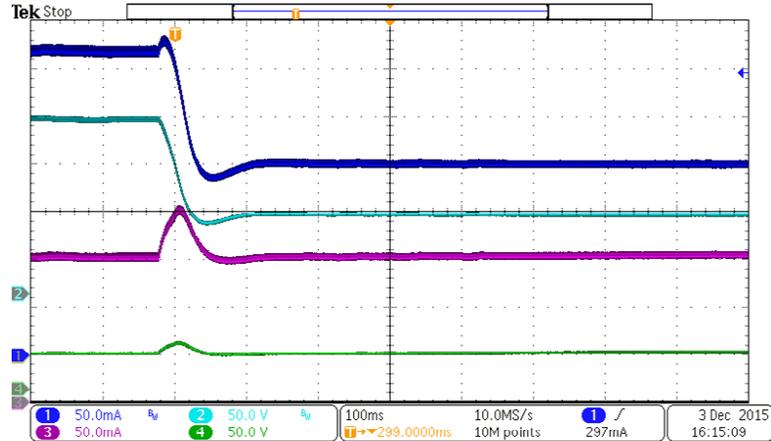
Fig. 7.32: Reference step down transients on SRC #1. From top to bottom are output current of SRC #1, input voltage of SRC #1, output current of SRC #2, and input voltage of SRC #2.
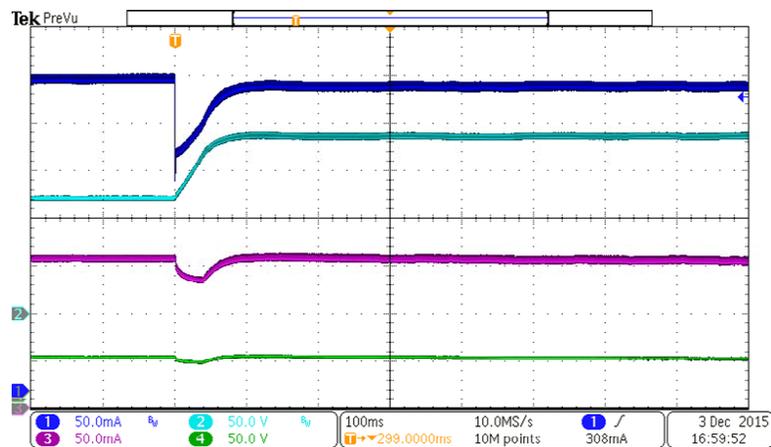


Fig. 7.33: Load step up transients on SRC #1. From top to bottom are output current of SRC #1, input voltage of SRC #1, output current of SRC #2, and input voltage of SRC #2.

Then, the experimental results for load step change on SRC #1 are shown. Fig. 7.33 shows the system response for SRC #1's load resistance stepped up from 700 Ω to 1 kΩ, while Fig. 7.34 shows the experimental results for SRC #1's load resistance stepped down from 1 kΩ to 700 Ω. The load resistance for SRC #2 is 1 kΩ during this test. The output current reference of SRC #1 is set to be 0.33 A, and the output current reference of SRC #2 is set to be 0.2A, for the same reason mentioned earlier .
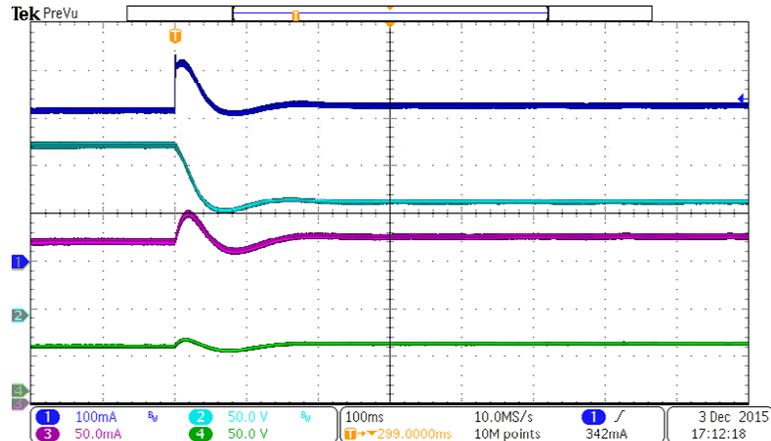
Fig. 7.34: Load step down transients on SRC #1. From top to bottom are output current of SRC #1, input voltage of SRC #1, output current of SRC #2, and input voltage of SRC #2.

From Fig. 7.31-7.34, it can be seen that the transient on SRC #1 introduces a small disturbance on SRC #2, which is expected since the current source is not ideal. The hardware results validated the control strategy proposed in this paper, which is that the SRC modules are controlled independently with no communications required among them, by having a controller crossover frequency lower than the source controller bandwidth.

### 7.3.3   System with One Cable and One SRC

The system architecture for the experiments is shown in Fig. 5.12, with the cable emulator illustrated in Fig. 7.26 and the SRC prototype shown in Fig. 7.13.

Hardware experiments are conducted on the system with the three different controller designs presented earlier to validate the proposed analysis and design considerations. The experimental results are shown in Fig. 7.35-7.37. In Fig. 7.35-7.37, the yellow trace (CH1) is SRC input voltage, the light blue trace (CH2) is SRC output voltage, the pink trace (CH3) is SRC input current, and the green trace (CH4) is SRC output current. From Fig. 7.35, it can be seen that the system is stable with the output current reference step up from 0.325 A to 0.335 A. From Fig. 7.36, it can be seen that the system becomes marginally stable when the output current reference step up from 0.33 A to 0.335 A. From Fig. 7.37,
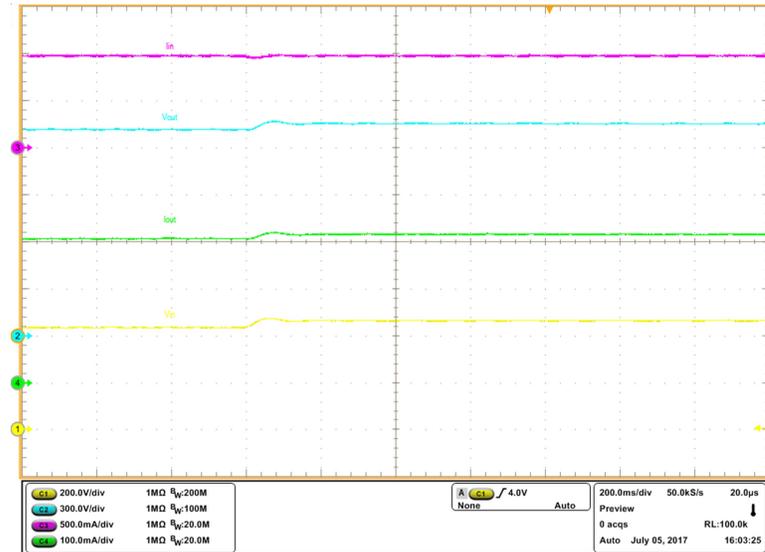
Fig. 7.35: Experimental results of reference step transient with the controller design 500/s, current reference jumps from 0.325 A to 0.335 A.
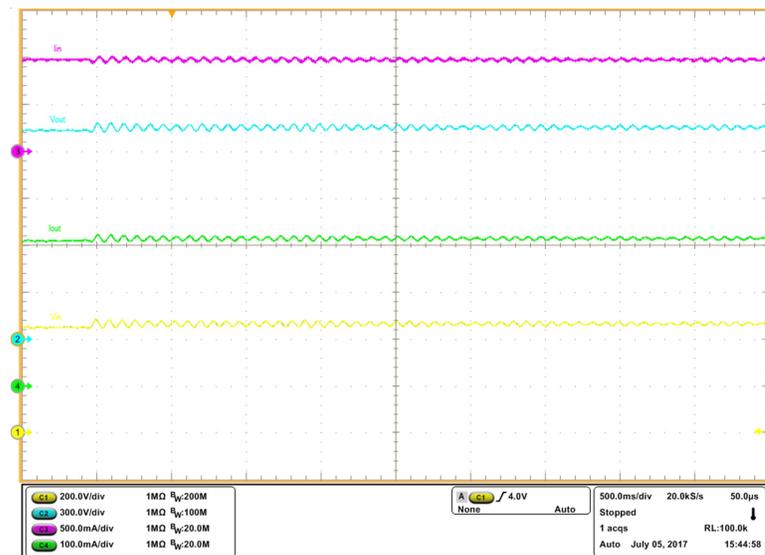


Fig. 7.36: Experimental results of reference step transient with the controller design 1000/s, current reference jumps from 0.33 A to 0.335 A.

it can be seen that the system is stable with 0.33 A output current reference, however, the system becomes unstable when the output current reference changes from 0.33 A to 0.335 A. Hence, the experimental results validates the analysis and controller design considerations presented in Section 5.4.
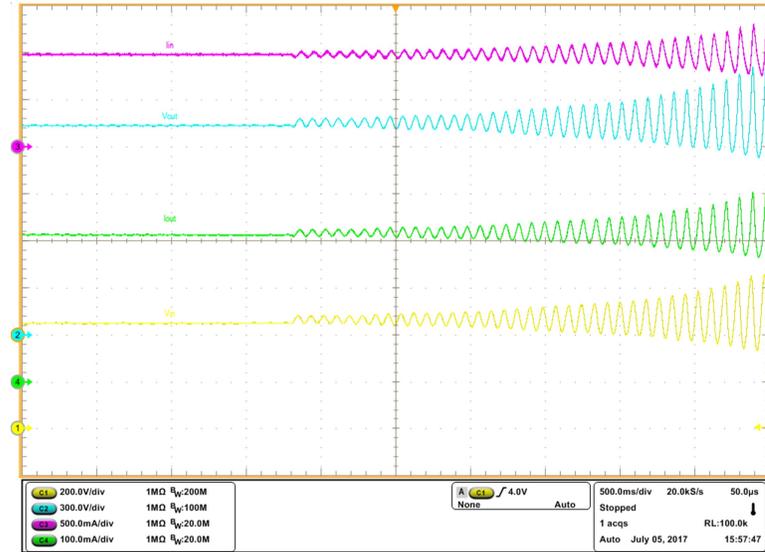
Fig. 7.37: Experimental results of reference step transient with the controller design 1033/s, current reference jumps from 0.33 A to 0.335 A.

Table 7.1: PARAMETERS OF THE SYSTEM

| | |
|---|---|
| $L_r$ [$\mu$**H**] | 174.2 |
| $C_r$ [**nF**] | 2.33 |
| $C_{in}$ [$\mu$**F**] | 4 |
| $f_s$ [**kHz**] | 250 |
| **Main MOSFETS (SiC)** | C2M1000170D |
| **Gate driver** | IXDN609YI |
| **Bypass MOSFET** | IXTH2N170D2 |
| **Floating capacitor** $C$ [$\mu$**F**] | 1 |
| **Bleed resistor** $R$ [**M$\Omega$**] | 1 |

## 7.4   System Operation and Protection

A scaled down version of the dc current distribution system for subsea application was built in the lab, which consists of two 100 km cable emulators and two 1 kW SRCs with 1 A input current and 0.33 A regulated output current. The parameters of the SRC are tabulated in TABLE 7.1. The photo of the cable emulator is shown in Fig. 7.26, while the photo of the developed SRC is shown in Fig. 7.13.

### 7.4.1   Operational Study Results

Hardware experiments including system startup, normal operation and shutdown were

conducted on the demo system to validate the proposed analysis and control strategies. The oscilloscope waveforms of the signals in the two SRCs are illustrated in Fig. 7.38, where CH1 is the input voltage of SRC #1, CH2 is the input voltage of SRC #2, CH3 is the output current of SRC #1 and CH4 is the output current of SRC #2. From Fig. 7.38, two steps can be clearly seen for startup. One step is the bypass branch releasing the cable current to SRC with open loop mode, and the other step is the SRC operates in closed loop mode with full input current.

### 7.4.2 Protection

The normal operation of the SRC with proposed protection circuit is demonstrated to verify the presented analysis and design. The SRC operates at 500 W output power with 1 A input current and 0.33 A regulated output current. The oscilloscope waveforms of the signals in the SRC are shown in Fig. 7.39, where CH1 is the primary bridge output voltage, CH2 is the voltage across the floating capacitor $C$, CH3 is the voltage across the resonant capacitor $C_r$ and CH4 is the resonant inductor current. From Fig. 7.39, it can be seen that the floating capacitor $C$ holds the peak voltage of the resonant capacitor $C_r$ as expected. With the proposed protection circuit, the SRC efficiency drops from 94.5% to 94.3% with 500 W output.

LTSpice simulations were run for normal operation and short-circuit fault cases to validate the presented capacitive clamping circuit operation with the converter parameters mentioned above. The results are shown in Fig. 7.40. From Fig. 7.40, it can be seen that the resonant capacitor voltage is well clamped during the fault transient as expected.

The normal operation to open and short circuit faults of the SRC with proposed protection circuit are demonstrated to verify the presented analysis and design. The SRC operates at 1k W output power with 1 A input current and 0.33 A regulated output current. The output current limit is 1 A, while the maximum bypassing current is set to be 1.3 A. The oscilloscope waveforms of the signals in the SRC are shown in Fig. 7.41 and Fig. 7.42. In Fig. 7.41, CH1 is the trunk cable current, CH2 is the SRC input voltage, CH3 is the output current and CH4 is the output voltage. In Fig. 7.42, CH1 is the SRC input voltage, CH2 is
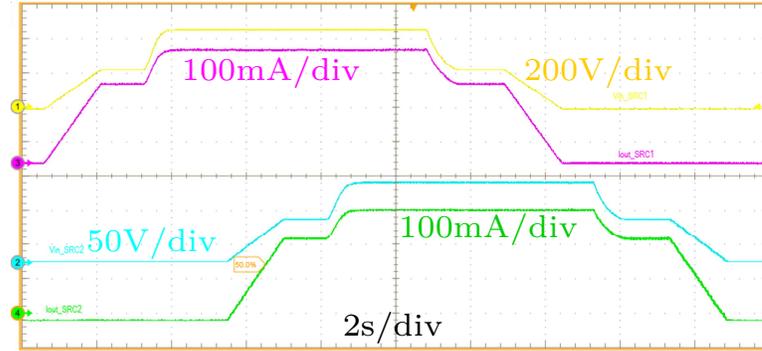
Fig. 7.38: Oscilloscope waveforms of the signals in the SRCs during startup, normal operation and shutdown. From top to bottom are the input voltage of SRC #1, output current of SRC #1, input voltage of SRC #2 and output current of SRC #2.
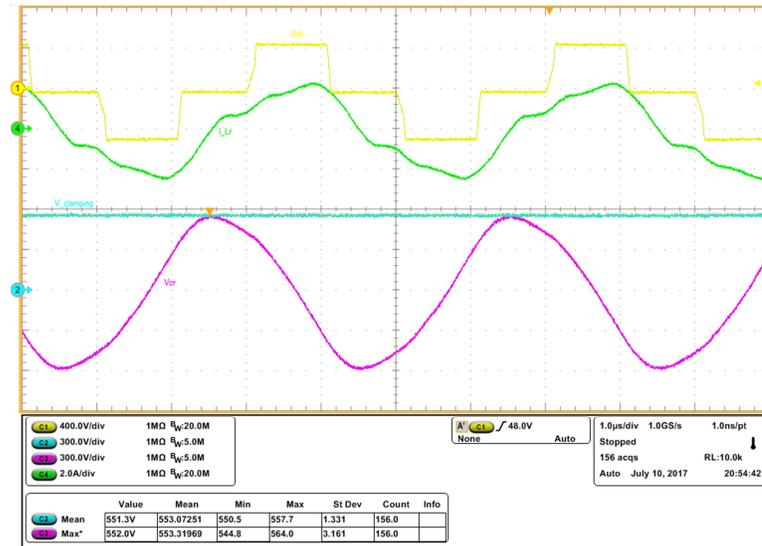


Fig. 7.39: Oscilloscope waveforms of the signals in the SRC with protection circuit. From top to bottom are the primary bridge output voltage, resonant inductor current, floating capacitor voltage, resonant capacitor voltage.

the trunk cable current, CH3 is the output current and CH4 is the output voltage. From Fig. 7.41 and Fig. 7.42, it can be seen that the SRC is well protected from both open and short circuit faults, the output current is limited to 1 A during the fault transient, and the input current is regulated to be 1.3 A during the fault response. The spikes in the results are due to bouncing of the relay used to perform output short/open circuit tests.
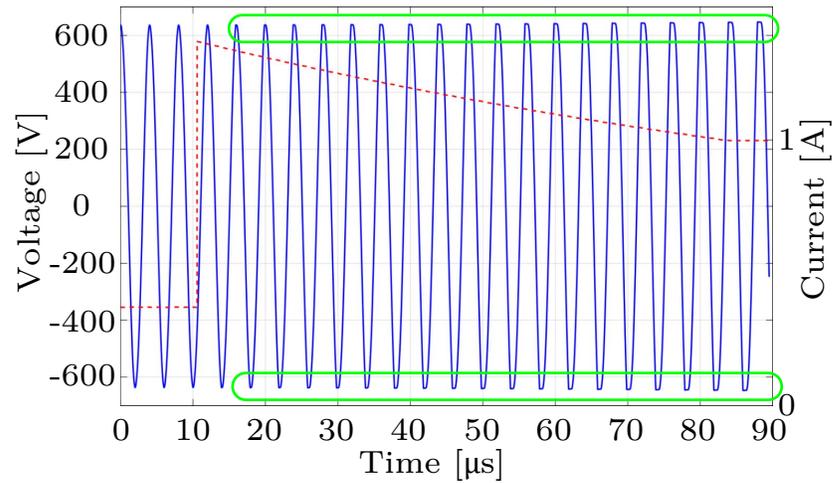
Fig. 7.40: Simulation results of normal operation to short-circuit fault transient.
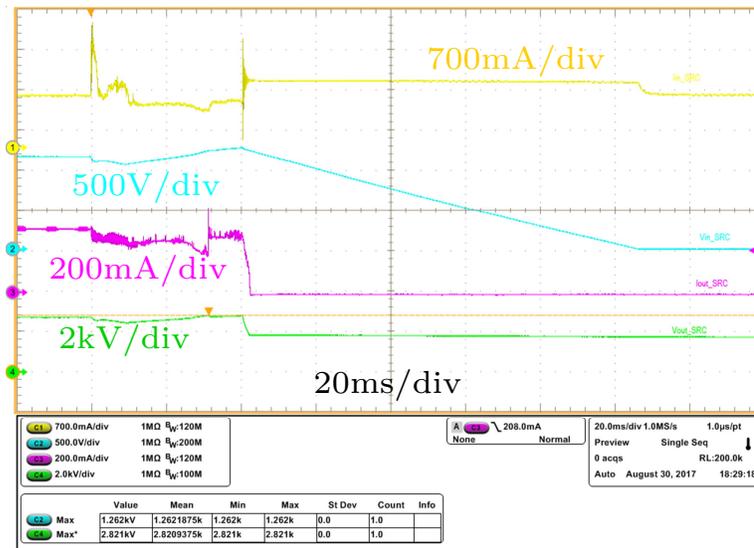


Fig. 7.41: Oscilloscope waveforms of the signals in the SRC during normal operation to open circuit fault. From top to bottom are the trunk cable current, input voltage, output current and output voltage.

### 7.4.3 Synchronous Rectification

The synchronous rectification is implemented on a Xilinx SPARTAN-6 FPGA device for a 1 kW PRC with an input current of 1 A and an output voltage range of 24 V - 250 V. The photograph of the PRC hardware prototype is illustrated in Fig. 7.43, while the parameters of the converter are tabulated in TABLE 7.2. In Fig. 7.43, the synchronous
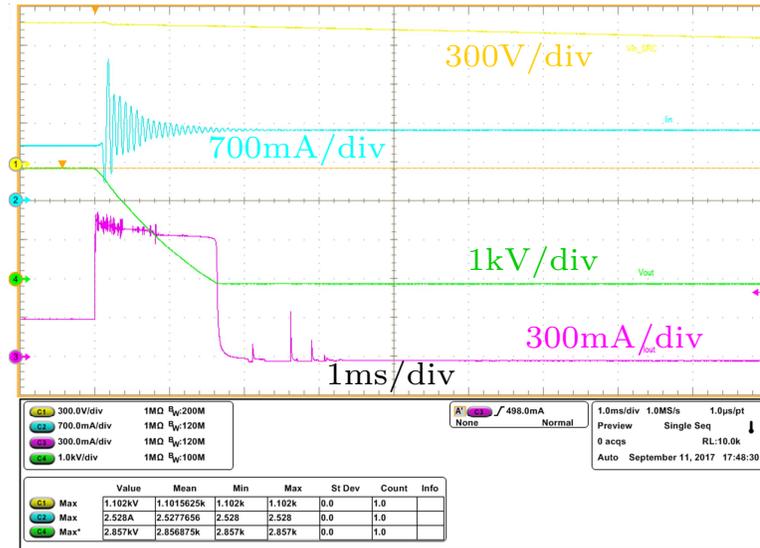
Fig. 7.42: Oscilloscope waveforms of the signals in the SRC during normal operation to short circuit fault. From top to bottom are the input voltage, trunk cable current, output current and output voltage.
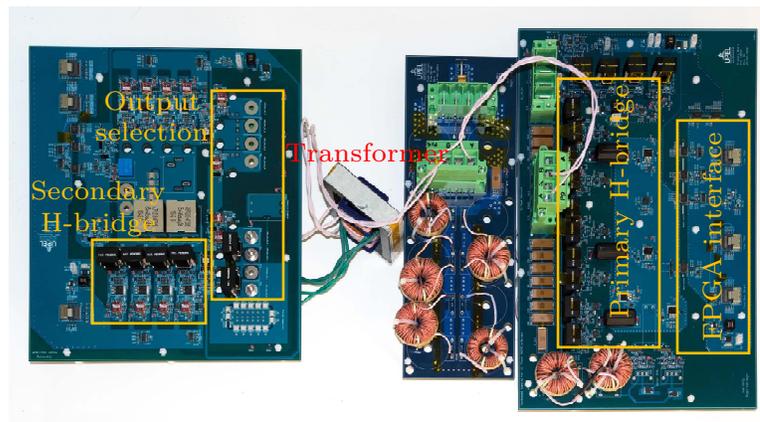


Fig. 7.43: The photograph of the 1 kW PRC prototype.

rectification is implemented for the secondary H-bridge.

The waveforms of the signals in the PRC converter operating at 250 kHz, 1 A input current, 250 V output voltage and 500 W output power is shown in Fig. 7.44. In Fig. 7.44, the yellow trace (CH1) is the gate to source voltage of the secondary left leg top switch, the light blue trace (CH2) is the primary bridge output voltage, the purple trace (CH3) is the resonant capacitor voltage, and the green trace (CH4) is the resonant tank inductor current. From Fig. 7.44, it can be seen that the gate to source voltage of the secondary left

Table 7.2: PARAMETERS OF THE 1 kW PRC

| Parameter | Value |
|:---:|:---:|
| $L_p$ $[\mu\mathbf{H}]$ | 423.4 |
| $C_p$ $[\mathbf{nF}]$ | 23.5 |
| $C_{out}$ $[\mu\mathbf{F}]$ | 2 |
| $f_s$ $[\mathbf{kHz}]$ | 250 |
| $I_{in}$ $[\mathbf{A}]$ | 1 |
| $V_{out}$ $[\mathbf{V}]$ | 24 - 250 |
| $P_{out}$ $[\mathbf{W}]$ | 50 - 1000 |
| $L_{f1}$ $[\mu\mathbf{H}]$ | 10 |
| $L_{f2}$ $[\mu\mathbf{H}]$ | 100 |
| $n_p{:}n_1{:}n_2{:}n_3{:}n_4$ | 16:0.56:1:1.8:3.23 |
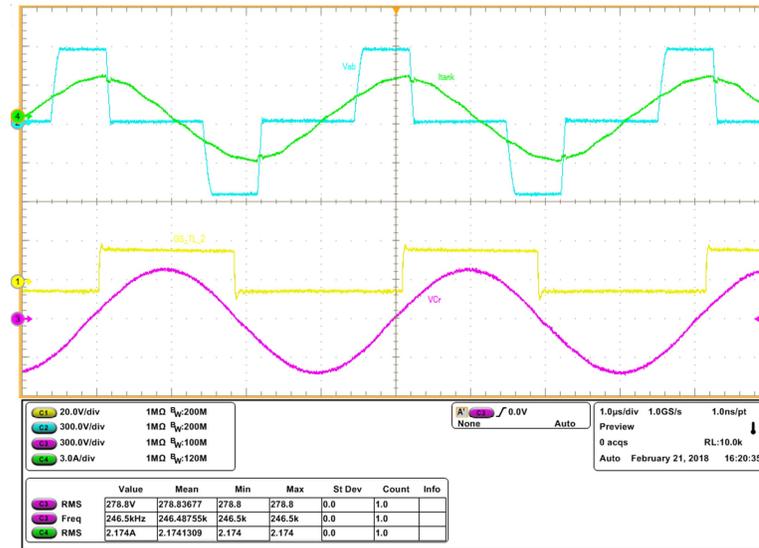


Fig. 7.44: Oscilloscope waveforms of the signals in the PRC operating at 1 A input current, 250 V output voltage and 500 W output power. The yellow trace (CH1) is the gate to source voltage of the secondary left leg top switch, the light blue trace (CH2) is the primary bridge output voltage, the purple trace (CH3) is the resonant capacitor voltage, and the green trace (CH4) is the resonant tank inductor current.

leg top switch is high when the resonant capacitor voltage is positive, and is low when the resonant capacitor voltage is negative, which demonstrates the synchronous rectification of the secondary H-bridge.

### 7.5   Summary

In this chapter, detailed experimental and simulation results and hardware design validations are provided. The analysis and design of the SRC with constant input current are demonstrated through two versions of the hardware prototypes, each of which corresponds to a design example. The derived small signal model and transfer function expressions are verified through simulations using white noise injection techniques. The system stability analysis and control is demonstrated using a system consists of two SRCs, and a system consists of one cable emulator and one SRC. The system operation and protection are also validated for the scaled down dc current distribution system.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

The dc current distribution systems have been widely used in a variety of applications, for both terrestrial and undersea scenarios. This dissertation focuses on analysis, design, modeling, control and protection of the SRCs applied in the dc current distribution systems. Compared with the dc voltage distribution systems, the dc current distribution systems have not been well studied yet, which opens the door to new opportunities and researches. The dc current distribution to series connected loads has been preferred for long distance and high reliability systems for its robustness against cable impedance and cable faults, especially for underwater applications where cost can be reduced by using sea water as the current return instead of submarine cable. The design procedures, small signal models, stability evaluation, control design, system operation and protection developed in this dissertation can be applied to other dc current distribution systems with other different dc-dc converter topologies. It has been demonstrated that the developed dc current distribution system with SRC as the dc-dc converter has high efficiency, low EMI, good dynamic performance and high reliability. In this chapter, the summary of contributions in this dissertation is given in Section 8.1. The future work that can be used to extend the work presented in this dissertation, and the new research topics and opportunities opened by the work done in this dissertation are discussed in Section 8.2.

## 8.1   Summary of Contributions

The work and results presented in this dissertation are summarized in this Section.

### 8.1.1   Output Characteristics Comparison of Resonant Converters with Constant DC Input Current

The resonant converters can be good candidates of the dc-dc converters in dc current

distribution systems, because of their high switching frequency, high power density, high efficiency and low EMI. The output characteristics and design of the resonant converters with constant dc voltage input have been well investigated in the literature, however, the resonant converters have a constant dc current input when they are used in the dc current distribution systems, and the behavior of the resonant converters with constant dc current input have not been studied.

Output characteristics of four commonly used resonant converter topologies, which are SRC, PRC, LCL resonant converter and DABSRC, were analyzed and compared based on steady state analysis applying fundamental approximation. For the SRC, the converter has a load independent output current behavior when operates at resonance, and can regulate its output current with short circuit load. For the PRC, the output behaves as a load independent natural voltage source when operates at resonance, which is a good candidate for applications require regulated output voltage. For the LCL resonant converter, it can be design to have a load independent current or a load independent voltage behavior at its output depending on the operating points. For the DABSRC, the converter has a load independent output voltage controlled by the three phase shift angles.

Based on the output characteristics presented in this dissertation, one can select the resonant converter topology that works best for them based on the specifications of the system or application. For the scenario investigated in this dissertation, the dc-dc converter needs to draw power from the dc constant current input, and provide power to the load with a regulated dc output current. Hence, the SRC, which can provide a load independent output current while operating at resonance is chosen to be the converter topology in this dissertation.

### 8.1.2 Analysis and Design Procedure of Series Resonant Converters with Constant DC Input Current

One of the key findings in this dissertation is that, for an SRC with dc constant current input, the output power cannot be controlled below a minimum value for either output current or output voltage regulation when operates away from resonance, and behaves as a

current source while operating at resonance. In such cases, traditional design considerations originated from SRC with constant dc voltage input may result in a situation that a steady state solution for the expected operating point does not exist.

The component stresses, including resonant inductor current, resonant capacitor differential voltage, resonant capacitor terminal to ground voltage and power loss, in the SRC are studied in detail with related design constrains derived. The output characteristics related design constrains are developed based on the in-depth output power analysis, current gain analysis and current source behavior analysis. Based on the derived design constrains, design procedures of an SRC with constant input current are developed for design with non-zero minimum output power and design with current source behavior, respectively.

Because of the series connection of the converters in the dc current distribution systems, the power transformer used in the converter has high voltage insulation requirement in general. The design optimization procedure is developed to eliminate the effects introduced by the parasitics in the high voltage transformer. Two design examples are presented by applying the developed design procedures and optimizations for the SRC with dc constant current input.

### 8.1.3 Small Signal Modeling of Series Resonant Converters with Constant DC Input Current

Series resonant converters (SRCs) being deployed in dc current distribution systems have constant input current, leading to variable input voltage. This results in significantly different steady state and dynamic behavior in comparison with traditional constant input voltage scenarios, and these differences and associated system design and stability challenges have not been well studied in the literature.

This dissertation solves challenges in both the steady state operation and small signal analysis of the SRC with constant input current introduced by the variable input voltage. This dissertation develops and validates small signal models using dynamic phasor modeling techniques for phase-shift modulated SRCs with constant input current and derives explicit analytical expressions for all key transfer functions, including input impedance and

control-to-output. The small signal models and transfer functions are suitable for feedback loop design, system stability evaluation and related design oriented analysis. The models allow both steady state and small signal quantities to be derived without undue complexity. In this dissertation, the following new contributions are provided. 1) Small signal models are developed for SRCs with constant input current, representing an operating condition that has not been studied in the literature and could be easily extended to other resonant topologies. 2) Explicit analytical expressions are provided for all key transfer functions, including input impedance and control-to-output, offering valuable resources to design feedback regulation and evaluate system stability.

### 8.1.4   Stability Analysis of DC Current Distribution Systems

The stability analysis and criterion presented in literature for the dc voltage distribution systems can not be applied to the dc current distribution systems directly because of the different system architectures. First, the impedance based stability criterion for a dc current distribution system is studied in this dissertation, where the minor loop gain is redefined. For a dc current distribution system that the cable impedance can be ignored, this dissertation develops a control strategy that stable operation of the system and independent regulation of the SRC output current are achieved through a low crossover frequency controller with no communications required among modules.

For a dc current distribution system with long transmission cable, the cable impedance cannot be ignored, or simply modeled as an inductor in series with a resistor. The model and impedance expressions for long transmission cables are derived in this dissertation, which are helpful for engineers and researchers to implement theoretical design and analysis. The relationship between closed-loop and open-loop input impedances is also discussed in this dissertation. Based on those theoretical expressions, this dissertation proposed stability analysis and design considerations by looking at bode plots and Nyquist plots of the system minor loop gain, which provides an accurate stability evaluation for the system. For a current distribution system with long transmission cable involved, the stability of the system is generally dominated by the impedance of the long transmission cable instead of the output

impedance of the power source. A system containing one current source, one cable and one load converter (SRC) is employed to demonstrate the proposed analysis and design. Further, the proposed analysis and design are also extended to systems with multiple cables and load converters.

### 8.1.5   Control Design and Protection

Based on the stability analysis, control strategy and controller design for the SRCs in the dc current distribution systems is developed in this dissertation. For the SRC, the controller design effects the closed-loop input impedance as presented in Section 5.3. With the designed controller, the stability analysis presented in Section 5.4 can be employed to evaluate the stability of the system accurately through Nyquist plot of the minor loop gain. This dissertation also discusses design of the shore-based dc current power supply which provides the regulated distribution current.

Protection techniques for an SRC operating as constant current input to constant current output, which includes the resonant capacitor voltage clamping during fault transients, the output current limiting during output short-circuit fault and the SRC module bypassing when fault happens, are proposed in this dissertation. These techniques can easily be extended to other resonant converters and also dc voltage distribution systems. The proposed protection circuit does not create additional circulating current during normal operation, which means a high efficiency can be maintained. The operation strategy of the system is presented in this dissertation allowing smooth and desired startup, normal operation and shutdown of the entire dc current distribution system. The design and analysis are validated through simulations and experimental results for a setup with two 100 km submarine cables and two 250 kHz, 1 kW SRCs with 1 A input current and 0.33 A regulated output current.

The control and system operation strategy presented in this dissertation are all implemented on a Xilinx SPARTAN-6 FPGA device and coded in Verilog HDL. The presented FPGA implementation provides engineers and researchers an idea of how to implement the startup and shutdown of a dc current distribution system, a integral controller design, synchronous rectification and converter protections. The presented knowledge can be easily

extended and applied to other FPGAs and programing languages.

## 8.2   Future Work

In additional to the design and control of the SRCs for dc current distribution applications, further research directions and possible opportunities have been identified in the process of finishing this dissertation. Those future research directions and possible opportunities are presented in this section with details.

### 8.2.1   Constant Current to Constant Voltage Output DC-DC Converter

The work presented in this dissertation is for output current regulated scenario, however, the output voltage of the dc-dc converter needs to be regulated for some dc current distribution applications. The analysis presented in Section 3.1 can be extended to design a dc-dc converter for this type of applications. Since the PRC with constant current input provides load independent output voltage while operating at resonance, it is the good candidate for these applications, which requires less control efforts and can regulates the output voltage when the converter has open circuit load.

Initial results for a PRC with constant input current which provides a regulated output voltage over wide load range were collected [126]. The circuit schematic of the PRC is illustrated in Fig. 3.4, while the picture of the hardware prototype is shown in Fig. 8.1. The parallel capacitor $C_p$ shown in Fig. 3.4 is placed on the secondary side of the transformer for lower voltage stress. The PRC converter can be further designed to archive a wide range of output voltage by using a transformer that has multiple secondary windings, having more than one secondary bridges and certain configuration networks. For the secondary bridge, instead of using diodes, MOSFETs can be used with synchronous rectification implemented to reduce the conduction loss and increase the converter efficiency.

### 8.2.2   Wireless Power Transfer for Underwater Automatic Vehicles

The SRC topology presented in this dissertation can be extend to wireless power transfer applications. As presented in Section 3.4.2, the ac resonant tank current is independent
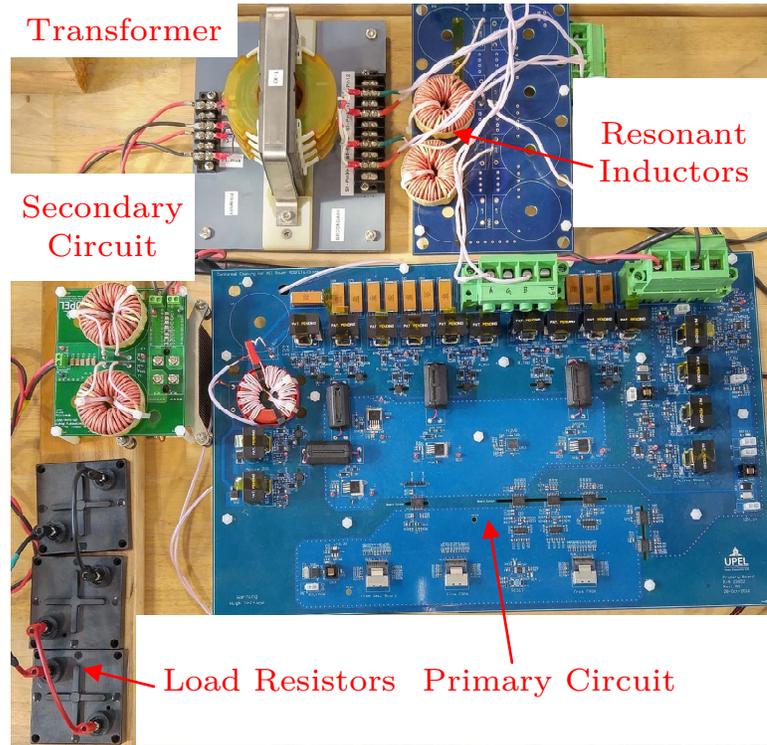
Fig. 8.1: Photo of the PRC hardware prototype.

from the load if the wireless power transfer primary coil is series compensated. The load independent primary coil current is a preferred merit for the wireless power transfer since it can decouple the primary side design and control and the secondary side design and control. If a series-series compensation is used for the wireless power transfer system that is fed from a dc constant current, the receiver side output voltage becomes load independent, which is suitable for battery charging and other applications.

A hardware prototype of the wireless power transfer system has been built, and initial tests were run to proof the concept. The circuit schematic of the system is shown in Fig. 8.2, and the photo of the hardware prototype is presented in Fig. 8.3. As shown in Fig. 8.2, the transformer $T_r$ is used to pump up the primary coil current in order to generate strong enough magnetic field when the dc distribution input current is low. The transformer $T_r$ can be eliminated if the dc distribution input current is high enough. The primary coil current can be controlled using the phase shift modulation. The diode bridge on the receiver side shown in Fig. 8.2 can be replaced by a H-bridge. With an active H-bridge, there are two
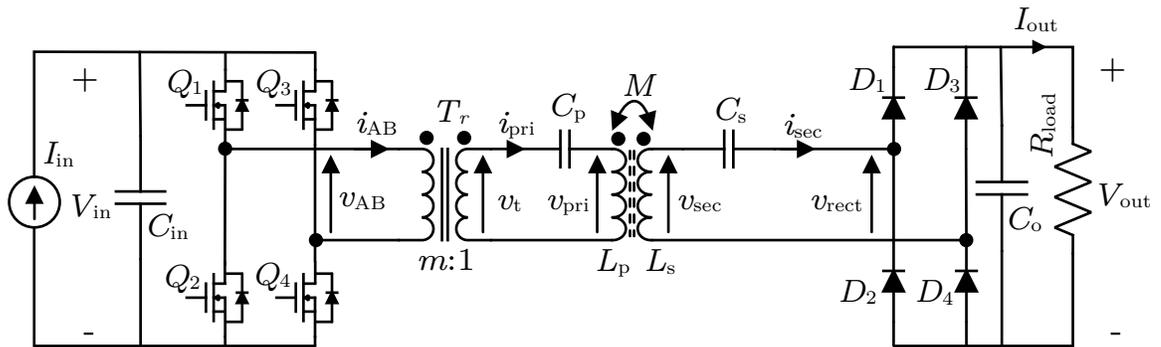
Fig. 8.2: Circuit diagram of the constant voltage output wireless power transfer topology fed from current distribution cable.
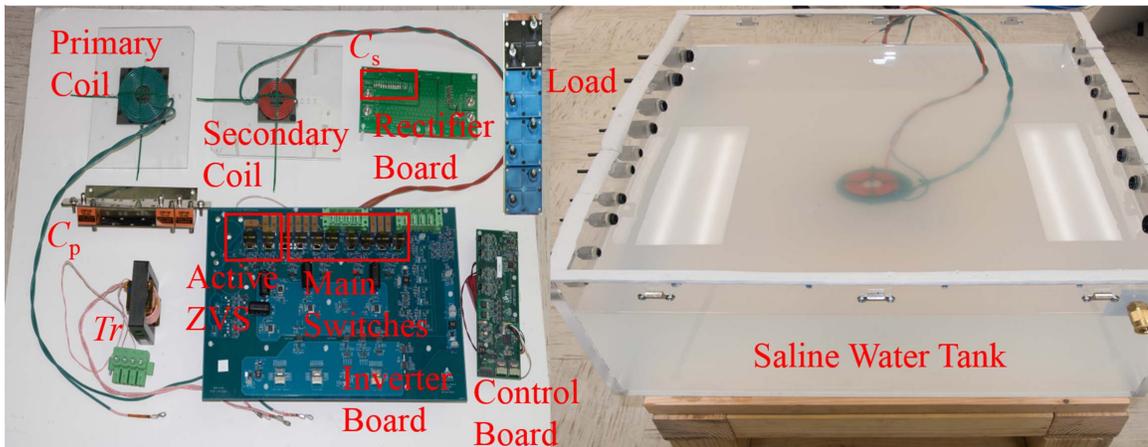


Fig. 8.3: Photo of the wireless power transfer hardware prototype.

possible control strategies. The first one is to run synchronous rectification, which means that the active H-bridge is just used to reduce the conduction loss. The second one is to have three phase shift angle control for the system, in which case bidirectional power flow is possible as well. For three phase shift angle control, communication between the transmitter (primary) and receiver is required.

### 8.2.3    Approaches for Achieving Wide Bandwidth Control

The control strategy presented in this dissertation can be further investigated based on the stability analysis. The controller bandwidth of the SRC converter presented in this dissertation is within hertz range, which is relatively low. The techniques and approaches to

implement wide bandwidth control of the dc-dc converters used in a dc current distribution system can be one of the future research directions.

One example of those approaches can be an energy buffer based solution. The diagram of the energy buffer concept is shown in Fig. 8.4. In [6], the authors presented an energy buffer with minimized energy storage capacitance for the LED driver, which can be used as a reference for this research. As shown in Fig. 8.4, the energy buffer is in parallel with the dc-dc converter. The energy buffer has an energy storage capacitor to either sink or provide energy during the system transients. The "Energy buffer" block in the figure can be some switching topologies such as Buck-boost topology or H-bridge topology. The objective of the energy buffer is to maintain either the input voltage or the input current of the dc-dc converter to be constant. The energy buffer has bidirectional power flow. The control of the energy buffer may contains three control loops: 1) Inner loop of energy buffer to regulate either the input voltage or the input current of the dc-dc converter. This control loop has the widest control bandwidth (fastest). 2) Output regulation of the dc-dc converter to regulate the output voltage or current from a constant input voltage or constant current regulated by the energy buffer. 3) Outer loop of the energy buffer to balance the voltage between $C_{energy}$ and $C_{in}$. This control loop has the narrowest bandwidth, which should be slower than the cable dynamics.

### 8.2.4 Topologies for DC/DC Converters Used in DC Current Distribution Systems

In this dissertation, four commonly used resonant converter topologies have been studied and compared. It can be noticed that all those four resonant converter topologies are actually voltage fed topologies, and just used in a constant dc input current scenario. For future works, some current fed resonant topologies can be one of the possible research directions. By using current fed topologies instead of voltage fed topologies in a dc current distribution system, the negative gain from phase shift control to the output can be avoid.

One of the possible current fed resonant converter topology is illustrated in Fig. 8.5. In Fig. 8.5, each switch in the primary H-bridge is an ac switch that consists of two anti
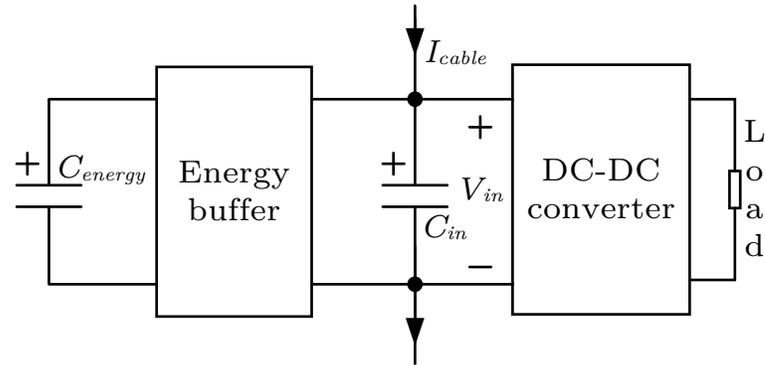
Fig. 8.4: Diagram of the energy buffer concept.
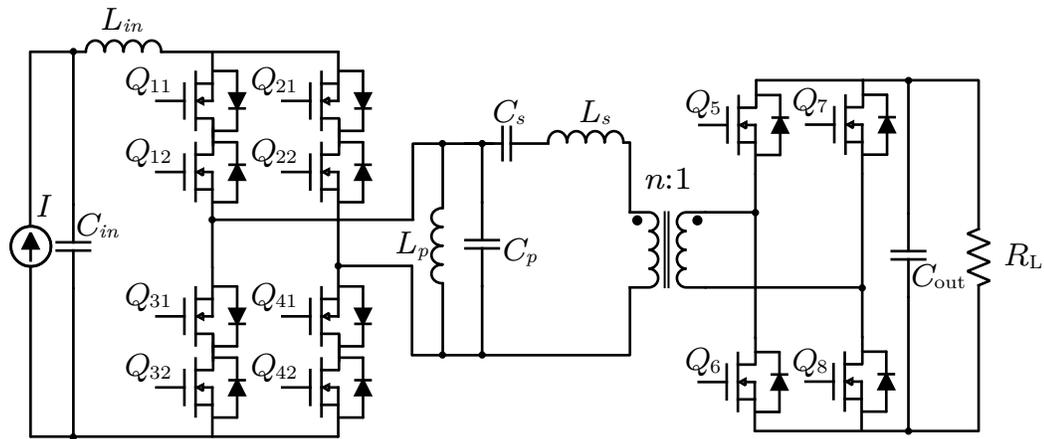


Fig. 8.5: Circuit diagram of a current fed resonant converter topology.

series MOSFETs, which can also be implemented in other forms. The reason of using ac switch in the circuit is that those primary H-bridges needs to block the negative voltage across it. The output current of the H-bridge shown in Fig. 8.5 is a phase shifted square waveform current, which is used to drive the resonant tank. The phase shift modulation for this converter topology is defined as the phase shift between the top two ac switches and the bottom two ac switches. The top two ac switches gate signals are complementary with some overlap time. The gain from phase shift control to the output of the converter is positive, and the phase shift modulation can be used to control the output from 0 to designed maximum value.

### 8.2.5 DC Current Distribution for Roadway Wireless Power Transfer

The dc current distribution system investigated in this dissertation can be further extended and leveraged to other applications. One possible application scenario is the roadway dynamic wireless power transfer systems, which dynamically charge the electrical vehicles while the vehicles is driving on the roadway. The power distribution to the transmitters integrated into the roadway is a big unsolved challenges for the implementation and adoption of roadway wireless power transfer.

The diagram of the proposed dc current distribution architecture for long distance roadway dynamic wireless power transfer is illustrated in Fig. 8.6. As shown in Fig. 8.6, a roadside converter provides a distribution dc current to the roadway section where a number of power transmitter modules are connected in series. One grid connection or roadside power converter is needed for one segment of the roadway, which reduces the system cost. The roadside power converter just need to provide the averaged power demand of a certain distance, which increases the utilization factor of the system. Compared with conventional low voltage distribution ($<$1kV), utilization of the dc current distribution architecture can archive higher distribution efficiency and lower cost, especially for higher power level distribution. More research on power transmitter module topology, power transmitter module and system control, and system stability evaluation can be done in future.
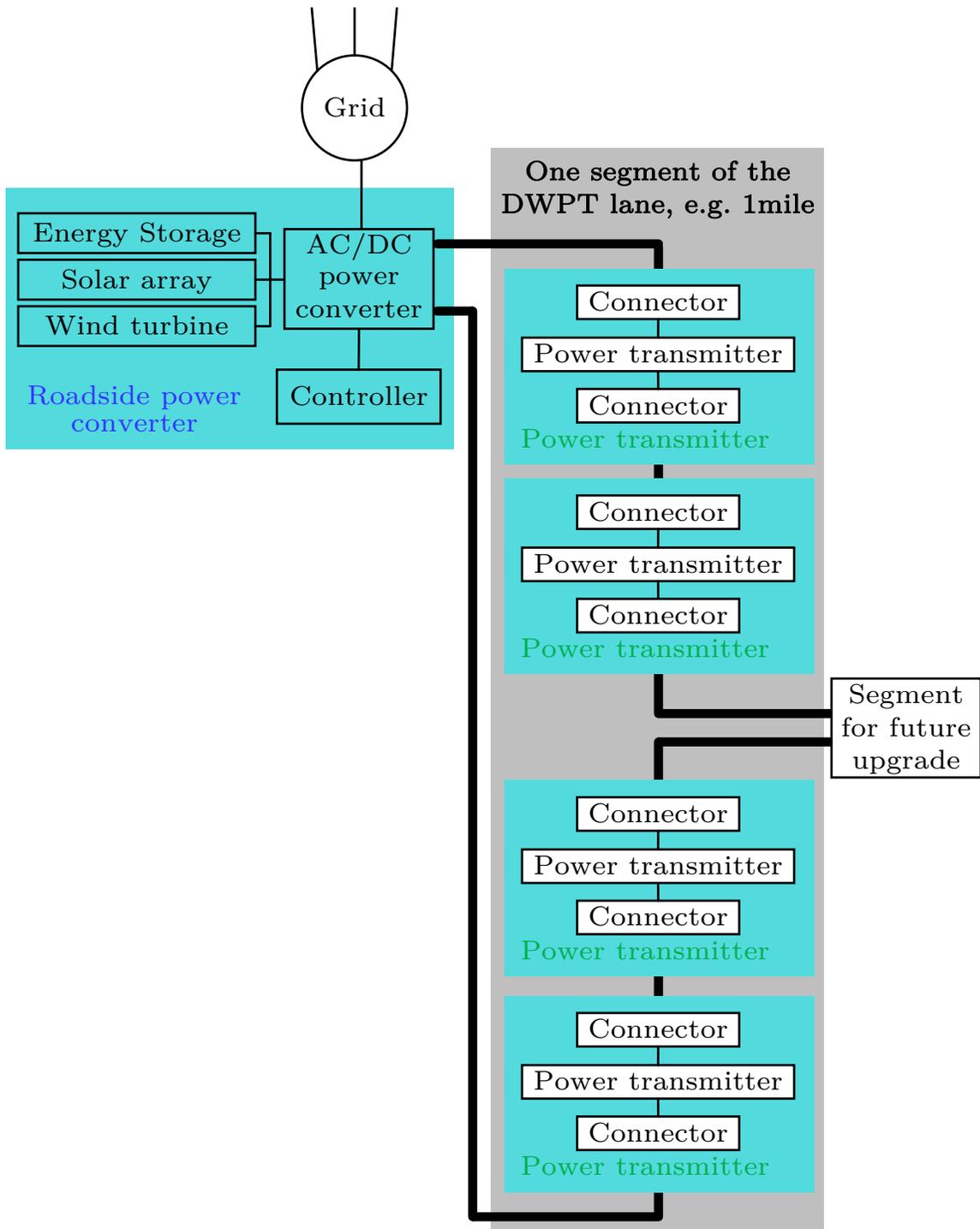
Fig. 8.6: Diagram of the roadway dynamic wireless power transfer using dc current power distribution architecture.

# REFERENCES

[1] U.S. Energy Information Administration. (2016) "Supply and Disposition of Electricity, 2006 through 2016". [Online]. Available: https://www.eia.gov/electricity/annual/html/epa_01_03.html.

[2] R. Faranda, H. Hafezi, and L. Martines, "Dc or ac distribution? an economic evaluation," in *2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I CPS Europe)*, June 2017, pp. 1–6.

[3] M. Starke, L. M. Tolbert, and B. Ozpineci, "Ac vs. dc distribution: A loss comparison," in *2008 IEEE/PES Transmission and Distribution Conference and Exposition*, April 2008, pp. 1–7.

[4] D. J. Hammerstrom, "Ac versus dc distribution systemsdid we get it right?" in *2007 IEEE Power Engineering Society General Meeting*, June 2007, pp. 1–5.

[5] R. Asad and A. Kazemi, "A quantitative analysis of effects of transition from ac to dc system, on storage and distribution systems," in *2012 Asia-Pacific Power and Energy Engineering Conference*, March 2012, pp. 1–5.

[6] Q. Hu and R. Zane, "Minimizing required energy storage in off-line led drivers based on series-input converter modules," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 2887–2895, Oct 2011.

[7] C. Branas, F. J. Azcondo, and R. Zane, "Power-mode control of multiphase resonant electronic ballast," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 4, pp. 1770–1778, April 2012.

[8] F. C. Lee, P. Barbosa, P. Xu, J. Zhang, B. Yang, and F. Canales, "Topologies and design considerations for distributed power system applications," *Proceedings of the IEEE*, vol. 89, no. 6, pp. 939–950, Jun 2001.

[9] H. Nguyen, D. Maksimovic, and R. Zane, "Active clamp llc resonant converter for point-of-load applications," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 1406–1412.

[10] F. Koyanagi and Y. Uriu, "A strategy of load leveling by charging and discharging time control of electric vehicles," *IEEE Transactions on Power Systems*, vol. 13, no. 3, pp. 1179–1184, Aug 1998.

[11] A. Shehabi, S. J. Smith, D. A. Sartor, R. E. Brown, M. Herrlin, J. G. Koomey, E. R. Masanet, N. Horner, I. L. Azevedo, and W. Lintner, "United states data center energy usage report," 06/2016 2016.

[12] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1184–1194, Sept 2004.

[13] C. L. Moreira, F. O. Resende, and J. A. P. Lopes, "Using low voltage microgrids for service restoration," *IEEE Transactions on Power Systems*, vol. 22, no. 1, pp. 395–403, Feb 2007.

[14] H. Kakigano, M. Nomura, and T. Ise, "Loss evaluation of dc distribution for residential houses compared with ac system," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, June 2010, pp. 480–486.

[15] D. Boroyevich, I. Cvetkovic, R. Burgos, and D. Dong, "Intergrid: A future electronic energy network?" *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 127–138, Sept 2013.

[16] Y. Cui, W. Zhang, L. M. Tolbert, D. J. Costinett, F. Wang, and B. J. Blalock, "Efficiency impact of mosfet output junction capacitance on a high step down ratio phase shift full bridge dc/dc converter," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 2083–2089.

[17] W. Zhang, B. Guo, F. Xu, Y. Cui, Y. Long, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Wide bandgap power devices based high efficiency power converters for data center application," in *Wide Bandgap Power Devices and Applications (WiPDA), 2014 IEEE Workshop on*, Oct 2014, pp. 121–126.

[18] Y. Cui, W. Zhang, L. M. Tolbert, D. J. Costinett, F. Wang, and B. J. Blalock, "Two phase interleaved isop connected high step down ratio phase shift full bridge dc/dc converter with gan fets," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 1414–1419.

[19] P. Magne, B. Nahid-Mobarakeh, and S. Pierfederici, "General active global stabilization of multiloads dc-power networks," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1788–1798, April 2012.

[20] P. S. Shenoy and P. T. Krein, "Differential power processing for dc systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1795–1806, April 2013.

[21] D. Boroyevich, I. CvetkoviÄĞ, D. Dong, R. Burgos, F. Wang, and F. Lee, "Future electronic power distribution systems a contemplative view," in *Optimization of Electrical and Electronic Equipment (OPTIM), 2010 12th International Conference on*, May 2010, pp. 1369–1380.

[22] H. Kirkham, B. M. Howe, V. Vorperian, and P. Bowerman, "The design of the neptune power system," in *OCEANS, 2001. MTS/IEEE Conference and Exhibition*, vol. 3, 2001, pp. 1374–1380 vol.3.

[23] B. M. Howe, H. Kirkham, and V. Vorperian, "Power system considerations for undersea observatories," *IEEE Journal of Oceanic Engineering*, vol. 27, no. 2, pp. 267–274, Apr 2002.

[24] X. Feng, Z. Ye, K. Xing, F. C. Lee, and D. Borojevic, "Individual load impedance specification for a stable dc distributed power system," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, vol. 2, Mar 1999, pp. 923–929 vol.2.

[25] L. R. Lewis, B. H. Cho, F. C. Lee, and B. A. Carpenter, "Modeling, analysis and design of distributed power systems," in *Power Electronics Specialists Conference, 1989. PESC '89 Record., 20th Annual IEEE*, Jun 1989, pp. 152–159 vol.1.

[26] S. Schulz, B. H. Cho, and F. C. Lee, "Design considerations for a distributed power system," in *Power Electronics Specialists Conference, 1990. PESC '90 Record., 21st Annual IEEE*, 1990, pp. 611–617.

[27] X. Feng, J. Liu, and F. C. Lee, "Impedance specifications for stable dc distributed power systems," *IEEE Transactions on Power Electronics*, vol. 17, no. 2, pp. 157–162, Mar 2002.

[28] X. Zhang, X. Ruan, and C. K. Tse, "Impedance-based local stability criterion for dc distributed power systems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 916–925, March 2015.

[29] W. Chen, X. Ruan, H. Yan, and C. K. Tse, "Dc/dc conversion systems consisting of multiple converter modules: Stability, control, and experimental verifications," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1463–1474, June 2009.

[30] K. Asakawa, J. Muramatsu, M. Aoyagi, K. Sasaki, and K. Kawaguchi, "Feasibility study on real-time seafloor glove monitoring cable-network-power feeding system," in *Underwater Technology, 2002. Proceedings of the 2002 International Symposium on*, 2002, pp. 116–122.

[31] H. Wang, T. Saha, and R. Zane, "Control of series connected resonant converter modules in constant current dc distribution power systems," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2016, pp. 1–7.

[32] K. Asakawa, J. Kojima, J. Muramatsu, and T. Takada, "Novel current to current converter for mesh-like scientific underwater cable network-concept and preliminary test result," in *OCEANS 2003. Proceedings*, vol. 4, Sept 2003, pp. 1868–1873 Vol.4.

[33] C. H. Wu and C. L. Chen, "High-efficiency current-regulated charge pump for a white led driver," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 10, pp. 763–767, Oct 2009.

[34] C. Simpson. (1995) "Battery charging". [Online]. Available: http://www.national.com/appinfo/power/files/f7.pdf.

[35] A. C. Lippincott and R. M. Nelms, "A capacitor-charging power supply using a series-resonant topology, constant on-time/variable frequency control, and zero-current switching," *IEEE Transactions on Industrial Electronics*, vol. 38, no. 6, pp. 438–447, Dec 1991.

[36] J. Goren and B. Kutchik, "Series resonant converters of ups," in *TELESCON 2000. Third International Telecommunications Energy Special Conference (IEEE Cat. No.00EX424)*, 2000, pp. 245–249.

[37] J. Biela, U. Badstuebner, and J. W. Kolar, "Design of a 5-kw, 1-u, 10-kw/dm3 resonant dcdc converter for telecom applications," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1701–1710, July 2009.

[38] J. J. Sandoval, S. Essakiappan, and P. Enjeti, "A bidirectional series resonant matrix converter topology for electric vehicle dc fast charging," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 3109–3116.

[39] H. Krishnaswami, "Photovoltaic microinverter using single-stage isolated high-frequency link series resonant topology," in *2011 IEEE Energy Conversion Congress and Exposition*, Sept 2011, pp. 495–500.

[40] N. Hasan, H. Wang, T. Saha, and Z. Pantic, "A novel position sensorless power transfer control of lumped coil-based in-motion wireless power transfer systems," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 586–593.

[41] N. Hasan, I. Cocar, T. Amely, H. Wang, R. Zane, Z. Pantic, and C. Bodine, "A practical implementation of wireless power transfer systems for socially interactive robots," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 4935–4942.

[42] F. J. Azcondo, R. Zane, and C. Branas, "Design of resonant inverters for optimal efficiency over lamp life in electronic ballast with phase control," *IEEE Transactions on Power Electronics*, vol. 22, no. 3, pp. 815–823, May 2007.

[43] L. Corradini, D. Seltzer, D. Bloomquist, R. Zane, D. MaksimoviÄĞ, and B. Jacobson, "Minimum current operation of bidirectional dual-bridge series resonant dc/dc converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3266–3276, July 2012.

[44] U. Badstuebner, J. Biela, and J. W. Kolar, "Power density and efficiency optimization of resonant and phase-shift telecom dc-dc converters," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, Feb 2008, pp. 311–317.

[45] Y. Yin, R. Zane, R. Erickson, and J. Glaser, "Dynamic analysis of frequency-controlled electronic ballasts," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, vol. 1, Oct 2002, pp. 685–691 vol.1.

[46] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio dc/dc converter cells for phase-modular solid-state transformers," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2015, pp. 5021–5029.

[47] D. Seltzer, L. Corradini, D. Bloomquist, R. Zane, and D. MaksimoviÄĞ, "Small signal phasor modeling of dual active bridge series resonant dc/dc converters with

multi-angle phase shift modulation," in *2011 IEEE Energy Conversion Congress and Exposition*, Sept 2011, pp. 2757–2764.

[48] F. Krismer, J. Biela, and J. W. Kolar, "A comparative evaluation of isolated bi-directional dc/dc converters with wide input and output voltage range," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, vol. 1, Oct 2005, pp. 599–606 Vol. 1.

[49] S. Suzuki and T. Shimizu, "A study on efficiency improvement of high-frequency current output inverter based on immittance conversion element," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, May 2014, pp. 1166–1172.

[50] H. Pollock, "Simple constant frequency constant current load-resonant power supply under variable load conditions," *Electronics Letters*, vol. 33, no. 18, pp. 1505–1506, Aug 1997.

[51] H. Seidel, "A high power factor tuned class d converter," in *Power Electronics Specialists Conference, 1988. PESC '88 Record., 19th Annual IEEE*, April 1988, pp. 1038–1042 vol.2.

[52] M. Borage, S. Tiwari, and S. Kotaiah, "Analysis and design of an lcl-t resonant converter as a constant-current power supply," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 6, pp. 1547–1554, Dec 2005.

[53] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, ser. Power electronics.  Springer US, 2001. [Online]. Available: https://books.google.com/books?id=On9-rJTR8ygC

[54] Y. Shirasaki, T. Nishida, M. Yoshida, Y. Horiuchi, J. Muramatsu, M. Tamaya, K. Kawaguchi, and K. Asakawa, "Proposal of next-generation real-time seafloor globe monitoring cable-network," in *OCEANS '02 MTS/IEEE*, vol. 3, Oct 2002, pp. 1688–1694 vol.3.

[55] A. Mohammadpour, L. Parsa, M. H. Todorovic, R. Lai, R. Datta, and L. Garces, "Series-input parallel-output modular-phase dc-dc converter with soft-switching and high-frequency isolation," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 111–119, Jan 2016.

[56] K. Modepalli, A. Mohammadpour, T. Li, and L. Parsa, "Three-phase current-fed isolated dc-dc converter with zero current switching," *IEEE Transactions on Industry Applications*, vol. PP, no. 99, pp. 1–1, 2016.

[57] S.-K. Han, H.-K. Yoon, G.-W. Moon, M.-J. Youn, Y.-H. Kim, and K.-H. Lee, "A new active clamping zero-voltage switching pwm current-fed half-bridge converter," *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1271–1279, Nov 2005.

[58] Q. Wu, Q. Wang, J. Xu, and Z. Xu, "Active-clamped zvs current-fed push-pull isolated dc/dc converter for renewable energy conversion applications," *IET Power Electronics*, vol. 11, no. 2, pp. 373–381, 2018.

[59] I. Castro, K. Martin, A. Vazquez, M. Arias, D. G. Lamar, and J. Sebastian, "An ac-dc pfc single-stage dual inductor current-fed push-pull for hb-led lighting applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 255–266, March 2018.

[60] Z. Guo, K. Sun, T. F. Wu, and C. Li, "An improved modulation scheme of current-fed bidirectional dc-dc converters for loss reduction," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4441–4457, May 2018.

[61] M. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*. Wiley, 2011. [Online]. Available: https://books.google.com/books?id=8ECecQAACAAJ

[62] H. R. Visser and P. P. J. van den Bosch, "Modelling of periodically switching networks," in *Power Electronics Specialists Conference, 1991. PESC '91 Record., 22nd Annual IEEE*, Jun 1991, pp. 67–73.

[63] O. P. Mandhana and R. G. Hoft, "Steady state analysis of dc to dc resonant converter," in *Applied Power Electronics Conference and Exposition, 1991. APEC '91. Conference Proceedings, 1991., Sixth Annual*, Mar 1991, pp. 580–586.

[64] R. Oruganti and F. C. Lee, "Resonant power processors, part i—state plane analysis," *IEEE Transactions on Industry Applications*, vol. IA-21, no. 6, pp. 1453–1460, Nov 1985.

[65] J. Lu, A. Kumar, and K. K. Afridi, "A step-superposition based analysis approach to modeling resonant converters," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[66] V. Vorperian and S. Cuk, "Small signal analysis of resonant converters," in *1983 IEEE Power Electronics Specialists Conference*, June 1983, pp. 269–282.

[67] R. J. King and T. A. Stuart, "Small-signal model for the series resonant converter," *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-21, no. 3, pp. 301–319, May 1985.

[68] M. G. Kim and M. J. Youn, "A discrete time domain modeling and analysis of controlled series resonant converter," *IEEE Transactions on Industrial Electronics*, vol. 38, no. 1, pp. 32–40, Feb 1991.

[69] G. C. Verghese, M. E. Elbuluk, and J. G. Rassakian, "A general approach to sampled-data modeling for power electronic circuits," in *1984 IEEE Power Electronics Specialists Conference*, June 1984, pp. 316–330.

[70] M. E. Elbuluk, G. C. Verghese, and J. G. Kassakian, "Sampled-data modeling and digital control of resonant converters," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 344–354, July 1988.

[71] F. da Silveira Cavalcante and J. W. Kolar, "Small-signal model of a 5kw high-output voltage capacitive-loaded series-parallel resonant dc-dc converter," in *2005 IEEE 36th Power Electronics Specialists Conference*, June 2005, pp. 1271–1277.

[72] A. F. Witulski, A. F. Hernandez, and R. W. Erickson, "Small signal equivalent circuit modeling of resonant converters," *IEEE Transactions on Power Electronics*, vol. 6, no. 1, pp. 11–27, Jan 1991.

[73] S. Tian, F. C. Lee, and Q. Li, "A simplified equivalent circuit model of series resonant converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3922–3931, May 2016.

[74] E. X. Yang, F. C. Lee, and M. M. Jovanovic, "Small-signal modeling of series and parallel resonant converters," in *Applied Power Electronics Conference and Exposition, 1992. APEC '92. Conference Proceedings 1992., Seventh Annual*, Feb 1992, pp. 785–792.

[75] C. T. Rim and G. H. Cho, "Phasor transformation and its application to the dc/ac analyses of frequency phase-controlled series resonant converters (src)," *IEEE Transactions on Power Electronics*, vol. 5, no. 2, pp. 201–211, Apr 1990.

[76] Y. Yin, R. Zane, R. Erickson, and J. Glaser, "Direct modeling of envelope dynamics in resonant inverters," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, vol. 3, June 2003, pp. 1313–1318 vol.3.

[77] Y. Yin, R. Zane, J. Glaser, and R. W. Erickson, "Small-signal analysis of frequency-controlled electronic ballasts," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 8, pp. 1103–1110, Aug 2003.

[78] L. Scandola, L. Corradini, and G. Spiazzi, "Small-signal modeling of combined phase shift and pulse width uniformly sampled modulators," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–7.

[79] ——, "Small-signal modeling of uniformly sampled phase-shift modulators," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5870–5880, Oct 2015.

[80] A. Emadi, J. P. Johnson, and M. Ehsani, "Stability analysis of large dc solid-state power systems for space," *IEEE Aerospace and Electronic Systems Magazine*, vol. 15, no. 2, pp. 25–30, Feb 2000.

[81] S. R. Rudraraju, A. K. Srivastava, S. C. Srivastava, and N. N. Schulz, "Small signal stability analysis of a shipboard mvdc power system," in *2009 IEEE Electric Ship Technologies Symposium*, April 2009, pp. 135–141.

[82] P. Shamsi and B. Fahimi, "Stability assessment of a dc distribution network in a hybrid micro-grid application," *IEEE Transactions on Smart Grid*, vol. 5, no. 5, pp. 2527–2534, Sept 2014.

[83] S. D. Sudhoff, S. F. Glover, P. T. Lamm, D. H. Schmucker, and D. E. Delisle, "Admittance space stability analysis of power electronic systems," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 36, no. 3, pp. 965–973, Jul 2000.

[84] S. D. Sudhoff and S. F. Glover, "Three-dimensional stability analysis of dc power electronics based systems," in *2000 IEEE 31st Annual Power Electronics Specialists*

*Conference. Conference Proceedings (Cat. No.00CH37018)*, vol. 1, 2000, pp. 101–106 vol.1.

[85] D. L. Logue and P. T. Krein, "Preventing instability in dc distribution systems by using power buffering," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, vol. 1, 2001, pp. 33–37 vol. 1.

[86] M. Kabalan, P. Singh, and D. Niebur, "Large signal lyapunov-based stability studies in microgrids: A review," *IEEE Transactions on Smart Grid*, vol. 8, no. 5, pp. 2287–2295, Sept 2017.

[87] W. Du, J. Zhang, Y. Zhang, and Z. Qian, "Stability criterion for cascaded system with constant power load," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1843–1851, April 2013.

[88] P. Magne, B. Nahid-Mobarakeh, and S. Pierfederici, "Active stabilization of dc microgrids without remote sensors for more electric aircraft," *IEEE Transactions on Industry Applications*, vol. 49, no. 5, pp. 2352–2360, Sept 2013.

[89] S. Singh, V. Kumar, and D. Fulwani, "Mitigation of destabilising effect of cpls in island dc micro-grid using non-linear control," *IET Power Electronics*, vol. 10, no. 3, pp. 387–397, 2017.

[90] A. Riccobono and E. Santi, "Comprehensive review of stability criteria for dc power distribution systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3525–3535, Sept 2014.

[91] C. M. Wildrick, F. C. Lee, B. H. Cho, and B. Choi, "A method of defining the load impedance specification for a stable distributed power system," in *Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE*, Jun 1993, pp. 826–832.

[92] X. Feng, Z. Ye, K. Xing, F. C. Lee, and D. Borojevic, "Impedance specification and impedance improvement for dc distributed power system," in *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*, vol. 2, 1999, pp. 889–894 vol.2.

[93] P.-L. Wong, F. C. Lee, and X. Zhou, "Stability study of pc power system," *IEEE Transactions on Industry Applications*, vol. 37, no. 1, pp. 73–80, Jan 2001.

[94] R. Haroun, A. E. Aroudi, A. Cid-Pastor, and L. Martinez-Salamero, "Stability issues in cascade connected switching converters for dc microgrid applications," in *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, May 2013, pp. 1324–1327.

[95] Z. Huang, S. C. Wong, and C. K. Tse, "Revisiting stability criteria for dc power distribution systems based on power balance," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 1, pp. 76–85, 2017.

[96] A. Rygg and M. Molinas, "Apparent impedance analysis: A small-signal method for stability analysis of power electronic-based systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1474–1486, Dec 2017.

[97] G. S. Thandi, R. Zhang, K. Xing, F. C. Lee, and D. Boroyevich, "Modeling, control and stability analysis of a pebb based dc dps," *IEEE Transactions on Power Delivery*, vol. 14, no. 2, pp. 497–505, Apr 1999.

[98] L. Herrera, W. Zhang, and J. Wang, "Stability analysis and controller design of dc microgrids with constant power loads," *IEEE Transactions on Smart Grid*, vol. 8, no. 2, pp. 881–888, March 2017.

[99] A. Riccobono, M. Cupelli, A. Monti, E. Santi, T. Roinila, H. Abdollahi, S. Arrua, and R. A. Dougal, "Stability of shipboard dc power distribution: Online impedance-based systems methods," *IEEE Electrification Magazine*, vol. 5, no. 3, pp. 55–67, Sept 2017.

[100] A. L. Julian and R. M. Cuzner, "Design, modelling and stability analysis of an integrated shipboard dc power system," in *2009 IEEE Electric Ship Technologies Symposium*, April 2009, pp. 428–432.

[101] H. Suryanarayana and S. D. Sudhoff, "Refinements in generalized immittance based stability analysis of dc power electronics based distribution systems," in *2015 IEEE Electric Ship Technologies Symposium (ESTS)*, June 2015, pp. 80–85.

[102] S. D. Sudhoff and J. M. Crider, "Advancements in generalized immittance based stability analysis of dc power electronics based distribution systems," in *2011 IEEE Electric Ship Technologies Symposium*, April 2011, pp. 207–212.

[103] J. G. Ciezki and R. W. Ashton, "Selection and stability issues associated with a navy shipboard dc zonal electric distribution system," *IEEE Transactions on Power Delivery*, vol. 15, no. 2, pp. 665–669, Apr 2000.

[104] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Conf. Rec. IEEE IAS Annu. Meeting*, 1976, pp. 366–382.

[105] J. Siegers, S. Arrua, and E. Santi, "Stabilizing controller design for multibus mvdc distribution systems using a passivity-based stability criterion and positive feedforward control," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 14–27, March 2017.

[106] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3075–3078, Nov 2011.

[107] B. S. Jacobson and R. A. DiPerna, "Series resonant converter with clamped tank capacitor voltage," in *Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition*, March 1990, pp. 137–146.

[108] H. Wang, T. Saha, and R. Zane, "Analysis and design of a series resonant converter with constant current input and regulated output current," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 1741–1747.

184

[109] W. Zhang, Y. Long, Y. Cui, F. Wang, L. M. Tolbert, B. J. Blalock, S. Henning, J. Moses, and R. Dean, "Impact of planar transformer winding capacitance on si-based and gan-based llc resonant converter," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 1668–1674.

[110] K. Changtong, R. W. Erickson, and D. Maksimovic, "A comparison of the ladder and full-order magnetic models," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, vol. 4, 2001, pp. 2067–2071 vol. 4.

[111] L. A. R. Tria, D. Zhang, and J. E. Fletcher, "Planar pcb transformer model for circuit simulation," *IEEE Transactions on Magnetics*, vol. 52, no. 7, pp. 1–4, July 2016.

[112] P. G. Blanken, "A lumped winding model for use in transformer models for circuit simulation," *IEEE Transactions on Power Electronics*, vol. 16, no. 3, pp. 445–460, May 2001.

[113] A. F. Witulski, "Introduction to modeling of transformers and coupled inductors," *IEEE Transactions on Power Electronics*, vol. 10, no. 3, pp. 349–357, May 1995.

[114] M. Xinkui and C. Wei, "More precise model for parasitic capacitances in high-frequency transformer," in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, vol. 2, 2002, pp. 1054–1057 vol.2.

[115] N. Y. Abed and O. A. Mohammed, "Physics-based high-frequency transformer modeling by finite elements," *IEEE Transactions on Magnetics*, vol. 46, no. 8, pp. 3249–3252, Aug 2010.

[116] H. Y. Lu, J. G. Zhu, V. S. Ramsden, and S. Y. R. Hui, "Measurement and modeling of stray capacitances in high frequency transformers," in *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*, vol. 2, 1999, pp. 763–768 vol.2.

[117] H. Y. Lu, J. G. Zhu, and S. Y. R. Hui, "Experimental determination of stray capacitances in high frequency transformers," *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1105–1112, Sept 2003.

[118] J. A. A. Qahouq, W. Al-Hoor, W. Mikhael, L. Huang, and I. Batarseh, "Analysis and experimental results of an adaptive-step-size switching-frequency auto-tuning digital controller," in *2008 IEEE Power Electronics Specialists Conference*, June 2008, pp. 4597–4602.

[119] I. J. Gabe, V. F. Montagner, and H. Pinheiro, "Design and implementation of a robust current controller for vsi connected to the grid through an lcl filter," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1444–1452, June 2009.

[120] M. Liukkonen, M. Hinkkanen, J. Kyyrä, and S. J. Ovaska, "Modeling of multiport dc busses in power-electronic systems," in *2013 IEEE International Conference on Industrial Technology (ICIT)*, Feb 2013, pp. 740–745.

[121] J. W. Phinney, D. J. Perreault, and J. H. Lang, "Synthesis of lumped transmission-line analogs," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1531–1542, July 2007.

[122] S. Zhang, S. Jiang, X. Lu, B. Ge, and F. Z. Peng, "Resonance issues and damping techniques for grid-connected inverters with long transmission cable," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 110–120, Jan 2014.

[123] W. W. Chen, R. Zane, and L. Corradini, "Isolated bidirectional grid-tied three-phase ac-dc power conversion using series-resonant converter modules and a three-phase unfolder," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9001–9012, Dec 2017.

[124] D. Seltzer and R. Zane, "Multi-mode control of series and parallel converters for bidirectional power systems," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2014, pp. 1–8.

[125] T. Saha, H. Wang, B. Riar, and R. Zane, "Analysis of zero voltage switching requirements and passive auxiliary circuit design for dc-dc series resonant converters with constant input current," in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Dec 2016, pp. 1–6.

[126] T. Saha, H. Wang, and R. Zane, "Analysis and design of a parallel resonant converter for constant current input to constant voltage output dc-dc converter over wide load range," in *The 2018 International Power Electronics Conference - ECCE ASIA -*, in press.

CURRICULUM VITAE

# Hongjie Wang

**Journal Articles**

- H. Wang, T. Saha, B. S. Riar and R. Zane, Design Considerations for Current Regulated Series Resonant Converters with Constant Input Current, *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1-1, 2018.

- H. Wang, T. Saha and R. Zane, Analysis and Design of a Series Resonant Converter with Constant Current Input and Regulated Output Current, *IEEE Transactions on Power Electronics*, *in submission*.

**Patents**

- H. Wang, R. Zane and T. Saha, *DC Power Supply From A Constant Current Source*, patent filed, Mar. 2018.

- H. Wang and R. Zane, *Dynamic Inductive Wireless Power Transmitter System*, patent filed, Sept. 2017.

- H. Wang and R. Zane, *Power Transmitter Module*, patent filed, Sept. 2017.

**Published Conference Papers**

- H. Wang, T. Saha, B. S. Riar and R. Zane, Small Signal Phasor Modeling of Phase-shift Modulated Series Resonant Converters with Constant Input Current, in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, *in press*.

- T. Saha, H. Wang, B. S. Riar and R. Zane, Analysis and Design of Wide Range Output Voltage Regulated Power Supply for Underwater Constant Input Current DC Distribution System, in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, *in press*.

- R. Hassan, H. Wang, M. M. Rehman, B. S. Riar and R. Zane,Nodal Impedance-Based Stability Analysis of DC Nanogrids, in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, *in press*.

- H. Wang, T. Saha, B. S. Riar and R. Zane, Operational study and protection of a series resonant converter with DC current input applied in DC current distribution systems, in *2018 IEEE International Power Electronics Conference (IPEC) -ECCE ASIA*, *in press*.

- T. Saha, H. Wang, and R. Zane, Analysis and design of a parallel resonant converter for constant current input to constant voltage output dc-dc converter over wide load range, in *2018 IEEE International Power Electronics Conference (IPEC) -ECCE ASIA*, *in press*.

- T. Saha, H. Wang, B. Riar and R. Zane, An improved active zero voltage switching assisting circuit with lower dv/dt for DC-DC series resonant converter with constant input current, in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, 2018, pp. 826-831.

- H. Wang, T. Saha and R. Zane, Impedance-based stability analysis and design considerations for DC current distribution with long transmission cable, in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-8.

- T. Saha and H. Wang and R. Zane, Zero voltage switching assistance design for DC-DC series resonant converter with constant input current for wide load range, in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-5.

- M. Evzelman, H. Wang, R. Zane and X. Zhao, Two-stage sinusoidal generator with calibration and pulse train amplitude feedback for ultrasonic applications, in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 2124-2130.

- H. Wang, T. Saha and R. Zane, Analysis and design of a series resonant converter with constant current input and regulated output current, in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 1741-1747.

- H. Wang, T. Saha and R. Zane, Design considerations for series resonant converters with constant current input, in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-8.

- T. Saha, H. Wang, B. Riar and R. Zane, Analysis of zero voltage switching requirements and passive auxiliary circuit design for DC-DC series resonant converters with constant input current, in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, Auckland, 2016, pp. 1-6.

- H. Wang, T. Saha and R. Zane, Control of series connected resonant converter modules in constant current dc distribution power systems, in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Trondheim, 2016, pp. 1-7.

- N. Hasan, H. Wang, T. Saha and Z. Pantic, A novel position sensorless power transfer control of lumped coil-based in-motion wireless power transfer systems, in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 586-593.

- N. Hasan, I. Cocar, T. Amely, H. Wang, R. Zane, Z. Pantic and C. Bodine, A practical implementation of wireless power transfer systems for socially interactive robots, in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 4935-4942.

- H. Wang, M. M. U. Rehman, M. Evzelman and R. Zane, SIMULINK based hardware-in-the-loop rapid prototyping of an electric vehicle battery balancing controller, in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Vancouver, BC, 2015, pp. 1-6.

- F. Zhang, M. M. U. Rehman, H. Wang *et al.*, State-of-charge estimation based on microcontroller-implemented sigma-point Kalman filter in a modular cell balancing system for Lithium-Ion battery packs, in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Vancouver, BC, 2015, pp. 1-7.