MODULAR, SCALABLE BATTERY SYSTEMS WITH INTEGRATED CELL BALANCING AND DC BUS POWER PROCESSING

by

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ABSTRACT

Modular, Scalable Battery Systems with Integrated
Cell Balancing and DC Bus Power Processing

by

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Traditional electric vehicle and stationary battery systems use series-connected battery packs that employ centralized battery management and power processing architecture. Though, these systems meet the basic safety and power requirements with a simple hardware structure, the approach results in a battery pack that is energy and power limited by weak cells throughout life and most importantly at end-of-life. The applications of battery systems can benefit significantly from modular, scalable battery systems capable of advanced cell balancing, efficient power processing, and cost gains via reuse beyond first-use application. The design of modular battery systems has unique requirements for the power electronics designer, including architecture, design, modeling and control of power processing converters, and battery balancing methods. This dissertation considers the requirements imposed by electric vehicle and stationary applications and presents design and control of modular battery systems to overcome challenges associated with conventional systems. The modular battery system uses cell or substring-level power converters to combine battery balancing and power processing functionality and opens the door to new opportunities for advanced cell balancing methods. This approach enables balancing control to act on cell-level information, reroute power around weaker cells in a string of cells to optimally

deploy the stored energy, and achieve performance gains throughout the life of the battery pack. With this approach, the integrated balancing power converters can achieve system cost and efficiency gains by replacing or eliminating some of the conventional components inside battery systems such as passive balancing circuits and high-voltage, high-power converters. In addition, when coupled with life prognostic based cell balancing control, the modular system can extend the lifetime of a battery pack by up to 40%. The modular architecture design and control concepts developed in this dissertation can be applied to designs of large battery packs and improve battery pack performance, lifetime, size, and cost.

(178 pages)

PUBLIC ABSTRACT

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Traditional electric vehicle and stationary battery systems use series-connected battery packs that employ centralized battery management and power processing architecture. Though, these systems meet the basic safety and power requirements with a simple hardware structure, the approach results in a battery pack that is energy and power limited by weak cells throughout life and most importantly at end-of-life. The applications of battery systems can benefit significantly from modular, scalable battery systems capable of advanced cell balancing, efficient power processing, and cost gains via reuse beyond first-use application. This thesis considers the requirements imposed by electric vehicle and stationary applications and presents a modular battery system architecture, including design, modeling and control methods, to overcome challenges associated with conventional systems. The modular battery system uses power converters to combine battery balancing and power processing functionality and opens the door to new opportunities for advanced cell balancing methods. With this approach, the power converters can achieve system cost and efficiency gains by replacing or eliminating some of the conventional components inside battery systems. In addition, when coupled with life prognostic based cell balancing control, the modular system can extend the lifetime of a battery pack by up to 40%. The design and control concepts developed in this thesis can be applied to designs of large battery packs and improve battery pack performance, lifetime, size, and cost.

Dedicated to my parents, Riaz and Musarrat

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Muhammad Muneeb Ur Rehman

CONTENTS

LIST OF TABLES

LIST OF FIGURES

ACRONYMS

BMS	Battery Management System
DAB	Dual Active Bridge
EOL	End of Life
HV	High Voltage
LV	Low Voltage
PI	Proportional Integral
rms	Root mean square
SOC	State of Charge
SOH	State of Health

CHAPTER 1

INTRODUCTION

With continued developments in automotive and stationary applications, large-scale energy storage technologies like battery systems are becoming a fundamental part of electric vehicles and modern electric grids. Battery packs offer portability and high energy density for electric-drive vehicle, aerospace, and military applications [1–4]. Furthermore, battery packs are a growing part of reliable and efficient power systems because they best address the reliability and flexibility needs of today's grid and improve its operating capabilities [5–9]. For many years, the expanding demand for battery energy storage in these ever diversifying areas has been met by incremental advancements in battery electro-chemistry. However, these advancements are often outpaced by growing demand for better performance, longer lifetime, and reduced cost for large battery packs.

Among applications in today's battery systems, electric-drive vehicles, including hybrid (HEV), plug-in hybrid (PHEV) and electric vehicles (EV) or, more generally, xEV's are the major users of large battery packs. Achieving widespread adoption of electric vehicles requires minimizing the cost, volume, and weight of the battery pack while still meeting the range and safety expectations for on-road vehicles [10]. Battery pack cost per kWh has dropped in recent years, and cell-level energy density is increasing; but we do not reap the full benefit of these advances [11–13]. This is due to the conservative operating limits applied by today's battery systems, as shown in Fig. 1.1. As a result, the full amount of a battery's energy cannot be accessed in today's state of the art battery system. The battery packs used in today's electric vehicles are typically 1.25 - 2x larger than what would be needed if the full capability of the battery chemistry could be accessed. Developing approaches to maximize battery pack performance in a cost-effective manner remains a significant technical challenge for energy storage systems.

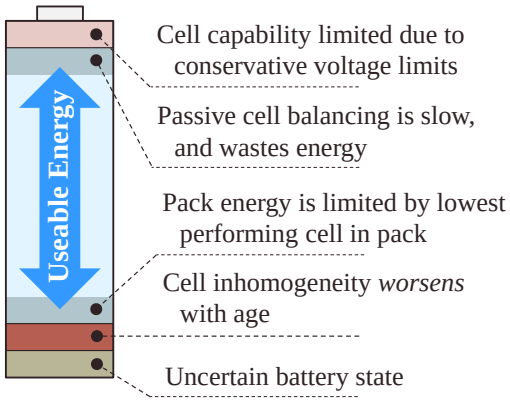


Fig. 1.1: Key limitations of today's battery systems.

Recent progress in power electronics and adaptive control algorithms present opportunities for battery pack developers to rethink battery system architecture and holistically optimize the existing components around the battery pack. This chapter takes a look at the challenges and limitations of today's battery systems and explore opportunities that can significantly improve battery pack performance and lifetime.

1.1 Today's Battery Systems

A key challenge in today's battery system is that battery pack consists of a string of individual battery cells connected, and managed in series [4]. No two cells within the pack are physically identical due to manufacturing and aging differences, and the circuit configurations used today limit the capacity of a string of cells to the weakest cell in that string [14–16]. As a result, the pack's performance and lifetime are limited to the weakest cell in the pack.

A general implementation of a complete battery system consists of a large high-voltage (HV) battery pack as the primary energy storage, a battery management system (BMS) to keep the HV battery in a state in which it can fulfill its functional design requirements, and one or more dc (or ac) bus to supply loads. A traditional battery system with a large battery pack, a central BMS, and single (or multiple) power processing dc/dc (or dc/ac) converters is shown in Fig. 1.2. In xEV applications, the HV battery pack provides power from tens

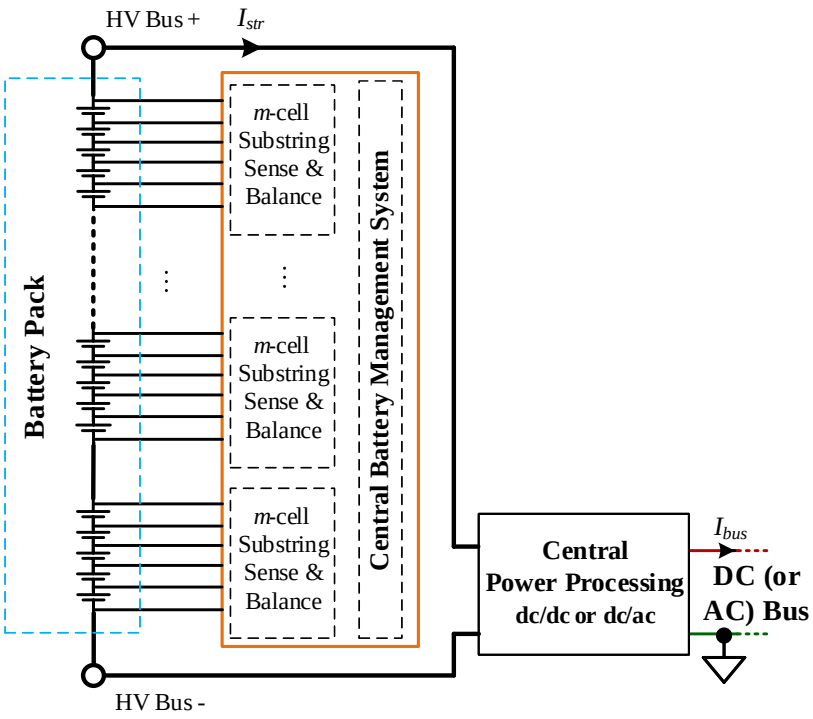


Fig. 1.2: Typical battery system made up of a large, high-voltage (HV) battery pack, a central battery management system (BMS), and one or more power processing dc/dc (or dc/ac) converters.

to hundreds of kilowatts to the vehicle drivetrain and supports auxiliary low-voltage (LV) loads inside the vehicle using a high-power, high step-down dc/dc converter, as shown in Fig. 1.3.

To meet high voltage and power requirements in vehicle and stationary applications, a large battery pack is made up of series and parallel connection of individual battery cells. The series connection of cells creates a built-in sensitivity and limitation due to mismatch of cell parameters such as capacity, series resistance, and self-discharge rates. The cell mismatch is inherent in manufacturing and can range from 1% to 10% at the beginning of life depending on the quality of manufacturing and level of cell binning applied [14,17,18]. Even more importantly, cells do not degrade evenly throughout life due to growth of the initial mismatch, temperature distribution, and other physical asymmetries across the battery

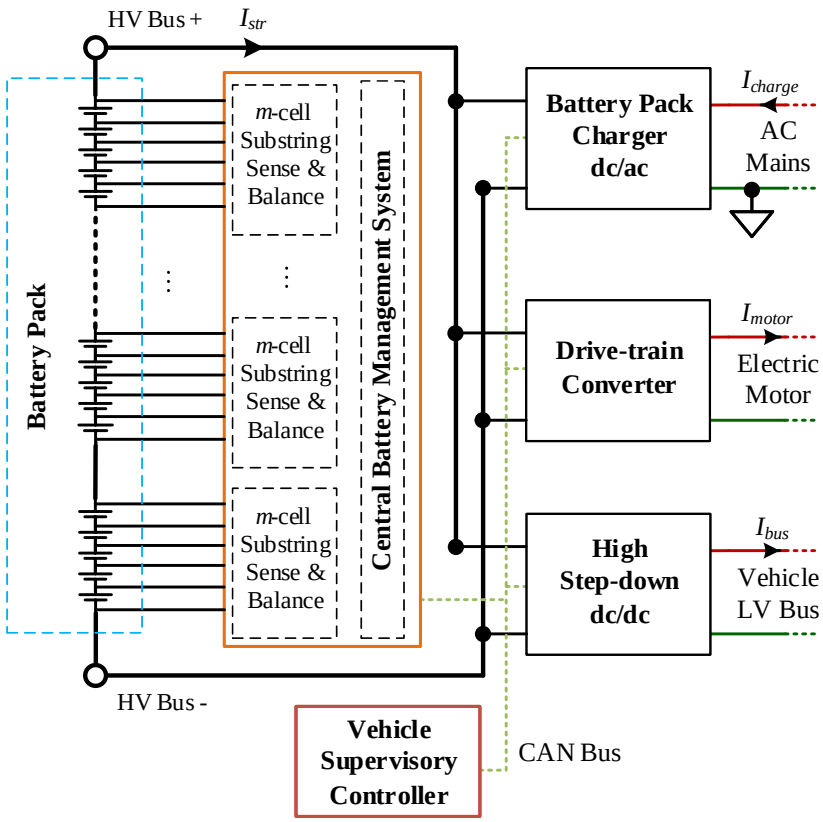


Fig. 1.3: Example of a traditional xEV battery system employing a large HV battery pack, several power converters to interface the battery pack to drivetrain, auxiliary loads, and a charger.

pack. These assymetries result in a parameter mismatch that can exceed 10% at end-of-first-life (EOL) for the pack [1, 19, 20]. The primary challenge is that the EOL is typically determined by the worst-case cell in a series connected string, and thus cell mismatch creates a significant reduction in the effective lifetime of a battery pack, as shown in Fig. 1.4 [1].

To mitigate the impact of mismatch among cells during charge and discharge cycles, one of a multitude of cell balancing systems are incorporated into the BMS in large battery packs [15, 21–24]. At a minimum, voltage balancing of cells must be performed periodically to avoid collapse of the available pack energy [25–27]. This is due in part to the set

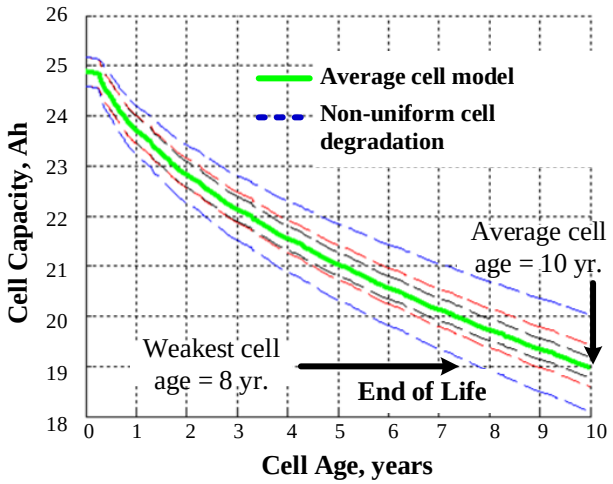


Fig. 1.4: Battery pack age is limited due to cell imbalance growth during pack lifetime. Pack end-of-life is reached when the weakest cell can not provide more than 75% of initial rated energy [1].

limits that cells are operated within, resulting in a divergence of cell state-of-charge with repeated charge/discharge cycles. Commercial battery packs include some form of battery cell balancing (active or passive) for this purpose. In spite of higher losses and performance limitations, many commercial systems today employ simple cell voltage balancing control using passive cell balancing circuits, where a sequential process is performed during charging to passively dissipate the excess energy of cells that reach the maximum voltage limit first [21]. This control method meets the basic requirement with a simple hardware structure. However, the approach still results in a pack that is energy and power limited by the worst case cells throughout life and most importantly at EOL, as shown in Fig. 1.4. The approach also requires wiring harnesses with bundles of wires to pass sensing of all cell voltages and temperature, and passive switch control networks to a central BMS controller.

Among balancing circuits used in today's BMS, active balancing is another balancing topology that matches cell voltage (or charge) through charge redistribution among cells within the pack rather than passively dissipating the energy of higher voltage cells [15,22,28]. The clear advantages are lower energy losses and reduced heat dissipation. However, the battery control objectives of active balancing circuits are the same as for passive balanc-

ing circuits. As a result, the approach still results in a pack that is energy and power limited by the worst case cells at EOL. Many circuit topologies have been proposed to actively shuttle energy from cell to neighboring cell using inductive, capacitive, or combined switching circuits [15,23,26]. The major limitations of existing active balancing systems are complex architectures, limited power processing capability, higher cost, and slow balancing speeds [28,29]. Active balancing circuits are progressively becoming more popular due to new opportunities for cell-level monitoring and control; however overall system benefits are yet to be fully demonstrated [30,31].

In addition to a large battery pack and a BMS, most battery systems employ some form of dc/dc or dc/ac power processing converters. For instance, xEV's employ a high power dc/dc converter to boost the battery voltage and process power for the traction inverter that interfaces with the propulsion electric motor. In addition, xEV's also require a high step-down, 1-3 kW rated dc/dc power converter that provides an interface between the HV battery pack and vehicle LV bus. The LV bus is connected to auxiliary loads inside the vehicle that include lighting, electric fans/pumps/compressors, and instrumentation electronics and an auxiliary (commonly lead-acid) LV battery [32]. There are a variety of engineering challenges related to the design of power converters used inside today's battery systems. For instance, the HV-to-LV dc/dc converter inside an xEV has high input voltage, high step-down conversion ratio, and large output current rating which result in cost, efficiency, and size trade-offs. Most commercial xEV HV-to-LV dc/dc converters have a moderate to high cost and size, and they achieve up to 90% efficiency.

1.2 Design Merits for New Battery Systems

Most of the commercial applications utilizing battery technologies, including automotive industry, are extremely cost and size conscious and continuously seek hardware and control approaches that lower cost/size and improve performance of battery systems through system design and architecture, component design and development, controls and algorithm development, and manufacturability and reusability. Before investigating new designs for battery systems, general evaluation guidelines for a practical battery system are summarized

here.

1. Any new hardware or control approach should at least retain system-level functionality of today's battery system that includes cell-voltage balancing, and power and energy delivery at specified voltage-levels.

2. Reduction in size, weight, and cost are considered favorable.

3. Size and cost of the battery system can be offset via performance gains, and lifetime extension for the battery pack.

   (a) Performance gains can be characterized as improving the efficiency and/or speed of cell balancing process, or expanding the energy utilization and/or power capability of the existing battery pack.

   (b) Lifetime extension can be described as new hardware or controls that enable longer lifetime for the same battery pack under the same energy and power requirements.

4. Ability of hardware (or controls) to quickly adapt to different battery size, chemistry, and balancing algorithms without the need to significantly re-design is desired.

5. Ability to easily re-use and reconfigure for different applications can be significantly advantageous. For instance, after end of first life, xEV batteries can be deployed for second-use in stationary applications such as electric grid. Modularity in hardware and readily available knowledge of battery's current state-of-health is required for such re-use.

1.3 New Concepts for Modular, Scalable Battery Systems

Advances in power electronics hardware and control software provide opportunities for significant improvements to battery systems. Though benefits may be accrued from incremental improvements in individual components of a battery system of Fig. 1.2, even greater benefits are obtainable by rethinking the battery system architecture at a system-level. This

work focuses on integration of several BMS-dc/dc functions, and unique modifications to the architecture, many of which focus on the performance limitations inherent in today's battery system.

1.3.1 Dissertation Contributions

The aim of this dissertation is to present new concepts for battery system architecture and control to improve performance and lifetime of battery systems used in xEV and stationary systems. This work presents an opportunity and approach to expand the benefit matrix and reduce the relative cost of battery systems. The approach is based on combining a modular hardware architecture with distributed (or central), continuous cell-level state estimation and control. The benefit of this approach is a fully modular battery system that can be expanded to any size pack with no additional sensing, control wires or high-speed digital communications requirements. Moreover, the system adjusts loading of individual cells to achieve high-level objectives such as maximizing pack energy, power capability, and lifetime.

The novelty of this work can be summarized as follows:

1. A new modular battery system architecture that uses scalable battery modules is proposed. A conceptual diagram of the proposed system is shown in Fig. 1.5. The battery module, shown in Fig 1.6, is the fundamental building block of the modular battery system and consists of a cell brick (group of one or more cells connected in series or parallel) and a dc/dc power converter. With this architecture, cell balancing and power processing functions are integrated into each of the battery module, enabling differential power processing down to cell-level. Furthermore, the battery module can be configured in multiple ways to achieve one or more DC bus systems.

   (a) Example 1: an xEV battery system with multiple DC bus voltages (HV and LV) is realized using a combination of battery modules, as shown in Fig. 1.7. This is done by placing module's input port in series to form the HV bus and output port in parallel to form a shared DC bus. In this configuration, the power for vehicle

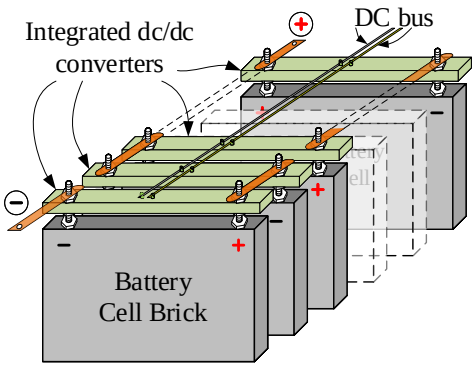
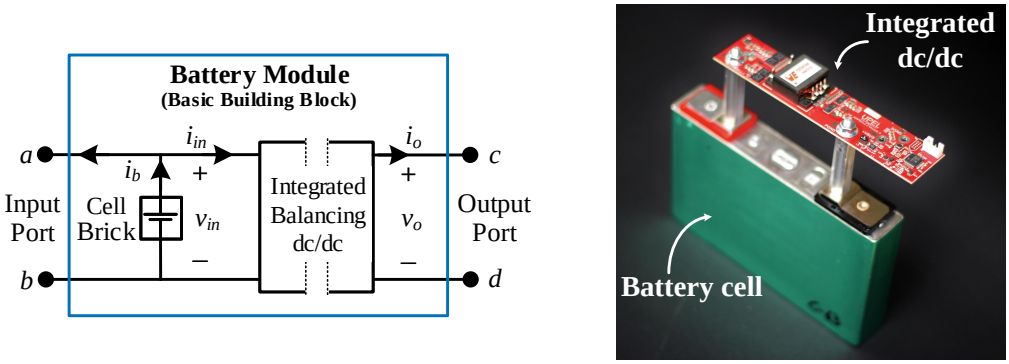


Fig. 1.5: Conceptual diagram of proposed modular system implementation.



(a) (b)

Fig. 1.6: (a) Proposed battery module, the basic building block that can be connected in various ways to achieve xEV and stationary battery systems, and (b) hardware implementation of a battery module.

propulsion is directly accessed from the series string and the vehicle auxiliary LV bus is tied to the shared DC bus. As shown in this work, this architecture offers simplicity, high efficiency, and cost gains when used for xEV applications by replacing the high step-down dc/dc converter and central BMS of Fig. 1.3 with small, low-power, low-voltage dc/dc converters of Fig. 1.7.

(b) Example 2: A more general, single DC bus system can be achieved by placing the output port of battery modules in a series-parallel combination to achieve required voltage, power, and energy ratings. The modular system, shown in Fig. 1.8, can offer great benefits when used for stationary applications like utility

and micro/nano-grids.

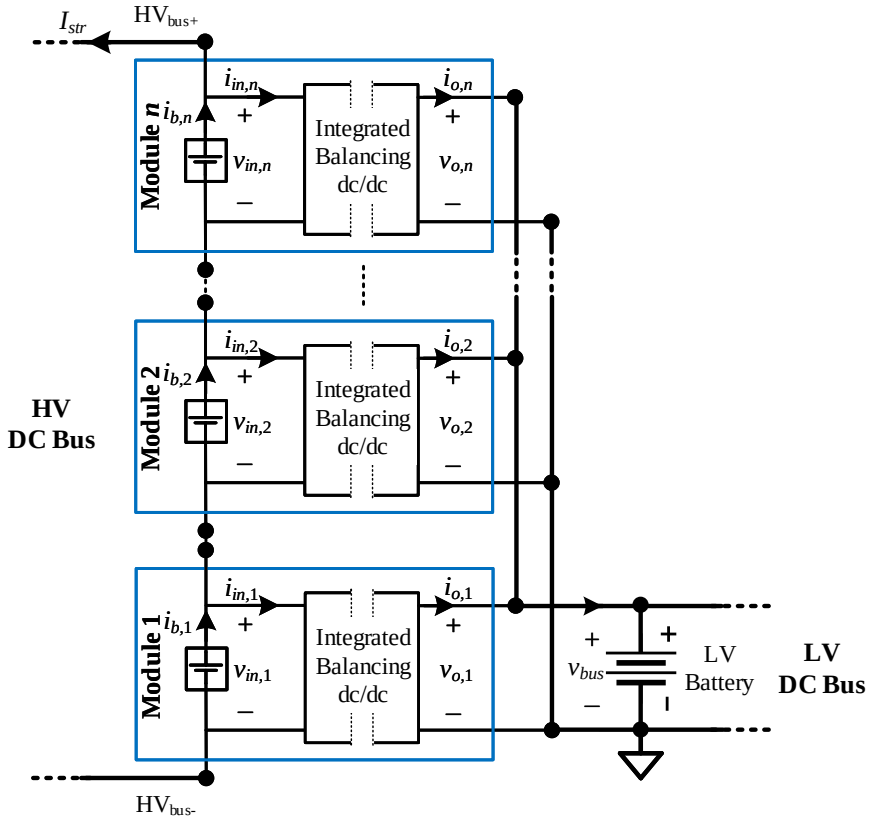


Fig. 1.7: Proposed xEV modular battery system employing several battery modules to make a HV bus for drivetrain, and LV bus for auxiliary loads.

2. New control methods are proposed for the integrated dc/dc converters used for cell balancing and bus voltage regulation functions in the modular battery system. A fully distributed control scheme is developed for the series-input, parallel-output xEV battery system shown in Fig. 1.7. A partially-distributed control approach is developed for the more general modular, reconfigurable battery system shown in Fig. 1.8. The control methods achieve reliable cell state regulation, cell current protection, and DC bus voltage regulation.

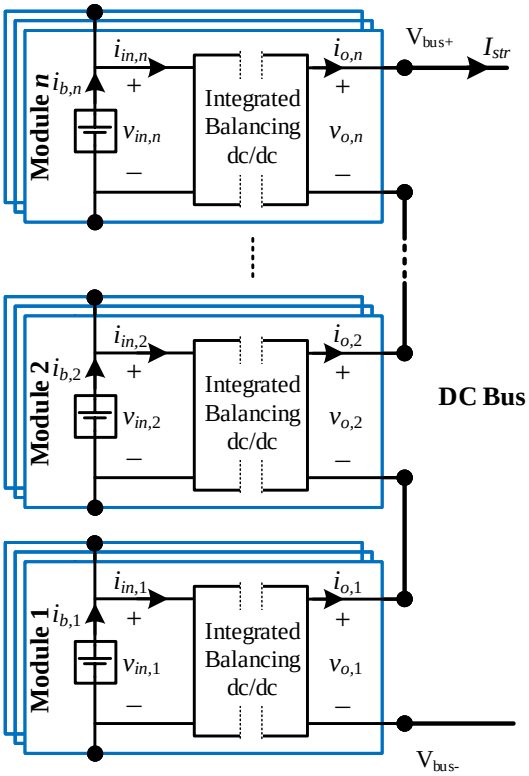


Fig. 1.8: Proposed general modular battery system employing several battery modules in parallel-series combination to achieve desired bus voltage, pack energy, and power ratings.

3. With the proposed architecture and control methods for integrated dc/dc converters, a number of existing technologies are improved upon. It is shown that accurate, online state-of-charge (SOC) and state-of-health (SOH) information, such as reported in [33–36], can be used to better control the battery system at a cell or substring level. Significant improvement in performance and extension in lifetime of battery pack can be achieved via advanced battery state control based on empirical battery life prognostic models. In addition, this opens the door to new opportunities for advanced cell-level control based on accurate physics-based cell models, enabling full utilization of previously untapped cell capability and further improvements in battery lifetime.

The original work and the results reported in this thesis contributed to projects focused on design and control of large xEV battery packs and plug-and-play battery systems. These projects were sponsored in part by Department of Energy under the ARPA-E Advanced Management and Protection of Energy Storage Devices (AMPED) program and later Office of Naval Research under the GREENs program. The projects were a collaboration between a multi-disciplinary team from Utah State University (USU), University of Colorado Boulder (CU Boulder), University of Colorado Colorado Spring (UCCS), National Renewable Energy Lab (NREL), and Ford Motor Company.

The modular system approach, design and control of integrated dc/dc converters, and cell balancing methods developed in this dissertation were applied on a 7.5 kWh (Li-ion NMC) Ford Plug-in Hybrid Electric Vehicle demonstration pack, shown in Fig. 1.9. This battery pack was used to validate the circuit design and control, and assess the value of advanced battery balancing methodology. The modular system approach was applied to one half of the pack with forty-two cells, and commercial passive balancing was applied to the other half of the pack for A/B comparison. With more than two years of accelerated dynamic cycling, the battery pack demonstrated significant improvement in battery lifetime. The modular system with advanced cell balancing control reduced cell capacity imbalance to half of that presented by the standard passive balancing system. While the pack did not reach end of life during this project, the degradation rate for battery half-pack with

Fig. 1.9: A commercial 7.5 kWh xEV battery pack that was used for A/B comparison between traditional passive balancing and the new concepts proposed in this thesis.

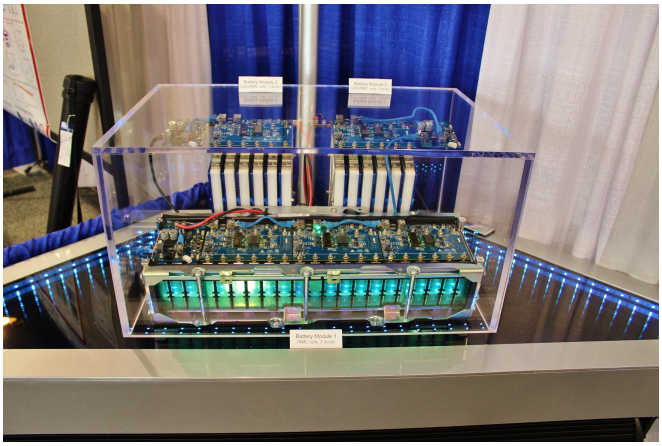


Fig. 1.10: A scaled micro-grid system with one 1.7 kWh Li-ion NMC battery pack, two 0.6 kWh NMC/LMO battery packs, one solar PV power source, and a few electronics loads that was used to demonstrate plug-and-play concepts proposed in this thesis.

the proposed system was projected to a 25% increased lifetime. Furthermore, the on-pack demonstration established that integrating power electronics into the battery pack can reduce cost, improve usable energy density through better capacity utilization, and improve lifetime for energy storage systems. This has put this technology on the development path for xEV manufacturers, but continued development activities for on-vehicle demonstration and manufacturing scale-up are required before wide deployment.

The concepts introduced in this dissertation were also extended to plug-and-play battery systems for stationary applications. A scaled micro-grid system with one 1.7 kWh Li-ion NMC battery pack, two 0.6 kWh NMC/LMO battery packs, one solar PV power source, and some electronic loads was demonstrated in lab, as shown in Fig. 1.10. Hardware experiments verified several features of the system including hot-swapping a battery pack or internal module, mixed-chemistry pack operation on a shared DC bus, power and energy sharing based on pack capability, and advanced lifetime control within each pack. The mixed-chemistry, plug-and-play concept demonstration established that integrating power electronics into the battery packs for stationary applications can reduce cost, improve system performance through better battery pack utilization, and improve lifetime for energy storage systems.

1.3.2 Dissertation Organization

This dissertation is organized into the following chapters.

Chapter 2 This chapter provides a broad overview of today's state of the art battery systems, focusing on the need for cell balancing in large battery packs and the performance of traditional cell balancing algorithms and circuits used in today's BMS. The chapter continues with an overview of battery system architecture and power converters used in xEV and stationary applications.

Chapter 3 This chapter presents original work on new concepts for modular battery systems. The fundamental building-block battery module is presented and the approach to integrate cell balancing and power processing functions into the battery module is developed. With special emphasis on xEV and stationary applications, this chapter features detailed development of the proposed modular battery system for these applications. The chapter continues with an investigation into power converter topologies to implement the integrated balancing and power processing functions.

Chapter 4 In this chapter, new system level control methods are developed for the modular battery system. Advanced cell balancing control methods and implementation techniques are constructed. A fully distributed control strategy that uses shared DC bus voltage as a communication channel is developed for the xEV battery system. Additionally, a shared central control approach is proposed for the more general battery systems. Due to the need for easy reconfiguration, the shared central control approach is extended to achieve parallel or series output operation of dc/dc power converters.

Chapter 5 This chapter provides comprehensive discussion on modeling, control, and analysis of a modular battery system. The distributed and partially-distributed control concepts proposed in Chapter 4 are analyzed and compensator designs are provided.

Chapter 6 This chapter provides hardware design and experimental results for the concepts presented in this dissertation. This includes hardware implementation of modular battery

system, validation of control methods for the integrated dc/dc power converters, and advanced balancing methods.

Chapter 7 This chapter summarizes the contributions of this dissertation, and provides a selection of additional new research directions, some of which have been raised through initial results at the time of this dissertation.

CHAPTER 2

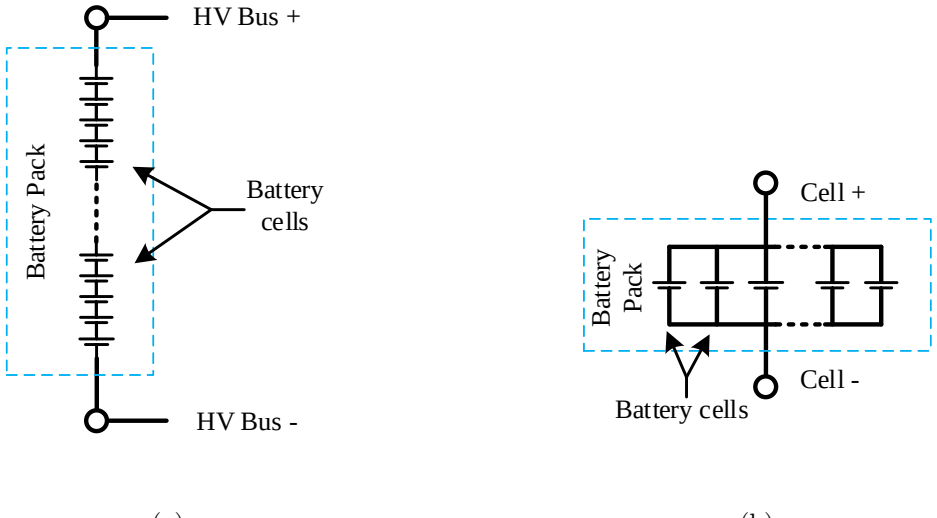
REVIEW OF BATTERY SYSTEMS

This chapter gives an overview of today's state of the art battery systems and its components that include a large battery pack, a battery management systems (BMS), and one or more dc/dc (or dc/ac) power converters. In Section 2.1, the topology of a large battery pack is discussed. In Section 2.2, battery management systems including typical battery balancing methods, and balancing circuits are reviewed. In Section 2.3, traditional battery system architectures and power converters used in xEV and stationary applications are studied.

2.1 Topology of a Large Battery Pack

Large battery packs used in both automotive and stationary applications consist of a number of individual battery cells grouped together. Battery cells are small electrical energy storage units with a typical terminal voltage range between 1 V to 4.5 V [37]. The voltage range, performance, energy density, cost, and safety characteristics of a battery cell are determined by its chemistry. For instance, Li-ion batteries offer high energy density, low self discharge rate, and high coulombic efficiency and as a result they are commonly used in size and weight conscious applications including portable consumer electronics, xEVs, and aerospace industry. Another common example is Lead-acid battery that has been used for more than a century in traditional vehicles for internal combustion engine startup. Lead-acid batteries are known for low-cost, low energy density, and ruggedness.

A single battery cell can not meet the power and energy requirements for vehicle and stationary applications due to its limited voltage and current range, and energy capacity (measured in Ah or Wh). Therefore, a large number of cells are grouped together to make a practical battery energy storage unit, as shown in Fig. 2.1 [38, 39]. Traditionally, applications with a high-voltage requirement connect large number of battery cells in series



(a) (b)

Fig. 2.1: A large battery pack with (a) series-connected cells to form a high-voltage (HV) DC bus for high-power capability, and (b) parallel-connected cells to form a super cell with high-energy capability.

configuration to form a high-voltage (HV) battery pack, as shown in Fig. 2.1a. Applications requiring high-current connect battery cells in parallel to form large capacity super cells, as shown in Fig. 2.1b. The series or parallel configuration is typically determined after taking power, efficiency, cost, and safety factors into consideration. It is common to design a practical battery pack with several small cells connected in series and parallel combination for a better cost-benefit trade off [40].

Most high power applications employ high capacity cells that are connected in series configuration to achieve high-voltage. This minimizes the battery current, keeps wire diameter small, and reduces conduction (I^2R) losses. For instance, electric-drive vehicles typically employ a 250 V - 400 V Li-ion battery pack that consists of hundreds of series connected cells capable of providing high currents [2, 41, 42].

2.2 Battery Management Systems (BMS)

Large battery packs used in xEV and stationary battery systems represent big investment and motivate additional circuitry for monitoring and protection of the pack. In

practice, battery systems employ a battery management system (BMS) that monitors state of individual cells of the pack, protects cells from damage in abuse or failure cases, and maintains battery pack in a balanced state in which it can fulfill its functional design requirements. In addition, BMS can estimate the power limits, energy capability, and state-of-health (SOH) of a battery pack and inform an application controller to make best use of the pack [43].

A general implementation of a BMS is shown in Fig. 2.2. Besides sensing individual battery cell voltage, pack current, and temperature, a key feature of BMS is cell balancing. The following subsections review why cell balancing is needed, and popular cell balancing methods and circuits.

2.2.1 Need for Cell Balancing

As discussed earlier, to meet the voltage and power requirements, a HV battery pack is made up of series and parallel connected battery cells. The series connection of cells creates an inherent sensitivity and limitation due to mismatch of cell parameters such as capacity, series resistance, self-discharge, and coulombic efficiency. The cell mismatch is inherent in manufacturing and can range from 1% to 10% at beginning of life depending on the quality of manufacturing and level of cell binning applied [14, 17, 18]. Even more importantly, cells do not degrade evenly throughout life due to growth of the initial mismatch, temperature distribution, and other physical asymmetries across the battery pack [1, 19, 20]. Charging or discharging a string of series-connected battery cells results in identical current passing through each individual cell regardless of any mismatch in cell parameters. As a result, cell state-of-charge (SOC) that is a measure of stored energy inside cell, diverges apart over time. For instance, cells may start with same SOC and capacity but because of different self-discharge rates, cell SOCs will diverge slowly even when cells are not in use. SOC imbalance can also be caused during charging or discharging because of different coulombic efficiency among cells. Since self-discharge rate, coulombic efficiency, and other cell parameters are a function of temperature, a temperature gradient across a large battery pack can lead to accelerated SOC imbalance among cells.

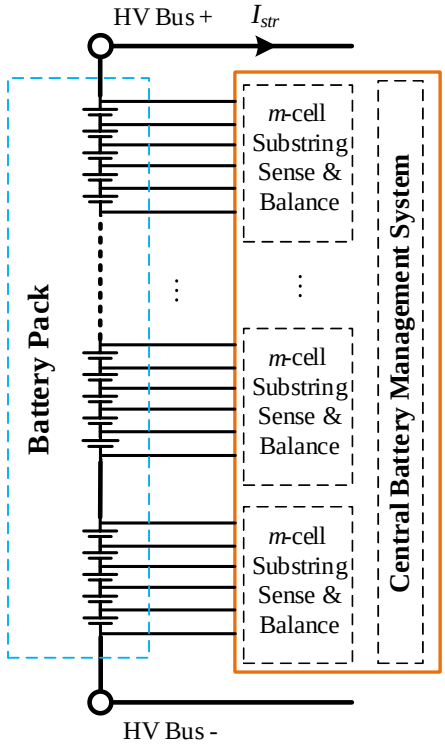


Fig. 2.2: General implementation of a battery management system (BMS) for large battery packs with series-connected cells.

SOC imbalance leads to an under performing pack and a large mismatch can even render the pack useless. A variety of SOC mismatch scenarios are shown in Fig. 2.3 for a battery pack with two series-connected cells. Under a small SOC mismatch as shown in Fig. 2.3a, the pack is operational but it can not perform to its rated capability due to limited usable energy (charge or discharge). If one of the cells is completely discharged, as shown in Fig. 2.3b, the pack is unable to discharge despite energy being available in cell 1. Similarly, if one of the cells is completely charged, as shown in Fig. 2.3c, the pack is unable to charge further despite cell 1's ability to charge more. In the very extreme case shown in Fig. 2.3d, the pack is unable to charge or discharge due to a very big SOC mismatch. Furthermore, mismatch in cell capacity leads to pack energy limited by the weakest cell. This is due to a temporary SOC imbalance caused by different cell capacities, as shown

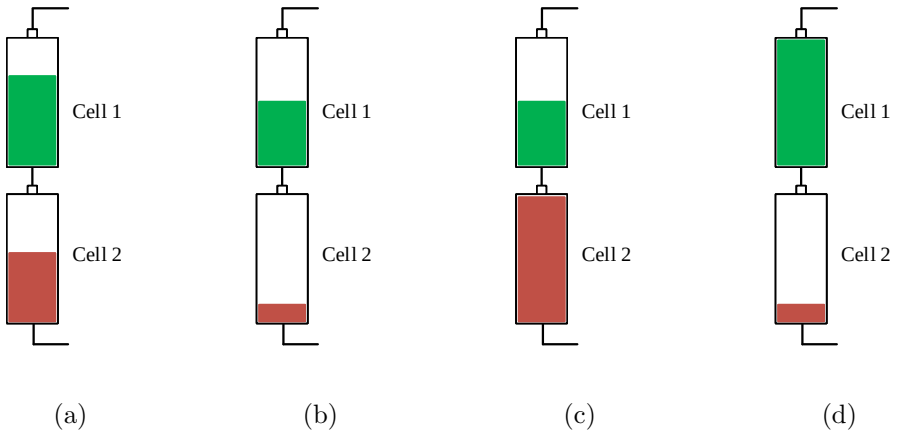


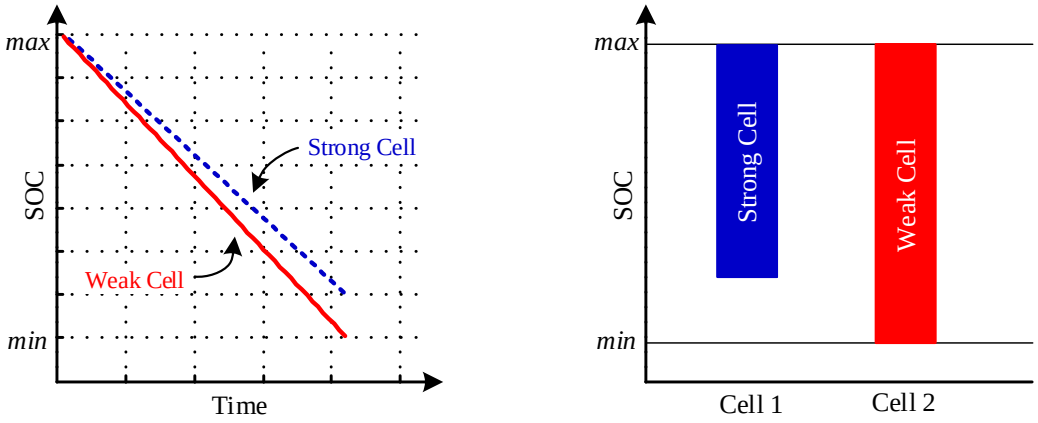
Fig. 2.3: A battery pack with two series-connected cells under different SOC imbalance scenarios: (a) pack can charge or discharge but mismatch limits usable capacity, (b) pack can charge but not discharge, (c) pack can discharge but not charge, and (d) pack can not charge or discharge.

in Fig. 2.4. For instance, consider a weak (9 Ah) cell in series with a strong (10 Ah) cell. Both cells experience identical current and as a result if both cells start at the same SOC at top-end, the weak cell will reach minimum SOC before the strong cell and thus limit the pack energy to 9 Ah, as shown in Fig. 2.4a. In contrast, if the cells were kept balanced at all points in time and SOC, as shown in Fig. 2.5, both cells would span their full SOC range and hence pack energy utilization can be improved.

To mitigate the effects of cell imbalance, BMS includes additional hardware and implements control to keep the battery pack in a balanced state in which it can fulfill its functional design requirements over its lifetime. Common cell balancing methods and associated hardware circuits are reviewed in the following subsections.

2.2.2 Cell Balancing Methods

One of many balancing strategies are incorporated into today's BMS. The choice of balancing strategy depends on associated cost, software and hardware complexity, efficiency, and need for balancing based on mismatch among cells and operating conditions. Traditionally, the BMS controller is implemented as a central supervisory controller and a series of substring balancing circuits which provide balancing functionality. A general implementa-

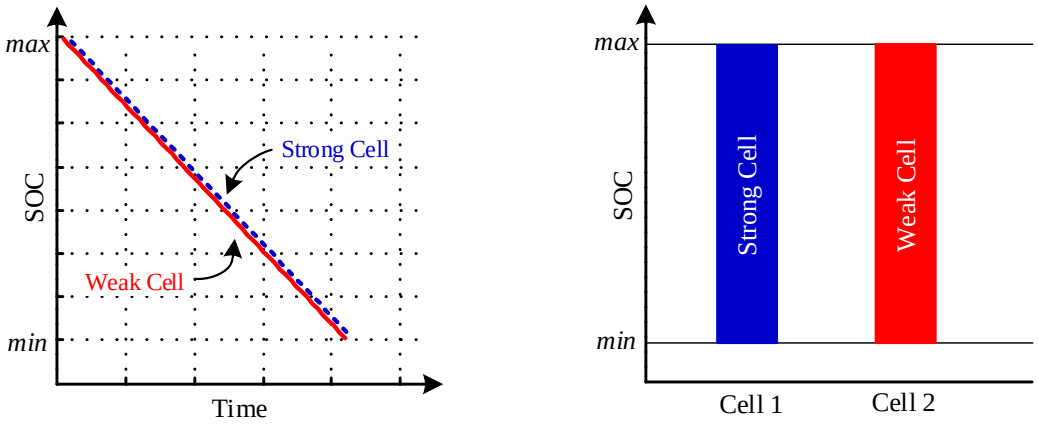


(a) (b)

Fig. 2.4: A weak (9 Ah) cell in series with a strong (10 Ah) cell starting from the same SOC at top-end under no runtime cell balancing during discharge: (a) the weak cell reaches minimum SOC before the strong cell, (b) weak cell spans *larger* SOC range than strong cell.

tion of a BMS is shown in Fig. 1.2. The objective of the central controller is to monitor and compare the state of all cells, e.g. cell voltage or cell state-of-charge (SOC), and actively or passively balance the cells using the balancing circuits [15, 21, 22, 25, 44–46].

Cell terminal voltage balancing is the simplest balancing strategy where a balancing circuit is used in parallel to each cell and excess energy of cells that reach the maximum voltage is dissipated passively or shuttled to other cells through an active circuit. Voltage balancing can be done using a very simple hardware structure and does not require much computational power since it only requires sensing cell voltage and comparing it with the minimum cell voltage in the pack to make balancing decisions. The approach is commonly used in applications that do not have a strong mismatch in cell parameters at beginning of life. However, despite voltage balancing, mismatch in cell state of health (SOH) grows over life due to temperature gradient across the pack and various other pack asymmetries. As a result, the voltage balancing approach still results in a pack that is limited by the weakest cell in the pack throughout pack lifetime. Moreover, voltage balancing is inefficient since



(a) (b)

Fig. 2.5: A weak (9 Ah) cell in series with a strong (10 Ah) cell starting from the same SOC at top-end under realtime cell balancing during discharge: (a) both cells stay balanced at any point in time and SOC, (b) SOC range or depth of discharge is *same* for both cells.

voltage is a poor indicator of SOC and the approach results in unnecessary balancing action during large current transients due to internal resistance mismatch among cells. Cell SOC balancing is another common balancing strategy where the balancing objective is to match cell SOC instead of cell voltage. Since cell SOC can not be measured directly, it is estimated using one of many SOC estimation algorithms, like Coulomb counting, and Kalman filter estimation. The SOC balancing approach results in more efficient balancing and requires computational power to estimate individual cell SOC.

Cell balancing can be performed once per cycle or in real-time. Among commercial balancing systems, it is common to balance cells once per cycle (commonly at top charge) thus ensuring that all cells are at exactly the same votlage/SOC after the charge cycle. Once per cycle balancing meets the basic balanced pack requirements but pack energy is still limited by the weakest cell, as shown in Fig. 2.4a. In addition, weak cell experiences larger depth of discharge for once per cycle balancing systems, as shown in Fig. 2.4b. As a result, balancing at top charge leads to accelerated aging of weak cells due to some cell aging mechanisms triggered by high SOC (commonly known as calendar aging) and larger

depth of discharge for the weak cell [1]. In contrast, real-time, continuous cell balancing leads to a balanced pack at all points in time and SOC, as shown in Fig. 2.5a. This results in a pack with all cells, strong or weak, experiencing same depth of discharge, as shown in Fig. 2.5b. Due to same high SOC at top-end for weak and strong cells, continuous SOC balancing still results in accelerated aging (calendar aging) for weak cells.

Balancing systems can be implemented as passive and active. Passive balancing systems dissipate excess energy from cells as heat. Based on balancing objective, the central BMS controller decides which cells need to dissipate energy and activates the balancing circuit connected to the cell. Excess energy in the cells is lost as heat in the passive balancing circuits until all cells come to a common balancing target state (voltage or SOC). Active balancing systems use ideally non-dissipative means to shuttle energy between cells in order to bring all cells to a common target state (voltage or SOC). The clear advantage of active balancing systems is higher efficiency and reduced heat dissipation.

Passive balancing systems are typically used for once per cycle balancing methods, commonly top SOC balancing which results in slow charging at top SOC, as shown in Fig. 2.6a. Real-time continuous passive balancing is disadvantageous as it leads to additional losses and heat generation due to unnecessary balancing action in response to temporary SOC mismatch produced by capacity mismatch. In contrast, active balancing can be performed once per cycle or in realtime. Due to charge shuttling, once per cycle, top-SOC active balancing is faster than top-SOC passive balancing, as shown in Fig. 2.6b. However, most active balancing systems implement runtime, continuous cell balancing, as shown in Fig. 2.6c, to allow better pack energy utilization and achieve same depth of discharge for strong and weak cells.

For lithium-ion batteries, temperature is another key factor that affects battery lifetime. Higher temperature, even though kept within safety limit, accelerates the degradation process over time. In a large xEV battery pack, cells at different locations may develop different temperatures due to heat generated inside the battery and heat transferred from external sources. As a result, uneven degradation happens and the cells with most serious

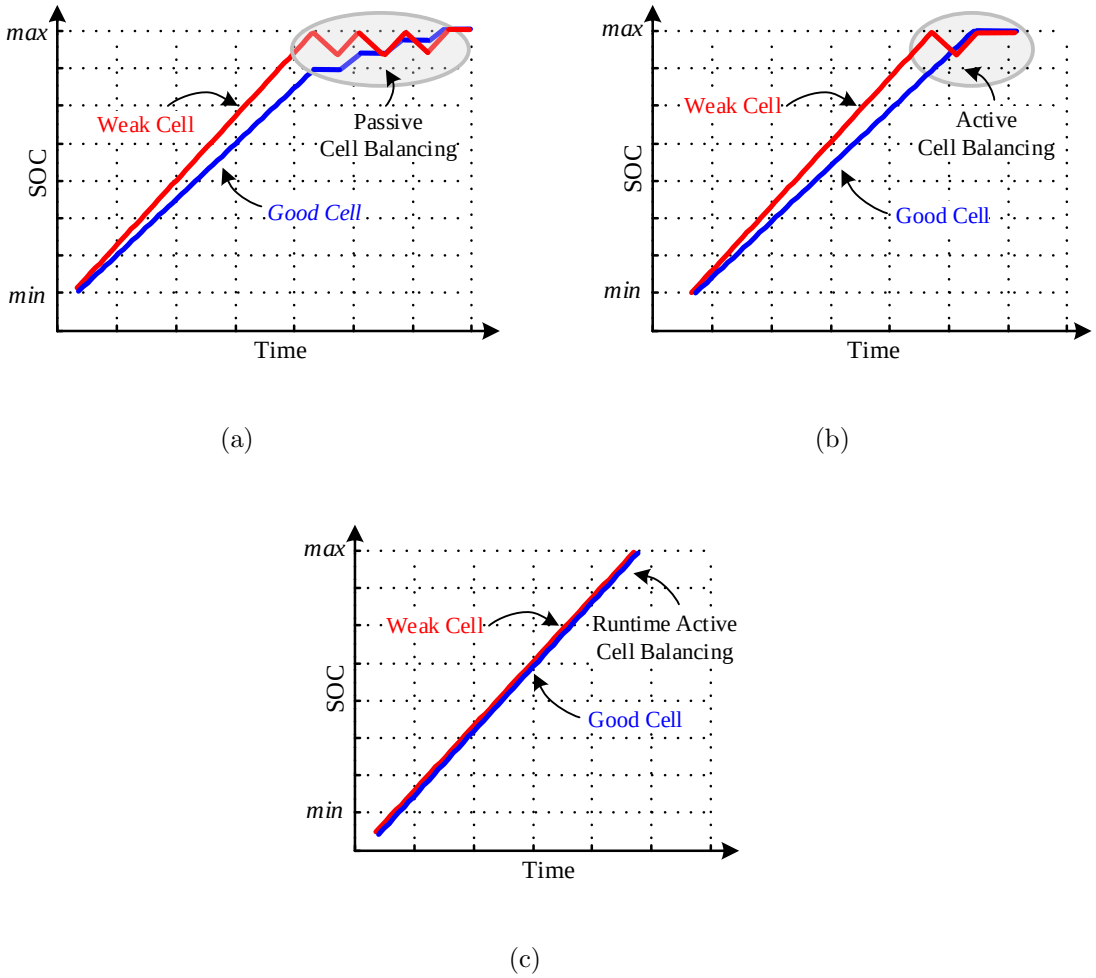


Fig. 2.6: SOC balancing using: (a) passive balancing methods that *dissipate* energy in higher SOC cell once per cycle at top-SOC , (b) active balancing methods that *shuttle* energy from higher SOC cell to lower SOC cell once per cycle at top-SOC, and (c) active balancing methods that *shuttle* energy from higher SOC cell to lower SOC cell in runtime keeping cells balanced at all times .

degradation become a limitation factor and shorten the battery lifetime. To control battery pack temperature and mitigate temperature differences within the pack, thermal management is usually applied so that excessive heat could be quickly dissipated. However, without tight cell-to-cell temperature control, variation among cells continue to expand throughout the life of the battery pack and pack performance is limited by the weakest cell in the string. This results in compromised power and energy rating, and a compromised battery lifetime.

A conventional BMS with voltage or SOC balancing is not able to alleviate the uneven degradation caused by temperature gradients across the battery pack.

2.2.3 Cell Balancing Circuits

The central BMS controller, shown in Fig. 2.2, monitors individual cell state and utilizes balancing circuits to implement balancing algorithms like voltage or SOC balancing. Balancing circuits can be categorized as passive and active. Passive balancing circuits consist of a simple switch and resistor network to dissipate the excess energy from higher voltage cells, as shown in Fig. 2.7. Based on balancing objective, the central BMS controller decides which cells need to dissipate energy and closes the switch to place the resistor in parallel to the cell. Excess energy in the cells is lost as heat in the resistors until all cells come to a common balancing target (voltage or SOC), as shown in Fig. 2.6a. Passive balancing systems require wiring harnesses with bundles of wires to pass sensing of all cell voltages and temperature, and passive switch control networks to the central controller [21]. Moreover, passive balancing resistors are designed to have large values in order to avoid instant excessive heat generation inside battery packs. This results in slow balancing speeds, limiting the speed of charging the battery pack when used for top SOC balancing, as shown in Fig. 2.6a. In spite of higher losses and performance limitations, many commercial systems today employ passive balancing circuits due to their simple hardware structure and relatively lower costs.

Active balancing systems use ideally non-dissipative means to shuttle energy between cells in order to bring all cells to a common target state (voltage or SOC), as shown in Fig. 2.6b. Active balancing methods began to appear over two decades ago [15, 22, 23, 26, 28, 29, 47, 48]. Active balancing circuits are typically implemented by adding a power converter in parallel to each cell and configuring the output of each converter to enable energy shuttling. The clear advantage of active balancing systems is higher efficiency and reduced heat dissipation. The battery control objectives of active balancing circuits are the same as for passive balancing circuits. Both systems work to balance cell voltage or SOC. However, most active balancing systems are capable of runtime, continuous cell balancing

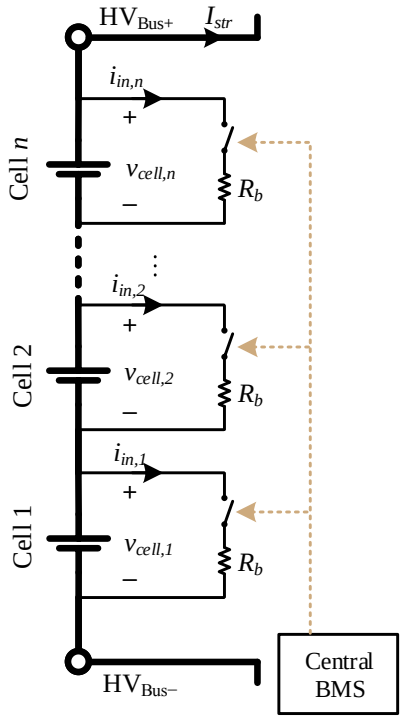
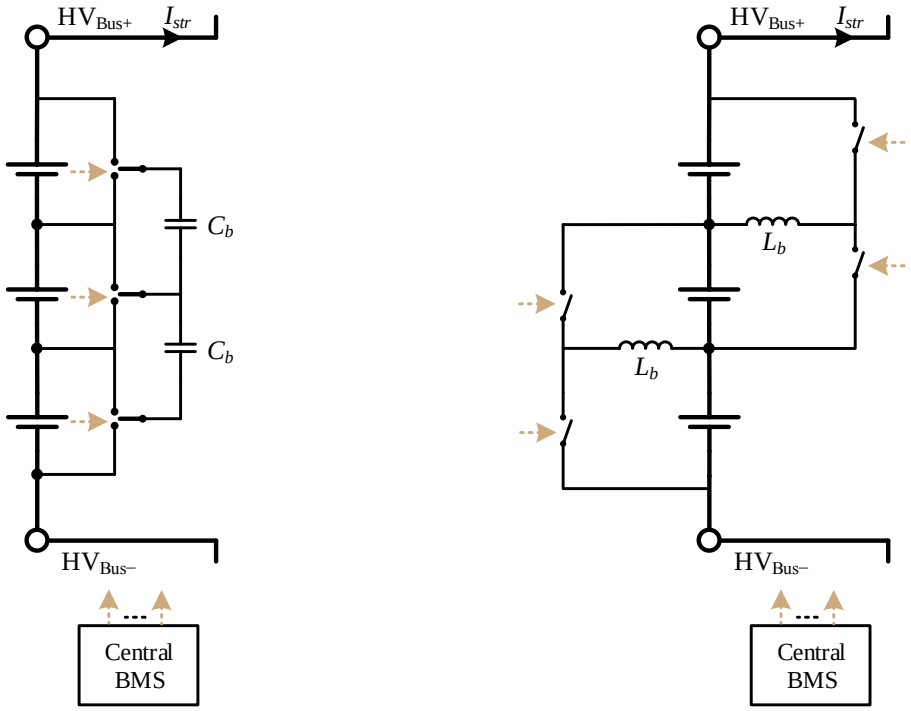


Fig. 2.7: General implementation of passive balancing circuits that dissipate excess energy using a resistor.

that allows better pack energy utilization.

In traditional active balancing systems, a basic serial balancing architecture is created with a balancing converter in parallel to each cell that shuttles energy to a neighboring cell, as shown in Fig. 2.2. Several converter topologies have been explored to optimize the design of balancing converter [21, 24, 37, 49]. The converter can be based on magnetic [23], capacitive [26], or combined elements. A multiple switched-capacitor active balancing approach is shown in Fig. 2.8a [22, 50–53]. The network of switches and capacitors is used to propagate energy from higher-voltage cells to lower-voltage cells. A similar approach using inductive elements is shown in Fig. 2.8b [48]. Both approaches create a direct path between neighboring cells to shuttle energy. However, shuttling energy between non-neighbor cells takes an indirect path which reduces the efficiency and performance of balancing system. It takes a long time to balance cells that are located physically far apart due to the long



(a) (b)

Fig. 2.8: Active balancing circuits based: (a) switched capacitors, (b) switched inductors.

balancing path and low throughput of the switching network. As a result, the major limitation of these switched network configurations is balancing speed, efficiency, performance, and large number of components. Different approaches to reduce number of components in switched capacitor or inductor networks have been explored in [21, 24, 54]. However, the proposed solutions have limited use due to slow balancing speed and lower efficiency.

Another active balancing solution to address the large number of components in the serial architectures is based on a multi-winding transformer [29, 47, 55]. Using the large multi-winding transformer, this system shuttles energy between any mismatched cells in the pack. A similar approach is to use a single balancing dc/dc converter whose input can be reconfigured between different cells [56–59]. This system has a single power converter instead of several capacitors or inductors but it still uses a switching network to reconfigure its input. Both approaches have several obstacles for practical implementation such as the limit on

the number of cells that could be balanced given the challenges of manufacturing a multi-winding transformer and a large switching network. Furthermore, the system complexity increases significantly due to complex wiring when the battery pack gets large, limiting the overall modularity of the system.

Several active balancing approaches employing bidirectional pwm or resonant power converters in parallel to individual battery cells have been explored [60–69]. These systems present a mixture of benefits and drawbacks for different battery applications. For instance, some systems improve balancing speed at the expense of higher cost [52, 53, 60]. While other systems improve balancing efficiency by incorporating more sophisticated converter topologies and control [44, 63–67]. There is a significant concern about modularity and ability of these balancing systems to scale with the battery pack [69].

Although active balancing circuits achieve better balancing performance and efficiency when compared to passive balancing circuits, present-day active balancing circuit offer small practical advantage over the low cost and simple hardware structure of passive balancing systems. To this end, active balancing is progressively becoming more popular as advanced battery cell models open doors to new opportunities for cell-level monitoring and control that is not possible through traditional passive balancing systems.

2.3 Battery System Architectures

In a traditional battery system, a large battery pack, its BMS, and one or more power converters are employed to support a variety of primary and secondary loads. A traditional battery system architecture is shown in Fig. 2.9. The power converters serve as critical interface between the battery pack and a DC (or AC) bus. These converters process the battery power to supply loads connected to the bus and optionally serve as the charging infrastructure. For instance, xEV battery system is a good example for a battery pack supporting multiple DC bus with different voltage and power requirements, as shown in Fig 2.10. xEV battery system uses a high-power drive-train converter (typically boost cascaded with 3-phase inverter) to run the electric motor. The drive-train converter is designed based on the type of electric motor and functional capability of the vehicle (pure-

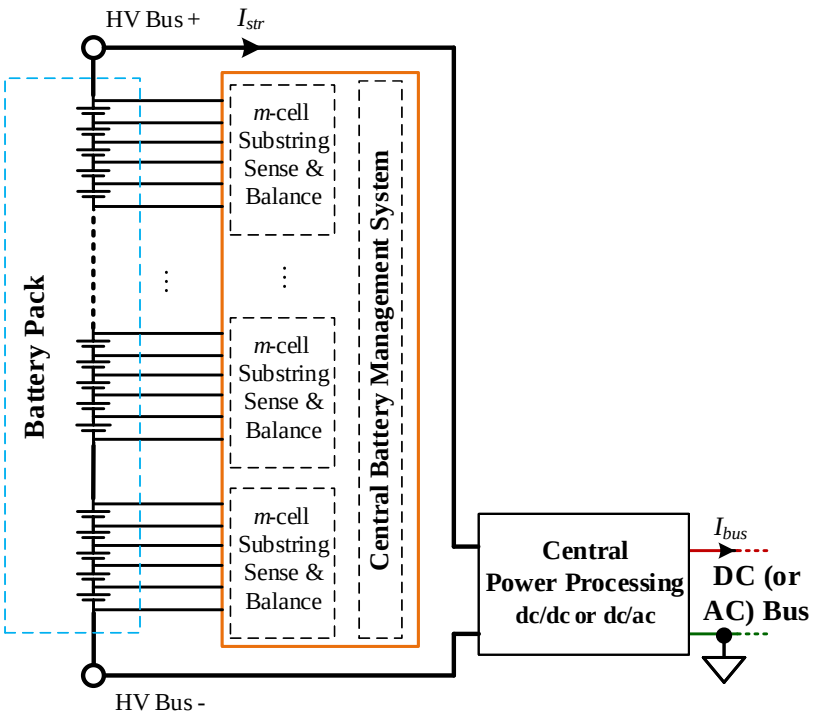


Fig. 2.9: Typical battery system made up of a large, high-voltage (HV) battery pack, a central battery management system (BMS), and one or more power processing dc/dc (or dc/ac) converters.

electric, hybrid, etc) [70–73]. In addition, a separate 2-3 kW rated high step-down dc/dc converter supplies auxiliary loads inside the vehicle. The high step-down dc/dc converter is required to supply a LV 12-16 V DC bus for auxiliary loads, such as lighting, electric fans/pumps/compressors, and instrumentation electronics [74–78]. Moreover, xEV battery systems employ a separate built-in or external ac/dc converter to charge the xEV battery pack. In existing xEVs, the battery balancing system and power converters are designed and operated independently. A vehicle supervisory controller ensures battery pack limits are observed and all components work within safety limits.

Stationary applications such as micro-grids require the use of similar bidirectional power converters as interconnects between battery packs and DC (or AC) bus [6–9]. One example of such systems employing solar PV panels and a backup diesel generator to support

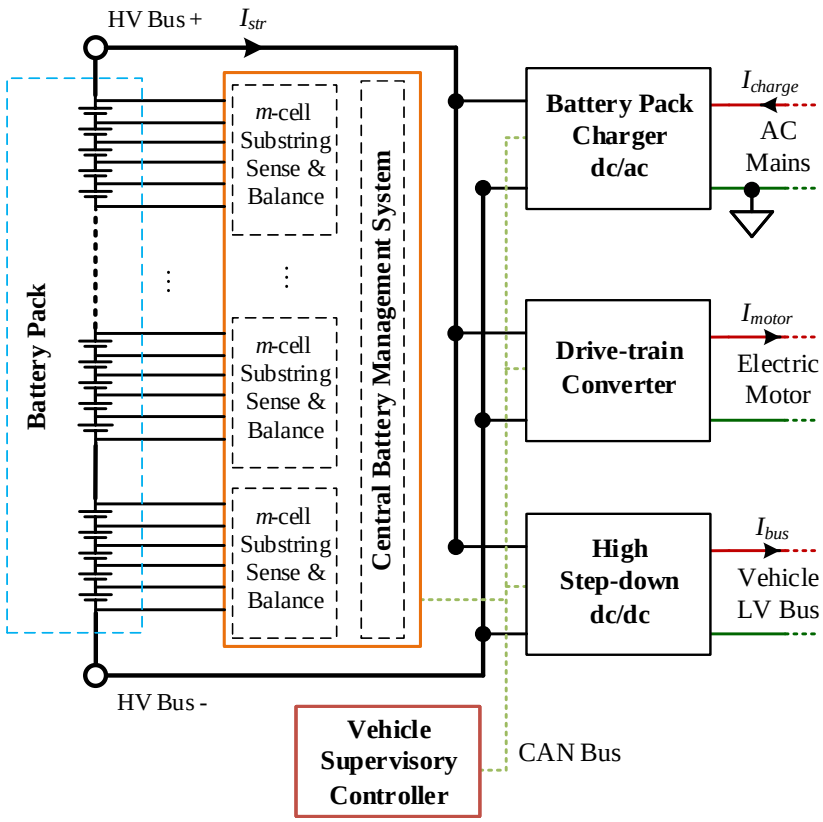


Fig. 2.10: Example of an xEV battery system employing a large HV battery pack, and several power converters to interface the battery pack to drivetrain, auxiliary loads, and a charger.

loads is shown in Fig. 2.11. In addition, an optional dc/dc converter can be used between battery pack and DC bus for safety, protection, and better battery control. Past studies have explored several different architectures, converter topologies, and control methods to optimize the system performance and improve benefits [79–87]. Approaches investigating system architecture and control have primarily focused on using a large series-connected battery pack and proposed control schemes to improve interaction between power converters [84–87]. There has also been a lot of interest in improving the power converter efficiency and optimizing the converter topology for better cost and performance [81–83]. Commer-

cial battery systems, use a central controller to supervise the power converters and manage the battery SOC or voltage [85, 88]. The converters are designed based on voltage, power, and isolation requirements and typically regulate the output voltage (or current). Engineering challenges are related to the high input voltage, potentially high step-down, and large power and current rating of the dc/dc converter, which result in cost, efficiency and size trade-offs

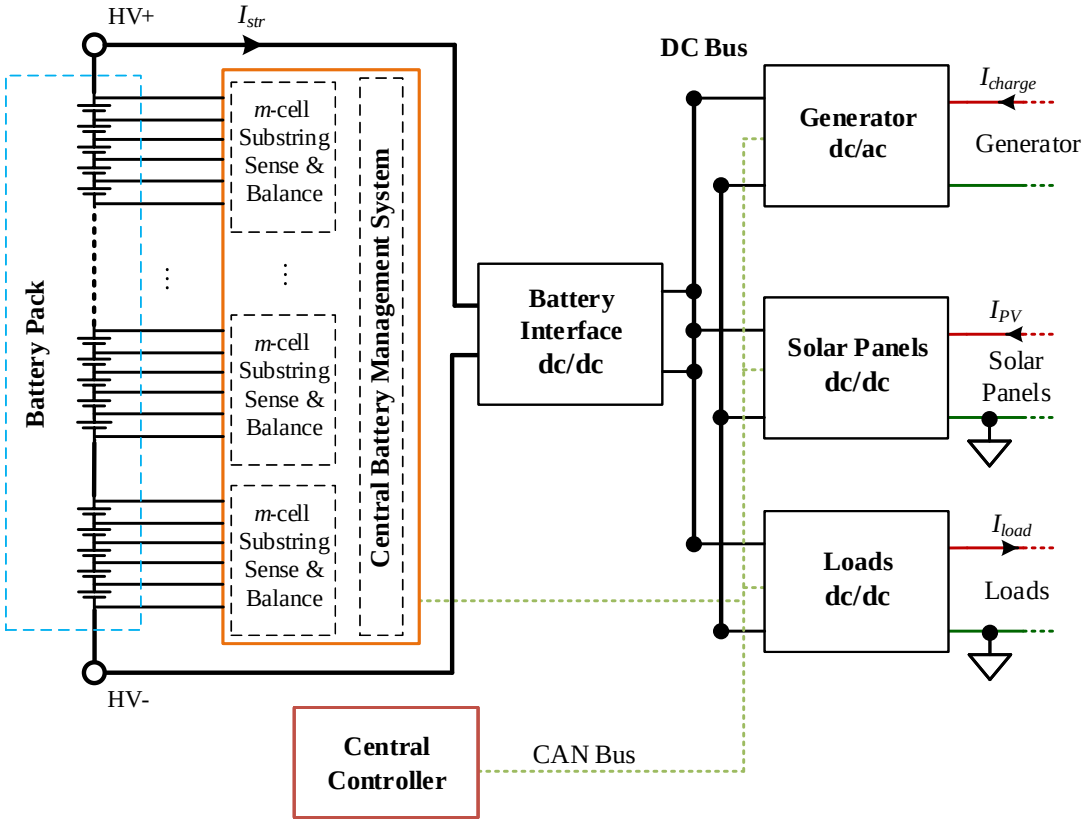


Fig. 2.11: Example of a stationary DC mirco-grid battery system employing a large HV battery pack, and several power converters to interface the battery pack to solar PV, loads, and a backup generator.

While many studies have been done on optimizing existing components of battery system, very few have looked at reimagining the system architecture to allow better per-

formance, efficiency, and reduced cost [30, 89–93]. Modular designs for renewable energy and battery systems are progressively being explored. The concept of modular design has been previously demonstrated in solar PV applications with emphasis on maximum power tracking and improved energy capture [89–92]. An isolated port architecture has been explored for solar PV systems using low-voltage, isolated power converters that can process differential power for each solar panel [89–91]. Similar approach with full power processing series-stacked power converters has been shown in [92]. Modular battery systems utilizing high conversion ratio dc/dc converters have been proposed but high step-up/down conversion ratio leads to trade-offs between voltage stress and efficiency. To avoid high conversion ratio, a modular design with series-stacked power converters is investigated in [30, 93]. Different from other battery systems, the modular converters need to process full battery cell current and hence require very high efficiency and reliability for practical usability.

2.4 Summary

Large battery packs used in vehicle and stationary applications are often designed as a single unit with several cells connected in series and parallel combination. The series connection achieves a high-voltage battery pack that minimizes battery current and conduction losses. However, the series connection creates an inherent sensitivity and limitation due to mismatch of cell parameters such as capacity, series resistance, and self-discharge rate. The cell mismatch is inherent in manufacturing and can range between 1% and 10%. Furthermore, over the age of the pack, individual battery cells age unevenly due to temperature differences and other asymmetries across the pack. As a result, battery pack lifetime is typically determined by the worst-case cell in the pack, and thus weak cells end up as the limiting factor for the whole pack. In existing systems, the entire battery pack is replaced once the weakest cell in the pack reaches a certain available capacity limit. For instance, most xEV manufacturers replace battery packs after the remaining capacity of the pack reaches 75% of the original value. This leads to under-utilization of healthier cells in the pack and adds system cost.

Commercial battery systems employ battery management systems to keep the battery

pack in a balanced state in which it can fulfill its functional design requirements. Several different balancing methods including cell voltage and SOC balancing have been explored in literature. While these balancing methods meet the basic requirement to keep the pack operational, they do not counter any battery cell degradation effects that occur due to time spent at high SOC, temperature gradients, and depth of discharge. Furthermore, commonly used passive balancing circuits drain excess energy as heat from cells to achieve balancing objectives, thus increasing the pack thermal balancing requirements. In spite of higher losses and performance limitations, passive balancing systems are popular in today's xEV and stationary energy storage systems due to their remarkable low cost and simple structure. In contrast, active balancing circuits offer higher efficiency and faster balancing speeds but market adoption is low due to higher cost and complexity. Active balancing is progressively becoming more popular due to new opportunities for advanced cell-level monitoring and control that are not possible through traditional passive balancing systems.

In addition to a large battery pack and its BMS, today's battery systems employ one or more power converters to support a variety of loads. The power converters are designed to provide an interface between a DC (or AC) bus and the battery pack. The engineering design challenges of power converters include high input voltage, potentially high conversion ratio, and large current and power ratings. These challenges result in cost, efficiency and size trade-offs. Furthermore, existing battery system components are designed and operated independently and as a result the system still results in a battery pack limited by its weakest cell throughout life. While modular battery pack designs have been explored recently, system benefits and practical usability has not been demonstrated.

To this end, today's battery pack is underutilized due to poor balancing methods and circuits resulting in oversized packs and no clear second-use for xEV battery packs. As a result, there is strong motivation to rethink battery system architectures and optimize battery packs and the existing components around them as a complete unit.

CHAPTER 3

ARCHITECTURE FOR MODULAR, SCALABLE BATTERY SYSTEMS

In the previous chapter, state of the art battery systems were reviewed. A common feature among traditional battery systems has been use of a large series-connected high-voltage (HV) battery pack that is managed by a central battery management system (BMS). Despite conservative safety limits applied to cells, the large battery pack is often limited by the weakest cell in the pack and is underutilized in its power and energy capability, reaching end-of-life (EOL) early. This is due to the poor balancing methods and circuits used in conventional BMS which lead to uneven cell degradation, higher heat dissipation and lack of circuit's ability to implement any advanced battery control methods. The availability of battery life prognostic models and advanced battery state estimation algorithms presents opportunities for better control of individual battery cells that can offer improved pack performance and lifetime. However, the cost and complexity of active balancing circuits to implement such methods has been a major hurdle towards improved battery systems. Moreover, previous work has largely focused on optimizing cell balancing circuit topologies and balancing speeds, while system benefits and practical usability has not been demonstrated.

The work presented in this chapter is a significantly different approach towards battery systems when compared to conventional cell balancing systems. This chapter presents new concepts for battery system design and architecture which provide the capability to implement advanced control methods for cell balancing and control without significant increase in complexity or cost of the BMS. To do so, the proposed architecture integrates cell balancing and power processing functions inside fundamental building block battery modules and eliminates existing balancing circuits and some (or all) of the existing power converters in conventional battery systems. With this approach, if the battery modules can be realized with similar efficiency and cost to the existing balancing circuits and power converters, then the advantages of continuous active balancing are provided at effectively

100% efficiency and no additional cost. The proposed modular approach achieves continuous balancing of all cells, requires minimum to no control communications among battery modules, is scalable to an arbitrary number of battery cells and naturally shares the load current according to the relative state-of-charge (SOC) and state-of-health (SOH) of the battery cells. Moreover, the modular battery pack can be built and configured to achieve the system level functionality of traditional xEV or stationary battery systems.

3.1 System Architecture with Integrated Cell Balancing and Power Processing

A new modular battery system architecture that uses reconfigurable battery modules is proposed. A conceptual diagram of the proposed system is shown in Fig. 3.1. The battery module, shown in Fig 3.2a, is the fundamental building block of the modular battery system and consists of a cell brick and an integrated dc/dc power converter. The module integrates a power converter on an individual battery cell which can now process power based on the SOC or SOH of the cell. As a result, the balancing and power processing functions are integrated into the dc/dc converter, enabling power processing down to cell-level. With this approach, cell lifetime and performance can be maximized via advanced battery balancing methods that were previously not possible due to the limited capability of conventional balancing circuits.

Unlike the high-power, high-voltage converters employed by traditional battery systems, the integrated dc/dc power converter employed in battery module is a low-voltage (LV) and relatively low-power converter. The converter can be designed to process a fraction of cell power or full cell power based on application and load power requirements. The battery module also includes a group of one or more cells connected in parallel called a cell brick. Ideally, a cell brick will be composed of a single cell. However, for higher energy or current capability several small cells can be grouped in parallel to make a high capacity super cell. Due to the parallel connection, all cells within the cell brick experience the same terminal voltage and balancing need within the cell brick is alleviated inside the module. For simplicity, a physical cell and a battery cell brick are both referred to as a battery cell in this work.

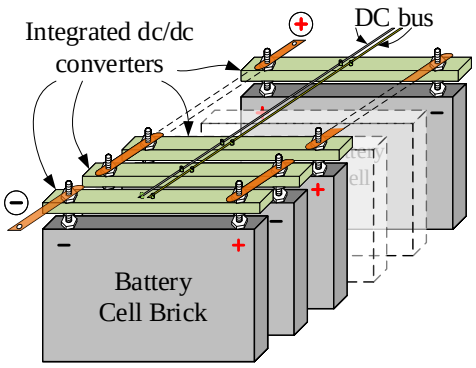
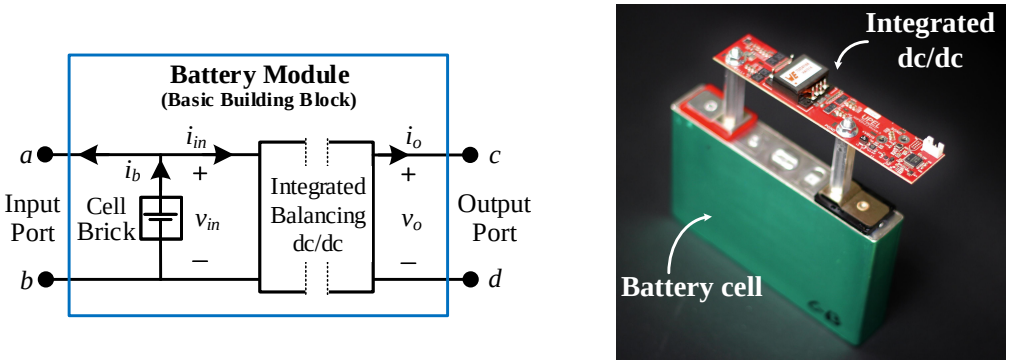


Fig. 3.1: Conceptual diagram of proposed modular system implementation.



(a) (b)

Fig. 3.2: (a) Proposed battery module, the basic building block that employs a battery cell brick and an integrated dc/dc power converter, and (b) an example hardware implementation of a battery module with one battery cell and an integrated dc/dc converter.

The basic battery module opens opportunities for new system architectures. The input and output port of the module can be configured in various ways to achieve one or more DC bus system. The input port {a, b} of battery module is shared between cell terminals and input terminals of integrated dc/dc converter while the output port {c, d} is simply the output terminals of the dc/dc converter. Multiple battery modules can be connected in parallel and/or series configuration at input or output port to achieve a large battery pack with desired voltage, power and energy rating. In the following subsections, an xEV battery system and a micro-grid battery system is designed using the basic battery module.

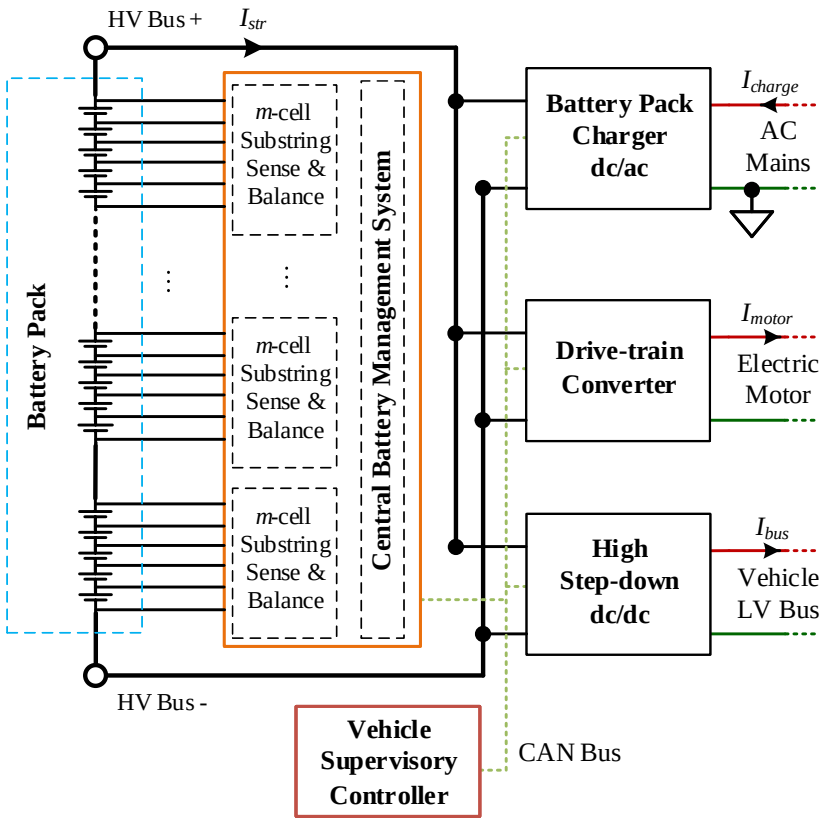


Fig. 3.3: Example of a traditional xEV battery system employing a large HV battery pack, several power converters to interface the battery pack to drivetrain, auxiliary loads, and a charger.

3.1.1 xEV Battery System

As discussed earlier in Chapter 2, a traditional xEV battery system includes a HV battery pack and BMS, a drive-train converter, a high step-down converter, and a battery charger, as shown in Fig. 3.3. The conventional xEV battery system has multiple DC buses that are used to deliver or absorb power. The drive-train converter provides an interface with a HV bus that supports propulsion and regenerative braking. The high step-down dc/dc converter connects to a LV (typically 12 V) bus that supports auxiliary loads. Stationary charging is achieved through the battery charger that can be built into the vehicle or used

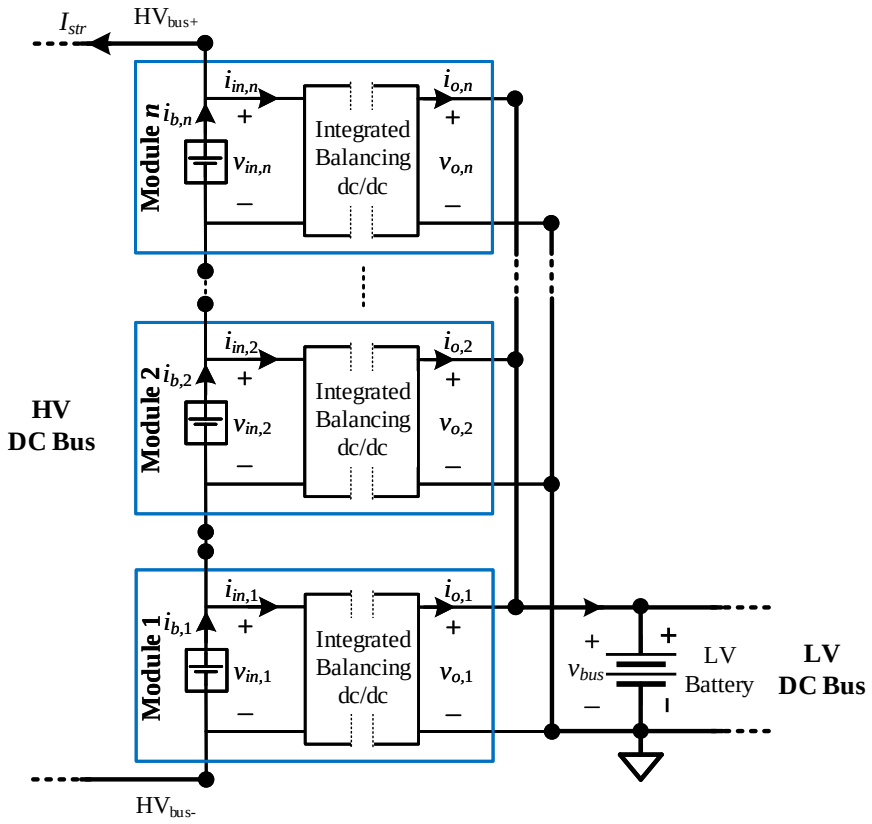


Fig. 3.4: Proposed xEV modular battery system employing several battery modules to make a HV bus for drivetrain, and LV bus for auxiliary loads.

externally. To this end, the conventional battery cell balancing system and power converters are designed and operated independently.

In this work, a modular architecture employing the battery module of Fig. 3.2 is proposed. In the proposed architecture, individual battery modules are connected in series-input, parallel-output configurations, as shown in Fig. 3.4. The battery cells are connected in a series-string to make a HV bus similar to the traditional xEV battery pack. By doing so, the vehicle propulsion and charging power can be directly processed from the series string of battery cells making HV bus. In addition to the HV bus, a shared DC bus is formed with each module's dc/dc output connected in parallel. While this shared DC bus can be used for shuttling charge between cells for balancing purposes, there is strong motivation to tie

the shared bus with the conventional LV bus inside the xEV system. With this proposed configuration, the conventional high step-down dc/dc converter functionality can now be divided among multiple dc/dc bypass converters sitting inside each battery module, as shown in Fig. 3.4. The dc/dc bypass converters experience a small step-up gain (4 V-to-12 V) and only need to process a fraction of the cell power to support the LV bus loads. The total LV bus load (typically 1-3 kW) is now divided among individual cells via the integrated balancing dc/dc converters that can act on cell-level information and reroute power around weaker cells in the string of cells to optimally deploy the stored energy. As a result, the conventional balancing circuits and high step-down dc/dc converter inside traditional xEV system are now eliminated and replaced by battery modules. Because integrated balancing dc/dc converters process only the LV bus power, they require power rating well below the cell discharge capabilities. Furthermore, this implementation permits operation with either bidirectional or unidirectional power converters. Since the unidirectional option only provides balancing functionality through division of the load on the shared bus, it does not have the additional losses and potential cell stress associated with traditional shuttling of charge between cells which is typical of active balancing circuits. If additional LV bus energy storage is required for vehicle system functionality, the LV battery, and shared LV DC bus may be connected directly or with an additional low-voltage, non-isolated near-one-to-one conversion ratio dc/dc converter. This architecture is similar to the isolated-port architecture developed for photovoltaic power systems that optimizes maximum power-point tracking via differential power processing converters [89].

Control of the integrated partial-power processing dc/dc converters is designed to produce small differences in the distribution of LV bus load among individual cells, resulting in regulated variations in each cell current which can be leveraged for runtime balancing of cells. Within some range of current limits, each dc/dc converter is controlled to regulate the cell SOC to a value consistent with the balancing reference. In this chapter, the control focuses on voltage balancing among the cells for simplicity of implementation. Balancing control based on cell estimated SOC or SOH is developed in next chapters. In the cell

Table 3.1: Comparison of conventional and proposed modular xEV battery system for an 84-cell battery pack

Parameters	**Conventional xEV battery system of Fig. 3.3**	**Modular xEV battery system of Fig. 3.4**
Power-stage isolation	Yes	Yes
Modular	No	Yes
Converter input voltage	250 - 400 V	2.5 - 4.5 V
Converter output voltage	11 - 16 V	11 - 16 V
System power	2 - 3 kW	2 - 3 kW
Converter power	2 - 3 kW	35 W
Converter quantity	1	84 (1-per-cell)
Converter output current	220 A	2.5 A
Balancing benefits	No	Yes

voltage balancing implementation, each converter has the control goal to match its own cell voltage to the average of the cell voltage in the battery pack, $v_{ref} = \frac{\sum v_{in,i}}{n}$, and is controlled to regulate its input current $i_{in,i}$ according to the difference between the individual cell voltage and target cell voltage. When a load is applied to the LV bus, the current will distribute among the modules relative to this difference. If cell voltages are balanced and have matched capacity, current distributes evenly among all modules; if a high dc gain controller is used, the system stabilizes with zero control error, i.e. with each cell voltage matched. If cell voltages are unbalanced, this control results in the power converters reducing discharge of the cells with voltage below the average voltage and increasing discharge current of cells above it, independent of the magnitude and direction of the overall pack string current. With this approach, the system can easily be scaled to an arbitrary number of cells in the pack, greatly simplifying the BMS.

The balancing action performed by each battery module requires some knowledge of the state of the rest of the battery pack (average voltage or SOC). This knowledge sharing can be achieved either through digital communications with a shared central controller or via

distributed control approach that can signal via DC bus voltage. As shown in this work, the shared central controller can be developed using partially-distributed approach employing local and central control loops that do not require very high-speed communication and still result in high bandwidth battery current control at the local dc/dc level. In contrast, a fully distributed approach can alleviate digital communication requirements necessary to produce correct division of LV bus load among cells. Instead of digital communications, the distributed approach uses the shared LV bus voltage itself as a means of communicating the balancing target (average voltage or SOC). Since the LV bus voltage itself is used to communicate the reference target for each dc/dc converter, V_{bus} must be allowed to vary proportional to the cell state of interest, which is the cell voltage for the case of voltage balancing. The nominal voltage and total variation can be set arbitrarily by the control law, but the variation must be sufficiently large to avoid noise limitations. In xEV system, the nominal bus voltage can be set close to $V_{bus} = 14$ V and use the control goal $V_{in,i} = KV_{bus}$. With typical Li-Ion battery cell voltage characteristics, this results in a bus voltage range of 11-16 V. This range is within what is typical of the LV bus of electric vehicles (11-17 V) [74]. Within the distributed approach, a modified central supervisory control may still be employed to perform higher level safety control objectives, depending on the specific goals of the system.

3.1.2 Micro-grid Battery System

Bidirectional power applications including renewable energy systems and DC micro grids employ various energy sources to supply loads on a common DC bus. Due to the intermittent nature of most renewable sources, an energy storage device is employed to share the load power during peak load or partial renewable generation conditions. Traditional DC micro-grid systems employ high-voltage, high-power converters to connect large series-connected battery packs to a DC bus. An example architecture of today's micro-grid system is shown in Fig. 3.5. The system includes several dc/dc (or dc/ac) power converters for loads, solar PV, and a backup generator. The battery interface converter serves as a safe interface between DC bus and battery. The battery pack energy storage is primarily used

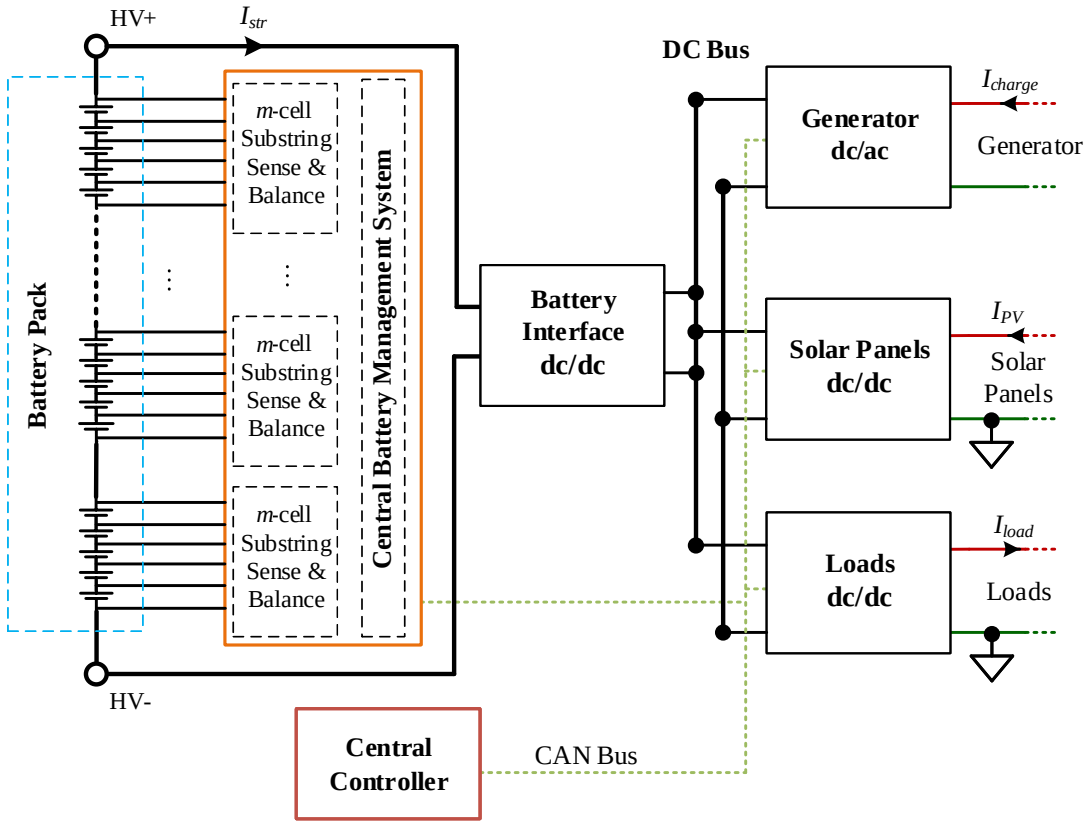


Fig. 3.5: Example of a traditional DC micro-grid battery system employing a large HV battery pack, several power converters to interface the battery pack to loads, solar PV, and a backup generator.

to offset peak loads and achieve stable operation at conditions where intermittent sources like solar PV can not meet the present power demands. The challenges of using a large series-connected battery pack including cell balancing and uneven cell degradation over lifetime are very similar to the conventional xEV system. The large battery pack requires a BMS and balancing circuits to keep the battery pack in a balanced and operational state. Furthermore, the balancing methods and circuits used in the BMS still result in a pack limited by the weakest battery cell in the series string.

There is also a significant interest in sharing multiple localized energy storage components across the DC bus in bidirectional power applications including renewable energy

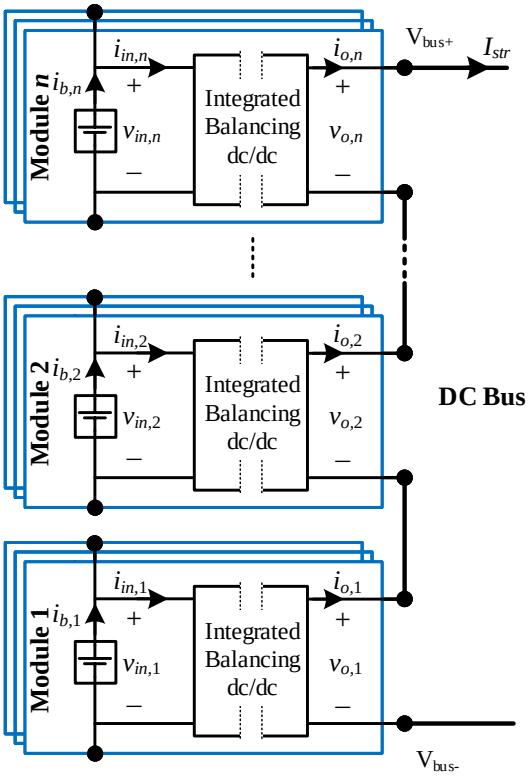


Fig. 3.6: Proposed general modular battery system employing several battery modules in parallel-series combination to achieve desired bus voltage, pack energy, and power ratings.

systems and DC micro grids [79, 94, 95]. This includes battery packs with different chemistry, pack voltage, power rating and energy capability. Traditional approach requires the use of high-power, wide voltage range, bidirectional dc/dc power converter as interconnects between localized battery packs and the DC bus [96–98]. Engineering challenges related to the design of such dc/dc power converters are wide input and output voltage range, and large power and current rating which result in cost, efficiency and size trade-offs. Furthermore, the traditional battery packs are not easily reconfigurable to work in multiple DC bus systems.

The modular concepts proposed in previous section can be applied to the battery systems used in micro-grid applications. The proposed modular battery system is shown

in Fig. 3.6. In the proposed approach, multiple battery modules of Fig. 3.2a are connected in series and parallel combination to interface a battery pack to the DC micro-grid. Since there is only one DC bus in the micro-grid, the modules are assembled as independent-input, series-output system. Moreover, several modules can be placed in parallel to increase the energy capacity or power rating of the battery pack. In this architecture, the group of dc/dc converters connected in series provide the voltage boost normally obtained through the series-connection of individual battery cells. As a result, the number of converter n placed in series can be selected to achieve near one-to-one conversion ratio for higher efficiency at the dc/dc level. Furthermore, with near one-to-one input to output voltage conversion ratio, the dc/dc converter only experiences small cell voltages at the input port and output port.

When used in in bidirectional power systems, the proposed modular configuration has several advantages such as easy reconfiguration and installation, reduced voltage and power rating, and increased power density. Furthermore, the proposed system architecture provides compatibility with multiple DC system voltages and upgradability to future systems at higher voltages using reconfigurable battery modules. These benefits when coupled with the ability to interface multiple cell chemistry battery systems offer cost gains and system interoperability between new and aged battery packs.

In contrast to the xEV system, the integrated dc/dc converter in the proposed modular battery system processes up to full power of the battery cell. This allows even more flexibility in adjusting each cell current via advanced battery control methods. As a result, the modular system offers great advantages in improving cell-level performance and pack lifetime when used with control based on life prognostic models. In addition, the dc/dc converter has the ability to completely cut off battery cell from output port without interrupting system operation. This can be done by either opening output port terminals {c, d} of one module and allowing remaining parallel modules to take over or shorting the output port terminals of all parallel modules and bypassing output current. This ability allows the system to stay operational even when a cell drops out.

3.2 Hardware Design Considerations

The building block battery module of Fig. 3.2a can be built in several ways. The key components of the module are a battery cell and an integrated balancing dc/dc converter. The choice of battery cell's chemistry, capacity, and absolute power capability is still determined by the application and can be chosen similar to the selection of cells for a series-connected battery pack. However, some of the cell binning and tight thermal control requirements that add cost to the traditional system can now be relaxed with active cell-level control. However, with life-based controls the battery modules can produce small difference in individual cell power to strongly reduce uneven degradation among cells and bring all cell to a homogeneous end of life. It should be noted that the nominal cell degradation is still driven primarily by the nominal operating conditions (average temperature, average time spent at high-SOC, etc.).

The integrated dc/dc converters inside each battery module can be implemented using any isolated dc/dc configuration. For the modular micro-grid system architecture of Fig. 3.6, a non-isolated dc/dc converter can work as well. Furthermore, the dc/dc converter can be rated to process full or differential cell power based on application requirements and module configuration. These topics are discussed next.

3.2.1 Choice of dc/dc Power Converter

The choice of integrated balancing dc/dc converter topology is an important decision. While mostly independent of the system architecture, the decision of dc/dc converter topology can be made using basic criteria such as low root mean square (rms) currents, low parts count, simple modulation strategy, and high efficiency. Each dc/dc converter experiences typical battery cell voltage (2 V to 4.5 V) at its input port. To achieve higher efficiency, the input-to-output voltage conversion ratio can be limited to a relatively small buck or boost gain. Among many other design choices, there are a few key considerations that are dependent on architecture and application as described next.

Bidirectional vs. Unidirectional

The proposed modular system architecture may operate with either bidirectional or unidirectional power converters. Unidirectional converters can be utilized in applications such as xEV where a primary path exists for directly charging or discharging the battery pack. For instance, the modular xEV battery system can be charged/discharge through the HV series string of battery cells. In this configuration, cell-level unidirectional converters can support auxiliary bus loads and perform cell balancing. Unidirectional operation relies on the bus load (auxiliary LV bus in xEV) to perform all cell balancing and removes any additional losses associated with typical active balancing strategies that shuttle and redistribute charge between cells. However, some applications may not guarantee sufficient load to support balancing of cells with large capacity mismatch under all conditions, e.g. fast charging of a parked vehicle. In this case, bidirectional converters can be used with the same control objective, resulting in sharing of the bus load and continuous redistribution of charge among cells for balancing. For application such as the microgrid system of Fig. 3.6, a bidirectional topology is required since the dc/dc converter controls cell charging or discharging.

Differential vs. Full Cell Power

The integrated balancing dc/dc power converter needs to be rated such that it can achieve cell-level balancing and supply loads on the DC bus. The dc/dc current required to perform cell balancing is a function of cell mismatch (capacity) and nominal charge or discharge rate of cells. In a balanced scenario, the dc/dc converters split the load currents equally. In most cases, the peak power on the DC bus exceeds the currents required for cell balancing. As a result, the dc/dc converter can be rated to support its equal share of peak DC bus load. By doing so, the overall system will be able to support peak load conditions and perform cell balancing during nominal load conditions.

It is expected that a series-input, parallel-output system configuration, such as shown in Fig. 3.4 for xEV system, is more advantageous for applications that have multiple DC bus voltages. This architecture allows large drivetrain currents to flow directly through series

string of battery cells offering higher efficiency while integrated balancing dc/dc converters support small loads on the auxiliary LV bus. For such a system, the integrated converter only need to process a fraction of the cell power capability. Hence the dc/dc converter only needs to be rated for differential power processing.

For the proposed modular micro-grid system, the integrated dc/dc converter needs to be rated for full cell power capability. This is due to the independent input configuration that allows isolation of battery cell from DC bus and ability to bypass or process full cell power.

Isolated vs. Non-isolated Topology

The integrated dc/dc converter can be implemented using any isolated dc/dc configuration. However, there are possible system configurations such as the micro-grid system of Fig. 3.2a where a non-isolated topology can offer higher efficiency and power density. For the xEV application, the presence of a series-input configuration necessitates an isolated topology for integrated dc/dc converter. Furthermore, the on-board xEV battery pack has strict isolation requirements from the rest of the system including the LV DC bus. As a result, an isolated topology is needed for xEV system. In contrast, the micro-grid system has an input independent configuration that allows a non-isolated topology to work. However due to the series-output configuration, the system still requires isolated communication to a central BMS controller.

3.2.2 Cost-optimized Substring Battery Module

The modular approach of Fig. 3.4 and Fig. 3.2a uses cell-level battery modules, offering active balancing capability down to cell-level. While the system offers great performance and lifetime benefits, it can end up with a large number of integrated dc/dc converters for very large battery packs. There is motivation to investigate modular battery systems that use a small substring of battery cells instead of a single cell as building blocks to design large, high-power battery packs. In this new modified approach, a battery module is designed by placing two or more cells in series and connecting an integrated dc/dc converter

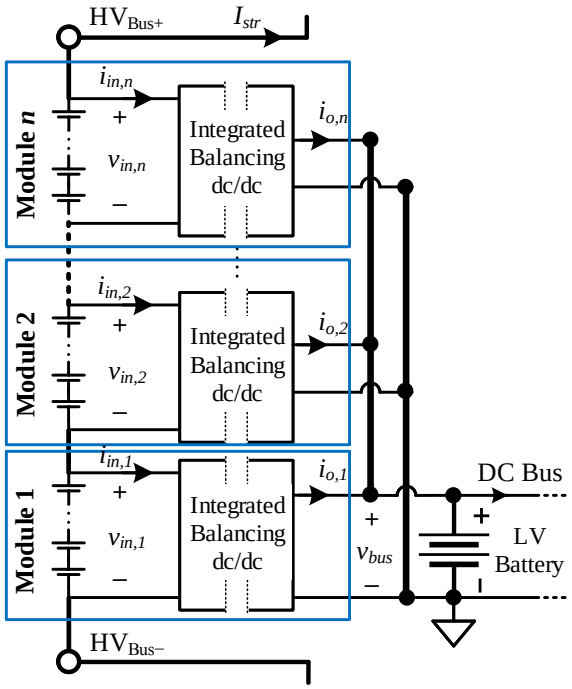


Fig. 3.7: A cost-optimized modular battery system with a substring of battery cells inside each module. The integrated dc/dc converter applies active balancing at the substring level while conventional passive balancing is applied within the substring of cells.

to the series substring. By doing so, the active balancing is applied to the group of cells and traditional passive balancing can be applied within the module. The module will be limited to the weakest cell within the small group of cells but the system will still be able to achieve a good percentage of lifetime benefits. With this approach, a cost-benefit trade-off is achieved by applying active balancing at a substring level instead of cell-level active balancing. Furthermore, the large battery pack is still constructed by configuring battery modules in series/parallel configuration, as shown in Fig. 3.7 for xEV system. A detailed design and analysis of the cost-optimized substring battery module is covered in [99].

3.3 Summary

In contrast to conventional cell balancing systems, a significantly different approach towards battery systems is presented in this chapter. New concepts are proposed for battery

system design and architecture which provide the capability to implement advanced control methods for cell balancing and control without significant increase in complexity or cost of the BMS. The proposed architecture integrates cell balancing and power processing functions inside fundamental building block battery modules and eliminates existing balancing circuits and some (or all) of the existing power converters in conventional battery systems. With this approach, if the battery modules can be realized with similar efficiency and cost to the existing balancing circuits and power converters, then the advantages of continuous active balancing are provided at effectively 100% efficiency and no additional cost. The proposed modular approach achieves continuous balancing of all cells, requires minimum to no control communications among battery modules, is scalable to an arbitrary number of battery cells and naturally shares the load current according to the relative state-of-charge (SOC) and state-of-health (SOH) of the battery cells. With special emphasis on xEV and stationary applications, this chapter featured detailed development of the proposed modular battery system for these applications. Discussion on integrated power converter topology, power rating, and isolation requirement for both applications is also provided.

CHAPTER 4

SYSTEM-LEVEL CONTROL FOR MODULAR BATTERY SYSTEMS

A new modular battery system architecture, presented in Chapter 3, combines battery balancing and power processing functions inside building block battery modules that enable differential power processing down to cell-level. With the modular system architecture, an integrated dc/dc power converter inside each battery module processes individual cell power to enforce cell balancing and achieves control goal for bus voltage regulation. For the xEV application, a series-input, parallel-output architecture was shown to achieve cell balancing via differential processing of low voltage (LV) bus loads. This architecture enables vehicle propulsion power to be directly accessed from series string of battery cells and it eliminates the traditional high step-down converter previously used to supply the LV bus. Moreover, an independent-input, parallel/series-output architecture was proposed for the micro-grid systems. In this approach, the combination of parallel and series output configuration is used to achieve desired voltage and power ratings. Similar to the modular xEV system, the integrated converters work together to regulate micro-grid bus voltage and produce small differences in individual cell power to enforce balancing objectives.

One of the key benefits of modular battery system is its ability to enforce traditional and advanced cell balancing functions. As shown in this work, the system can implement traditional cell voltage and SOC balancing methods, discussed in Chapter 2, using distributed and central control approaches. In addition, the modular system offers the ability to implement advanced cell balancing methods that are based on battery life prognostic models such as [1, 16, 19, 100, 101]. In addition to traditional cell balancing, this work explores advanced cell-level balancing methods to address the issue of growth in cell capacity mismatch. The cell-level control relies on battery life prognostic models of [1, 16, 100] and employs the modular cell-level balancing architecture to remove accelerated aging effects exhibited by weak cells. To implement these cell balancing methods, an approach based

on objective maps is developed in the first part of this chapter. This approach allows traditional and advanced cell balancing methods to be implemented in a simple and scalable manner for large battery packs.

The modular battery system integrates cell balancing and power processing into cell-level dc/dc converters. As a result, the system-level control goal is to achieve both DC bus voltage regulation, and cell balancing among battery modules. To achieve these functions, the control action performed by each battery module requires some knowledge of the state of the entire battery pack. This is because the power delivered or absorbed by each battery module is determined relative to the state, average voltage or state-of-charge (SOC), of the rest of the battery pack. In addition, each module regulates the DC bus voltage to a set-point and supplies bus loads. While cell balancing is a relatively slow process, bus voltage is typically regulated within some voltage margins and requires faster control bandwidth to achieve that. As a result, the modular battery system has multiple control goals and each goal has its regulation and bandwidth requirements.

These control goals can be met using a central or distributed control and communications approach. The pack information sharing can be achieved either through digital communications with a shared central controller or via distributed control approach that can signal via DC bus voltage. The modular system will benefit in terms of improved cost and low system complexity if very high-speed digital communication is avoided for sharing full battery pack information. Furthermore, there is strong motivation to run high bandwidth and time critical control loops inside local battery modules for robustness and safety. A fully distributed approach can alleviate communication requirements necessary to produce correct division of bus load among cells. In this chapter, a distributed approach that uses the shared bus voltage itself as a means of communicating the balancing target (average voltage or SOC) is presented. The fully distributed approach does not rely on high-speed digital communications for any of the control loops and instead uses locally available information for all control actions. In addition, a shared central controller that does not require very high-speed communication is developed using partially-distributed

approach employing local and central control loops to regulate battery current at the local dc/dc level and bus voltage at the system-level.

This chapter focuses on system-level control concepts while the details of compensator design and loop-gain analysis will be the topic of next chapter. In section 4.1, an objective map based approach is developed for implementing traditional cell balancing methods using the modular battery system. A distributed control strategy for modular xEV battery system is proposed in section 4.2. This work is then extended in the direction of a partially-distributed control strategy for xEV systems in section 4.3. Section 4.5 expands the objective map based approach to show implementation of advanced cell balancing methods. A summary of system-level control methods developed in this chapter is provided in section 4.5.

4.1 Objective Map Based Approach for Cell Balancing

The modular battery system integrates cell balancing and power processing into cell-level dc/dc converters. The converters are designed to produce small differences in the distribution of load among individual cells, resulting in regulated variations in each cell current which can be leveraged for runtime cell balancing. To achieve cell balancing, the control action performed by each battery module requires some knowledge of the state of the full battery pack. As the battery pack scales up, the need for system level control methods that allow simple ways to achieve load sharing and cell balancing become very important.

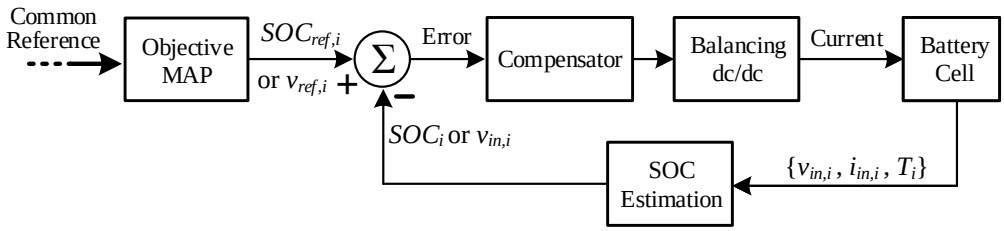


Fig. 4.1: Cell-level control approach for modular battery system where each dc/dc converter uses an objective and a common reference signal to determine its target cell voltage or SOC.

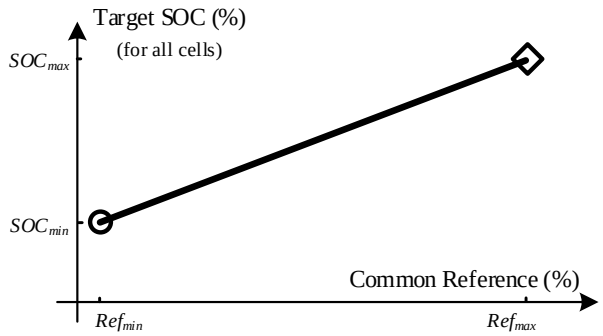


Fig. 4.2: An example objective map that can be used for regulating cell SOC to a common reference among all cells.

In this work, a control approach based on 'objective maps' is developed. An objective map is programmed into each dc/dc converter that allows the converter to use a common, shared reference to determine its target cell SOC, as shown in Fig. 4.1. Each converter then regulates its input current according to the difference between target SOC and its cell SOC. This approach achieves continuous balancing of all cells, requires no control communications among converters, is scalable to an arbitrary number of battery cells and naturally shares the load current according to the relative SOC and capacities of the battery cells.

The objective map can be a simple linear relationship that can be pre-programmed into each battery module. An example objective map with one-to-one linear mapping between a common reference signal and cell SOC is shown in Fig. 4.2. The common reference serves as a shared signal among all dc/dc modules which gives information about the rest of the system. The choice of common reference is important and it needs to be a shared feature among all battery modules.

4.2 Distributed Control using Shared DC Bus

The modular xEV battery system architecture, developed in Chapter 3, divides the conventional high step-down dc/dc converter functionality among multiple integrated dc/dc converters, with one converter per battery cell. The system architecture is shown in Fig. 4.3.

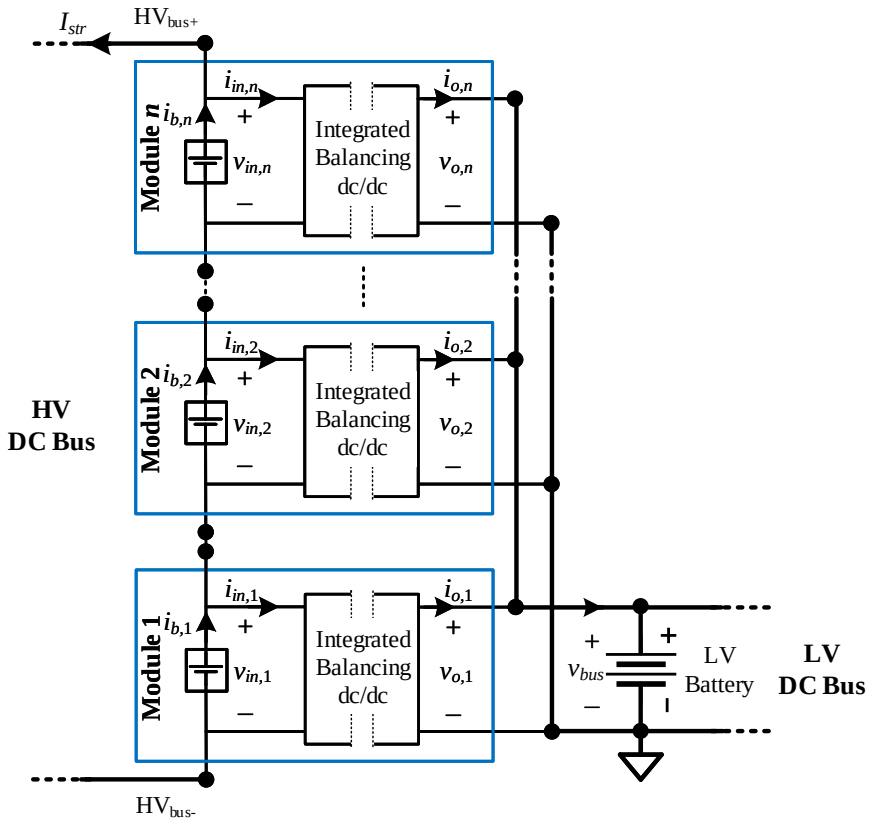


Fig. 4.3: Modular xEV battery system, presented in Chapter 3, employing several battery modules to make a HV bus for drivetrain, and LV bus for auxiliary loads.

In this configuration, individual dc/dc converters are connected in series-input, parallel-output configuration with each input connected directly in parallel with a battery cell. The total LV bus load current is then divided among the cells through the partial-power processing integrated converters. Control of the individual converters is designed to produce small differences in the distribution of LV bus load among individual cells, resulting in regulated variations in each cell current which can be leveraged for runtime balancing of cells.

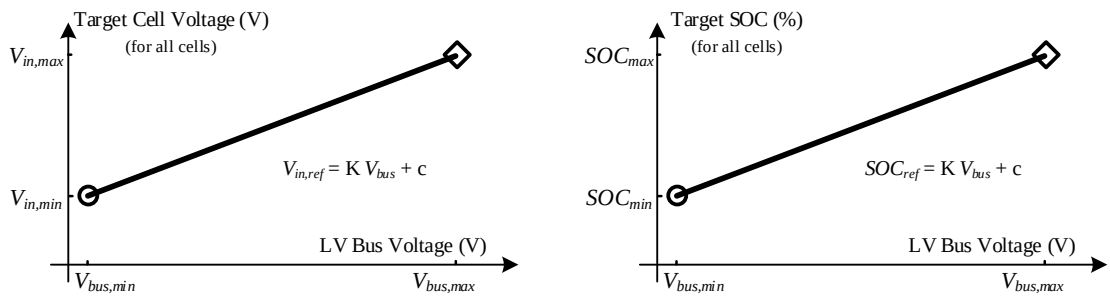
Due to the large number of converters in the modular system, practically controlling the bus voltage with good stability and robustness becomes a challenge. While a central controller can be used to split loads among dc/dc converters, such method relies on high-

speed digital communication, and therefore may not be desirable for time-critical closed-loop regulation. A distributed control approach can increase system performance and robustness, as no communication is required for time critical control.

In this section, a distributed control approach for parallel-output cell-level dc/dc converters is presented. An example implementation of the system with proposed approach is shown in Fig. 4.1. In order to alleviate communication requirements necessary to produce correct division of bus load among cells, the proposed approach relies on local information, $\{v_{in,i},\ i_{in,i},\ T_i,\ v_{o,i}\}$, at each dc/dc level. The control goal of each integrated dc/dc converter is same, i.e. regulate the LV bus voltage and balance its own cell to a reference value by splitting LV bus load proportional to its cell state of charge. Each dc/dc employs a compensator to regulate cell SOC or input voltage to a target value. The target SOC is computed using a 'common reference' signal and an objective map that translates the common reference to a target SOC, as shown in Fig. 4.2.

For the modular xEV system of Fig. 4.3, LV DC bus voltage can be used as a common reference. Since the integrated dc/dc converters are connected in parallel at the output port, they all sense the same shared LV bus voltage in xEV battery system. As a result, the LV bus voltage itself is used as a means of communicating the average balancing target voltage or SOC. This is done using the objective map of Fig. 4.4 which shows target cell voltage or SOC as a linear function of the bus voltage value. For simplicity of implementation, control goal can be based on voltage balancing among the cells, as shown in Fig. 4.4a, but balancing based on cell estimated SOC or SOH can be implemented in the same manner, as shown in Fig. 4.4b. With this approach, each dc/dc converter regulates the cell voltage or SOC to a value consistent with the current bus voltage within its range of current limits.

In the voltage balancing implementation, each integrated dc/dc converter has the control goal $V_{ref,i} = V_{in,i} = KV_{bus}$, and is controlled to regulate its input current $i_{in,i}$ according to the difference between the cell voltage and scaled bus voltage. A block-level control diagram for cell voltage balancing is shown in Fig. 4.5. When a load is applied to the LV bus, the load current will distribute among the dc/dc converters relative to the voltage



(a) (b)

Fig. 4.4: An example objective map that can be used for regulating (a) cell voltage, or (b) cell SOC to a common reference, in this case LV bus voltage, among all cells.

difference. If cell voltages are balanced and have matched capacity, load current distributes evenly among all converters; if a high dc gain controller is used, the system stabilizes with zero control error, i.e. with a bus voltage equal to the scaled cell voltages. Further, the bus voltage tracks the cell voltages as variations in pack SOC and current cause the bus voltage to vary. If cell voltages are unbalanced, this control results in the power converters reducing discharge of the cells with voltage below the scaled bus voltage and increasing discharge current of cells above it, independent of the magnitude and direction of the overall pack string current. With this approach, no further communication is required between individual dc/dc converters. Furthermore, the system can easily be scaled to an arbitrary number of cells in the pack, greatly simplifying the BMS.

Since the shared bus voltage itself is used to communicate the reference target for each dc/dc bypass converter, V_{bus} must be allowed to vary proportional to the cell state of interest, which is the cell voltage for the case of voltage balancing. The nominal voltage and total variation can be set arbitrarily by the control law, but the variation must be sufficiently large to avoid noise limitations. As an example for xEV system, the nominal bus voltage reference is set close to $V_{bus} = 14$ V and the control goal is set to $V_{in,i} = \mathrm{K}V_{bus}$ with K = 0.25. With typical Li-Ion battery cell voltage characteristics, this results in a bus voltage range of 11-16 V. This range is within what is typical of the LV bus of electric

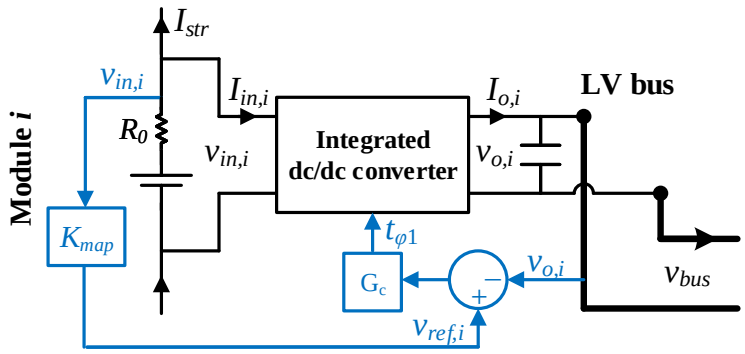


Fig. 4.5: Control diagram for integrated dc/dc converter to achieve distributed bus voltage regulation and automatic cell voltage balancing.

vehicles (11-17 V) [74].

4.2.1 Multiple Battery Packs on A Shared DC Bus

As discussed in Chapter 2, there is a significant interest in sharing multiple localized battery packs with different chemistry, pack voltage, power rating, and energy capability components across the DC bus, as shown in Fig. 4.6. In addition, the DC bus is typically connected to other forms of power sources, such as solar PV and diesel generator, and multiple DC or AC loads. Such a system presents a challenge of evenly sharing load current and battery pack charging current without presence of a central controller. Furthermore, circulating currents between battery packs are undesired.

The concept of using bus voltage as a means to communicate a reference cell voltage or SOC can be extended to communicate pack voltage or SOC in applications such as micro-grid systems where multiple battery packs are connected on a shared DC bus. This can be done using the objective map of Fig. 4.4 where each battery pack target SOC is now determined as a function of the DC bus voltage. Similar to the modular xEV system, each battery pack now has the control goal $V_{ref,i} = V_{pack,i} = KV_{bus}$, and is controlled to regulate its input current $i_{in,i}$ according to the difference between the pack voltage (or SOC) and scaled bus voltage.

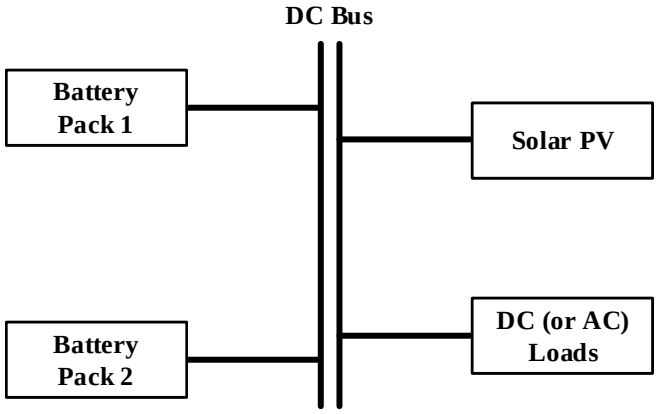
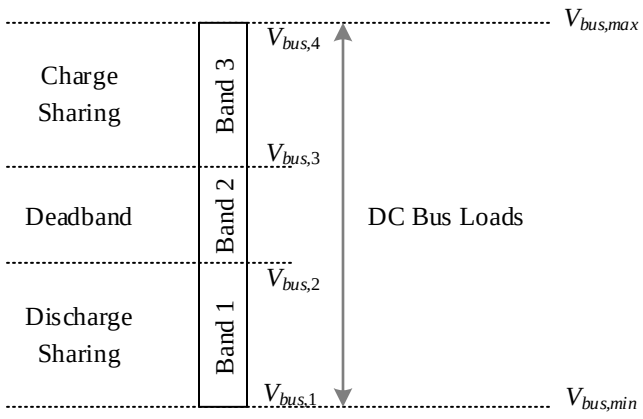
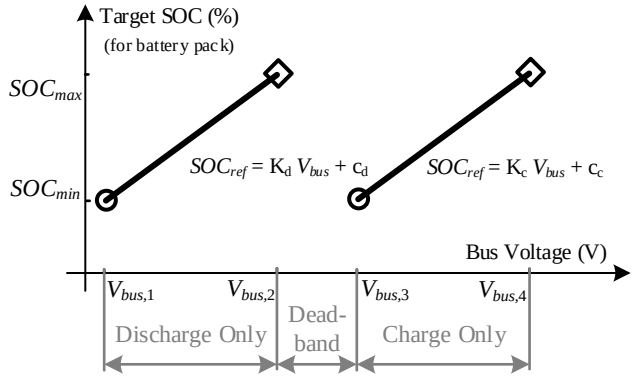


Fig. 4.6: Plug-and-play micro-grid battery system with multiple battery packs connected to DC bus.

For the micro-grid system, the bus voltage based objective map can be partitioned in multiple segments to prioritize renewable power sources and avoid circulating charge/discharge currents between battery packs. For example, the bus voltage can be divided into multiple bands, as shown in Fig. 4.7a, to enable battery packs to only charge and discharge within a certain bus voltage band. Furthermore, renewable sources like solar PV can be assigned the higher priority by programming the PV source with a control goal of supplying maximum power if bus voltage falls below $V_{bus,max}$. An example objective map to implement the bus voltage partitioning is shown in Fig. 4.7b. In this map, if the bus voltage is in Band 1 $\{V_{bus,1}$-$V_{bus,2}\}$, each battery pack shares the load current according to their relative SOC and capacities. Similarly, in Band 3 $\{V_{bus,3}$-$V_{bus,4}\}$, the battery packs share charging current based on their relative SOC and capacities. Band 2 $\{V_{bus,2}$-$V_{bus,3}\}$ serves as a dead-band between the charging and discharging bands. This approach allows for compatible families of various power sources and achieves plug-and-play integration and operation. By partitioning the DC bus voltage in segments, each power source can be prioritized for charging and load sharing without the need for a central controller.



(a)



(b)

Fig. 4.7: (a) DC bus voltage is partitioned to enforce current sharing and no circulating currents between battery packs, and (b) an example objective map for battery pack control to achieve separate charge and discharge bands.

4.3 Partially-Distributed Control using Local and Central Controllers

In the modular xEV battery system, DC bus voltage regulation and battery cell balancing are inherently coupled due to the integrated system. This means that based on mismatches in cell SOC and capacity within the battery pack, each dc/dc converter supplies a different amount of power to support the total DC bus load and achieve battery cell balancing. In section 4.1, an objective map based approach has been developed to achieve

cell balancing. In section 4.2, a distributed control approach utilizing the objective map and bus voltage as the common reference signal is presented. In this section, a partially-distributed control approach is presented that extends the balancing objective map to be used in a central supervisory controller. In addition, central and local control architecture is presented to show that time critical control loops can be accomplished at the dc/dc stage.

The partially distributed control scheme, shown in Fig. 4.9, is implemented by controlling the input current of all dc/dc modules in a distributed fashion, and the output voltage and cell SOC using a central supervisory controller. The proposed approach is based on a multi-loop, linear feedback control that is distributed between the central BMS controller and individual dc/dc modules of Fig. 4.3. For the objective map, average SOC of the full battery pack is used as a common reference signal, as shown in Fig. 4.8. If traditional SOC balancing is required, the balancing map is simplified to a one-to-one mapping between individual cell SOC and the average SOC. By doing so, the pack average SOC becomes a target SOC for each cell. The partially-distributed control approach results in same functional behavior as the distributed control scheme with the exception of a communication channel between each dc/dc and the supervisory controller. However, as shown in this work, safety critical control loops still run within each dc/dc converter, making the control approach suitable for traditionally central control systems.

In this control approach, the dc/dc modules are designed identically as a building block. Each dc/dc module employs a local current feedback-loop that regulates its input current to a reference current command, $I_{in,ref,i}$. This local feedback loop provides input current regulation with a desired bandwidth, designed to meet system specifications. The input current control can be replaced by output current without loss of generality. However, the input current has the added benefit of direct control of battery cell current that ensures cell current limit protection and safety. Furthermore, the input current measurement is shared with battery SOC and SOH estimation controllers.

A central, supervisory control approach utilizing central BMS controller is proposed for DC bus voltage regulation and cell SOC control, as shown in Fig. 4.9. The central

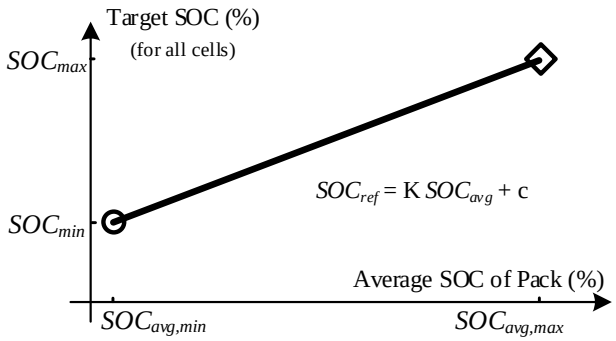


Fig. 4.8: An example objective map that can be used for regulating individual cell SOC relative to the average SOC among all cells.

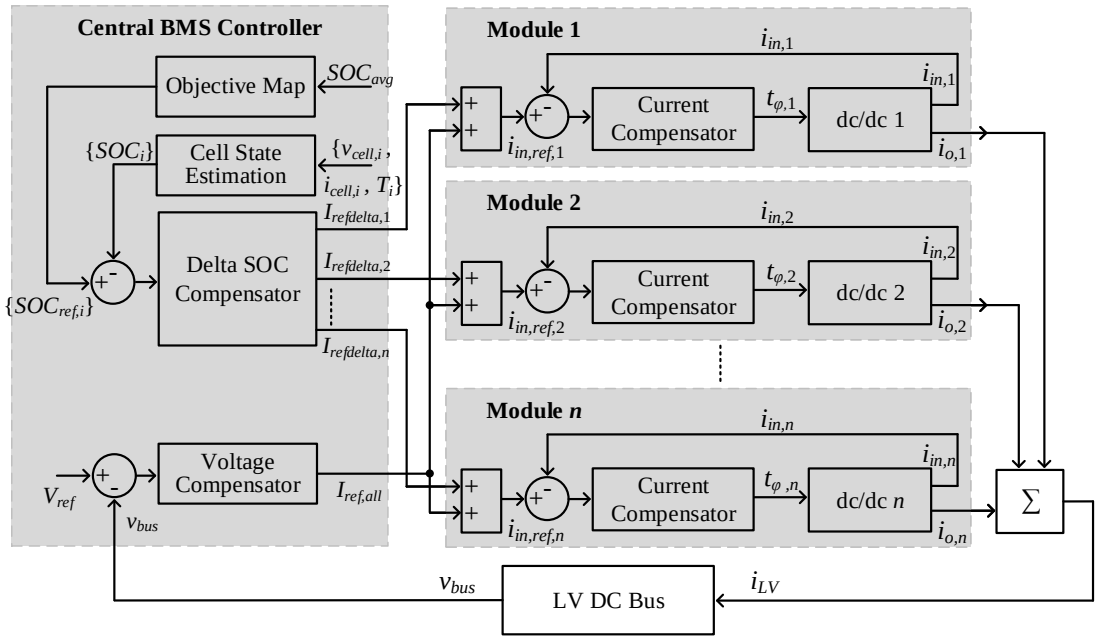


Fig. 4.9: Partially-distributed control approach for the modular xEV battery system. Each dc/dc module has a local current feedback-loop that runs at a fast rate to regulate input current. The central BMS controller incorporates the voltage and delta SOC compensators and to perform bus voltage regulation and cell balancing.

BMS controller generates one common current reference command and n individual delta current reference commands. This is done using two separate outer control loops inside the central BMS controller, referred to here as voltage loop and SOC loop. Each of the outer

voltage and SOC loop only acts on the well behaved inner dc/dc input current loop, which in many cases can be represented as a single pole, low-pass system. Thus the existence of local current feedback loop inside each dc/dc converter greatly simplifies the control of bus voltage and cell SOC regulation. Since all dc/dc converters share their output voltage, a common voltage-loop can be designed for DC bus voltage regulation. This is possible by averaging all building block DC/DC converters and representing them with a unit averaged module. The voltage-loop compensator provides a common current reference command, $I_{ref,all}$ to all the dc/dc modules. Thus, outside of the operation of SOC loop, the common current reference command is shared equally among the inner current loops of the dc/dc modules. The outer SOC loop utilizes a delta SOC compensator that provides individual delta current reference commands, $I_{refdelta,i}$ to each dc/dc module. The delta current reference commands produce small variations in the input current of each dc/dc module to enable cell balancing. Therefore, the voltage and delta SOC compensators combined provide the required LV bus voltage regulation and cell balancing control with additional safety features associated with the internal current loop.

Two conditions are set to decouple the outer voltage and SOC feedback loops and avoid competition among them. I). The voltage loop is designed to run at a higher bandwidth than the SOC loop. II). The sum of all delta current commands is set to zero, $\Sigma_{i=1}^{n} I_{refdelta,i} = 0$ and the current commands are set within the input current limits for the DC/DC modules. Condition I ensures that DC bus voltage loop has a fast response and any undesired perturbation due to load change or delta current command is rejected well. In addition, condition II guarantees that the net effect of delta current commands is zero and SOC loop does not perturb the voltage loop. The two conditions together decouple the outer loops without sacrificing any system performance requirements. The voltage loop can be designed for a high bandwidth (several Hz to kHz) to meet desired steady-state and transient response requirements under large step changes in loads. Furthermore, the SOC loop can be designed for a moderate bandwidth (mHz to Hz) without loss of performance since cell SOC is a relatively slow changing process for large, several Ah capacity xEV bat-

tery cells. The decoupling of the two outer loops greatly simplifies the compensator design process and also simplifies the communication requirements, with the common current reference command $I_{ref,all}$ broadcast at a fast rate and the individual delta current reference commands $I_{refdelta,i}$ transmitted at a slow to moderate rate.

Using the partially-distributed control approach, the LV DC bus voltage can be regulated to a fixed voltage set-point provided by the supervisory vehicle controller. Furthermore, there might be motivation for the voltage set-point to be defined as a representative of the Li-ion battery pack SOC to improve overall converter efficiency as described in [102,103]. The proposed approach allows these existing techniques to be easily incorporated into the modular battery system.

In addition to the xEV battery system, the partially-distributed control architecture of Fig. 4.9 can also be utilized for series-output battery modules used in micro-grid system. The common and delta reference approach allows the system to achieve cell balancing and DC bus voltage regulation. The implementation details, compensator design, and analysis for parallel-output and series-output battery modules is presented in Chapter 5.

4.4 Advanced Cell Balancing Strategies and Its Objective Maps

Previous sections in this chapter have provided a control framework to implement traditional cell balancing objective maps for the modular battery systems. As described in Chapter 2, traditional cell balancing methods meet the basic requirements to keep battery pack functional, however, these balancing methods lead to uneven degradation across cells in the battery pack. This behavior results in reduced lifetime of the battery pack and limited power/energy capability.

In this section, advanced active cell-level control approaches are explored to address the issue of growth in cell capacity mismatch. The cell-level control relies on battery life prognostic models and integrated balancing dc/dc converter to remove accelerated aging effects exhibited by weak cells and to achieve higher energy capability of the pack. First, the reasons for accelerated aging in cells is explained. Next, the objective map based approach is extended to develop life balancing map for cells. The life balancing map enables

battery modules to load individual cells differentially and reduce the growth in cell capacity mismatch over lifetime. Furthermore, the life map incorporates differences in cell series resistance to improve the power/energy limits of each cell.

4.4.1 Battery Pack Life Extension

The balancing methods presented here are based on insights gained from life prognostic models and analysis of cell degradation in large xEV battery packs [16, 100, 102]. In xEV applications, battery pack lifetime is determined by the time it takes the pack to reach a threshold remaining usable capacity. This point is generally dictated by the weakest cell in the pack. Hence a parameter of particular interest for extending battery pack lifetime is cell capacity. Due to manufacturing tolerances, cells in large battery pack begin their life cycle with capacity imbalance which can range from 1% to 10%, depending on the quality of manufacturing and level of cell binning applied [14]. Analysis from life prognostic models of xEV Li-ion battery packs shows that capacity fade is a strong function of cell temperature, maximum SOC, and the amount of time spent at maximum SOC. Due to natural temperature gradients across the battery pack, cells do not degrade evenly over their lifetime. As a result, there is significant growth of capacity imbalance over time causing faster capacity fade on some cells than others and leading to shortened pack lifetime. Moreover lower capacity cells naturally charge faster and hence reach the maximum SOC before other cells, which are then typically balanced to equal SOC with traditional balancing objectives. Large capacity imbalance leads to shortened pack lifetime due to the weaker cells limiting pack usable energy.

The life of the battery is associated with two terms: calendar life and cyclic life. The calendar life expresses the theoretical lifetime of a battery when sitting at rest at a given temperature and SOC. Cycle life is associated with aging of battery during repeated charge and discharge. These two terms collectively define the degradation of the battery. The cells degrade faster when stored at higher temperatures and high SOC values leading to shorter calendar life [16, 100]. Battery packs used in typical xEV applications spend a significant amount of time resting on high SOC which leads to faster degradation. As a result, calendar

life degradation can be an important factor in shortened lifetime of a battery pack.

The objective of the life balancing algorithm is to reduce cell-to-cell performance mismatch over time. Based on calendar life degradation, there are two main factors (temperature and SOC) that can be used to minimize the mismatch in the cells. Temperature plays a significant role in aging. Although life balancing cannot impact the average effect of temperature aging, it can reduce the cell-to-cell mismatch resulting from temperature gradients in a battery pack. The maximum SOC value of the cells is the second factor that influences aging. Since, cells stored at different SOC values degrade at different rates, the life balancing algorithm controls the maximum resting SOC of cells based on their relative capacities: higher capacity cells are driven to higher maximum SOC and lower capacity cells are driven to lower maximum SOC, as shown in Fig. 4.10. The difference in maximum SOC, achieved by controlling each cell to a unique SOC reference, decreases growth in capacity mismatch and hence extends the lifetime of the battery pack. The proposed control takes a different approach as compared to traditional SOC balancing which is known to target all cells to the same SOC.

4.4.2 Improved Pack Energy/Power Capability

Life prognostic models do not show nearly as strong of a correlation between time spent at minimum SOC on capacity fade as they do at maximum SOC. Thus, to maintain as much usable energy as possible at beginning of life, a different objective can be used to map the minimum SOC reference. A common objective is to bring the cell to the minimum SOC allowed while still capable of providing maximum power without going below the minimum cell voltage limit [103]. In traditional BMS systems with a common SOC reference for all cells, the minimum SOC limit is based on the cell with the worst case (largest) series resistance, R_s. Therefore if the SOC balancing objective is applied, then the SOC range for all cells is limited by the worst case cell to avoid exceeding V_{min} for maximum discharge current at the lower end, as shown in Fig. 4.11b. An alternative control objective is to offset each cell's SOC according to its own series resistance such that each cell maximizes its SOC range and is not limited by the worst case cell resistance, as shown in Fig. 4.11c.

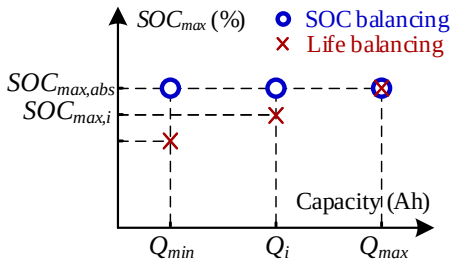


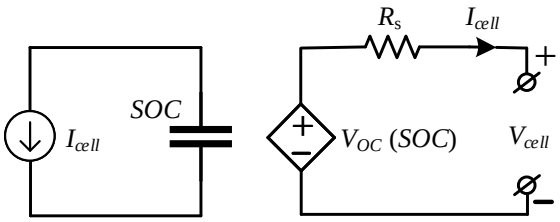
Fig. 4.10: Traditional SOC balancing approach (shown in blue circles) targets all cells to identical maximum SOC regardless of capacity mismatch. Life balancing approach (shown in red crosses) drives individual cells to different maximum SOCs based on their relative capacities.

For the same power capability, this objective achieves higher pack energy when compared to Fig. 4.11b. Since the modular battery system is capable of individual cell control to achieve the SOC difference at maximum SOC, the same approach can be used to set the minimum SOC for each individual cell as a function of it's own series resistance R_s, thus further maximizing pack usable energy within power limits.

4.4.3 Combined Life/Energy/Power Objective Map

The objectives presented here can be combined to achieve the benefits of extended lifetime and improved energy capability. This can be done by mapping the common SOC reference, traditionally used to control all cells to the same SOC, to a unique SOC reference for each cell. The reference map used for traditional SOC balancing in a continuous fashion is shown in Fig. 4.12a. In this map, a common reference signal, e.g. the average SOC of the battery pack, is used to find the target SOC for all cells. For a given common reference value, the balancing circuits force all the cells to the same target SOC. The combined life extension objective map can be derived in a similar fashion as shown in Fig. 4.12b, where the life control approach is accomplished by defining a unique map for each cell based on its online estimation of capacity Q and series resistance R_s.

The combined life extension objective map is created by first setting the two boundary points and an intermediate transition point. The right boundary point shown by the



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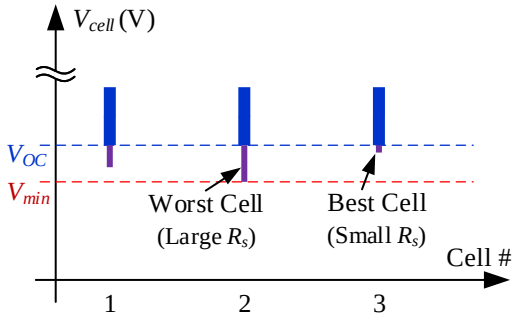

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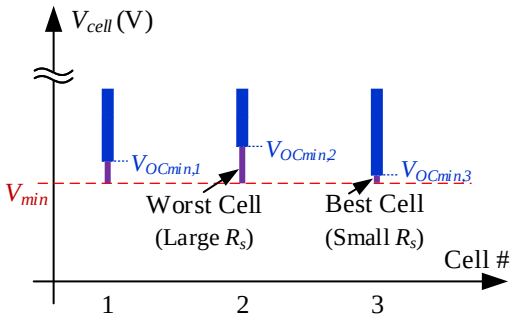
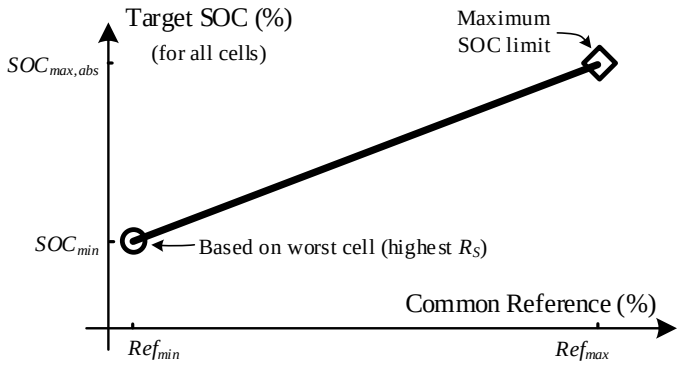


(c)

Fig. 4.11: (a) Simplified equivalent circuit cell model showing dependence of cell voltage on cell SOC and series resistance R_s. (b, c) Example of battery terminal voltages with maximum discharge current applied. Blue thick bars represent open circuit voltage, V_{OC}, violet thin bars represent voltage drop due to cell series resistance, R_s. (b) SOC balancing with power limit, (c) improved energy/power capability balancing approach.



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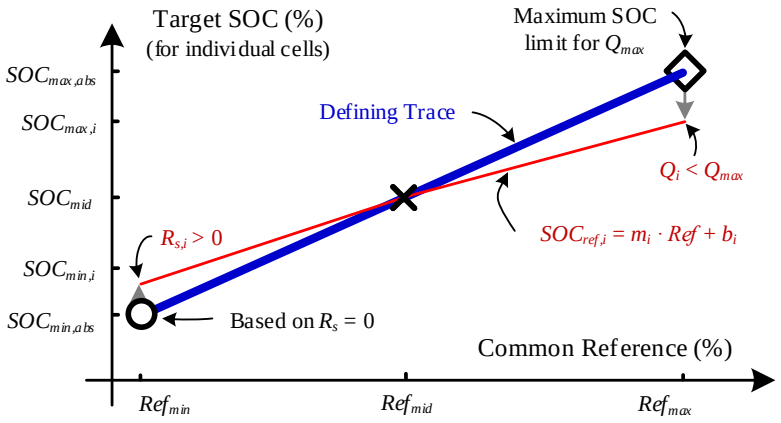


(b)

Fig. 4.12: (a) Objective map used for traditional SOC balancing to control all cells to the same SOC, (b) life extension objective map showing two cases: (thick blue) defining trace for an ideal cell with maximum capacity, Q_{max} and zero series resistance $R_s = 0$, and (thin red) illustration map for a real cell with capacity $Q_i < Q_{max}$ and series resistance $R_s > 0$.

diamond marker in Fig. 4.12b, is based on the cell with maximum capacity, Q_{max}, in the battery pack. This cell is pushed to the maximum allowable SOC level, $SOC_{max,abs}$, a point that corresponds to the maximum value of the common reference signal, Ref_{max}. The left boundary point shown by the circle marker in Fig. 4.12b, is based on an ideal battery cell with zero series resistance, $R_s = 0$. This sets the lowest possible SOC on the map,

$SOC_{min,abs}$, which stems from the physical minimum open-circuit voltage for an ideal battery cell, and corresponds to the minimum value of the common reference signal, Ref_{min}. The transition point shown by the cross-mark in the middle of the graph in Fig. 4.12b, is used to transition from capacity based map to a resistance based map. A linear map between the two boundary points outlines a 'defining trace' as shown by the thick blue line in Fig. 4.12b. The transition point lies at the middle of this linear trace.

Next, the maximum and minimum operation points for each cell in the battery pack are calculated based on their measured capacity and series resistance, as a function of the common reference signal and the absolute boundary points on the defining trace. Maximum SOC operation point, $SOC_{max,i}$, for cell i with capacity Q_i is calculated as,

$$SOC_{max,i} = SOC_{max,abs} - K(Q_{max} - Q_i), \tag{4.1}$$

where $SOC_{max,abs}$ is the absolute maximum SOC at top-end of charging defined in the first step, Q_{max} is the capacity of the maximum capacity cell in the pack, and K is a gain factor which determines how aggressively the lifetime objective map counteracts growth in capacity fade. The minimum SOC operation point, $SOC_{min,i}$, for cell i is calculated using cell series resistance $R_{s,i}$ from the simplified equivalent circuit model in Fig. 4.11a. By assuming requirements for maximum pack string current, I_{max}, and minimum cell terminal voltage limit, V_{min}, the cell minimum open-circuit voltage is calculated as,

$$V_{OCmin,i} = V_{min} + R_{s,i}I_{max}. \tag{4.2}$$

$V_{OCmin,i}$ is the minimum allowed open-circuit voltage for cell i and can be directly translated to the minimum SOC boundary, $SOC_{min,i}$, that the cell will be allowed to settle at the bottom-end of the charge. The open-circuit voltage limit can be translated to SOC limit using the V_{OC}-to-SOC curve of the cell. Each cell is forced to converge and match its SOC at the mid-point Ref_{mid}. This allows for a transition point in the map which can be used as a reference point for switching between capacity or resistance based map in a

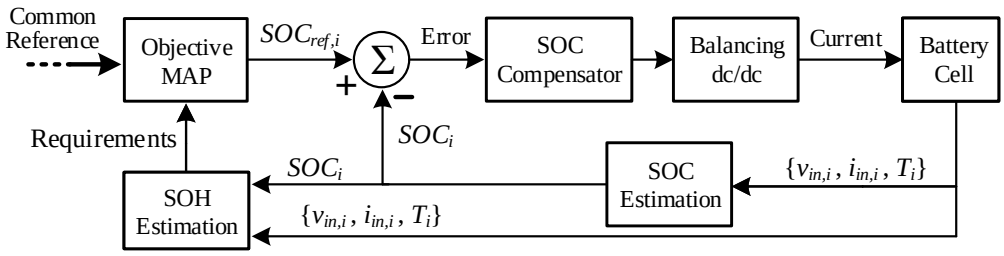


Fig. 4.13: Cell-level distributed control approach with life extension objective map where the life control is accomplished by defining a unique map for each cell based on its estimated capacity Q_i and series resistance $R_{s,i}$. Balancing dc/dc regulates each cell's SOC_i to its target SOC, $SOC_{ref,i}$.

distributed system. The final step in obtaining the life extension objective map is creating a linear approximation between the two boundary points $SOC_{max,i}$ and $SOC_{min,i}$ and the mid-point SOC_{mid} for cell i. The resulting map will have two linear traces with different slopes for cell i, shown by the red thin traces in Fig. 4.12b, as:

$$SOC_{ref,i} = m_i Ref + b_i, \tag{4.3}$$

where m_i is the slope, and b_i is the offset of the linear fit. By enforcing the relationship of Fig. 4.12b, each cell in the battery pack spans different SOC range according to the measured cell parameters of capacity and series resistance.

The life balancing objective can be easily incorporated into the distributed and partially-distributed control methods. A block diagram of the control approach with life extension is shown in Fig. 4.13. To achieve the life extension benefits, the *Objective Map* block enforces the relationship of Fig 4.12b and results in unique SOC references for each battery cell.

4.5 Summary

This chapter developed system-level control ideas for the modular battery system. Since, the modular system integrates cell balancing and power processing into cell-level dc/dc converters, the control action performed by each battery module requires information

about the rest of the system. To achieve cell balancing among battery modules and DC bus voltage regulation, an approach based on objective maps is developed in the first part of this chapter. This approach allows traditional and advanced cell balancing methods to be implemented in a simple and scalable manner for large battery packs. The objective map approach is integrated into a distributed control architecture that utilizes local sensor information to implement control actions. The distributed control approach uses the shared DC bus voltage as a common reference signal to communicate battery pack SOC. With this approach, each dc/dc converter regulates the cell voltage or SOC to a value consistent with the current bus voltage within its range of current limits. This chapter also develops an alternative control approach, named partially-distributed control, that employs local and central controller to achieve balancing and bus voltage regulation. It is shown that the approach is easily scalable and utilizes fast local dc/dc control loops for safety critical functions and central control loops for other functions. In the last part of this chapter, the objective map approach is expanded to demonstrate implementation of advanced cell balancing methods that can improve the lifetime and power/energy of battery packs.

CHAPTER 5
MODELING AND CONTROL OF PARALLEL/SERIES OUTPUT DC/DC CONVERTERS

The modular battery system architecture, presented in Chapter 3, combines battery balancing and power processing functions inside building block battery modules. Based on application and system architecture, an integrated dc/dc power converter inside each battery module is connected in series or parallel configurations at the input and output ports. For the xEV application, a series-input, parallel-output architecture was shown to achieve cell balancing via differential processing of LV bus loads. An independent-input, parallel/series-output architecture was proposed for the micro-grid systems. In both systems, the integrated converters work together to regulate bus voltage and produce small differences in individual cell power to enforce balancing objectives. Chapter 4 developed system-level control methods for the modular battery system, introducing distributed and partially-distributed control schemes for cell balancing and voltage regulation.

The goal of this chapter is to study the control methods described in chapter 4 and do modeling, design, and analysis of control loops for the parallel and series output integrated dc/dc converters. Before going into design and analysis of control loops, the choice of dc/dc converter along with its switching modulation scheme and analytical model are discussed in section 4.1. The distributed control strategy for modular xEV battery system, first presented in Chapter 3.2, is discussed and analyzed in section 4.2. This work is then extended in the direction of a partially-distributed control strategy for xEV systems in section 4.3. For the micro-grid application, a more general partially-distributed control approach is developed in section 4.4. A summary of control methods developed in this chapter is provided in section 4.5.

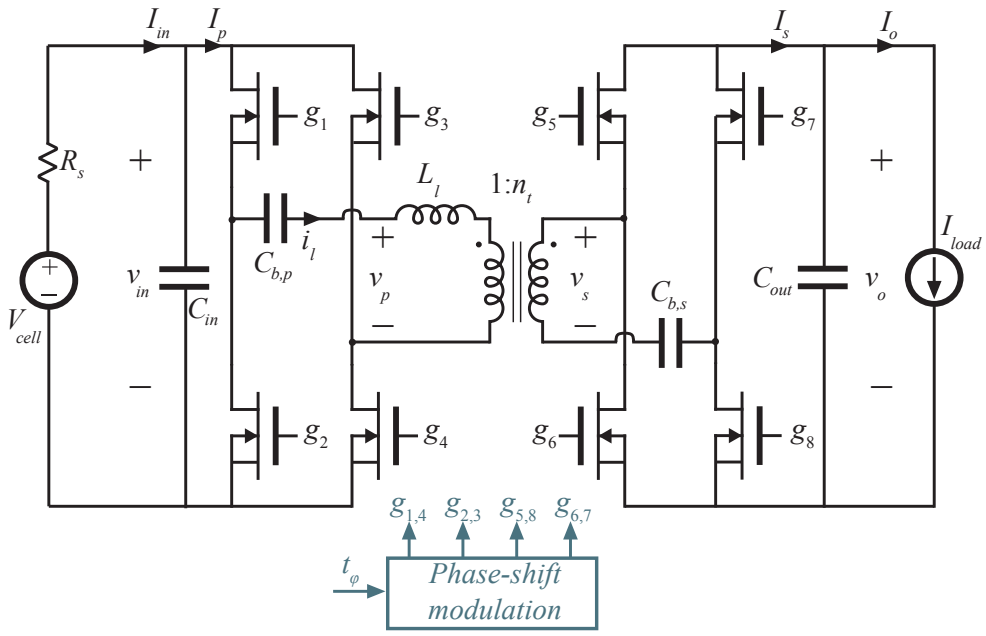


Fig. 5.1: Circuit schematics of a conventional dual-active bridge (DAB) converter.

5.1 Modeling of Integrated dc/dc Converter

The integrated dc/dc converter can be implemented using any isolated and in some cases non-isolated dc/dc topology, as discussed in Chapter 3. In this work, the modular system is implemented using an isolated dual-active bridge (DAB) converter as an example. DAB converter is a bidirectional topology that offers high efficiency and low rms currents among isolated dc/dc topologies over the relatively narrow range of operating voltages [74, 104–106]. A schematic for DAB converter is shown in Fig. 5.1 and circuit parameters for an example design are given in Table 5.1.

The DAB converter has a primary and a secondary side active H-bridge which are switched via gate signals $[g_1 - g_4]$ and $[g_5 - g_8]$ respectively. In this work, the traditional method of phase-shift modulation between primary and secondary side bridges is used to control the current through the DAB tank/leakage inductance, L_l [104]. The active bridges are switched to produce square voltage waveform v_p and v_s, as shown in Fig. 5.2. In a switching time period T_s, a small amount of phase-shift, t_φ (in units of time) between

Table 5.1: Example design parameters for a cell-level dual-active bridge converter

Parameter	**Value**
DAB Input Voltage (V_{in})	2.7-4.3 V
DAB Output Voltage (V_o)	11-17 V
Transformer Turns-ratio (n_t)	1:4
Tank Inductance (L_l)	40 nH
Input Capacitance (C_{in})	198 μF
Output Capacitance (C_{out})	198 μF
Primary DC Blocking Capacitance ($C_{b,p}$)	176 μF
Secondary DC Blocking Capacitance ($C_{b,s}$)	80 μF
Input Series Resistance (R_s)	$\approx$ 2 mΩ
Switching Frequency (f_s)	200 kHz
Maximum Efficiency (η)	93%
Power Rating (P_{rated})	40 W

primary and secondary bridge is used as the control variable to set the current, i_l through the tank inductor. The average input and output currents of the converter over a switching period are determined by averaging appropriately scaled inductor current.

In order to proceed with the control design of DAB converter for the modular battery system, the small-signal, averaged control-to-output voltage ($G_{vo,\varphi}$), control-to-input voltage ($G_{vin,\varphi}$), and control-to-input current ($G_{iin,\varphi}$) transfer functions need to be developed. In order to do so, the average input and output currents of the converter over a single switching period are considered. In the lossless case, when switching transitions are neglected, the average primary and secondary bridge current are evaluated from the waveforms in Fig. 5.2. These averages are approximated under the assumption that any variations in $v_{in}(t)$ and $v_o(t)$ occur slowly with respect to switching behaviors and can therefore be approximated as constant in a given switching period, T_s

$$\langle i_p \rangle |_{T_s} \approx \int_0^{T_s} i_p(t)dt = \frac{v_o(t)}{n_t L_l T_s} \left(T_s t_\varphi - 2{t_\varphi}^2 \right) \ , \tag{5.1}$$

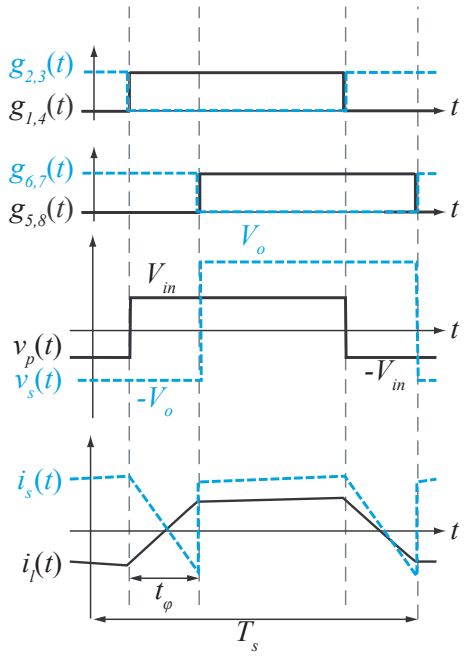


Fig. 5.2: Steady-state operating waveforms of a conventional dual-active bridge (DAB) converter with phase-shift modulation.

$$\langle i_s \rangle |_{T_s} \approx \int_0^{T_s} i_s(t)dt = \frac{v_{in}(t)}{n_t L_l T_s} \left(T_s t_\varphi - 2{t_\varphi}^2 \right) \ . \tag{5.2}$$

Here v_o is the output voltage of DAB, n_t is the transformer turns ratio, L_l is the tank inductance, T_s is the switching period, and t_φ is the phase-shift command expressed in units of seconds. As expected, the currents can be controlled via phase-shift, t_φ. In the scenario where tank inductance is small and conduction losses are high, the steady-state averaged input and output current can be expressed as given in [99, 106].

Next, these relationships are perturbed, and linearized for small-signal variation in the frequency domain.

$$\hat{i}_p = K_{i\varphi}\hat{t}_\varphi + K_{iv}\hat{v}_o \ , \tag{5.3}$$

$$\hat{i}_s = \frac{K_{i\varphi}}{n_t}\hat{t}_\varphi + K_{iv}\hat{v}_{in} \ , \tag{5.4}$$

where small signal variables are denoted with hats. $K_{i\varphi}$ and K_{iv} are scalar gains evaluated at the steady-state operating point and given by,

$$K_{i\varphi} = \frac{V_o}{n_t L_l T_s}\left(T_s - 4T_\varphi\right) \tag{5.5}$$

$$K_{iv} = \frac{1}{n_t L_l T_s}\left(T_s T_\varphi - 2{T_\varphi}^2\right) \ . \tag{5.6}$$

The input impedance seen by the converter at the port defined by the voltage v_{in} is,

$$Z_i = R_s||C_{in} = \frac{R_s}{1 + sR_sC_{in}} \ , \tag{5.7}$$

where R_s is the series resistance between the battery and input port of DAB converter, and includes cell internal resistance, connection, and wiring resistances. Similarly, the impedance seen at the output of the converter defined by the voltage v_o is,

$$Z_o = R_{dab}||C_{out}||Z_{out} \ , \tag{5.8}$$

where R_{dab} is the low frequency output resistance of the DAB converter itself, which is determined primarily by losses and ZVS transitions in the converter, both of which are neglected in this analysis [107]. C_{out} is the output capacitance of the DAB converter. Z_{out} models the total impedance as seen by the DAB converter at its output port. Based on the output port connection, Z_{out} is determined by impedances of other converters that may be connected in parallel at the output port, and the type of output load which can be a power sink/source or a current sink/source. For this work, without any loss of generality we consider a current sink load with high impedance at the output port which results in,

$$Z_o \approx R_{dab}||C_{out} = \frac{R_{dab}}{1 + sR_{dab}C_{out}} \ . \tag{5.9}$$

Then the small-signal input voltage, v_{in}, and output voltage, v_o, are given by

$$\hat{v}_{in} = \hat{i}_p Z_i = K_{i\varphi} Z_i \hat{t}_\varphi + K_{iv} Z_i \hat{v}_o \tag{5.10}$$

$$\hat{v}_o = \hat{i}_s Z_o = \frac{K_{i\varphi} Z_o}{n_t} \hat{t}_\varphi + K_{iv} Z_o \hat{v}_{in} \ . \tag{5.11}$$

Thus, after solving (5.10) and (5.11), the control-to-input voltage and control-to-output voltage transfer functions of the converter in open loop are,

$$G_{vin,\varphi} = \frac{\hat{v}_{in}}{\hat{t}_\varphi} = K_{i\varphi} \frac{Z_i \left(1 + K_{iv} \frac{Z_o}{n_t}\right)}{1 - K_{iv}^2 Z_i Z_o} \ , \tag{5.12}$$

$$G_{vo,\varphi} = \frac{\hat{v}_o}{\hat{t}_\varphi} = K_{i\varphi} \frac{Z_o \left(\frac{1}{n_t} + K_{iv} Z_i\right)}{1 - K_{iv}^2 Z_i Z_o} \ . \tag{5.13}$$

The input current, i_{in}, can be expressed as a function of DAB primary-side current, i_p, as,

$$\hat{i}_{in} = \frac{1}{1 + sR_s C_{in}} \hat{i}_p = H_{in} \hat{i}_p \ . \tag{5.14}$$

Replacing v_o from (5.11) into (5.3) and using (5.14), the control-to-input current transfer function of the converter in open-loop is,

$$G_{iin,\varphi} = \frac{\hat{i}_{in}}{\hat{t}_\varphi} = \frac{H_{in} K_{i\varphi} + \frac{H_{in} K_{iv} K_{i\varphi}}{n_t} Z_o}{1 - H_{in} K_{iv}^2 Z_o R_s} \ . \tag{5.15}$$

This provides the necessary framework needed for diving into design of control algorithms for the modular battery system. If a different topology is chosen for integrated dc/dc converter, a similar analysis can be done to find out the control-to-input and control-to-output relationships.

5.2 Distributed Control for Series-input, Parallel-output xEV Battery System

The modular xEV battery system architecture, developed in Chapter 3, divides the conventional high step-down dc/dc converter functionality among multiple integrated dc/dc converters, with one converter per battery cell. The system architecture is shown in Fig. 5.3. In this configuration, individual dc/dc converters are connected in series-input, parallel-output configuration with each input connected directly in parallel with a battery cell. The total LV bus load current is then divided among the cells through the partial-power

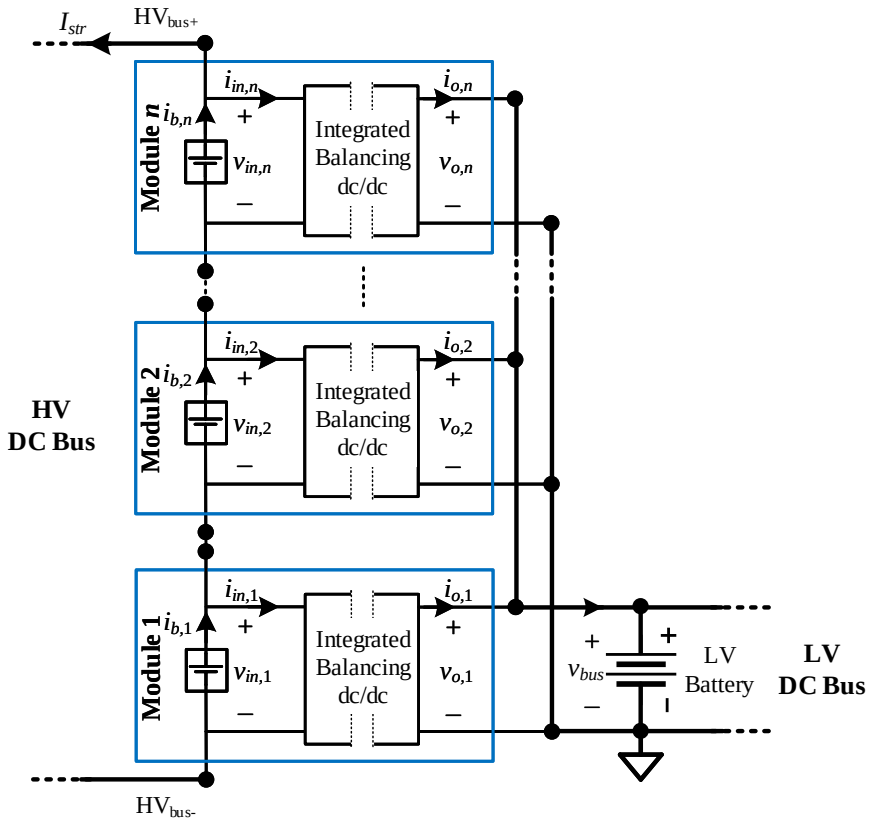


Fig. 5.3: Proposed xEV modular battery system employing several battery modules to make a HV bus for drivetrain, and LV bus for auxiliary loads.

processing integrated converters. Control of the individual converters is designed to produce small differences in the distribution of LV bus load among individual cells, resulting in regulated variations in each cell current which can be leveraged for runtime balancing of cells.

Due to the large number of converters in the modular system, practically controlling the bus voltage with good stability and robustness becomes a challenge. While a central controller can be used to split loads among dc/dc converters, such method relies on high-speed digital communication, and therefore may not be desirable for time-critical closed-loop regulation. A distributed control approach can increase system performance and robustness, as no communication is required for time critical control.

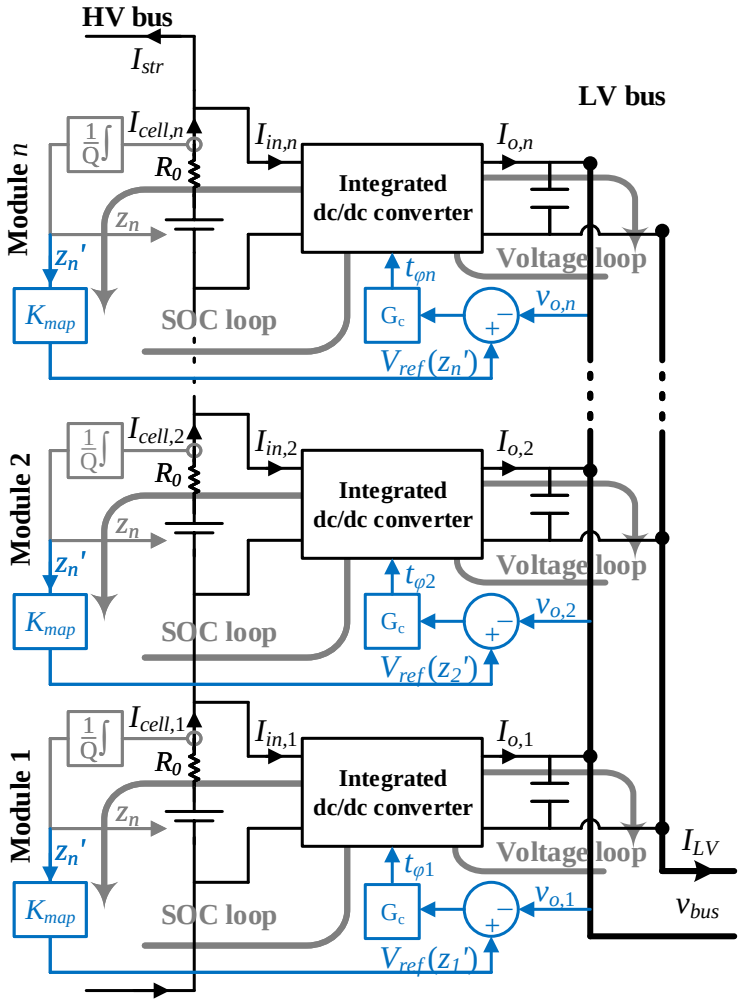


Fig. 5.4: Proposed distributed control method for xEV modular battery system employing local output voltage and cell SOC loop inside each battery module.

In order to alleviate communication requirements necessary to produce correct division of LV bus load among cells, a distributed bus voltage regulation control is proposed. An implementation of the distributed approach at cell-level integrated dc/dc converter is shown in Fig. 5.4. The control goal of each integrated dc/dc converter is same i.e. regulate the LV bus voltage and balance its own cell to a reference value by splitting LV bus load proportional to its cell state of charge (SOC). In the proposed distributed control, the LV bus voltage itself is used as a means of communicating the average balancing target voltage

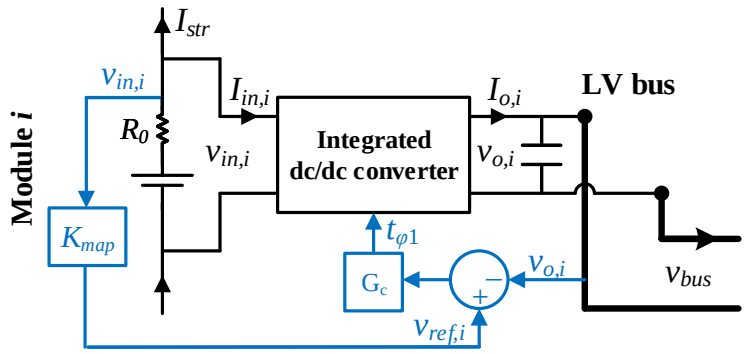
or SOC. Within some range of current limits, each dc/dc converter regulates the cell voltage or SOC to a value consistent with the current bus voltage.

For simplicity of implementation, control goal can be based on voltage balancing among the cells but balancing based on cell estimated SOC or SOH can be implemented in the same manner. These control goals will be discussed in the next sections.

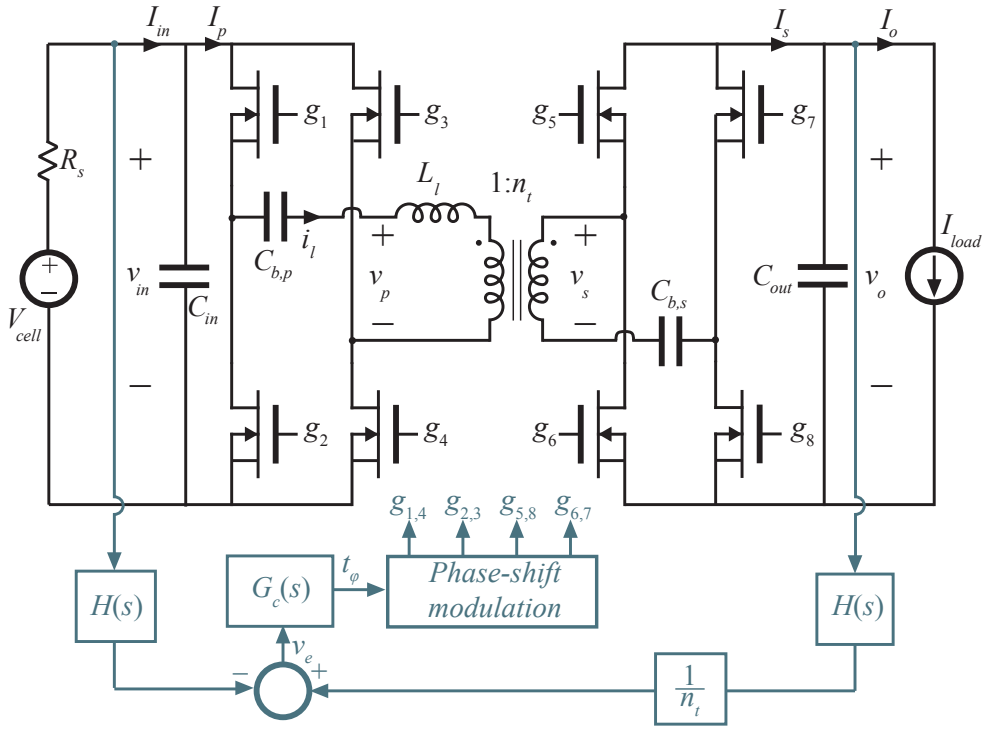
5.2.1 Cell Voltage Balancing and DC Bus Voltage Regulation

In the voltage balancing implementation, each integrated dc/dc converter has the control goal $V_{ref,i} = V_{o,i} = K_{map}V_{in,i}$, and is controlled to regulate its input current $i_{in,i}$ according to the difference between the cell voltage and scaled bus voltage. A block-level control diagram for cell voltage balancing and an example implementation using DAB is shown in Fig. 5.5. When a load is applied to the LV bus, the load current will distribute among the dc/dc converters relative to the voltage difference. If cell voltages are balanced and have matched capacity, load current distributes evenly among all converters; if a high dc gain controller is used, the system stabilizes with zero control error, i.e. with a bus voltage equal to the scaled cell voltages. Further, the bus voltage tracks the cell voltages as variations in pack SOC and current cause the bus voltage to vary. If cell voltages are unbalanced, this control results in the power converters reducing discharge of the cells with voltage below the scaled bus voltage and increasing discharge current of cells above it, independent of the magnitude and direction of the overall pack string current. With this approach, no further communication is required between individual dc/dc converters. Furthermore, the system can easily be scaled to an arbitrary number of cells in the pack, greatly simplifying the BMS.

Since the shared bus voltage itself is used to communicate the reference target for each dc/dc bypass converter, V_{bus} must be allowed to vary proportional to the cell state of interest, which is the cell voltage for the case of voltage balancing. The nominal voltage and total variation can be set arbitrarily by the control law, but the variation must be sufficiently large to avoid noise limitations. As an example for xEV system, the nominal bus voltage reference is set close to $V_{bus} = 14$ V and the control goal is set to $V_{in,i} = \mathrm{K}V_{bus}$.



(a)



(b)

Fig. 5.5: (a) Control diagram for integrated dc/dc converter to achieve distributed bus voltage regulation and automatic cell voltage balancing, and (b) an example hardware implementation of this distributed control on dual-active bridge (DAB) converter.

With typical Li-Ion battery cell voltage characteristics, this results in a bus voltage range of 11-16 V. This range is within what is typical of the LV bus of electric vehicles (11-17 V [74]). For the example design of Fig. 5.5b, the controller uses values for input and output voltages

sensed through sensing gain $H(s)$ to generate an error signal, defined in the Laplace domain as,

$$v_e(s) = H(s)\left(\frac{v_o(s)}{n_t} - v_{in}(s)\right) \ , \tag{5.16}$$

where n_t is the DAB transformer turns ratio. The error signal is fed through a compensator $G_c(s)$ to produce a control signal t_φ that adjusts the phase-shift of the transistor gate modulation signals. The desired control-to-error transfer function can be calculated using (5.12) and (5.13) and is given by,

$$G_{e\varphi} = \frac{\hat{v}_e}{\hat{t}_\varphi} = K_{i\varphi}\frac{\frac{Z_o}{n_t{}^2} - Z_i}{1 - K_{iv}^2 Z_i Z_o} \ . \tag{5.17}$$

For the system parameters given in Table 5.1, a bode plot of 5.17 is given in Fig. 5.6a.

The system is compensated with a standard proportional-integral (PI) compensator of the form,

$$G_c = G_\infty\left(1 + \frac{\omega_z}{s}\right) \ , \tag{5.18}$$

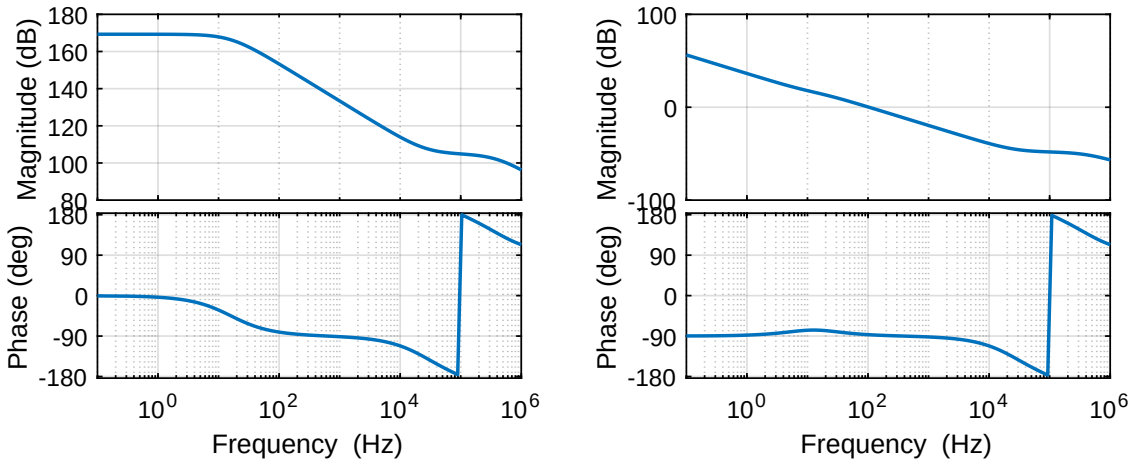
and the resulting system loop gain is given by,

$$T(s) = G_{e\varphi}G_c \ . \tag{5.19}$$

The compensator gain G_∞ is selected to place the crossover frequency of the system at 100 Hz with ω_z placed a decade below. The resulting loop gain is plotted in 5.6b. Analytical predictions indicate a phase margin of 89° and gain margin of 48 dB. The compensator achieves zero steady-state error in regulating the converter input voltage to match the shared bus voltage, recognizing that the cell voltage may be higher or lower due to the series resistance.

LV Bus Load Current Sharing

To evaluate the current sharing characteristics of n parallel-output integrated dc/dc converters, the model shown in Fig. 5.7 is used. Each battery module's variable quantities



(a) (b)

Fig. 5.6: (a) Bode plot of the magnitude and phase of the control-to-error signal $G_{e\varphi} = \frac{\hat{v}_e}{\hat{t}_\varphi}$, and (b) bode plot of the magnitude and phase of compensated system loop gain $T(s)$ with the proposed PI compensator.

are denoted by a subscript between 1,2...n where i is the ith battery module. A first order equivalent circuit model is used to represent battery cell inside each module. The cell SOC, denoted by z_i, is defined as,

$$z_i(t) = z_i(t_0) - \frac{1}{Q_i}\int_{t_0}^{t} i_{cell,i}(t)dt \ . \tag{5.20}$$

where Q_i is the total capacity of the battery cell, usually measured in Ah or mAh. The cell open-circuit voltage depends on the state of charge of the cell; when a cell is fully charged, its open-circuit voltage is higher than when it is discharged. This behavior is modeled by the dependent voltage source $v_{ocv,i}$, whose voltage depends on $z_i(t)$ at any given time. The relationship between open-circuit voltage and cell SOC is a nonlinear function primarily dictated by the battery internal chemistry. For this work, a linear relationship between $v_{ocv,i}$ and z_i is assumed, which simplifies the analysis to allow insight into the operating principles. This assumption is justified by the fact that common SOC operation range (SOC = 20% - 90%) of many commercially available cells can be well approximated by a linear relation. A series resistance $R_{s,i}$ is used to model the internal voltage drop of a cell when

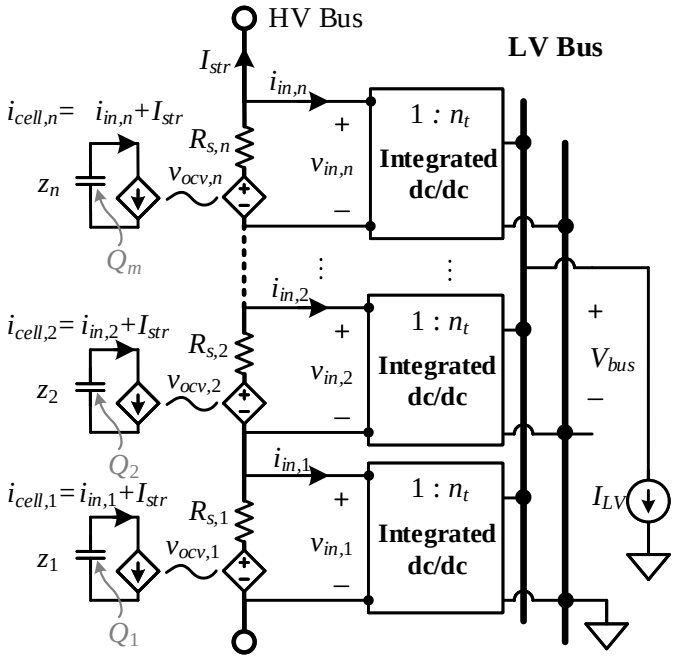


Fig. 5.7: Modular battery system with battery cell model.

its loaded. Voltage $V_{in,i}$, sensed by each dc/dc converter, is the cell terminal voltage,

$$V_{in,i} = V_{ocv,i} - i_{cell,i}R_{s,i} \ . \tag{5.21}$$

The following analysis evaluates load current sharing among integrated converters under conditions where a mismatch in cell series resistance, initial state of charge, or cell capacity exists among cells in a pack.

Case A: Resistance Mismatch among Cells

First, non-uniform resistance $R_{s,i}$ among cells is considered. For analysis, a thought experiment is performed based on the following initial condition assumptions: the state of charge of all the batteries is equal $z_1 = z_2 = ... = z_n$ and as a result the open-circuit cell voltages are all equal to let's say $v_{ocv,nom}$, each cell's capacity is equal to nominal capacity, $Q_{nom} = Q_1 = Q_2 = ... = Q_n$, and the series resistance of all cells except the resistance of cell n are equal to nominal resistance, $R_{s,nom} = R_{s,1} = R_{s,2} = ... = R_{s,n-1}$. The internal

series resistance of cell n equals,

$$R_{s,n} = R_{s,nom} + \Delta R_s \ . \tag{5.22}$$

In this thought experiment, the system is activated with each integrated dc/dc running the voltage balancing control law, as shown in Fig. 5.7. The dc/dc converters regulate each battery cell terminal voltage to V_{bus}/n_t, and in doing so the cell terminal voltages become equal, $V_{in,1} = V_{in,2} = ... = V_{in,n} = V_{bus}/n_t$. Since the initial SOC and v_{ocv} of all battery cells are equal, the converter input currents are initially given by,

$$i_{in,i} = \frac{v_{ocv,nom} - \frac{V_{bus}}{n_t}}{R_{s,nom}} \ , \tag{5.23}$$

for all cells except for cell n, which has the initial input current,

$$i_{in,n} = \frac{v_{ocv,nom} - \frac{V_{bus}}{n_t}}{R_{s,nom} + \Delta R_s} \ . \tag{5.24}$$

As a result, due to ΔR_s, the current through battery cell n is initially lower than the other cells and it is discharging slower than other cells. Since the battery open-circuit voltage is dependent on cell SOC, the slow change in SOC of cell n causes its open-circuit voltage, $v_{ocv,n}$ to decrease slower than other cells. Over time, this results in an increase in voltage difference $v_{ocv,n} - V_{bus}/n_t$ that triggers the input current, $i_{in,n}$ to increase. This effect continues until the system reaches an equilibrium, where cell n tracks other cells at an equal discharge rate but with a constant open-circuit voltage offset, $\Delta v_{ocv,n}$.

$$v_{ocv,n} = \frac{V_{bus}}{n_t} + \Delta v_{ocv,n} \ . \tag{5.25}$$

In this equilibrium state, all battery cells charge and discharge at the same dV/dt rate, meaning that all battery cells have identical current and cell terminal voltage. The primary impact of resistance mismatch is an offset in cell open-circuit voltage (and thus SOC) during charge and discharge. The resistance mismatch only impacts LV load current

sharing during transients, but does not impact current sharing under equilibrium constant charge or discharge currents.

Case B: SOC Mismatch among Cells

The same assumptions are valid as in case A, except that the resistances are now all equal and cell open-circuit voltages are not equal due to mismatch in SOC, $v_{ocv,1} = v_{ocv,2} = ... = v_{ocv,(n-1)} = V_{bus}/n_t$, and $v_{ocv,n}$ is given by (5.25). At the startup, the current of cell n will be higher than the rest of the cells due to higher $v_{ocv,n}$. As a result, cell n will discharge at faster rate, lowering its SOC and terminal voltage faster than the rest of the cells, until $\Delta v_{ocv,n}$ will be eliminated. At this point, the system will be in equilibrium and the converters will share the load evenly. Thus initial SOC mismatch is balanced as expected and does not impact LV load current sharing in the equilibrium.

Case C: Capacity Mismatch among Cells

In the case of cell capacity mismatch, we assume that all cell capacities are equal to the nominal capacity, $Q_1 = Q_2 = ... = Q_{n-1} = Q_{nom}$, except for the capacity of cell n, which is lower by ΔQ_n,

$$Q_n = Q_{nom} + \Delta Q_n \ . \tag{5.26}$$

The rest of the assumptions made in case A are still valid in this case, except the resistance, which is assumed to be equal among all the cells, as in case B. All cell currents are equal to a nominal value $I_{in,nom} = i_{in,1} = i_{in,2} = ... = i_{in,n-1}$, except for the current of cell n, which is unknown.

The analysis is done assuming the system has reached an equilibrium point, with constant average voltage increase/decrease rate among all the cells. Using the assumption of linear dependency between cell SOC and open circuit voltage, the rate of charge/discharge of all equal capacity cells could be expressed based on the capacitor equation

$$\frac{dV_{in,nom}}{dt} = \frac{I_{str} + I_{in,nom}}{Q_{nom}} \ , \tag{5.27}$$

while the rate of charge/discharge of cell n is

$$\frac{dV_{in,n}}{dt} = \frac{I_{str} + I_{in,n}}{Q_{nom} - \Delta Q_n} \ , \tag{5.28}$$

The difference between the nominal current, current of equal capacity cells, and the current of cell n is defined as,

$$\Delta I_{in,n} = (I_{str} + I_{in,nom}) - (I_{str} + I_{in,n}) \ , \tag{5.29}$$

and the nominal current $I_{in,nom}$ can be expressed as a function of the load current and the difference current $\Delta I_{in,n}$,

$$I_{in,nom} = \frac{n_t I_{LV} + \Delta I_{in,n}}{n} \ . \tag{5.30}$$

Since the system has reached the equilibrium point, the charge/discharge rate is equal among all the cells. Comparing the right hand side of (5.27) and (5.28) yields,

$$\frac{I_{str} + I_{in,nom}}{I_{str} + I_{in,n}} = \frac{Q_{nom}}{Q_{nom} - \Delta Q_n} \ . \tag{5.31}$$

Substituting (5.29) into (5.31) and solving for $\Delta I_{in,n}$ results in,

$$\Delta I_{in,n} = \frac{\Delta Q_n}{Q_{nom}} (I_{str} + I_{in,nom}) \ . \tag{5.32}$$

Equation (5.32) yields the worst case current mismatch of the different capacity cell, cell n, as a function of its capacity mismatch, string current, I_{str} and nominal load current per cell, $I_{in,nom}$. Based on (5.30), the delta current (5.32) is expressed as a function of LV bus load current I_{LV},

$$\Delta I_{in,n} = \frac{\Delta Q_n}{Q_{nom} - \frac{\Delta Q_n}{n}} (I_{str} + \frac{n_t I_{LV}}{n}) \ . \tag{5.33}$$

The first term in (5.33) can be well approximated by the ratio $\Delta Q_n / Q_{nom}$, showing that the current mismatch is a function of the relative capacity mismatch and the battery cell current.

The results of (5.32) and (5.33) demonstrate that if linear dependency between SOC and cell terminal voltage is assumed, the mismatch in current sharing will scale up with cells capacity mismatch. This is a desired behavior, where higher capacity cells provide more load current, i.e. sharing the load based on their energy storage ability. As an example, consider a large relative capacity mismatch of 5%, no string current for simplicity, and nominal converter input current of 10 A, which scales to the LV load side as a 2.5 A using the scaling factor n_t of Table 5.1 and assume 100% efficiency. The resulting current mismatch based on (5.32) is given by $\Delta I_{in,n}$ = (0.05*10 A) = 0.5 A on the battery side and only 125 mA on the LV bus side. The design of integrated converters can include the current limit based on maximum LV bus load sharing current amplitude topped with the expected current sharing mismatch.

5.2.2 Cell SOC/SOH Balancing and DC Bus Voltage Regulation

Similar to distributed cell voltage balancing, cell SOC or SOH balancing can be implemented for the modular xEV battery system, as shown in Fig. 5.4. In the SOC balancing implementation, each integrated dc/dc converter has the control goal $V_{ref,i} = V_{o,i} = K_{map}SOC_i$, and is controlled to regulate its input current $i_{in,i}$ according to the difference between the cell SOC and scaled bus voltage. A block-level control diagram showing cell SOC balancing control embedded inside each dc/dc converter is shown in Fig. 5.8. When a load is applied to the LV bus, the load current will distribute among the dc/dc converters relative to the SOC difference. If cell SOCs are balanced and have matched capacity, load current distributes evenly among all converters; if a high dc gain controller is used, the system stabilizes with zero control error, i.e. with a bus voltage equal to the scaled cell SOC. Further, the bus voltage tracks the cell SOC according to the value of mapping, K_{map}. If cell SOC are unbalanced, this control results in the power converters reducing discharge of the cells with SOC below the scaled bus voltage and increasing discharge current of cells above it, independent of the magnitude and direction of the overall pack string current. With this approach, no further communication is required between individual dc/dc converters. Furthermore, the system can easily be scaled to an arbitrary number of cells in the pack.

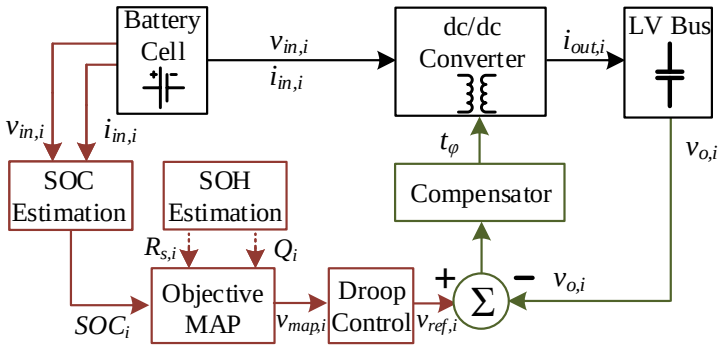


Fig. 5.8: Control diagram for integrated dc/dc converter to achieve distributed bus voltage regulation and automatic cell SOC balancing.

With this control architecture, the modular xEV battery system of Fig. 5.4 includes a voltage loop and an SOC loop for each dc/dc converter, as shown in Fig. 5.8. In addition, the output voltage loop of each dc/dc converter senses the DC bus voltage and performs a control action based on the objective map based control goal. A unit averaging method is used in the output voltage compensator design, i.e. all cells and dc/dc converter units are assumed to have the same parameters and thus the system is averaged and treated as one virtual unit. As a first step, the battery cell is assumed to behave as a constant voltage source with no interactions with the output voltage loop. Under these assumptions a standard PI compensator is designed based on the control-to-output transfer function (5.13) of virtual unit and implemented in each individual converter. Each converter then independently computes the mapped voltage, $v_{map,i}$ under its control objective and regulates its cell SOC and output voltage.

If a high gain controller is used, the dc/dc converters behave like parallel output voltage sources and a slight voltage sensing error can lead to uneven current sharing among them. To achieve uniform current sharing among dc/dc converters, a droop control is introduced. Droop control is an effective way to enforce even load sharing among paralleled voltage source units operating in a closed loop. In the cell balancing system, a virtual droop resistor is added to the SOC loop, as shown in Fig. 5.8. In order to make the loading of

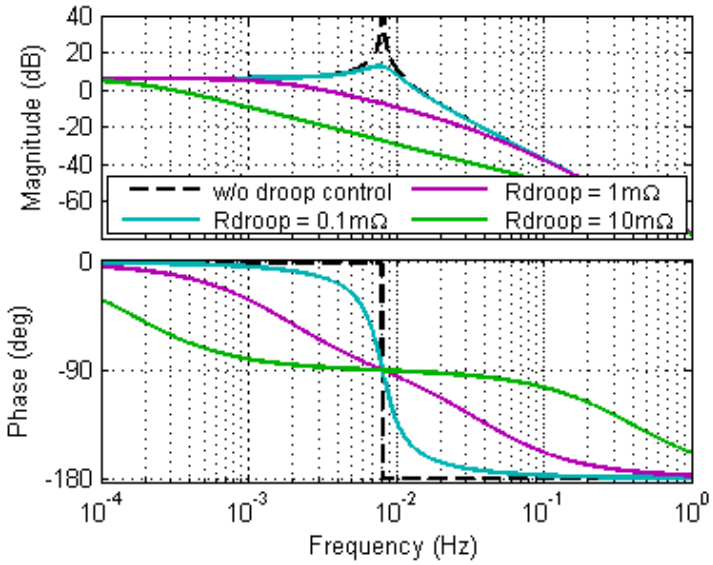


Fig. 5.9: Bode plot of the magnitude and phase of the SOC loop gain with PI controller and R_{droop} = [0, 0.1, 1, 10] mΩ.

each bypass module equal, the droop control algorithm is the same for each converter, with the mapped voltage updated as,

$$v_{ref,i} = v_{map,i} - i_{in,i} R_{droop} \ . \tag{5.34}$$

With droop control, the SOC loop gain can be evaluated as,

$$T_{SOC} \approx (n-1) \frac{1}{1 + (\frac{nR_{droop}}{K_{map}} + \frac{K_p}{K_i})s + \frac{n}{K_i K_{DABi} K_{map}} s^2} \tag{5.35}$$

which shows that droop control resistance affects poles of the SOC loop gain and damps the system response, as shown in Fig. 5.9. With no droop control, $R_{droop} = 0$, the phase margin is close to zero. Increasing droop resistance improves the phase margin of the system. However it is important to note that an increase in droop resistance decreases the cross-over frequency of the SOC loop gain and therefore decreases the system bandwidth for the SOC loop, which translates into a prolonged SOC balancing process. For the system parameters of Table 5.1, a droop resistance of 6.4 $m\Omega$ is chosen as a suitable trade-off between good control bandwidth and acceptable stationary error. A detailed stability analysis for droop

control applied to modular battery system is covered in [99].

DC Bus Load Sharing with Cell Capacity Mismatch

To evaluate the current sharing characteristics of n parallel-output dc/dc converters running SOC balancing objective map, the model shown in Fig. 5.7 is used. Each battery module's variable quantities are denoted by a subscript between 1,2...n where i is the ith battery module. A first order equivalent circuit model is used to represent battery cell inside each module. The cell SOC, denoted by z_i, is defined as given in (5.20). If each cell has a different capacity then the system will split the load differentially to keep cell SOC balanced. The converter input current of cell i can be expressed as,

$$I_{in,i} = \frac{(I_{str} + \frac{I_{LV}}{n})\Delta Q_i}{Q_{nom}} \tag{5.36}$$

where Q_{nom} is the nominal capacity of all cells in pack, ΔQ_i is the difference between capacity of cell i, Q_i, and nominal capacity. As shown by (5.36), the current required to keep SOC of all cells balanced is a function of pack string current, bus load current, and the ratio of capacity mismatch to nominal capacity.

Estimating Capacity Difference using LV Bus Load Sharing

If the control law inside each battery module is designed based on SOC balancing objective map, then the DC bus load will be split among converters based on their SOC as shown by (5.36). Eq. (5.36) can be used to estimate the capacity mismatch as follows,

$$\Delta Q_i = \frac{I_{in,i} Q_{nom}}{(I_{str} + \frac{I_{LV}}{n})} \tag{5.37}$$

where the capacity mismatch is written as a function of the nominal cell capacity. This can also be written as a function of cell i capacity as,

$$\Delta Q_i = \frac{I_{in,i} Q_i}{(I_{str} + \frac{I_{LV}}{n})(1 + \frac{I_{in,i}}{(I_{str} + \frac{I_{LV}}{n})})} \tag{5.38}$$

The capacity mismatch information can be used to run the SOH balancing objective

map. However, with the SOH objective map, DC bus voltage is not a simple constant-gain multiple of pack SOC and hence does not represent average SOC of the pack. With SOH balancing, each battery module is running an objective map similar to,

$$SOC_{ref,i} = m_i V_{bus} + b_i \tag{5.39}$$

where m_i and b_i are chosen based on the life objective map gain. With this control action, the capacity mismatch of cell i can be written as,

$$\Delta Q_i = \frac{m_{nom} Q_{nom}}{m_i I_{str}} (I_{in,i} + I_{str}) - Q_{nom} \tag{5.40}$$

under the condition of uniformly distributed cell capacity values and no DC bus load. This result shows that the capacity mismatch can be determined using just local information to implement SOH balancing.

5.3 Partially-Distributed Control for Series-input, Parallel-output xEV Battery System

In this section, an alternate control method, named partially-distributed control, is analyzed for the modular xEV battery system of Fig. 5.3. The control goals for the modular system are still the same. The converters, as a group, need to regulate their output voltage that is connected to LV DC bus, supply power to DC bus loads, and balance battery cells to a common reference. The partially distributed control does not use bus voltage as a means of communication. As a result, the bus voltage can be regulated to a fixed setpoint. This capability can be very useful since traditionally xEV LV bus is tied to a LV lead acid battery whose SOC is maintained by regulating the bus voltage to a specific voltage setpoint. By regulating output voltage to a fixed reference, the partially distributed control can maintain the state-of-charge of the lead-acid battery.

As discussed earlier, due to the integrated system, the DC bus voltage regulation and battery cell balancing are inherently coupled. Based on mismatches in cell SOC and

capacity within the battery pack, each converter needs to supply a different amount of power to support the total DC bus load and achieve battery cell balancing. To control power delivered by each module, there are n control objectives which can be achieved using n controllable variables. Based on design requirements and ease of measurement, the desired control variables can be chosen among a combination of input and output current and voltage variables with the goal to achieve control objectives in a stable manner.

In this work, a partially distributed control scheme, shown in Fig. 5.10, is developed which decouples voltage regulation and cell balancing and achieves all control objectives in a stable manner. The proposed scheme is implemented by controlling the input current of all dc/dc modules in a distributed fashion, and the output voltage and cell SOC using a central supervisory controller. The proposed approach is based on a multi-loop, linear feedback control that is distributed between the central BMS controller and individual dc/dc modules of Fig. 5.3.

As a building block, the dc/dc modules are designed identically. Each dc/dc module employs a local current feedback-loop that regulates its input current to a reference current command, $I_{in,ref,i}$. This local feedback loop provides input current regulation with a desired bandwidth, designed to meet system specifications. The input current control can be replaced by output current without loss of generality. However, the input current has the added benefit of direct control of battery cell current that ensures cell current limit protection and safety. Furthermore, the input current measurement is shared with battery SOC and SOH estimation controllers.

A central, supervisory control approach utilizing central BMS controller is proposed for DC bus voltage regulation and cell SOC control, as shown in Fig. 5.10. The central BMS controller generates one common current reference command and n individual delta current reference commands. This is done using two separate outer control loops inside the central BMS controller, referred to here as voltage loop and SOC loop. Each of the outer voltage and SOC loop only acts on the well behaved inner dc/dc input current loop, which in many cases can be represented as a single pole, low-pass system. Thus the existence of

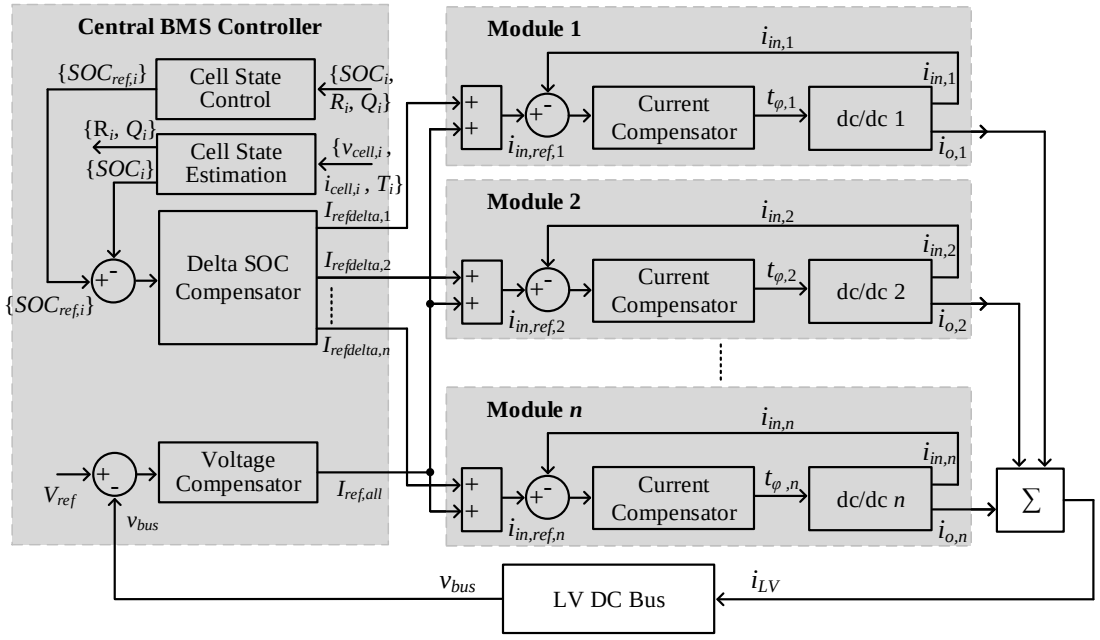


Fig. 5.10: Partially-distributed control approach for the modular xEV battery system. Each dc/dc module has a local current feedback-loop that runs at a fast rate to regulate input current. The central BMS controller incorporates the voltage and delta SOC compensators and provides a common current reference and an individual delta current reference to perform LV bus voltage regulation and cell balancing.

local current feedback loop inside each dc/dc converter greatly simplifies the control of bus voltage and cell SOC regulation. Since all dc/dc converters share their output voltage, a common voltage-loop can be designed for DC bus voltage regulation. This is possible by averaging all building block DC/DC converters and representing them with a unit averaged module. The voltage-loop compensator provides a common current reference command, $I_{ref,all}$ to all the dc/dc modules. Thus, outside of the operation of SOC loop, the common current reference command is shared equally among the inner current loops of the dc/dc modules. The outer SOC loop utilizes a delta SOC compensator that provides individual delta current reference commands, $I_{refdelta,i}$ to each dc/dc module. The delta current reference commands produce small variations in the input current of each dc/dc module to enable cell balancing. Therefore, the voltage and delta SOC compensators combined provide the required LV bus voltage regulation and cell balancing control with additional

safety features associated with the internal current loop.

Two conditions are set to decouple the outer voltage and SOC feedback loops and avoid competition among them. I). The voltage loop is designed to run at a higher bandwidth than the SOC loop. II). The sum of all delta current commands is set to zero, $\Sigma_{i=1}^{n} I_{refdelta,i} = 0$ and the current commands are set within the input current limits for the dc/dc modules. Condition I ensures that DC bus voltage loop has a fast response and any undesired perturbation due to load change or delta current command is rejected well. In addition, condition II guarantees that the net effect of delta current commands is zero and SOC loop does not perturb the voltage loop. The two conditions together decouple the outer loops without sacrificing any system performance requirements. The voltage loop can be designed for a high bandwidth (several Hz to kHz) to meet desired steady-state and transient response requirements under large step changes in loads. Furthermore, the SOC loop can be designed for a moderate bandwidth (mHz to Hz) without loss of performance since cell SOC is a relatively slow changing process for large, several Ah capacity xEV battery cells. The decoupling of the two outer loops greatly simplifies the compensator design process and also simplifies the communication requirements, with the common current reference command $I_{ref,all}$ broadcast at a fast rate and the individual delta current reference commands $I_{refdelta,i}$ transmitted at a slow to moderate rate.

Using the partially-distributed control approach, the LV DC bus voltage can be regulated to a desired voltage set-point provided by the supervisory vehicle controller. Traditionally, EVs employ one of a multitude of voltage references, including a lead-acid battery temperature-dependent voltage set-point or a desired voltage value which keeps the lead-acid battery SOC fixed [32]. Furthermore, there might be motivation for the voltage set-point to be defined as a representative of the Li-ion battery pack SOC to improve overall converter efficiency as described in [102, 103]. The proposed approach allows these existing techniques to be easily incorporated into the modular battery system. In addition, the control method is applicable for a wide variety of vehicle applications, including light-duty and heavy-duty vehicles and public transit buses, which may have different DC bus voltage

ranges for auxiliary LV loads, such as 12 V, 24 V, 28 V, or 48 V.

In the partially-distributed control approach, a separate cell state control block provides reference SOC for each cell, $SOC_{ref,i}$, as shown in Fig. 5.10. For traditional SOC balancing objective, this controller can be programmed to provide a common reference such as average pack SOC to all cells. Further advanced state objectives, such as extended life and higher power capability for cells [19,101,103], can also be implemented using the cell state controller by adjusting the reference SOC, $SOC_{ref,i}$ for each cell.

Next, loop gain analysis is provided for each feedback loop of the partially-distributed control approach and designs are provided for the required current, voltage and SOC compensators. The first step in doing so is to select an appropriate dc/dc converter topology for the modular system. Similar to previous section, the isolated dual-active bridge converter with phase-shift modulation control is selected as a bidirectional topology for dc/dc converter in this analysis. The isolated DAB converter schematic is shown in Fig. 5.1 and the parameters are given in Table 5.2.

Table 5.2: Example design parameters for a substring-level dual-active bridge converter.

Parameter	**Value**
DAB Input Voltage (V_{in})	16-26 V
DAB Output Voltage (V_o)	11-17 V
Transformer Turns-ratio (n_t)	3:2
Tank Inductance (L_l)	265 nH
Input Capacitance (C_{in})	40 μF
Output Capacitance (C_{out})	60 μF
Primary DC Blocking Capacitance ($C_{b,p}$)	90 μF
Secondary DC Blocking Capacitance ($C_{b,s}$)	60 μF
Input Series Resistance (R_s)	$\approx$ 8 mΩ
Switching Frequency (f_s)	200 kHz
Maximum Efficiency (η)	95%
Power Rating (P_{rated})	480 W

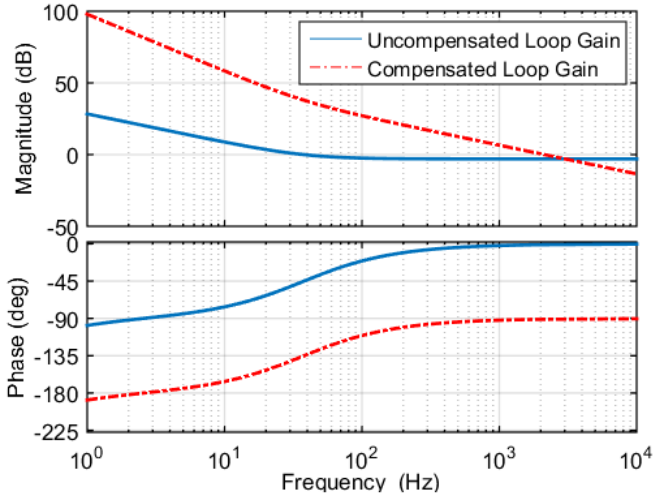


Fig. 5.11: Bode plot showing magnitude and phase of uncompensated (solid blue) and compensated loop gain (dotted red) for the local input current feedback-loop in each dc/dc module.

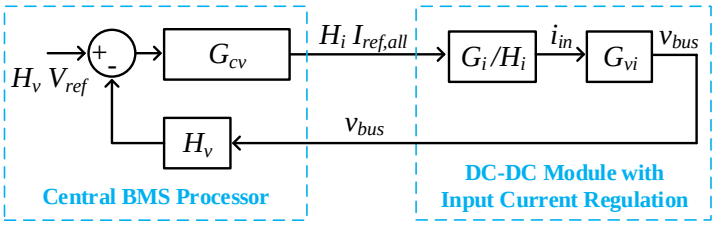


Fig. 5.12: Outer voltage loop acting on the well-regulated inner current loop. The output voltage sensing and compensator are implemented inside the central BMS controller which broadcasts reference current to all the dc/dc modules.

In order to proceed with the control design of the DAB for the proposed system, the local current feedback loop gain and the current compensator design need to be developed. The average control-to-input and control-to-output transfer functions of the DAB converter over a single switching period were derived in earlier section. The current loop is compensated with a standard integral compensator, G_{ci}, resulting in the loop gain $T_i(s) = G_{iin,\varphi}G_{ci}H_iH_{t_\varphi}$. H_i is the current sensor gain, and H_{t_φ} is the PWM modulator gain. For the system parameters of Table 5.2, a bode plot of uncompensated and compensated loop gain is given in Fig. 5.11. Analytical predictions indicate a cross-over frequency of 2 kHz and phase margin of 89^o at nominal operating point of $P_{out} = 360$ W

per dc/dc. This completes the design and analysis of local current feedback-loop inside each dc/dc module, shown in Fig. 5.10. The closed-loop response of this inner current loop is given by,

$$G_i(s) = \frac{T_i(s)}{1 + T_i(s)} \ . \tag{5.41}$$

Next the design of voltage compensator inside the central BMS controller is considered. A unit-averaging method is employed for the system analysis, i.e. all dc/dc modules are assumed to have similar parameters and a virtual dc/dc module, defined using the averaged parameters of all modules, is used for analysis. For a well behaved inner current loop, any variation in the DC operating-point of dc/dc modules does not cause a major variation in the input current closed-loop response, $G_i(s)$. The voltage loop need only act on the well-regulated inner current loop, as shown in Fig. 5.12. In order to proceed with voltage loop analysis, the converter input current-to-output voltage transfer function, G_{vi}, needs to be evaluated. The converter control-to-output voltage transfer function, $G_{v\varphi}$, is

$$G_{v\varphi}(s) = \frac{\hat{v}_{bus}}{\hat{t}_\varphi} = K_{i\varphi} \frac{Z_o \left(\frac{1}{n_t} + K_{iv} Z_i \right)}{1 - K_{iv}^2 Z_i Z_o} \ . \tag{5.42}$$

Using (5.15) and (5.42), the converter input current-to-output voltage transfer function can be found as,

$$G_{vi}(s) = \frac{\hat{v}_{bus}}{\hat{i}_{in}} = \frac{\hat{v}_{bus}}{\hat{t}_\varphi} \frac{\hat{t}_\varphi}{\hat{i}_{in}} \ . \tag{5.43}$$

The voltage loop gain is given by, $T_v(s) = H_v G_{cv} \frac{G_i}{H_i} G_{vi}$. H_v is the voltage sensor gain, and G_{cv} is the voltage compensator which is designed as a standard proportional-integral (PI) compensator. Analytical results show a phase margin of 102^o and a crossover frequency of 100 Hz, which is well below the input current loop bandwidth. A bode plot of uncompensated and compensated voltage loop gain is shown in Fig. 5.13.

A similar approach is used to analyze the SOC loop. The battery cell is modeled as an integrator scaled by cell capacity,

$$G_{SOC,i} = \frac{1}{3600 Q s} \ , \tag{5.44}$$

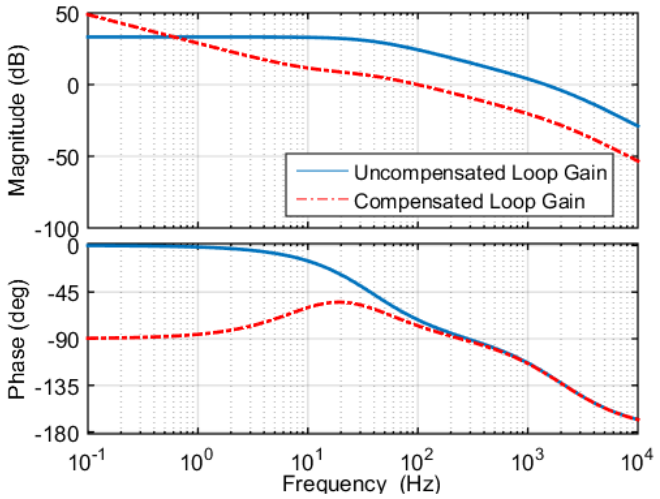


Fig. 5.13: Bode plot showing magnitude and phase of uncompensated (solid blue) and compensated loop gain (dotted red) for the output voltage feedback-loop at nominal operating point of $P_{out} = 360$ W per dc/dc.

where Q is the capacity of the cell in units of Ah. Since the voltage loop works in parallel with the SOC loop, the effect of voltage compensator is incorporated into the analysis as shown by Fig. 5.14. The loop gain of the system can be found from Fig. 5.14 to be,

$$T_{SOC} = (G_{SOC,i}G_{cSOC} + G_{vi}G_{cv}H_v)\frac{G_i}{H_i} \ . \tag{5.45}$$

where G_{cSOC} is the delta SOC compensator which is designed as a standard proportional controller. The delta SOC compensator outputs a delta current reference command for each individual DC/DC module and ensures that the substring SOC tracks its reference SOC. The resulting loop gain is plotted in Fig. 5.15. Analytical predictions show crossover frequency of 20 mHz and phase margin of 90^o. The slow response is expected due to the large capacities of the battery cells.

5.4 Partially-Distributed Control for Independent-input, Series-output Battery System

This section expands the partially-distributed control approach and applies it to the series output systems. The series output battery modules can be used to make up a HV

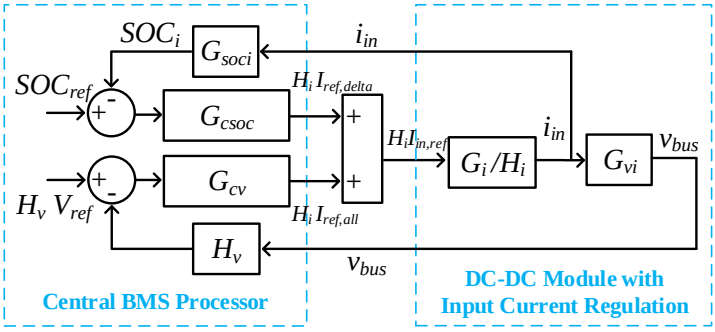


Fig. 5.14: Outer SOC and voltage loop acting on the well-regulated inner current loop. The SOC estimation and SOC compensator are implemented inside the central BMS controller which sends individual delta reference current to all the DC/DC modules.

bus for xEV system or a shared DC bus for micro-grid system. The control goals of each dc/dc converter are still the same, i.e., supply DC bus load and process power relative to the SOC and capacity of a battery cell. In the parallel output dc/dc converters, the differential power processing was achieved via sharing load current. In contrast, the series-output system achieves differential power processing by splitting the total bus voltage and producing small difference in their input-to-output conversion ratios. The focus of this section will be to highlight the key differences between parallel and series-output system and how the partially distributed control, developed in previous section, can be applied to series output system with small changes.

For the series output system, the building block dc/dc converter are designed to have a well-regulated inner current loop, similar to the parallel-output system. This internal feedback loop provides current regulation with a high bandwidth to meet system specifications and a well-designed inner current loop hides the dynamics of the dc/dc converter. In most cases the closed-loop current response can be represented as a single pole system.

A shared, central voltage loop is proposed to achieve DC bus voltage regulation, as shown in Fig. 5.16. The voltage loop employs a shared voltage compensator that provides a common current reference, $I_{ref,all}$ to all the dc/dc converters. Thus, outside any cell balancing action, the common current reference is shared equally among the module converters. The voltage loop only acts on the inner current loop and the voltage compensator

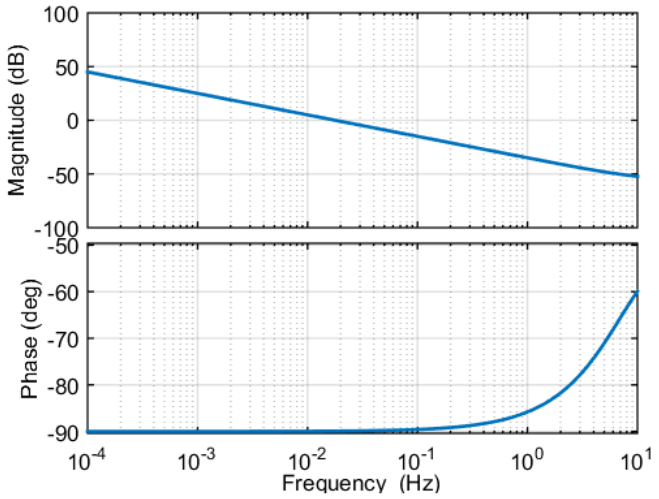


Fig. 5.15: Bode plot showing magnitude and phase of compensated loop gain for the SOC loop in the presence of bus voltage feedback-loop.

can be designed by unit averaging the n dc/dc converters and using standard control loop design. The voltage compensator is embedded inside the central controller and appropriate gains are selected. In the series-output configuration, the total sum of output voltages of individual dc/dc converters and the DC bus impedance determines the total output voltage of the module.

Since the building block dc/dc converters are all designed the same, the converters can be approximated by a single unit averaged converter for the purpose of voltage compensator design. Loop gain for the series output converter is given as,

$$T_v = nH_v G_{vi}(s) \frac{T_i(s)}{1 + T_i(s)} \frac{1}{H_i} G_{cv} \ . \tag{5.46}$$

A standard proportional-integral voltage compensator is designed to achieve a bandwidth of 100 Hz. Analytical predictions show a phase margin of 84.7^o. When series output converters are operated in current regulation mode, the output voltage of any two converters may be mismatched by as much as the full bus voltage, such that a single converter processes the full module power. A key objective of the modular system is to use low-power, low-voltage rating dc/dc converters that do not have to support full HV DC bus voltage and power. However, the shared, central voltage compensator alone does not ensure output voltage

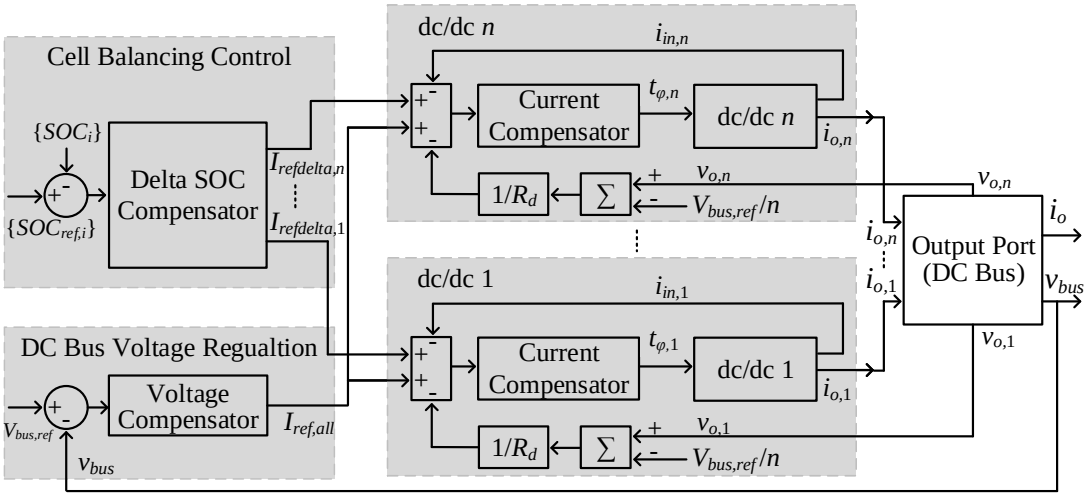


Fig. 5.16: In the partially-distributed control, each dc/dc converter has a well-designed inner current loop to regulate current. An outer voltage loop regulates DC bus voltage and an outer delta SOC loop enforces cell balancing.

sharing among converters in series-output configuration. This is due to the finite tolerance in power stage components and other asymmetries which leads to uneven voltage sharing despite regulating a common output current. In order to achieve desirable output voltage sharing among converters, droop control is employed. The operation mechanism of droop control is to program the output impedance of each dc/dc to achieve voltage sharing among converters, as shown in Fig. 5.17 [108]. The common current reference, $I_{ref,all}$ is modified and an updated current reference, $I_{ref,i}$ is computed using droop control. Each converter regulates its output current to the updated current reference $I_{ref,i}$ which is written as a function of converter output voltage as given below,

$$I_{ref,i} = I_{ref,all} - \frac{v_{o,i}}{R_d} \ . \tag{5.47}$$

where the droop resistance, R_d determines the converter output characteristics.

To realize the active power distribution among dc/dc converters and achieve cell balancing, a delta SOC compensator is introduced, as shown in Fig. 5.16. Similar to the parallel output case, the delta SOC compensator provides individual delta current refer-

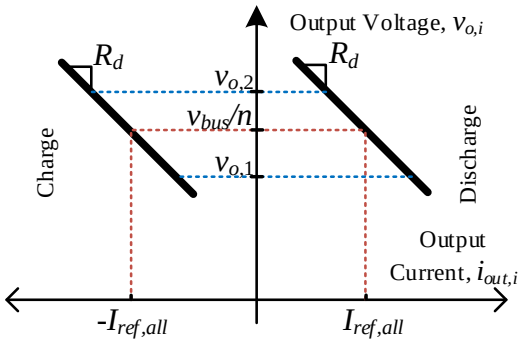


Fig. 5.17: Output characteristics of each dc/dc converter demonstrating droop behavior during battery cell charge and discharge.

ence commands, $I_{ref,delta}$ which produce small variations in the output current of each module. In parallel-output converters, $I_{ref,delta}$ led to different charge or discharge rate for each battery cell allowing SOC regulation. For series-output converters, since the DC bus current is common among all converters due to their series connection, $I_{ref,delta}$ controls the output voltage of each dc/dc by varying the virtual droop current, as shown in Fig. 5.18. This results in different power output for each converter and hence enables cells with different SOC to be charged or discharged at different rates. The value of droop resistance determines voltage variation for a given delta output current and hence it can be selected for a desired output voltage and current range. Furthermore, to decouple the SOC loop from DC bus voltage loop, the delta SOC compensator ensures that the sum of all delta current references is zero. This allows delta SOC compensator to operate independently under saturation limits.

The dc/dc converters are typically designed to operate in bidirectional current mode and limited positive voltage range. Within the current limits, $-I_{max}$ and $+I_{max}$ the delta compensator can achieve active power distribution among parallel-connected converters. The wide range of power, $-I_{max} * V$ to $+I_{max} * V$, allows the delta compensator to achieve faster cell balancing in parallel output configuration. If the sub-module converters are

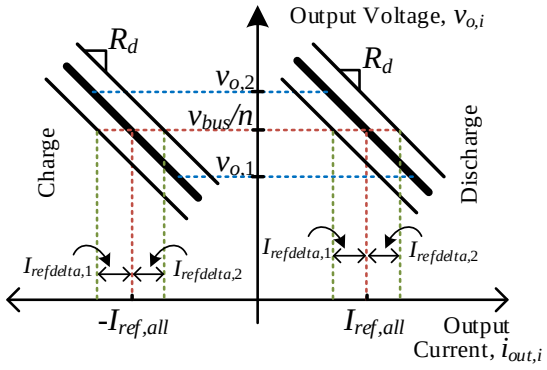


Fig. 5.18: Example behavior of two series-output dc/dc converters demonstrating droop behavior during battery cell charge and discharge.

operated within narrow positive voltage limits, V_{min} to V_{max}, the possible output power variation is limited between $V_{min} * I_o$ and $V_{max} * I_o$. Therefore the speed of cell balancing can be relatively slow for series-connected converters compared to parallel-connected converters. In either case, the balanced operation of battery cells is achievable due to the active balancing capability of dc/dc converters.

5.5 Summary

In this chapter, modeling, design and analysis of control methods is presented for the integrated dc/dc converters used for cell balancing and bus voltage regulation functions in the modular battery system. The parallel and series configurations of integrated dc/dc converters at input and output ports presents opportunities for new control algorithms to be devised. A fully distributed control scheme is developed for the series-input, parallel-output xEV battery system. The control law inside each dc/dc converter is programmed to enable DC bus voltage regulation, and differential power processing to achieve cell balancing functions. Different scenarios with mismatch in series resistance, SOC, or cell capacity are analyzed to validate control behavior. A partially-distributed control approach is developed for the xEV battery system and the micro-grid battery system. It is shown that the par-

tially distributed approach can be used to achieve reliable cell state regulation, cell current protection, and DC bus voltage regulation for both parallel and series output systems.

CHAPTER 6

EXPERIMENTAL RESULTS AND HARDWARE VALIDATION

This chapter presents prototype hardware designs and experimental results to verify the proposed modular battery system architecture, system-level control methods, and system performance. Prototype hardware designs are built for cell-level battery modules consisting of a single cell and a dc/dc power converter. An xEV battery system is built to demonstrate integrated cell balancing and bus voltage regulation using the battery module prototype. The battery system is operated under cell voltage, state of charge, and state of health balancing objective maps and it is shown that the system can achieve balancing functionality with distributed or partially-distributed control implementations. In addition to the cell-level battery module, a cost-optimized battery module that applies active balancing to a substring of cells is built. The battery module is configured to make parallel/series output xEV and microgrid battery systems. Results are shown for robust system operation under state of charge and state of health balancing objective maps.

6.1 Modular xEV Battery System with Cell-level dc/dc Converter

A prototype for a cell-level battery module is built, as shown in Fig. 6.1. The battery

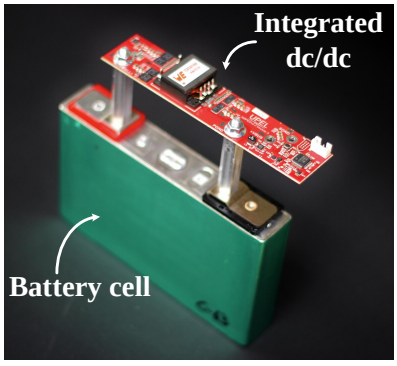


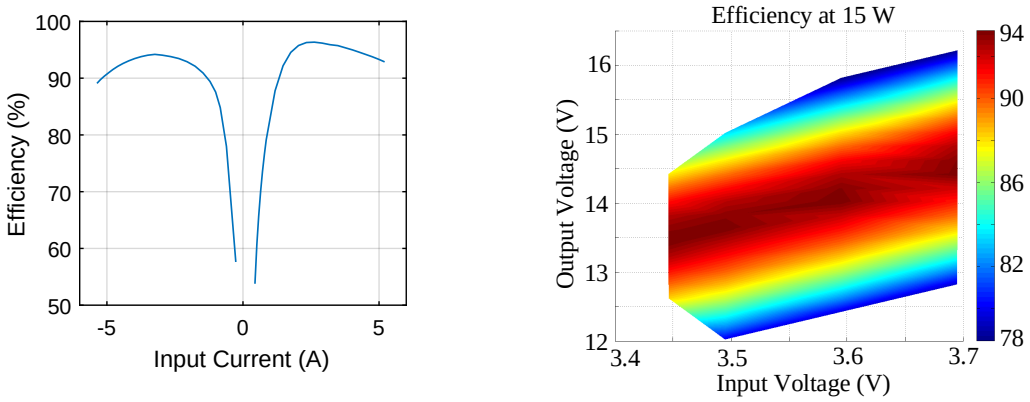
Fig. 6.1: Hardware implementation of a battery module consisting of one Li-ion NMC battery cell and one dual-active bridge dc/dc converter.

Table 6.1: Hardware design parameters for a cell-level dual-active bridge converter prototype

Parameter	**Value**
DAB Input Voltage (V_{in})	2.7-4.3 V
DAB Output Voltage (V_o)	11-17 V
Transformer Turns-ratio (n_t)	1:4
Tank Inductance (L_l)	40 nH
Input Capacitance (C_{in})	198 μF
Output Capacitance (C_{out})	198 μF
Primary DC Blocking Capacitance ($C_{b,p}$)	176 μF
Secondary DC Blocking Capacitance ($C_{b,s}$)	80 μF
Input Series Resistance (R_s)	$\approx$ 2 mΩ
Switching Frequency (f_s)	200 kHz
Maximum Efficiency (η)	93%
Power Rating (P_{rated})	40 W

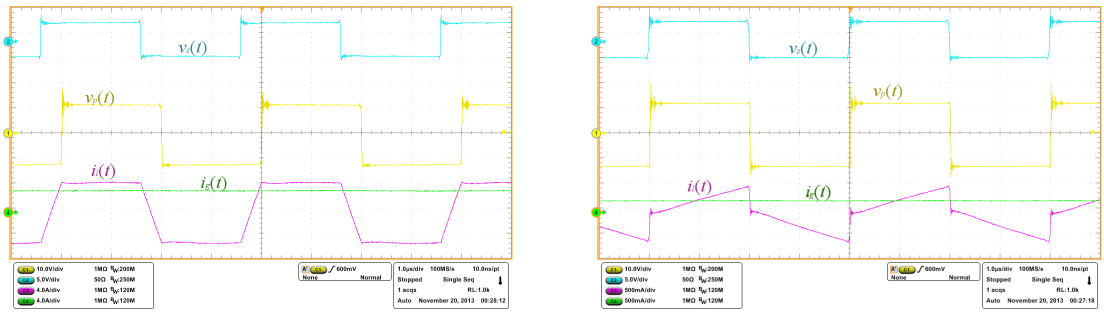
module consists of a single battery cell with a dual-active bridge (DAB) dc/dc converter. The converter parameters and devices are given in Table 6.1. Each DAB dc/dc converter is rated for input currents up to i_{in} = 10 A, resulting in a dc/dc output power of 40 W. The battery module can be configured in parallel/series input and output configurations. The DAB transformer turns ratio n_t is selected to match the desired ratio from battery voltage to nominal bus voltage for xEV application. The dc/dc converter achieves 93% power stage efficiency at nominal 15 W output power, which is comparable to the 92-94% efficiency of the state of the art high step down HV bus to 12 V converters reported in [74, 109]. A detailed efficiency characterization of the dc/dc converter is shown in Fig. 6.2. Savings in volume compared to traditional HV-to-LV dc/dc converters may also be possible as the dc/dc converters can be integrated in the existing space for the connections to the battery cells, as shown in the implementation of Fig. 6.1.

Converter control and modulation are implemented on a Texas Instruments Piccolo microcontroller (TMS320F28027). Phase shift modulation is implemented using internal



(a) (b)

Fig. 6.2: Efficiency of cell-level balancing dc/dc converter, (a) efficiency over varying input current, (b) efficiency map over input and output voltage range at output power of 15 W.



(a) (b)

Fig. 6.3: Experimental open-loop operating waveforms of DAB converter for (a) 12 W and (b) 0 W load power. Ch1: transformer primary voltage, Ch2: transformer secondary voltage, Ch3: primary side transformer current, Ch4: converter input current.

High Resolution Pulse Width Modulation (HRPWM) resources. High resolution capability is supplemental to the conventional Enhanced Pulse Width Modulator (ePWM) modules on the microcontroller. The ePWM modules are clocked from the system clock of 60 MHz and have a maximum resolution of one clock period. The HRPWM extends the time resolution through micro edge positioning to approximately 150 ps, which is the time resolution of the phase shift modulator. The phase shift can be limited in the code for unidirectional power operation with a maximum input current of approximately $i_{in} = 10$ A. Steady-state open-loop waveform are shown in Fig. 6.3 for operation at 3.5-to-12 V,12 W and 0 W output power.

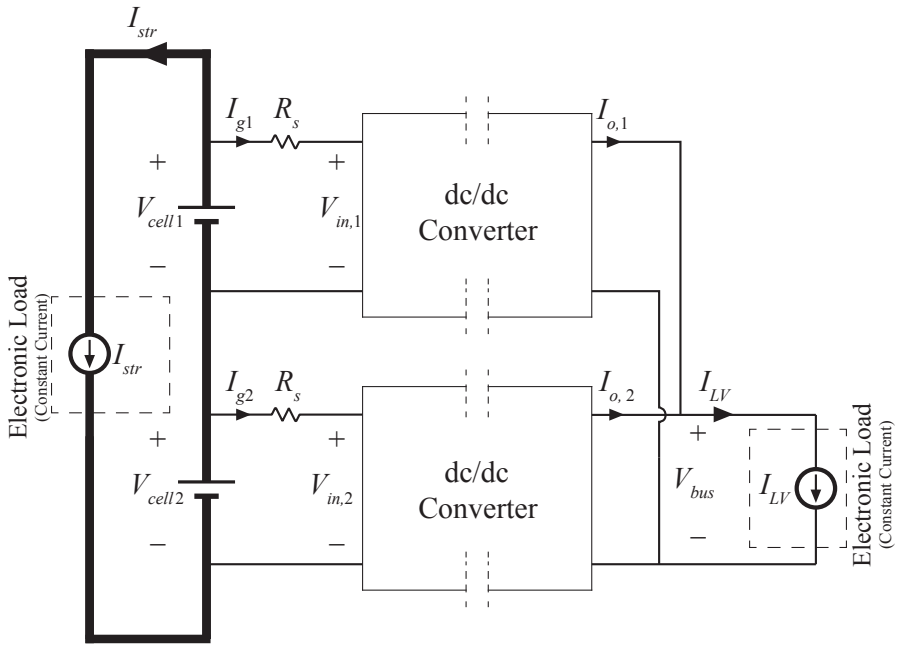


Fig. 6.4: Experimental test setup for evaluating cell balancing and LV load supply operation of the modular xEV battery system. Two battery cells are connected in a series string with one DAB converter in parallel with each battery cell, as proposed in 3.4. External supplies and loads are used to control the currents I_{str} and I_{LV}. Digital multimeters are used to measure $v_{in,1}$, $v_{in,2}$, V_{bus}, and i_{LV}.

6.1.1 Cell Voltage Balancing

For hardware evaluation, the battery module is configured to implement the modular xEV battery system of Fig. 3.4. In this section, experimental results are reported for distributed control implementing the voltage balancing objective map of Fig. 4.4a where each dc/dc converter has the control goal $V_{ref,i} = V_{in,i} = KV_{bus}$. To implement closed feedback loop, the controller was implemented by discretizing the continuous time PI compensator of 5.18 using the Tustin approximation with frequency prewarping centered on $f_c = 100\ Hz$. The implemented controller difference equation is given by

$$t_\varphi[n] = t_\varphi[n-1] + (0.231 \times 10^{-6})\,(v_e[n] - 0.937 v_e[n-1]) \ , \tag{6.1}$$

where v_e is in units of volts and t_φ is in units of seconds, based on the design assumption that $H(s) = 1$ and the phase-shift modulator has unity gain as well. The ADC converters

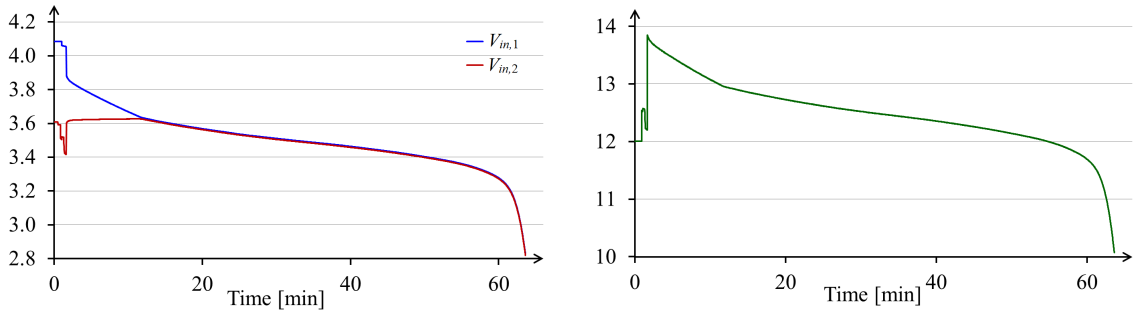
have gains of 1.25 mV per bit and 4.35 mv per bit for input and output voltage respectively.

As a first step, an evaluation system consisting of two battery cells and two DAB dc/dc converters is constructed. To verify balancing functionality, two prototype converters were connected with series input and parallel output as shown in Fig. 6.4. Each converter has one 3.6 Ah NMC cell at its input. The series battery string is connected to a constant current power supply and a constant current electronic load that provide charging and discharging to the full string. The parallel outputs of the converters are connected to the shared LV DC bus, V_{bus}, and to a constant current electronic load.

To demonstrate voltage balancing throughout a full discharge cycle, the two battery cells were initialized with open-circuit voltages of 4.1 V and 3.6 V for Cell 1 and Cell 2, respectively, and the external supplies and loads were set to $I_{str} = 0$ A and $I_{LV} = 1$ A. The resulting convergence over time of cell voltages is shown in 6.5a and bus voltage in 6.5b. Initially, both converters are off, showing their open-circuit voltages. Then, Cell 2 is turned on first, followed by Cell 1. Then, for the first approximately 10 min, the load current is supplied entirely from Cell 1 due to its higher cell voltage while the voltage on Cell 2 remains constant. As the two cell voltages converge, the load current is gradually shared among the two cells as seen by the change in slope of the discharge curves.

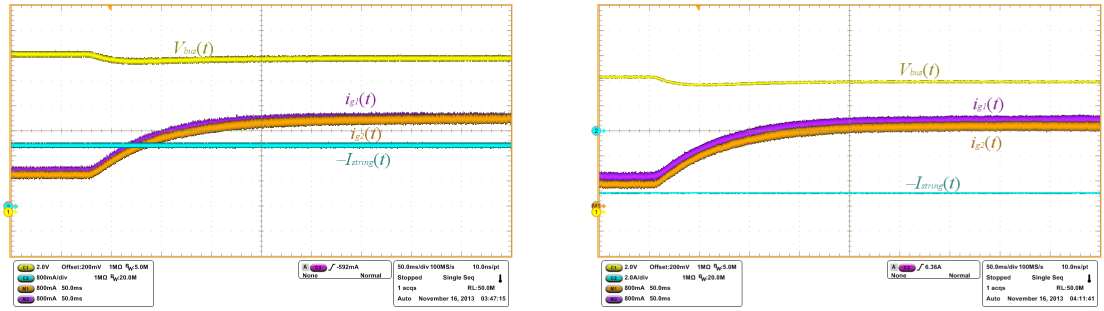
Transient tests were performed to demonstrate the combined ability to maintain cell voltage balancing and track LV load requirements in the presence of step changes in string and load currents. The results for step changes in load current from 0.5 A to 1.5 A are shown in 6.6a for $I_{str} = -2$ A and in 6.6b for $I_{str} = +5$ A. It can be seen that the converter input currents respond similarly to changes in load current independent of total string current. The results for step changes in string current with a constant load current $I_{LV} = 0.5$ A are shown in 6.7a for a step change from 0 A to $I_{str} = -2$ A and in 6.7b for for a step change from 0 A to $I_{str} = +5$ A. In each case, the converter input currents are relatively undisturbed despite the significant changes in charging or discharging string currents.

Next, an evaluation system consisting of twenty one battery cells and twenty one dual-active bridge (DAB) dc/dc bypass converters, as shown in Fig. 6.8, has been constructed.



(a) (b)

Fig. 6.5: Experimental discharge data for a battery string with two series 3.6 Ah NMC cells and DAB converters connected as shown in 6.4. Battery cells are initialized with open-circuit voltages of 4.1 V and 3.6 V for Cell 1 and Cell 2, respectively, and $I_{str} = 0$ A and $I_{LV} = 1$ A. Results are shown for (a) converter input voltages, $v_{in,1}$ and $v_{in,2}$, and (b) V_{bus}.

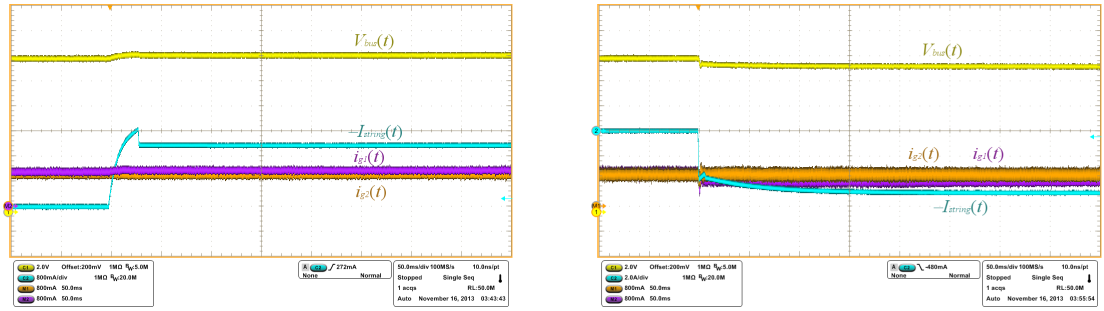


(a) (b)

Fig. 6.6: Experimental results for step changes in load current from $I_{LV} = 0.5$ A to $I_{LV} = 1.5$ A. (a) $I_{str} = -2$ A and (b) $I_{str} = +5$ A. Ch1: V_{bus}, Ch2: $-I_{str}$, M1: $i_{in,1}$, M2: $i_{in,2}$.

The converter parameters and devices are given in Table 6.1. With a dc/dc output power of 40 W, the combined system output power rating is approximately 800 W. The parallel outputs of the converters are connected to the shared bus, Vbus, and to a constant current electronic load.

To verify balancing functionality, twenty-one prototype converters were connected in series at the input and in parallel at the output, as shown in Fig. 6.8. Each converter has one 25 Ah Panasonic Li-Ion NMC cell at its input. The series battery string is connected to a constant current HV power supply and a constant current HV electronic load that provides charging and discharging to the full string. The parallel outputs of the converters are connected to the shared LV DC bus and to a constant current electronic load. To



(a) (b)

Fig. 6.7: Experimental results for step changes in string current with constant $I_{LV} = 0.5$ A. (a) Step from $I_{str} = 0$ A to $I_{str} = -2$ A and (b) step from $I_{str} = 0$ A to $I_{str} = +5$ A . Ch1: V_{bus}, Ch2: $-I_{str}$, M1: $i_{in,1}$, M2: $i_{in,2}$.

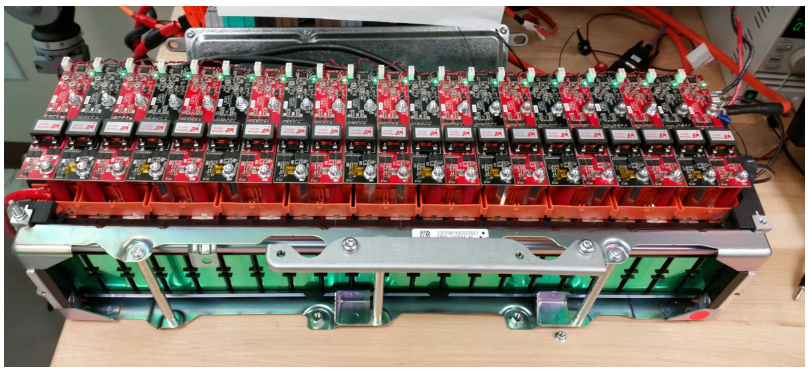


Fig. 6.8: Experimental setup consisting of twenty one Li-ion NMC battery cells and twenty one dual-active bridge dc/dc converters.

demonstrate voltage balancing throughout a full discharge cycle, the battery pack was initialized to an average SOC of 80%, with up to 16% SOC mismatch between the individual cells. External power supplies and the loads were set to sink $I_{str} = 10$ A and $I_{LV} = 25$ A. The results are summarized in Fig. 6.9, where each trace represents the cell terminal voltages and currents as logged by each of the twenty-one dc/dc modules. Observing the converter currents, it becomes clear that at the beginning due to the large initial terminal voltage difference, part of the converters are supplying no current at all, while the others are saturated at the maximum current limit, as shown in Fig. 6.9c. Over time, as the cell voltage mismatch decreases the balancing system brings the cell voltages to the equilibrium state, where all of the cells are discharged at the same rate. At the same time all the dc/dc currents converge to share the LV load evenly. The LV bus voltage as seen by each of the

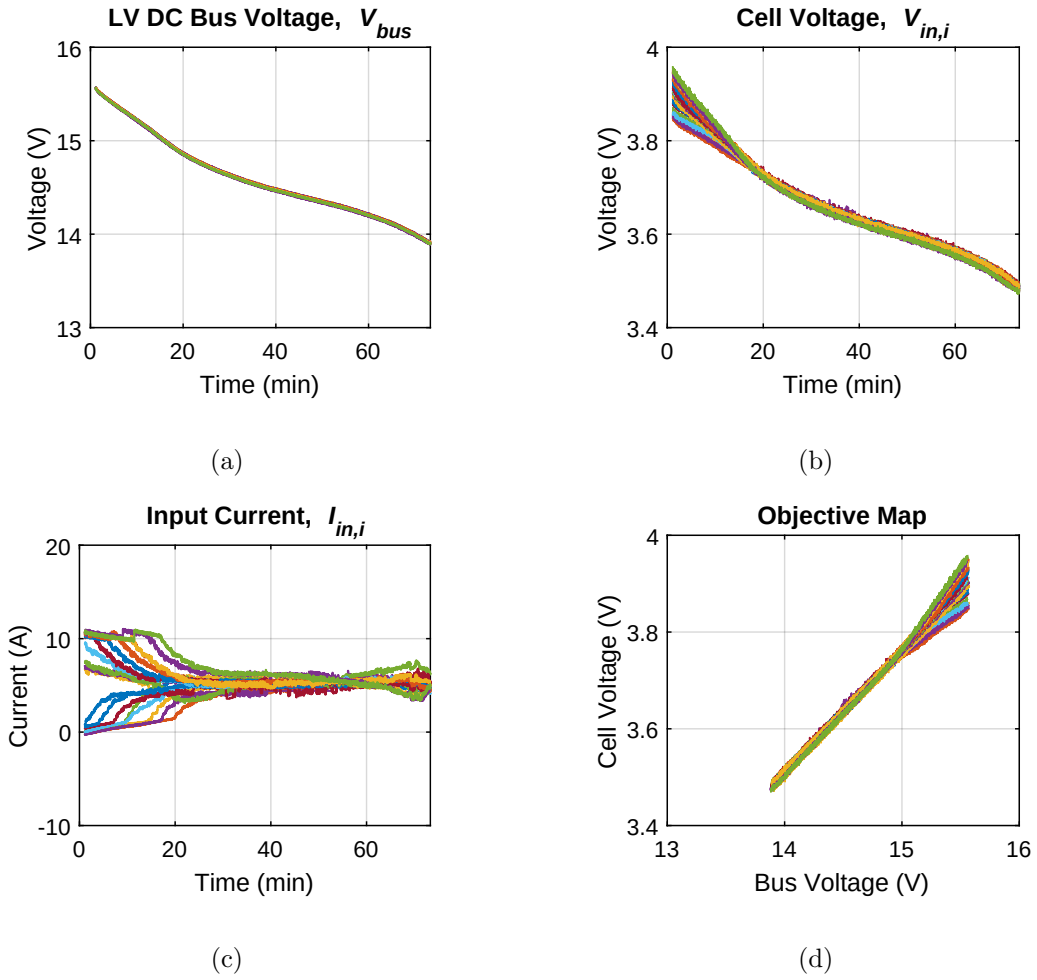


Fig. 6.9: Experimental results for cell voltage balancing: discharge of twenty-one cell battery pack, string current of I_{str} =10 A and LV load of I_{LV} =25 A, (a) LV DC bus voltage, (b) cell voltage, (c) converter input current, and (d) cell voltage balancing objective map. Each trace/color represents a single cell out of twenty one cells.

converters follows the scaled average value of the twenty-one cell pack. Since each of the converters senses the same bus voltage (Fig. 6.9a), the LV bus voltage successfully serves as a common reference for the converters. Each converter enforces the control goal embedded in it and implements the cell voltage balancing objective map, as shown in Fig. 6.9d. It should be noted that the example of Fig. 6.9 presents a proof of system balancing capabilities, in the case when initial SOC mismatches are relatively high. In practical scenarios, with balancing performed continuously, the SOC mismatches remain much smaller.

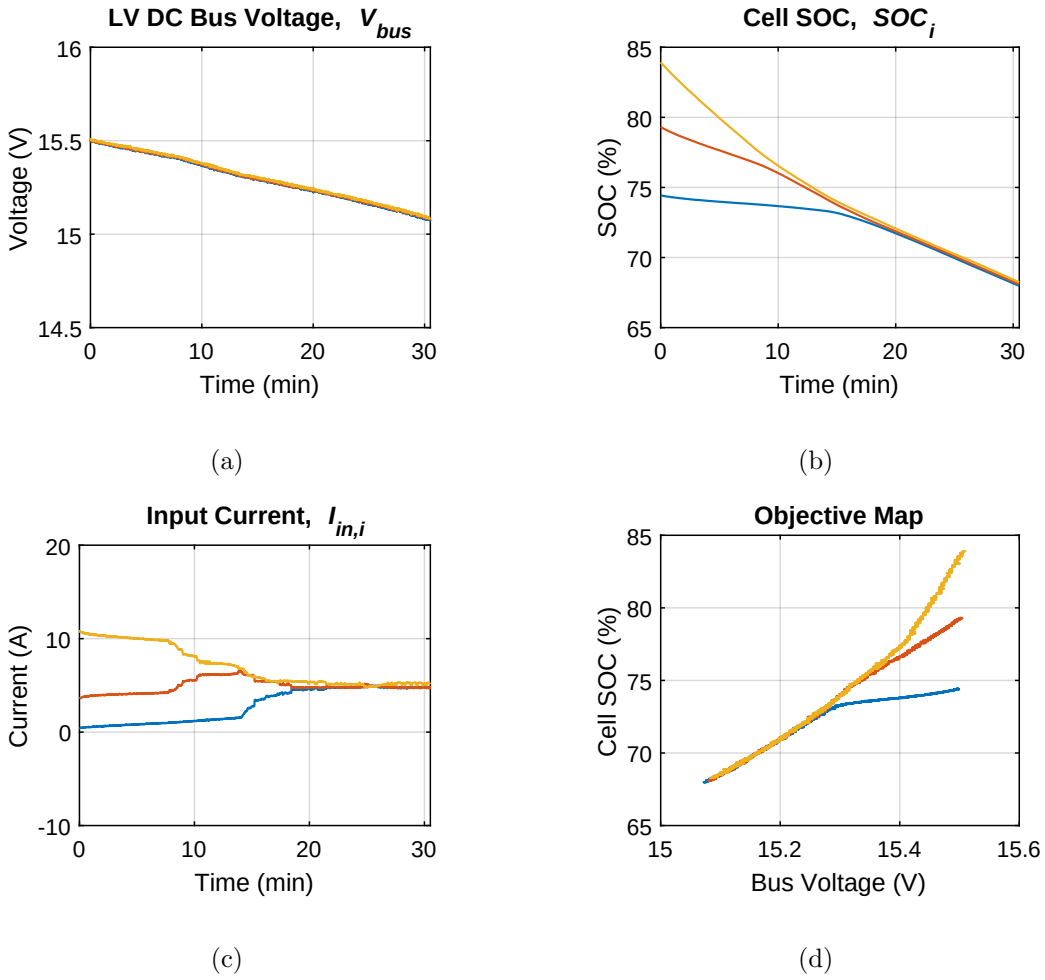


Fig. 6.10: Experimental results for distributed cell SOC balancing system including droop control. Battery cells are initialized with SOC of 84%, 79%, and 74%, battery pack string current is 0 A, and LV bus load is 3 A. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOC balancing objective map.

6.1.2 Cell SOC Balancing

An evaluation system consisting of three battery cells and three dc/dc converters is constructed in hardware. The converters are implemented using the isolated DAB of Fig. 6.1 with parameters of Table 6.1. Three Li-ion NMC 25 Ah battery cells are used. Each dc/dc converter is embedded with the SOC balancing objective map of Fig. 4.4b. To demonstrate stable cell SOC balancing, three cells are initialized with an SOC of 84%, 79%, and 74%, no string current, and LV load of 3 A (constant current), R_{droop} value is selected to be 6.4 mΩ. The system is set to operate in a unidirectional mode to supply the LV bus load.

The experimental results showing convergence of cell SOC over time is shown in Fig. 6.10. As the cell SOCs converge, the load current is gradually shared among the cells. Results demonstrate stable converter currents with no oscillations, which renders the distributed control approach with virtual droop method as a robust stabilizing technique in this case. In addition, the results demonstrate the SOC objective map using bus voltage as a common reference, as shown in Fig. 6.10d.

6.1.3 Cell SOH Balancing

A laboratory prototype comprised of a series string of twenty-one 25 Ah Li-ion NMC battery cells and the twenty-one DAB is used, as shown in Fig. 6.8. The twenty-one series-connected NMC battery cells form a 2 kWh battery pack with HV bus voltage approximately equal to 80 V. To demonstrate balancing functionality, the HV bus is connected to an EV drive-train simulator implemented using programmable power supply capable of charging and discharging the pack at high currents. The LV bus is connected to a constant-power load.

Life-extension control based on the SOH objective map of Fig. 4.12b through a full charge cycle is tested under three different conditions. The SOH objective map is programmed with a low, medium, and high life-gain, with a greater delta high SOC mismatch as the gain increases. The balancing system was set to run life extension objective map based on bus voltage as common reference signal, as described by Fig. 4.12b. With this map, the SOC of each cell is limited at top-end of charging according to cell capacity and programmed life gain, while at the bottom end the SOC is biased by cell series resistance. A mismatch in capacity was coded into the system to demonstrate the unique SOC limits of individual cells.

In the low life-gain experiment, the battery cells were initialized with an SOC of 25%, the string current was set to be 15 A, and the LV bus load was set to be 350 W. The resulting map between bus voltage (common reference) and individual cell SOC is shown in Fig. 6.11d. The cell SOC, converter input current, and shared bus voltage over the course of experiment are also shown in Fig. 6.11. Initially, all converters share load current

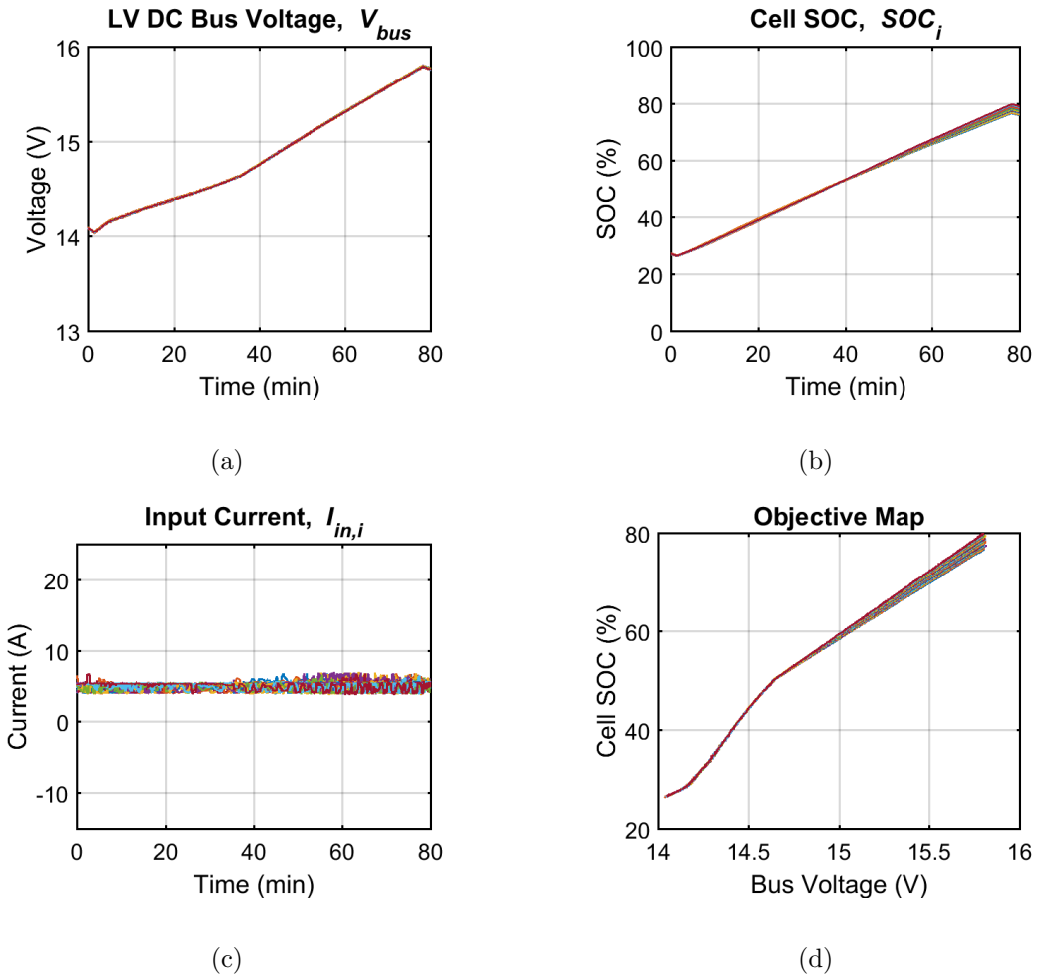


Fig. 6.11: Experimental results for cell SOH balancing under a low life gain objective map. Battery cells are charged at a constant string current of 0.6C (15 A), and LV bus load is set to 350 W. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOH balancing objective map with low life gain.

with small differences needed to keep individual cell SOC on the objective map. Around 50% SOC mark, the converters demonstrate differential load sharing to achieve different SOC_{max} points at the top-end of charge. Since a low life gain objective is used, the dc/dc converter have to process a small amount of differential current to achieve the target SOC for individual cells, as shown in Fig. 6.11c. The delta SOC at top-end is close to 7% just as programmed.

In the medium life-gain experiment, the battery cells were initialized with an SOC of 15%, the string current was set to be 25 A, and the LV bus load was set to be 350 W. The

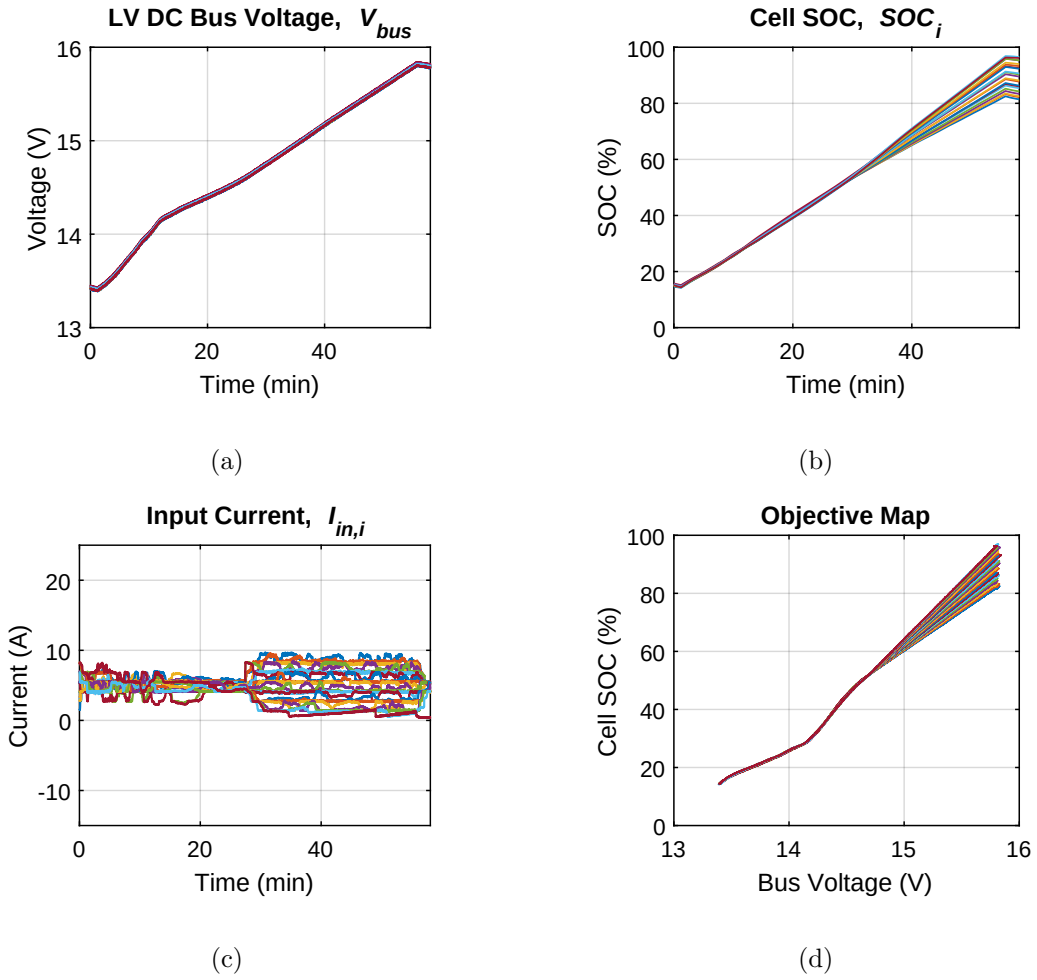


Fig. 6.12: Experimental results for cell SOH balancing under a medium life gain objective map. Battery cells are charged at a constant string current of 1C (25 A), and LV bus load is set to 350 W. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOH balancing objective map with medium life gain.

resulting map between bus voltage (common reference) and individual cell SOC is shown in Fig. 6.12d. The cell SOC, converter input current, and shared bus voltage over the course of experiment are also shown in Fig. 6.12. Initially, all converters share load current with small differences needed to keep individual cell SOC on the objective map. Around 50% SOC mark, the converters demonstrate differential load sharing to achieve different SOC_{max} points at the top-end of charge. With a medium life gain objective being used, the dc/dc converter are pushed harder to process differential amounts of current and achieve the target SOC for individual cells, as shown in Fig. 6.12c. The delta SOC at top-end is

close to 15% just as programmed.

In the high life-gain experiment, the battery cells were initialized with an SOC of 35%, the string current was set to be 25 A, and the LV bus load was set to be 350 W. The resulting map between bus voltage (common reference) and individual cell SOC is shown in Fig. 6.13d. The cell SOC, converter input current, and shared bus voltage over the course of experiment are also shown in Fig. 6.13. Initially, all converters share load current with small differences needed to keep individual cell SOC on the objective map. Around 50% SOC mark, the converters demonstrate differential load sharing to achieve different SOC_{max} points at the top-end of charge. With a high life gain objective being used, the dc/dc converter are pushed to their saturation limits to process differential amounts of current and achieve the target SOC for individual cells, as shown in Fig. 6.13c. The delta SOC at top-end is close to 20% just as programmed.

Lastly, the life-extension control based on the SOH objective map of Fig. 4.12b is tested through a full discharge cycle. The SOH objective map is programmed with a low life-gain. With this map, the SOC of each cell is limited at top-end of charging according to cell capacity and programmed life gain, while at the bottom end the SOC is biased by cell series resistance. In the battery pack discharge experiment, the battery cells were initialized with an SOC of 85%, the string current was set to be based on a dynamic vehicle drive cycle profile called US06, and the LV bus load was set to be 350 W. The US06 drive cycle is an aggressive load profile with peak currents greater than 5C (100 A) and regenerative currents up to 4C (100 A). This experiment demonstrates system operation under a practical vehicle driving scenario. The results validate the life objective map between bus voltage (common reference) and individual cell SOC is shown in Fig. 6.14d. The cell SOC, converter input current, and shared bus voltage over the course of experiment are also shown in Fig. 6.14. Due to the aggressive load profile, the dc/dc converter process differential amounts of current throughout the load cycle and achieve the target SOC for individual cells, as shown in Fig. 6.14c.

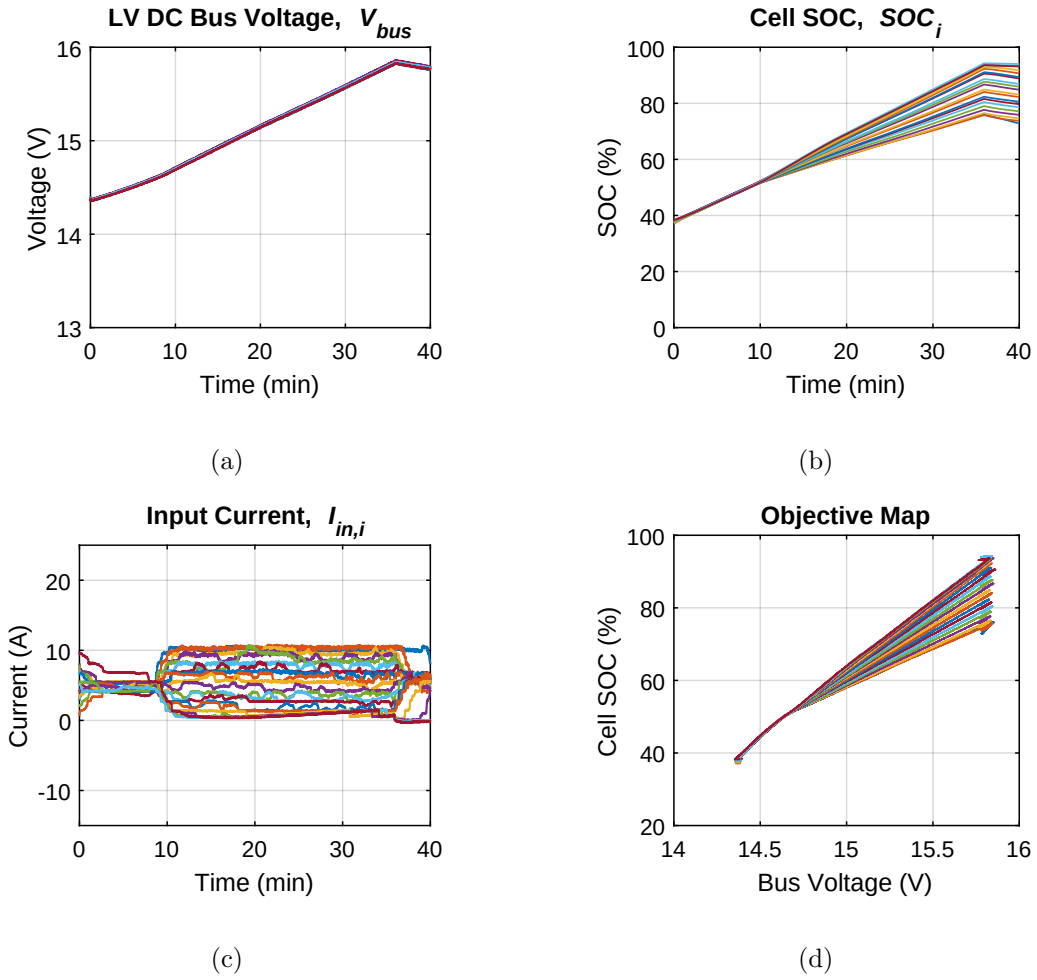


Fig. 6.13: Experimental results for cell SOH balancing under a high life gain objective map. Battery cells are charged at a constant string current of 1C (25 A), and LV bus load is set to 350 W. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOH balancing objective map with high life gain.

6.2 Modular xEV Battery System with Substring-level dc/dc Converter

In the previous section, experimental results validated active voltage, SOC, and SOH balancing capability using cell-level battery modules. In this section, design and experimental results of a cost-optimized substring level dc/dc converter are presented. The substring module, first described in Chapter 3 (Fig. 3.7), has a group of series-connected cells at its input port and performs active cell SOC or SOH balancing for the group of cells and passive balancing within the group of cells.

A prototype for substring-level battery module is built, as shown in Fig. 6.15. The

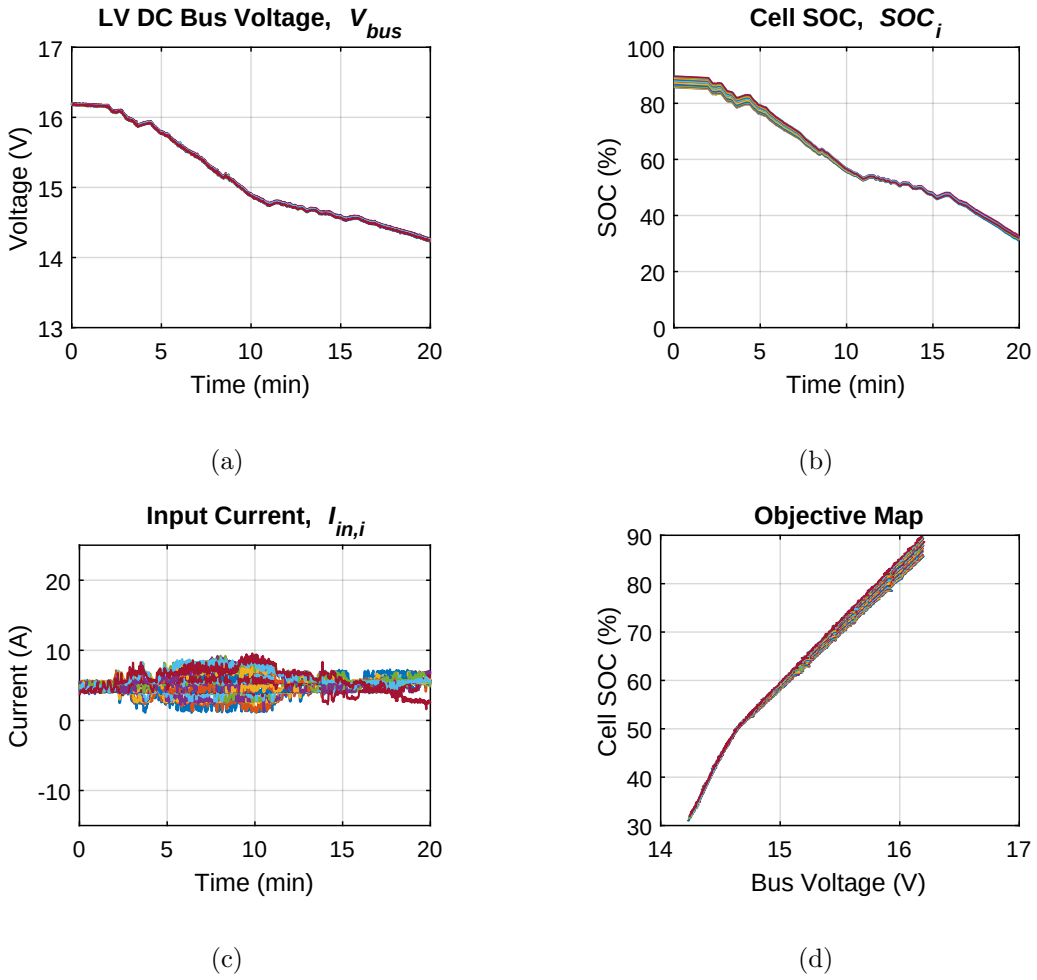


Fig. 6.14: Experimental results for cell SOH balancing under a high life gain objective map. Battery cells are discharging under a dynamic drive profile (US06) with an average discharge rate of 2.5C (62 A), and LV bus load is set to 350 W. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOH balancing objective map with high life gain.

battery module consists of six series-connected battery cells, a dual-active bridge (DAB) dc/dc converter, and a custom passive balancing solution using a commercial chip. The converter parameters and devices are given in Table 6.2. Each DAB dc/dc converter is rated for input currents up to $i_{in} = 25$ A, resulting in a dc/dc output power of 480 W. The battery module can be configured in parallel/series input and output configurations. The DAB transformer turns ratio n_t is selected to match the desired ratio from battery voltage to nominal bus voltage for xEV and microgrid applications. The transformer configuration

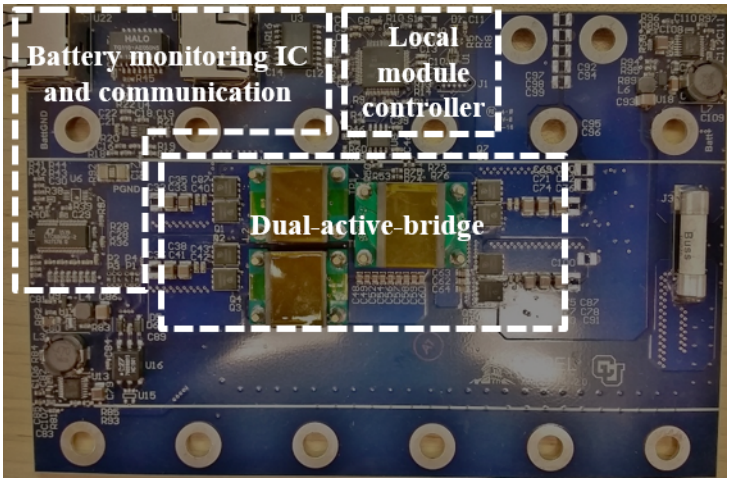


Fig. 6.15: Hardware implementation of a substring-level battery module consisting of six series-connected battery cell and one dual-active bridge dc/dc converter.

can be chosen to achieve 14 V or 28 V output voltage. This allows validatation of control methods at different voltage levels for both xEV and microgrid battery system. The dc/dc converter achieves 95.5% power stage efficiency at nominal 150 W output power, which is better than the 92-94% efficiency of the state of the art high step down HV bus to 12 V converters reported in [74, 109]. A detailed efficiency characterization of the dc/dc converter is shown in Fig. 6.16. Similar to the cell-level design, savings in volume compared to traditional HV-to-LV dc/dc converters are also possible for the substring dc/dc converter as it can be integrated in the existing space around the battery cells.

Converter control and modulation are implemented on a Texas Instruments Piccolo microcontroller (TMS320F28035). Phase shift modulation is implemented using internal High Resolution Pulse Width Modulation (HRPWM) resources. High resolution capability is supplemental to the conventional Enhanced Pulse Width Modulator (ePWM) modules on the microcontroller. The ePWM modules are clocked from the system clock of 60 MHz and have a maximum resolution of one clock period. The HRPWM extends the time resolution through micro edge positioning to approximately 150 ps, which is the time resolution of the phase shift modulator. The phase shift can be limited in the code for unidirectional or bidirectional power operation. Steady-state open-loop waveform are shown in Fig. 6.17 for operation at 18-to-27 V, 67 W and 145 W output power.

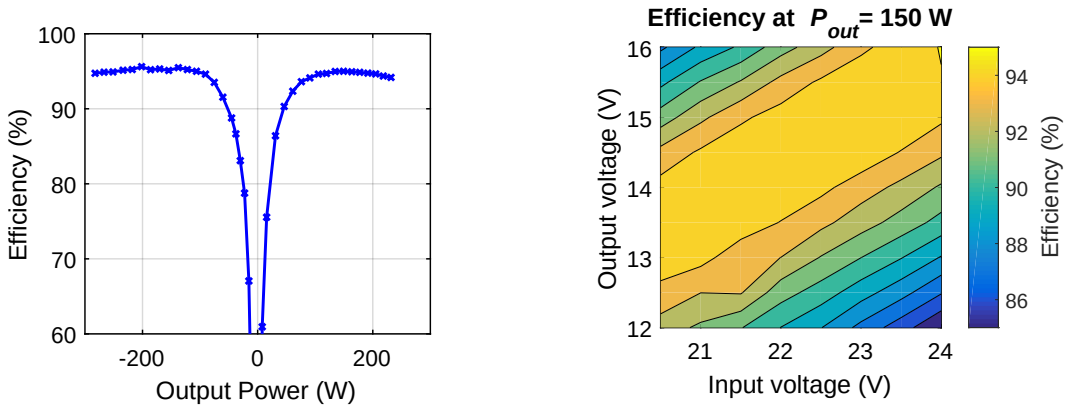
Table 6.2: Hardware design parameters for a substring-level dual-active bridge converter prototype.

Parameter	**Value**
DAB Input Voltage (V_{in})	16-26 V
DAB Output Voltage (V_o)	27-37 V
Transformer Turns-ratio (n_t)	2:3
Tank Inductance (L_l)	265 nH
Input Capacitance (C_{in})	40 μF
Output Capacitance (C_{out})	60 μF
Primary DC Blocking Capacitance ($C_{b,p}$)	90 μF
Secondary DC Blocking Capacitance ($C_{b,s}$)	60 μF
Input Series Resistance (R_s)	$\approx$ 8 mΩ
Switching Frequency (f_s)	200 kHz
Maximum Efficiency (η)	95%
Power Rating (P_{rated})	480 W

6.2.1 Cell SOC Balancing

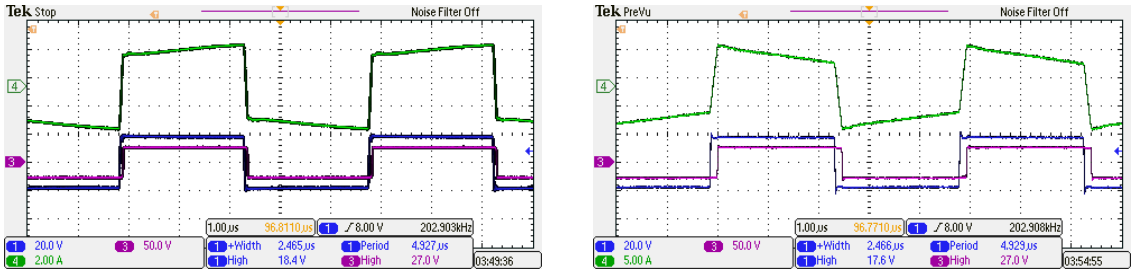
An evaluation system consisting of three substring-level battery modules, eighteen battery cells and three dc/dc converters is constructed in hardware, as shown in Fig. 6.18. Li-ion NMC 25 Ah battery cells are used. For this evaluation system, the partially distributed control approach of Fig. 4.9 is employed using a central BMS controller. Furthermore, the objective map is programmed to use average SOC as the common reference, similar to shown in Fig. 4.8.

To demonstrate cell SOC balancing throughout a full charge cycle, three dc/dc converters were operated with three battery cell substrings, initialized with SOC of 27%, 23%, and 18%. The pack string current I_{str} was set to 15 A in charging mode and the DC bus load was set in current sink mode at 10 A. The system was programmed to do traditional SOC balancing using the objective, $SOC_{ref} = SOC_{avg} = \frac{SOC_1+SOC_2+SOC_3}{3}$. The bus voltage was set to be proportional to the average SOC of the Li-ion battery pack by setting the voltage set-point as $v_{bus} = KSOC_{avg} + c$. The resulting convergence in SOC over time, the



(a) (b)

Fig. 6.16: Efficiency of substring-level balancing dc/dc converter, (a) efficiency over varying output power, (b) efficiency map over input and output voltage range at output power of 150 W.



(a) (b)

Fig. 6.17: Experimental open-loop operating waveforms of substring-level DAB dc/dc converter for (a) 67 W and (b) 145 W load power. Ch1: transformer primary voltage (blue), Ch3: transformer secondary voltage (pink), Ch4: inductor current (green).

converter input currents and bus voltage are shown in Fig. 6.19. Initially all dc/dc converters split the loads differentially based on their SOC differences. The cell with higher SOC provides more current to the bus load and the cell with lower SOC provides less current to the bus load. As the substring SOCs converge over time, the load current is gradually shared among the dc/dc modules. In addition, the results validate the SOC objective map using average SOC as a common reference, as shown in Fig. 6.19d.

Next, the cell SOC balancing experiments were repeated to demonstrate partially-distributed control regulating DC bus voltage to a fixed reference during a discharge cycle. Three dc/dc converters were operated with three battery cell substrings, initialized with

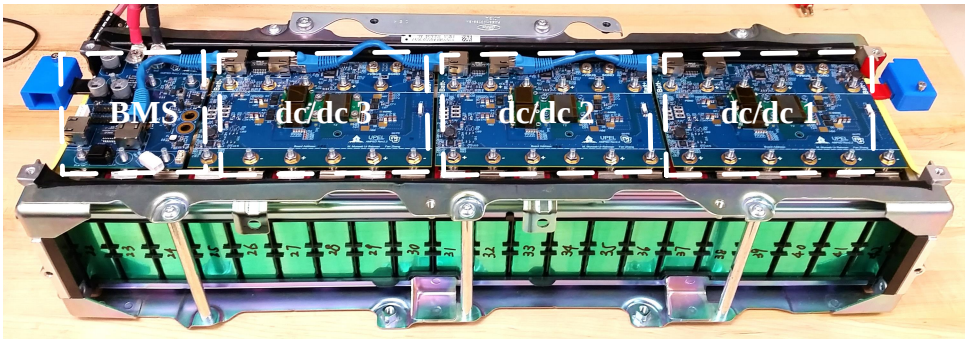


Fig. 6.18: Experimental setup consisting of eighteen Li-ion NMC battery cells and three substring-level dual-active bridge dc/dc converters.

SOC of 82%, 86%, and 90%. The pack string current I_{str} was set to 8 A in discharging mode and the LV load was set in current sink mode at 10 A. The system was programmed to do traditional SOC balancing using the objective, $SOC_{ref} = SOC_{avg} = \frac{SOC_1+SOC_2+SOC_3}{3}$. The bus voltage was set to a fixed voltage set-point as $v_{bus} = 34$ V. The resulting convergence in SOC over time, the converter input currents and bus voltage are shown in Fig. 6.20. Initially all dc/dc converters split the loads differentially based on their SOC differences. The cell with higher SOC provides more current to the bus load and the cell with lower SOC provides less current to the bus load. As the substring SOCs converge over time, the load current is gradually shared among the dc/dc modules. In addition, the DC bus voltage is kept fixed during the discharge cycle, as shown in Fig. 6.20a. The results also validate the SOC objective map using average SOC as a common reference, as shown in Fig. 6.20d.

A similar experiment was repeated to demonstrate partially-distributed control regulating DC bus voltage to a fixed reference during a charge cycle. The battery cells are initialized with equal SOC, the pack string current I_{str} was set to 15 A in charging mode and the LV load was set in current sink mode at 10 A. The bus voltage was set to a fixed voltage set-point as $v_{bus} = 34$ V. The resulting convergence in SOC over time, the converter input currents and bus voltage are shown in Fig. 6.21. The results validate cell balancing and bus voltage regulation.

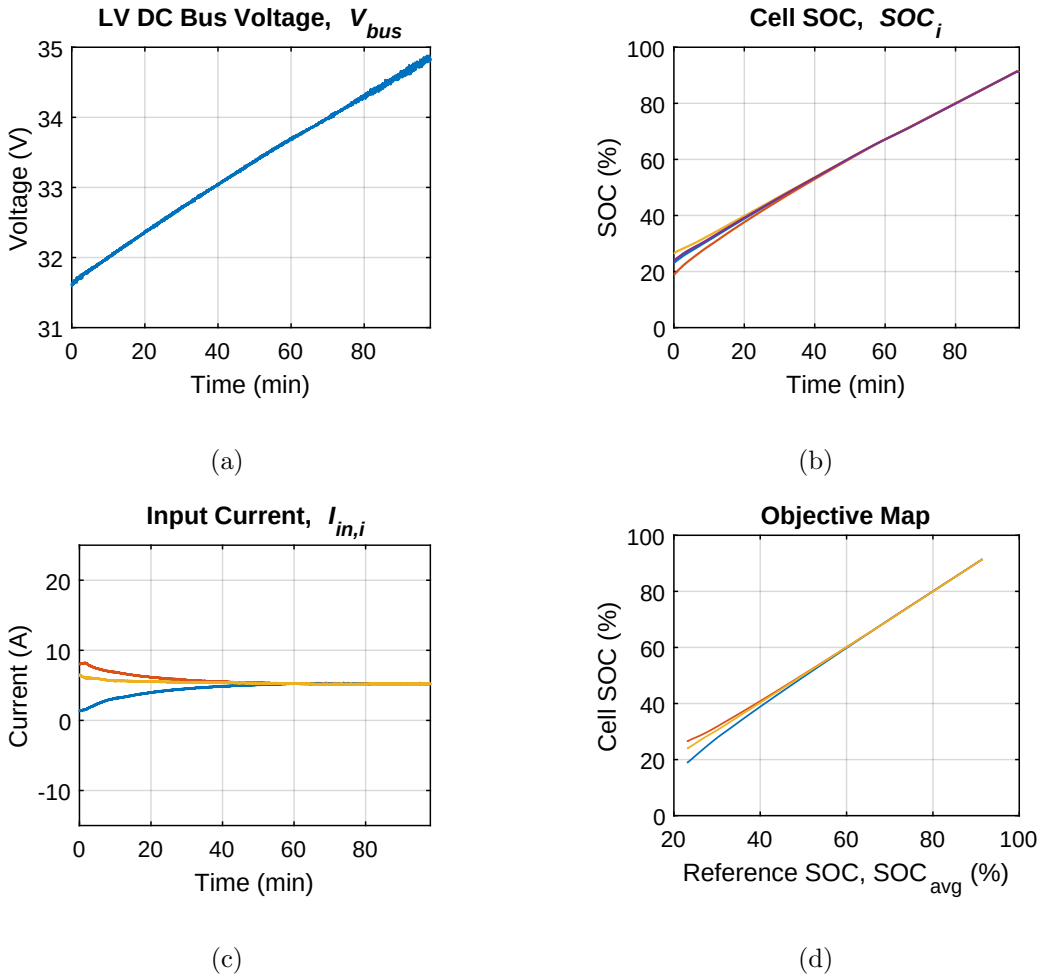


Fig. 6.19: Experimental results for cell SOC balancing system using the partially distributed control approach. Battery cells are initialized with SOC of 27%, 23%, and 18%, battery pack string current is -15 A, and LV bus load is 10 A. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOC balancing objective map.

6.2.2 Cell SOH Balancing

Life-extension control based on the SOH objective map of Fig. 4.12b was tested under full charge and discharge cycles. The SOH objective map is programmed with a medium life-gain. The balancing system was set to run life extension objective map based on partially distributed control. With this map, the SOC of each cell is limited at top-end of charging according to cell capacity and programmed life gain, while at the bottom end the SOC is biased by cell series resistance.

In the charging cycle experiment, the battery cells were initialized with an SOC of

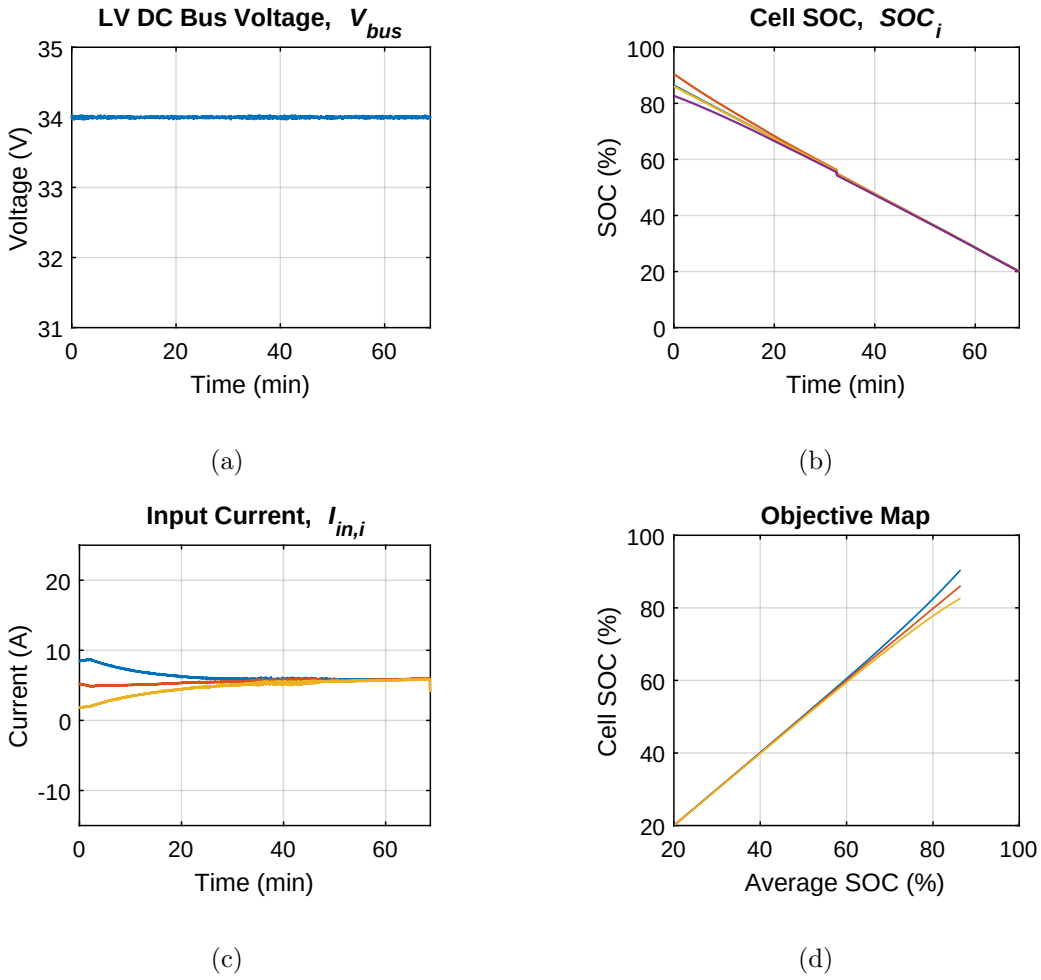


Fig. 6.20: Experimental results for cell SOC balancing system using the partially distributed control approach. Battery cells are initialized with SOC of 82%, 86%, and 90%, battery pack string current is +8 A, and LV bus load is 10 A. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOC balancing objective map.

25%, the string current was set to be 25 A, and the LV bus load was set to be 10 A. The resulting map between bus voltage (common reference) and individual cell SOC is shown in Fig. 6.22d. The cell SOC, converter input current, and shared bus voltage over the course of experiment are also shown in Fig. 6.22. All converters share load current differentially to keep individual cell SOC on the objective map. With a medium life gain objective being used, the dc/dc converter are pushed harder to process differential amounts of current and achieve the target SOC for individual cells, as shown in Fig. 6.22c. The delta SOC at top-end is close to 12% just as programmed.

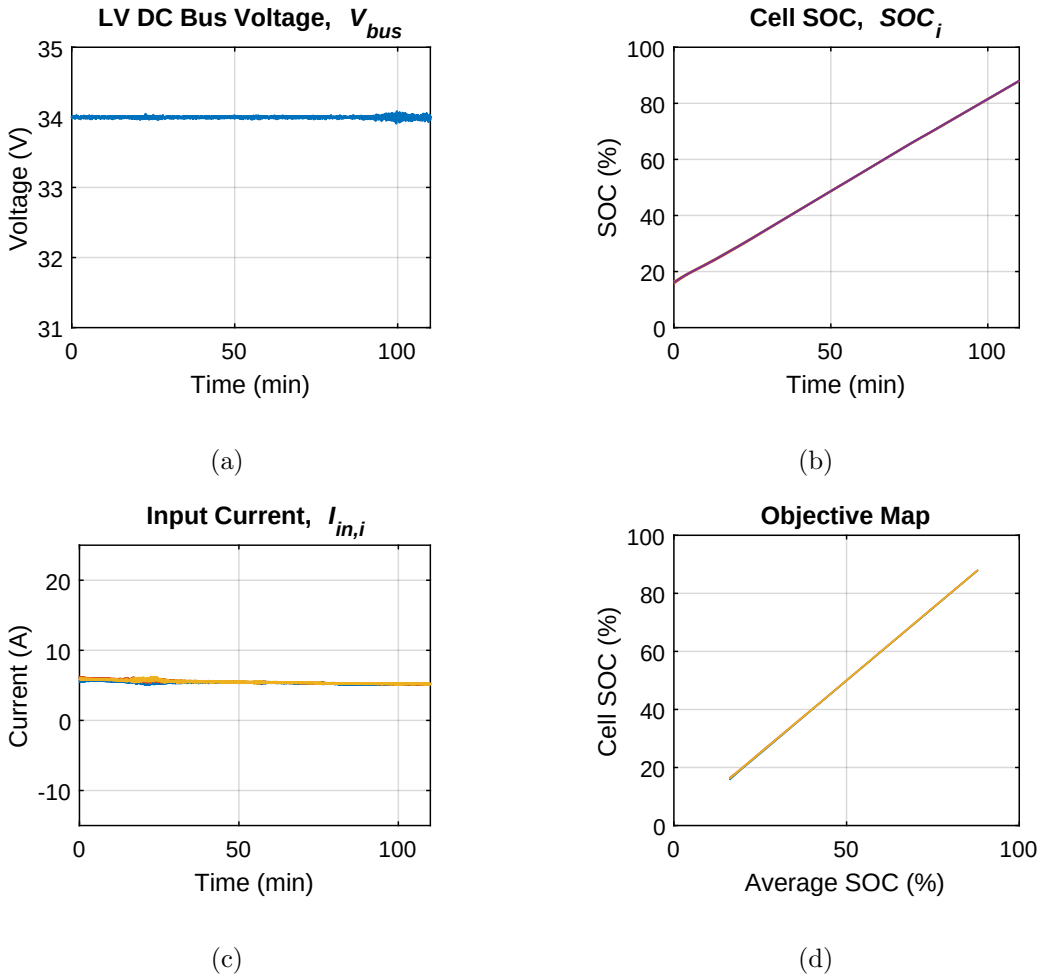


Fig. 6.21: Experimental results for cell SOC balancing system using the partially distributed control approach. Battery cells are initialized with equal SOC, battery pack string current is -15 A, and LV bus load is 10 A. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOC balancing objective map.

In the discharging cycle experiment, the battery cells were initialized with an SOC of 85%, the string current was set by a dynamic vehicle drivecycle (US06), and the LV bus load was set to be 10 A. The resulting map between bus voltage (common reference) and individual cell SOC is shown in Fig. 6.23d. The cell SOC, converter input current, and shared bus voltage over the course of experiment are also shown in Fig. 6.23. All converters share load current differentially to keep individual cell SOC on the objective map. With a medium life gain objective being used and an aggressive load profile, the dc/dc converter are pushed harder to process differential amounts of current and achieve the target SOC

for individual cells, as shown in Fig. 6.23c. The delta SOC at top-end is close to 12% just as programmed.

6.3 Modular Microgrid Battery System

In this section, results are presented for parallel/series output battery modules. The dc/dc converter of Fig. 6.15 is used with parameters listed in Table 6.2.

6.3.1 Parallel/Series Output dc/dc Converters

An evaluation system consisting of two substring-level battery modules, twelve battery cells and two dc/dc converters is constructed. The battery modules are configured to independent-input, and parallel or series output. For this system, the partially distributed control approach of Fig. 5.16 is employed using a central BMS controller. Furthermore, the objective map is programmed to use average SOC as the common reference, similar to shown in Fig. 4.8.

In the independent-input, parallel-output configuration, the battery cells were initialized with an SOC of 84% and 76%, and the LV bus load was set to be 270 W. The dc/dc converter are programmed to regulate bus voltage proportional to average SOC and the objective map is defined to be SOC balancing. The resulting map between bus voltage (common reference) and individual cell SOC is shown in Fig. 6.24d. The cell SOC, converter input current, and shared bus voltage over the course of experiment are also shown in Fig. 6.24. Initially the cell substring with higher SOC provides more current to the bus load and the substring with lower SOC provides less current to the bus load. As the substring SOCs converge over time, the load current is gradually shared among the dc/dc modules.

Next, the dc/dc converters are configured to be in series-output configuration. In this experiment, the battery cells were initialized with an SOC of 70% and 65%, and the LV bus load was set to be 330 W. The dc/dc converter are programmed to regulate bus voltage proportional to average SOC and the objective map is defined to be SOC balancing. The resulting map between bus voltage (common reference) and individual cell SOC is shown in Fig. 6.25d. The cell SOC, converter input current, and shared bus voltage over the course of

experiment are also shown in Fig. 6.25. Initially the cell substring with higher SOC provides more power to the bus load and the substring with lower SOC provides less power to the bus load. As the substring SOCs converge over time, the load power is gradually shared among the dc/dc modules. With the series-output, the differential power is achieved via difference in output voltage that reflects as different currents on the input side, as shown in Fig. 6.25c.

6.3.2 Multiple Battery Packs on A Shared DC Bus

The battery modules were also designed to demonstrate plug-and-play operation for a mixed-chemistry battery system for DC microgrid application, as shown in Fig. 6.26. The key objective was to demonstrate that modules with different battery chemistry, and varying energy and power capability can be connected to a common DC bus and supply loads in a microgrid. In this common DC bus system, the battery modules will differentially process power based on their relative capacity. The microgrid application presents a system which is different from electric vehicle application in a variety of ways. In contrast to the electric vehicle system, the modular microgrid system does not need a high-voltage series-string of battery cells and there is no string current through the cells. In this system, the dc/dc converters process the full power of the battery cells. The modules use shared DC bus to communicate SOC information and relative capacity. The battery modules are designed to reconfigurable such that the system can achieve multiple DC bus voltage using the same dc/dc converters. This is done by reconfiguring the dc/dc converter outputs to be parallel or series.

A hardware setup is built for the plug-and-play mixed chemistry system. The hardware setup includes three battery modules i. Module 1 contains three dc/dc converters, each connected to six NMC prismatic cells at its input, ii. Module 2 contains one dc/dc converter, connected to six NMC/LMO pouch cells at its input, and iii. Module 3 contains one dc/dc converter, connected to six NMC/LMO pouch cells at its input. The hardware system is shown in Fig. 6.26. The setup was tested under various charging and discharging scenarios. The setup includes the battery modules connected in parallel at the output DC bus. The

DC bus is also connected to an electronic load and a voltage supply that emulates solar PV behavior, as shown in Fig. 6.26. The battery modules run using the bidirectional map of Table 4. Module average SOC, 0% to 100% is mapped to DC bus voltage, 12 V to 16 V.

The plug-and-play system, shown in Fig. 6.26, was tested under various transient and stead-state scenarios. Some of the key load transient response results are shown in Fig. 6.27. Fig. 6.27a shows a transient from no load condition to a 17 A constant current load condition. The battery modules respond well to regulate the DC bus voltage to its target value, 15 V. The response time is about 20 ms. Fig. 6.27b shows the transient response to a change in load from 15 A to 1 A. The DC bus voltage is well regulated during the transient experiment. Fig. 6.27c and Fig. 6.27c demonstrate load transients in the charging scenarios. The response of the system to a load transient of -2 A to -17 A is captured in Fig. 6.27c. Fig. 6.27d shows transient response to a change in charging current from -17 A to -2 A. In all scenarios, the results show correct current sharing and a well damped response with good voltage regulation characteristics.

The plug-and-play mixed chemistry system is designed to share load according to their relative capacities and keep the average SOC of battery packs equal. Each battery pack can run life objective map for the cells inside the pack. The evaluation system ran tests under charging and discharging scenarios to verify the system behavior. Results demonstrating battery module operation while supplying DC bus loads are shown in Fig. 6.28. In this experiment, the battery packs are initialized with different SOC. The DC bus is connected to a 17 A constant current load. The battery modules initially share currents to bring their average SOC together. As these modules come closer to equal SOC, they share currents according to their relative capacities.

6.4 Summary

Detailed experimental results and hardware design validation is provided in this chapter. The modular xEV battery system is demonstrated using cell-level and substring-level dc/dc converter prototypes. The system is experimentally verified for different size of battery packs. In addition, the objective maps for cell voltage, SOC, and SOH are demonstrated

using the distributed control approach. The system operation is also verified for partially distributed control approach. The microgrid battery system is also demonstrated using parallel/series-output dc/dc converter modules. The distributed control approach is verified for the shared DC bus system consisting of multiple battery packs, solar PV, and loads on the DC bus.

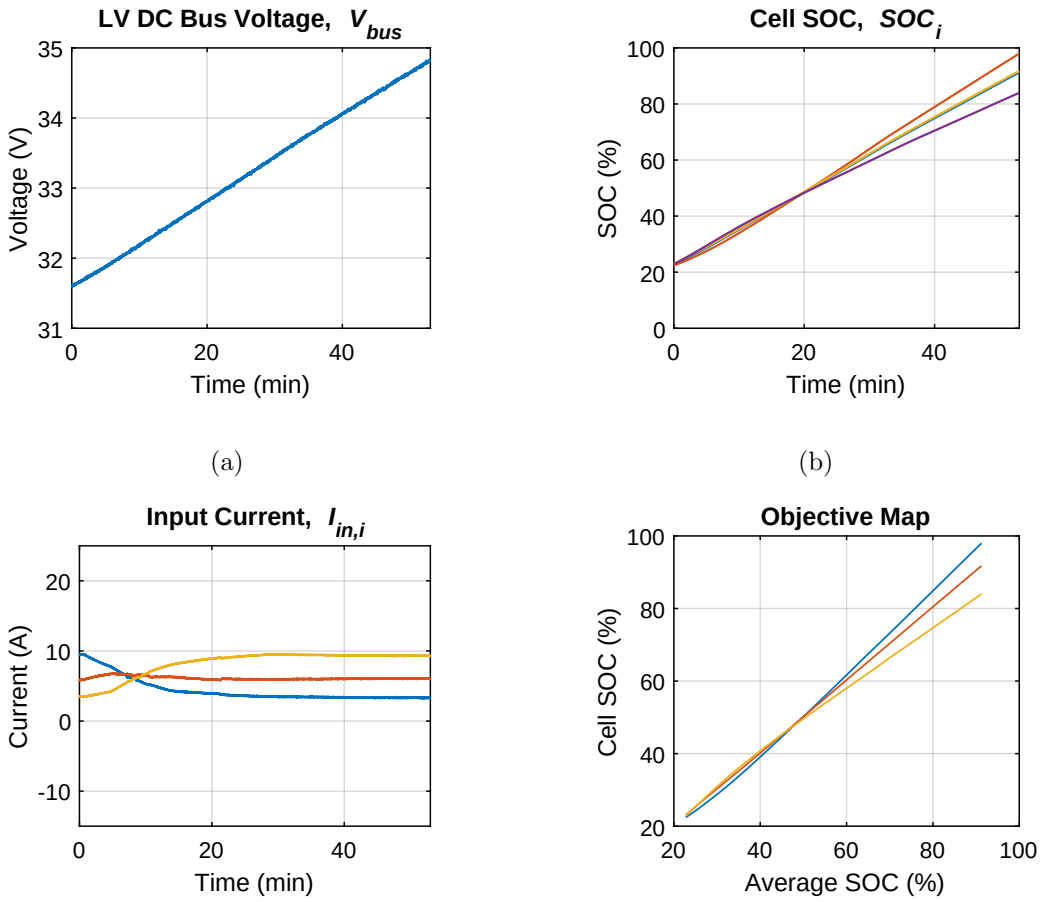


Fig. 6.22: Experimental results for cell SOH balancing under a medium life gain objective map using partially-distributed control. Battery cells are charged at a constant string current of 1C (25 A), and LV bus load is set to 10 A. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOH balancing objective map with high life gain.

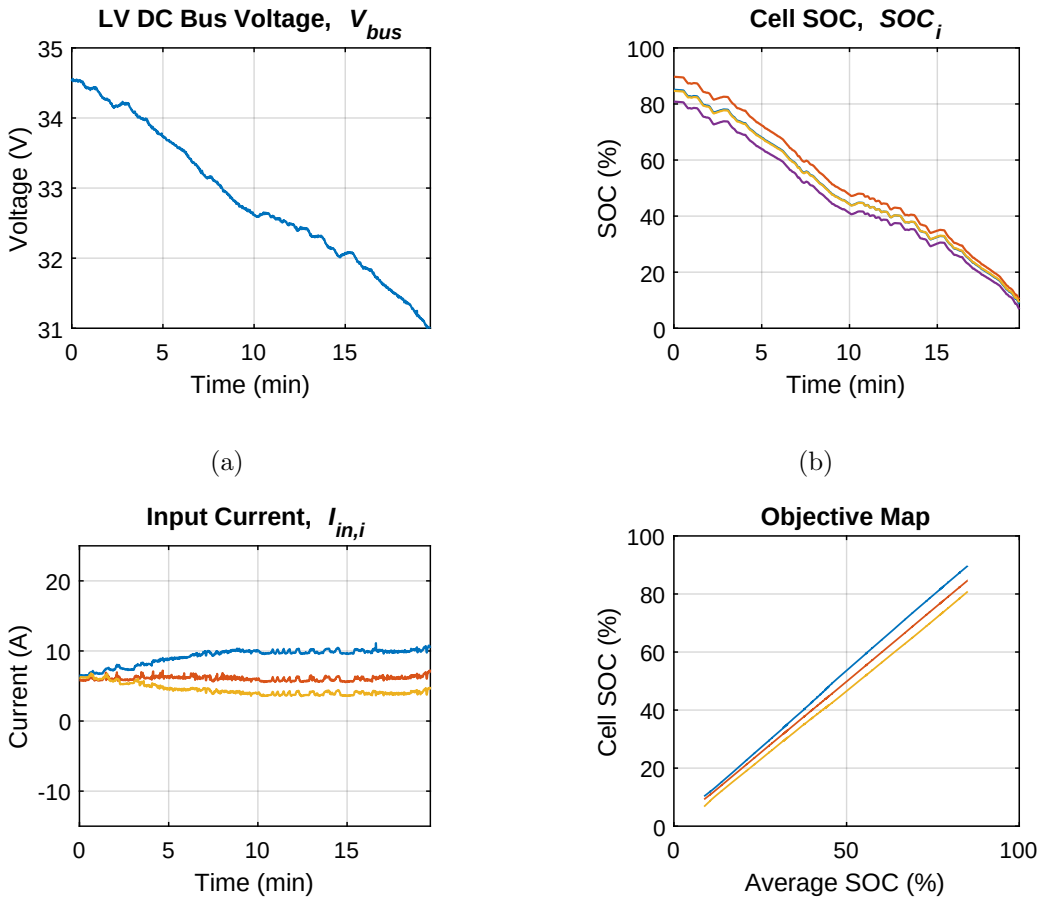


Fig. 6.23: Experimental results for cell SOH balancing under a medium life gain objective map using partially-distributed control. Battery cells are discharging under a dynamic drive profile (US06) with an average discharge rate of 2.5C (62 A), and LV bus load is set to 10 A. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOH balancing objective map with medium life gain.

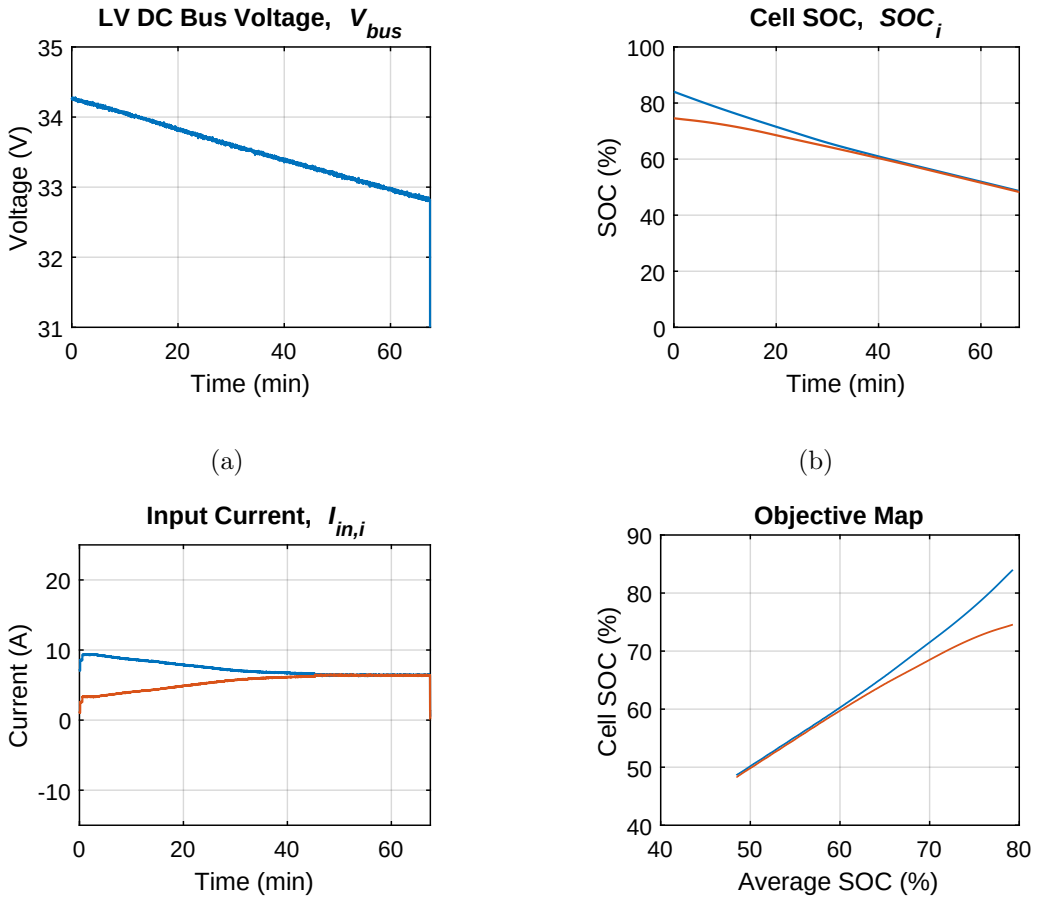


Fig. 6.24: Experimental results for independent-input, parallel-output microgrid system implementing cell SOC balancing using partially-distributed control. Battery modules are supplying a LV bus load of 270 W. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOC balancing objective map.

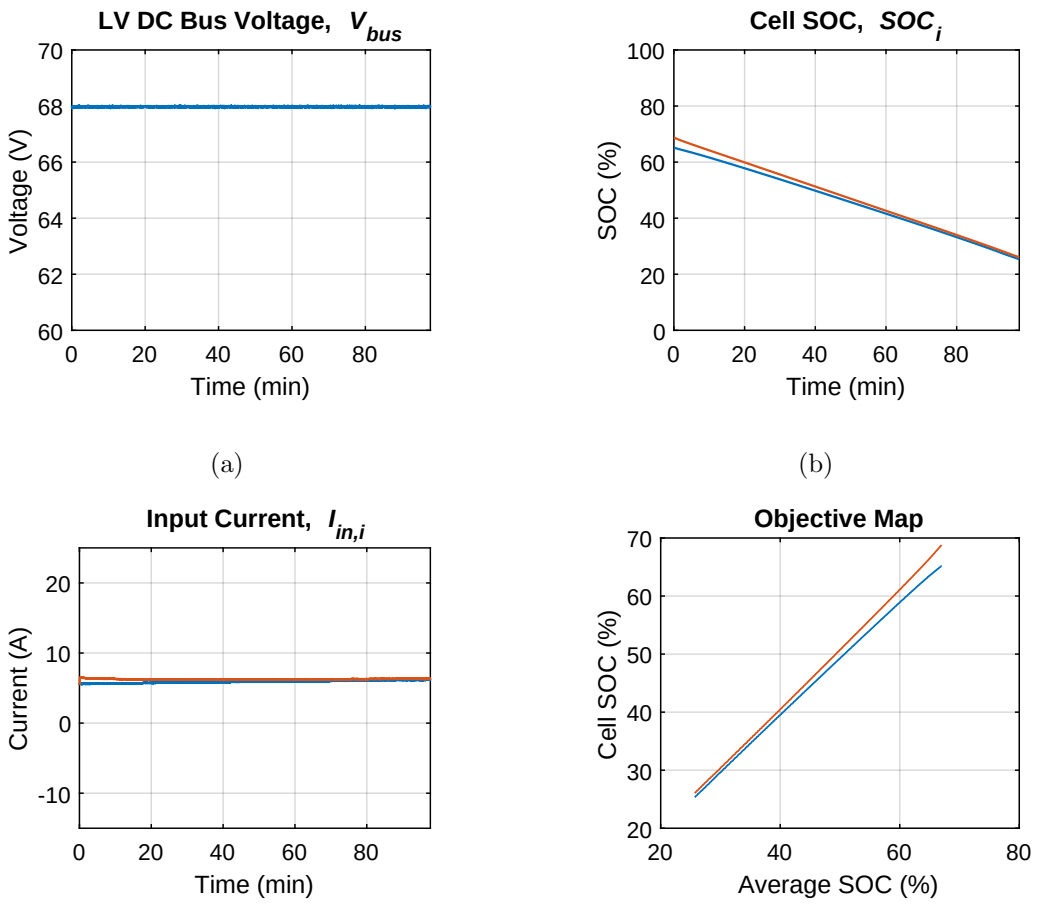


Fig. 6.25: Experimental results for independent-input, series-output microgrid system implementing cell SOC balancing using partially-distributed control. Battery modules are supplying a LV bus load of 270 W. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOC balancing objective map.

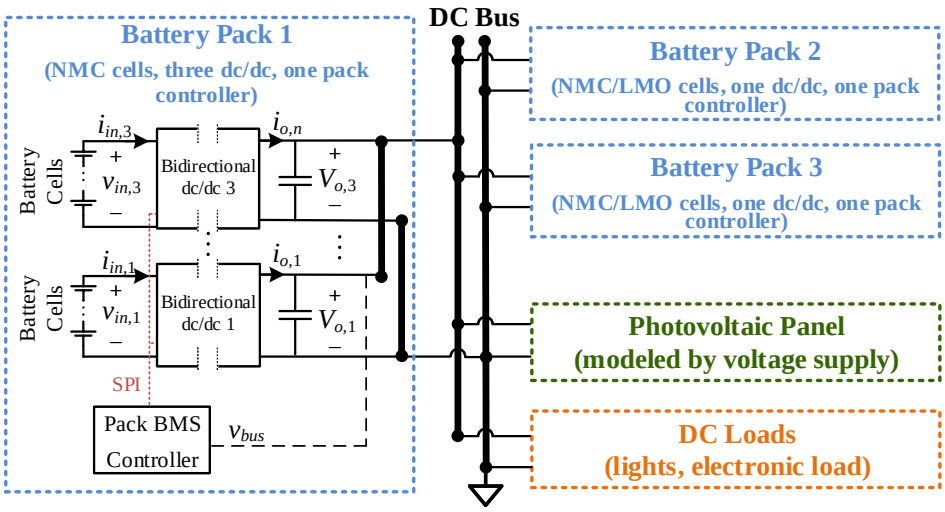


Fig. 6.26: Hardware experiment setup multiple battery packs, renewable sources, and DC loads connected to a shared DC bus.

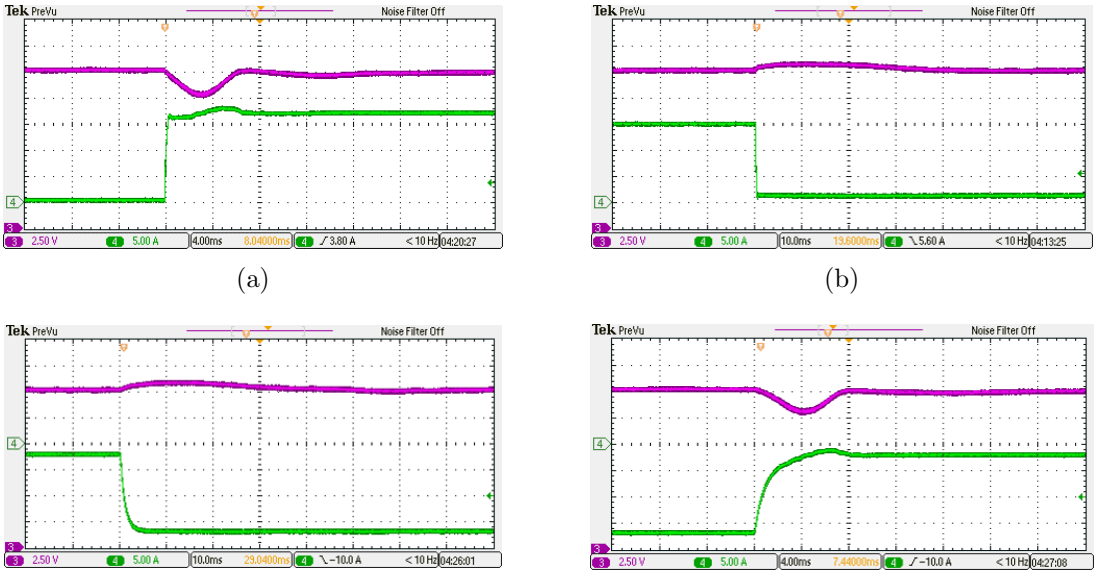


Fig. 6.27: Experimental results for step changes in bus load current for (a) $I_{load} = 0$ A to $I_{load} = 17$ A, (b) $I_{load} = 15$ A to $I_{load} = 1$ A, and renewable source current (c) $I_{PV} = -2$ A to $I_{PV} = -17$ A, and (d) $I_{PV} = -17$ A to $I_{PV} = -2$ A. Ch3: V_{bus} (pink), Ch4: $I_{load/PV}$ (green).

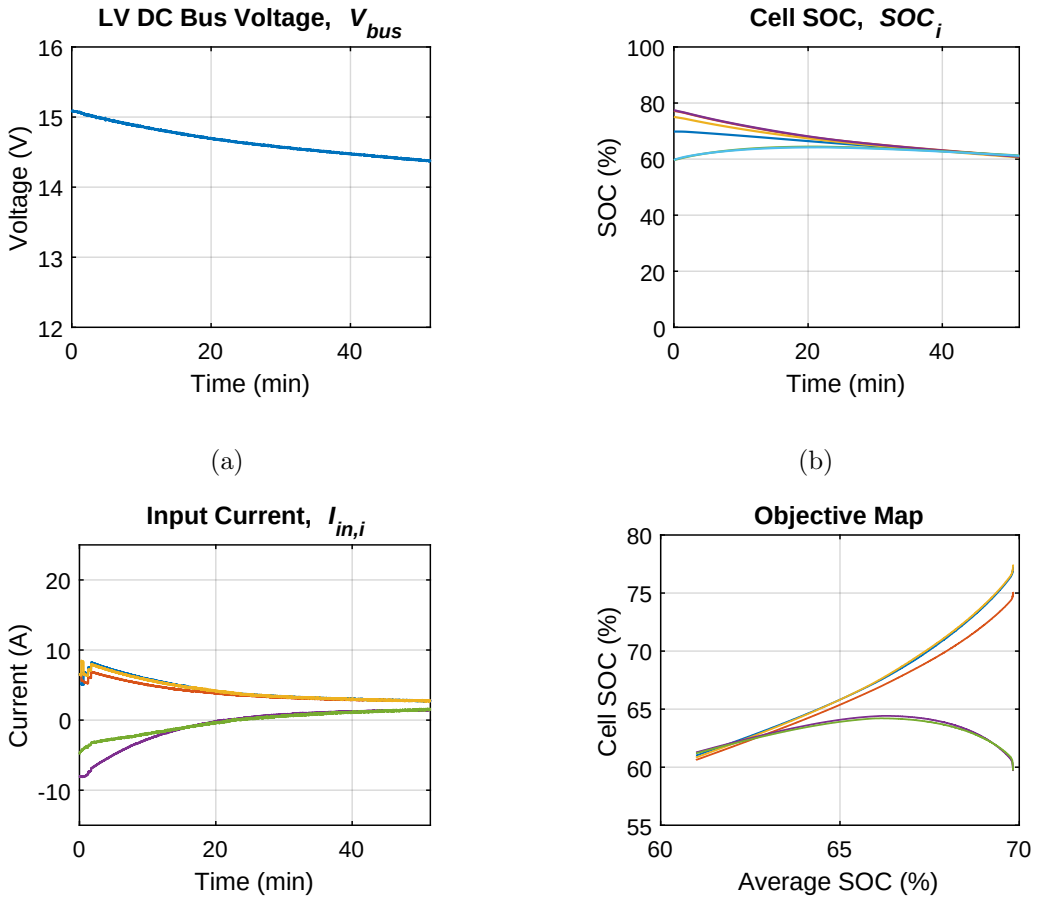


Fig. 6.28: Experimental results for DC microgrid system with multiple battery packs, solar PV, and DC loads. Battery packs implement cell SOC balancing using shared DC bus voltage objective map. DC bus load is set to 270 W. Results are shown for (a) bus voltage, (b) cell SOC, (c) converter current, and (d) cell SOC balancing objective map.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

The design of modular battery systems offers unique requirements including architecture, design, modeling and control of power processing converters, and battery balancing methods. This work focuses on design and control of modular battery systems for automotive and stationary applications. The modular battery system uses cell or substring-level power converters to combine battery balancing and power processing functionality and opens the door to new opportunities for advanced cell balancing methods. With this approach, the integrated balancing power converters can achieve system cost and efficiency gains by replacing or eliminating some of the conventional components inside battery systems such as passive balancing circuits and high-voltage, high-power converters. The design and control concepts developed in this thesis are applied to designs of large vehicle and microgrid battery packs. It is shown that the battery pack performance, lifetime, size, and cost can be significantly improved with the modular design and advanced control techniques.

7.1 Summary of Contributions

The work and the results reported in this thesis are summarized here.

7.1.1 Modular Battery System Architecture

Motivated by the challenges faced by conventional battery systems, a new modular battery system architecture that uses scalable battery modules is presented. The battery module serves as the fundamental building block of the modular battery system and consists of a cell brick (group of one or more cells connected in series or parallel) and a dc/dc power converter. With this approach, cell balancing and power processing functions are integrated into each of the battery module, enabling differential power processing down to cell-level. Furthermore, the battery module can be configured in multiple ways to achieve one or more

DC bus system.

An xEV battery system with multiple DC bus voltages (HV and LV) is realized using a combination of battery modules. This is done by placing module input port in series to form the HV bus and output port in parallel to form a shared DC bus. In this configuration, the power for vehicle propulsion is directly accessed from the series string and the vehicle auxiliary LV bus is tied to the shared DC bus. It is shown in this work that the modular architecture offers simplicity, high efficiency, and cost gains when used for xEV applications by replacing the high step-down dc/dc converter and central BMS with small low-power, low-voltage dc/dc converters. A more general, single DC bus system is constructed by placing the output port of battery modules in a series-parallel combination to achieve required voltage, power, and energy ratings. The modular system offers great benefits when used for stationary applications like utility/micro/nano-grids.

The modular approach achieves continuous balancing of battery cells, requires minimum to no control communications among battery modules, is scalable to an arbitrary number of battery cells and naturally shares the load current according to the relative state-of-charge (SOC) and state-of-health (SOH) of the battery cells. With special emphasis on xEV and stationary applications, this thesis featured detailed development of the proposed modular battery system for these applications. Discussion on integrated power converter topology, power rating, and isolation requirement for both applications is also provided.

7.1.2 System-level Control and Advanced Battery Cell Balancing Methods

New system-level control methods are presented for the modular battery system that integrates cell balancing and bus voltage regulation functions into small dc/dc converters. This work presents an objective map based control approach to implement traditional cell voltage and SOC balancing methods. In addition, the control approach is extended to implement advanced cell balancing methods that are based on battery life prognostic models. To implement the cell balancing methods, the control approach is based on objective maps. This approach allows traditional and advanced cell balancing methods to be implemented

in a simple and scalable manner for large battery packs.

A fully distributed control scheme is developed for the series-input, parallel-output xEV battery system. The distributed approach alleviates communication requirements necessary to produce correct division of DC bus load among cells. The control scheme uses the shared bus voltage itself as a means of communicating the balancing target (average voltage or SOC), does not rely on high-speed digital communications for any of the control loops and instead uses locally available information for all control actions. The distributed control approach is extended to demonstrate balancing and load sharing among multiple battery pack on a shared DC bus. A partially-distributed control approach is developed for the more general single DC bus battery system. The control methods achieve reliable cell state regulation, cell current protection, and DC bus voltage regulation.

With the modular architecture and new control methods for integrated dc/dc converters, a number of existing technologies are improved upon. It is shown that accurate, online state-of-charge (SOC) and state-of-health (SOH) information can be used to better control the battery system at a cell or substring level. Significant improvement in performance and extension in lifetime of battery pack can be achieved via advanced battery state control based on empirical battery life prognostic models. In addition, this opens the door to new opportunities for advanced cell-level control based on accurate physics-based cell models, enabling full utilization of previously untapped cell capability and further improvements in battery lifetime.

7.1.3 Comprehensive Control Design and Analysis

A comprehensive discussion on modeling, design, and analysis of control loops for the parallel and series output integrated dc/dc converters is provided. The choice of dc/dc converter along with its switching modulation scheme and analytical model are discussed. Since the dc/dc converters combine cell balancing and bus voltage regulation functions in the modular battery system, this thesis presents control loop designs to decouple the two functions. A fully distributed control scheme is devised for the xEV battery system. The control law inside each dc/dc converter is programmed to enable DC bus voltage regulation,

and differential power processing based on cell state of charge and capacity. Designs for compensator and loop gain analysis are presented. Different scenarios with mismatch in series resistance, SOC, or cell capacity are analyzed to validate control behavior. A partially-distributed control approach is developed for the xEV battery system and the micro-grid battery system. The approach is especially useful for systems where the bus voltage can not be varied and used as a means to communicate. It is shown that the partially distributed approach can be used to achieve balancing function using a shared central controller.

7.1.4 Modular Battery System Design and Validation

The work and the results reported in this thesis contributed to projects focused on design and control of large xEV battery packs and plug-and-play battery systems. These projects were sponsored in part by Department of Energy under the ARPA-E Advanced Management and Protection of Energy Storage Devices (AMPED) program and later Office of Naval Research under the GREENs program. The projects were a collaboration between a multi-disciplinary team from Utah State University (USU), University of Colorado Boulder (CU Boulder), University of Colorado Colorado Spring (UCCS), National Renewable Energy Lab (NREL), and Ford Motor Company.

The modular system approach, design and control of integrated dc/dc converters, and cell balancing methods developed in this thesis were applied on a 7.5 kWh (Li-ion NMC) Ford Plug-in Hybrid Electric Vehicle demonstration pack, shown in Fig. 1.9. This battery pack was used to validate the circuit design and control and assess the value of advanced battery balancing methodology. The modular system approach was applied to one half of the pack with forty-two cells, and commercial passive balancing was applied to the other half of the pack for A/B comparison. With more than two years of accelerated dynamic cycling, the battery pack demonstrated significant improvement in battery lifetime. The modular system with advanced cell balancing control reduced cell capacity imbalance to half of that presented by the standard passive balancing system. While the pack did not reach end of life during this project, the degradation rate for the battery half-pack with proposed system was projected to a 25% increased lifetime. Furthermore, the on-pack demonstration established

that integrating power electronics into the battery pack can reduce cost, improve usable energy density through better capacity utilization, and improve lifetime for energy storage systems. This has put this technology on the development path for xEV manufacturers, but continued development activities for on-vehicle demonstration and manufacturing scale-up are required before wide deployment.

The concepts introduced in this thesis were also extended to plug-and-play battery systems for stationary applications. A scaled micro-grid system with one 1.7 kWh Li-ion NMC battery pack, two 0.6 kWh NMC/LMO battery packs, one solar PV power source, and some electronic loads was demonstrated in lab, as shown in Fig. 1.10. Hardware experiments verified several features of the system including hot-swapping a battery pack or internal module, mixed-chemistry pack operation on a single DC bus, power and energy sharing based on pack capability, and advanced lifetime control within each pack. The mixed-chemistry, plug-and-play concept demonstration established that integrating power electronics into the battery packs for stationary applications can reduce cost, improve system performance through better battery pack utilization, and improve lifetime for energy storage systems.

7.2 Future Work

In addition to the modular battery system applications, further research directions have been identified in the process of completing this thesis. A selection of future research directions are presented here, some of which have been analyzed through initial results, while others remain to be explored at the time of this thesis.

7.2.1 Plug-and-Play Modular Battery System for Stationary Applications

The more general modular battery system architecture of Fig. 3.6 opens research avenues for application in stationary systems (utility grid, micro/nano grid). Since most microgrid applications only require a single DC bus, a non-isolated converter topology can be used for better efficiency and power density. A hardware prototype has been built and initial results have been shown to verify cell balancing and voltage regulation. A picture of

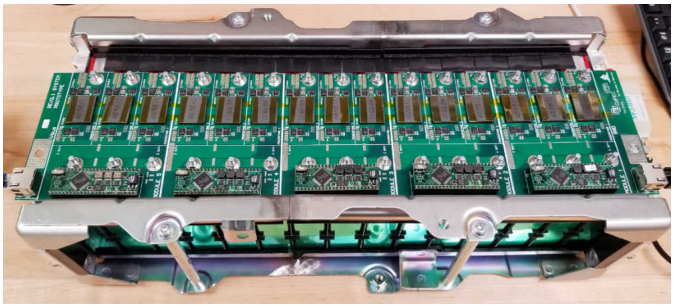


Fig. 7.1: Hardware prototype for the single DC bus modular battery system of Fig. 3.6. The prototype includes fifteen NMC battery cells with fifteen non-isolated buck-boost dc/dc converters that are connected in parallel/series output configuration.

the prototype system is shown in Fig. 7.1.

In addition, stationary systems can utilize multiple different battery packs with different size, chemistry, and priority requirements. The system can benefit from utilizing battery packs that can offer high power capability or high energy capability and optimize overall performance. The modular design and control concepts presented here can be extended in the direction of achieving these performance goals.

7.2.2 Integration of Used xEV Battery Packs in Second-use Applications

Typical xEV battery packs have very strict energy and power density requirements. When discharged from vehicle, xEV battery packs still have a good energy storage capacity left at the end of vehicle use application. Since, the volume and energy density requirements are relatively relaxed for stationary applications, used xEV battery packs can be utilized in stationary application. However, the state of a used xEV battery pack is typically unknown and presents challenges. The life prognostic model based control used in this thesis offers to eliminate these challenges and provides knowledge of battery pack at end of first life. In addition, the life control can be utilized later second use applications to optimize usage and lifetime of battery packs in stationary applications. An initial evaluation system of Fig. 6.26 proved system capability to handle different battery packs. Further investigation into system performance and life benefits is a topic for future research.

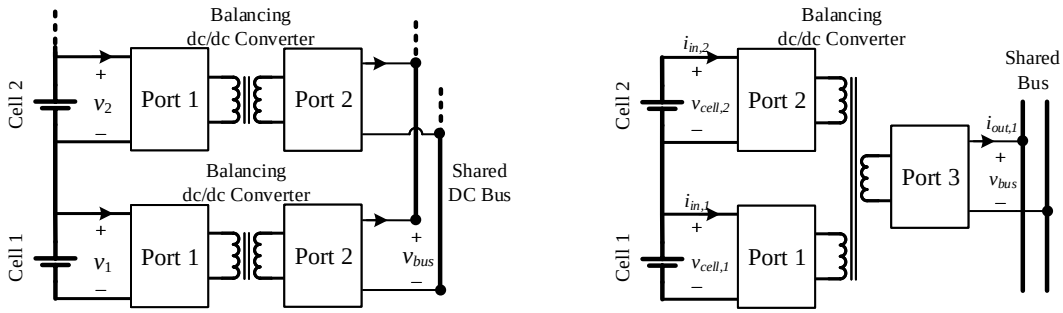
7.2.3 Micro-grid DC Bus Modeling and Analysis

DC microgrid systems utilize multiple power sources and sinks including solar PV, battery packs, diesel generator, and DC or AC loads. There is motivation to utilize renewable sources to full extent when available. This can be achieved by embedding a control goal based on the objective map approach presented in Chapter 4. In order to establish source priority and current sharing among power sources, the objective map can be designed to assign desired source priority similar to shown in Chapter 6. Further work can be done on optimizing system behavior and analyzing system stability under various operating scenarios.

7.2.4 Cost and Efficiency Optimization: Multi-port Converter Topologies

The modular architecture uses dc/dc converters that achieve continuous balancing of all cells by naturally sharing the load current according to the relative SOC and capacities of the battery cells. As described in Chapter 3, the converter can be realized using various isolated converter topologies. Existing work has only focused on a single, per-cell or per sub-string converter, shown in Fig. 7.2 that has an input port connected to a single cell and an output port connected to the DC bus. There is an opportunity to explore converter topologies that have more than a single input and output port and can actively balance more than one cell. For instance, a multi-port converter can open avenues for connecting multiple cells at input ports and shared DC bus at the output port of the bypass converter. This approach can expand the benefit matrix and reduce the relative cost of modular active balancing systems. If applied at cell-level, the multi-port dc/dc converter can balance two or more cells with fewer components and reduced cost. For application at substring level, the multi-port topology can increase the resolution of active balancing.

Initial results for a three-port topology were collected. The proposed topology, referred to here as differential dual-active bridge or DDAB, introduces changes in the conventional two-port dual-active bridge (DAB) converter and proposes a third-port that can process a small fraction of cell power to enforce cell balancing. The third port is achieved using a center-tap primary winding transformer and an additional inductor while using the same



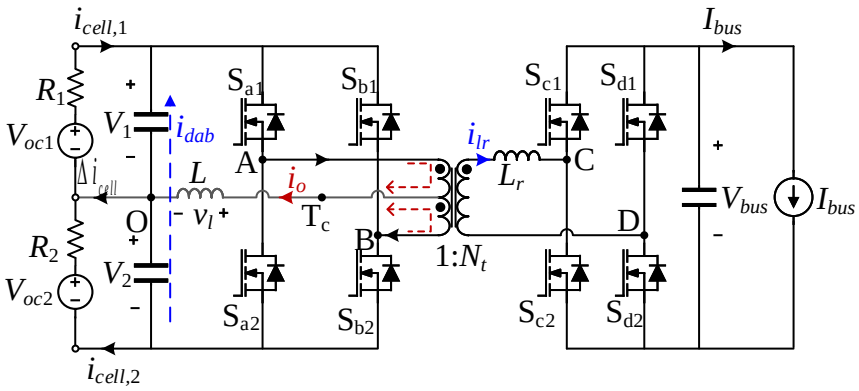
(a) (b)

Fig. 7.2: (a) Two-port balancing dc/dc converter with input (port 1) connected to a single cell, and an output (port 2) connected to shared DC bus, (b) three-port balancing dc/dc converter with port 1 and port 2 connected to two cells and port 3 connected to shared DC bus.

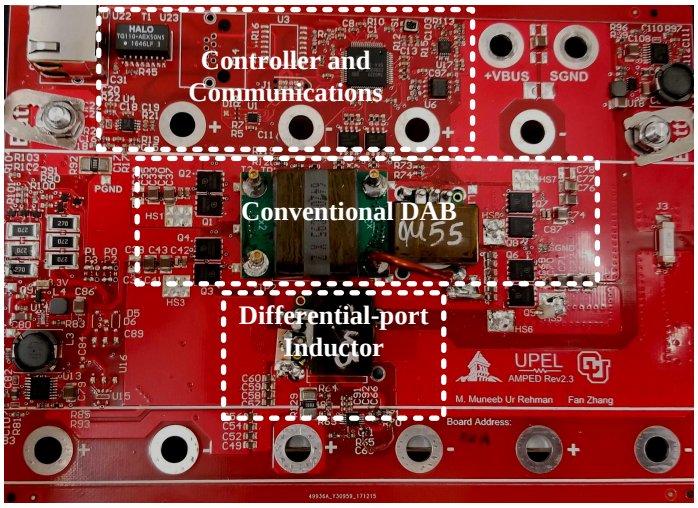
number of switches and auxiliary components as a typical DAB, as shown in Fig. 7.3. The result is active cell-level balancing for two battery cells using a single three-port converter. To process the small cell mismatch power, the proposed modulation scheme introduces very weak control coupling and thus allows the secondary-side power to be differentially split between the two cells at the primary side using a simple proportional-integral compensator. Furthermore, the secondary-side port can be easily configured at different voltage and power levels like the modular active balancing systems.

7.2.5 Cell Balancing Based on Physics-based Cell Models

The balancing methods presented in this thesis relied on equivalent circuit based models for cell state of charge and state of health estimation. While these models provide reasonable well SOC estimation for most applications, there is room for improvement in calculating power limits and identifying operating conditions that lead to faster cell degradation. Conventional battery management systems rely on cell terminal voltage limits to identify no-go regions. However, research shows that voltage limits may be violated for a short time in some situations without causing any faster aging and 'normal' voltages may also cause fast degradation in some situations, particularly for an aged cell [34, 43, 110].



(a)



(b)

Fig. 7.3: Example three-port dc/dc topology: differential dual-active bridge topology (DDAB) that interfaces two cells to the shared DC bus and achieves balancing functionality, (a) circuit schematic, (b) hardware prototype.

Physics based cell models provide mathematically more accurate predictions for cell SOC and cell degradation mechanisms. Along with more sophisticated control, the physics based models and the modular battery system presented in this dissertation can lead to much greater benefits in cell lifetime and expanded power and energy capability.

7.3 Publications

The work and the results reported in this thesis contributed to the following publications.

1. D. Costinett, K. Hathaway, **M. Muneeb Ur Rehman**, M. Evzelman, R. Zane, Y. Levron, and D. Maksimovic,"Active Balancing System for Electric Vehicles with Incorporated Low Voltage Bus," 29th IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, 2014. **Best Poster Presentation Award**

2. **M. Muneeb Ur Rehman**; Evzelman, M.; Hathaway, K.; Zane, R.; Plett, G.L.; Smith, K.; Wood, E.; Maksimovic, D., "Modular approach for continuous cell-level balancing to improve performance of large battery packs," IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014. **2nd Prize Paper**

3. **M. Muneeb Ur Rehman**; F. Zhang; Evzelman, M.; Zane, R.; Maksimovic, D., "Control of a series-input, parallel-output cell balancing system for electric vehicle battery packs," 16th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, 2015.

4. F. Zhang; **M. Muneeb Ur Rehman**; Zane, R.; Maksimovic, D., "Improved Steady-State Model of the Dual-Active-Bridge Converter," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015.

5. H. Wang; **M. Muneeb Ur Rehman**; M. Evzelman; and R. Zane, "SIMULINK based hardware-in-the-loop rapid prototyping of an electric vehicle battery balancing controller," 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, 2015, pp. 1-6.

6. F. Zhang; **M. Muneeb Ur Rehman**; H. Wang; Y. Levron; G. Plett; R. Zane; D. Maksimovic, "State-of-charge Estimation based on Microcontroller-implemented Sigma-point Kalman filter in a Modular Cell Balancing System for Lithium-Ion Battery Packs," 16th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, 2015.

7. **M. Muneeb Ur Rehman**; F. Zhang; R. Zane; and D. Maksimovic, "Design and control of an integrated BMS/DC-DC system for electric vehicles", 17th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), June, 2016.

8. **M. Muneeb Ur Rehman**; F. Zhang; M. Evzelman; R. Zane; K. Smith; and D. Maksimovic, "Advanced Cell-level Control for Extending Electric Vehicle Battery Pack Lifetime", IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016. **1st Prize Paper**

9. M. Evzelman, **M. Muneeb Ur Rehman**, K. Hathaway, R. Zane, D. Costinett and D. Maksimovic, "Active Balancing System for Electric Vehicles With Incorporated Low-Voltage Bus," in IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7887-7895, Nov. 2016.

10. **M. Muneeb Ur Rehman**; F. Zhang; R. Zane; and D. Maksimovic, "Control of bidirectional DC/DC converters in reconfigurable, modular battery systems", 32nd IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017.

11. F. Zhang; **M. Muneeb Ur Rehman**; R. Zane; and D. Maksimovic, "Hybrid Balancing in a Modular Battery Management System for Electric-Drive Vehicles", IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, 2017.

12. D. Yelaverthi; **M. Muneeb Ur Rehman**; R. Zane, "Three-port Dual Active Bridge Converter for Active Balancing in Large Battery Packs", 2018, *in submission.*

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