

BIDIRECTIONAL THREE-PHASE AC-DC POWER CONVERSION
USING DC-DC CONVERTERS AND A THREE-PHASE UNFOLDER

by

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ABSTRACT

Bidirectional Three-Phase AC-DC Power Conversion
Using DC-DC Converters and a Three-Phase Unfolder

by

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Strategic use of energy storage systems alleviates imbalance between energy generation and consumption. Battery storage of various chemistries is favorable for its relatively high energy density and high charge and discharge rates. Battery voltage is in dc, while the distribution of electricity is still predominantly in ac. To effectively harness the battery energy, a dc-ac inverter is required. For low-voltage applications (<500 V and <100 kW), a three-phase two-level voltage source inverter (VSI) is the preferred topology due to its simplicity. The VSI is pulse-width modulated at high frequency to obtain the desired line currents. The high switching frequency typically results in increased switching loss and generation of large voltage harmonics that require filtering. A dc-dc stage, commonly of a dual-active bridge (DAB) topology, is often used between the battery and VSI to step up the battery voltage and provide galvanic isolation. It is also operated at high frequency to reduce passive component sizes.

To reduce size and weight over the conventional two-stage converter, this dissertation proposes an alternative two-stage topology based on a three-phase unfolding inverter (unfolder). The proposed topology reduces the number of high-frequency switching stages. The unfold stage operates at line frequency to directly connect each dc-dc stage output

with the corresponding phase depending on the phase angle. The line-frequency operation generates negligible switching loss and minimal current harmonics in the unfolders but does not allow control of line currents. They are instead shaped by the high-frequency dc-dc stage.

A line filter is still required to attenuate harmonics from the dc-dc stage but is reduced in size through integration with existing passive components. To quantify the size reduction, major passive and filter components are designed in an unfolding converter with the dc-dc stage implemented with two dual-bridge series resonant converter (DBSRC) modules. An optimized DBSRC design procedure is provided to minimize conduction loss when used with unfolders. The procedure is used to generate an example 10-kW design. A 40% reduction on total passive and filter component volume is concluded when compared to a conventional DAB-VSI converter of the same ratings.

The shaping of the three-phase line currents using the two DBSRC modules in the dc-dc stage is investigated through various controller designs. The design process is assisted by development of detailed dynamic models of the unfolding converter. Various more basic controllers are attempted before settling on a final version. A feedforward controller enables operation at non-unity power factors by fine-tuning the applied unfolded and reference current sectors. An integral output feedback controller tuned using linear quadratic regulator ensures stability with a highly inductive grid or load. These benefits are combined into a robust rotating-frame controller. It is verified in simulation and experiment. It meets the IEEE 1547 harmonic requirement and produces total harmonic distortion below 5% at any values of power factor and line inductance.

(175 pages)

PUBLIC ABSTRACT

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Strategic use of energy storage systems alleviates imbalance between energy generation and consumption. Battery storage of various chemistries is favorable for its relatively high energy density and high charge and discharge rates. Battery voltage is in dc, while the distribution of electricity is still predominantly in ac. To effectively harness the battery energy, a dc-ac inverter is required.

A conventional inverter contains two high-frequency switching stages. The battery-interfacing stage provides galvanic isolation and switches at high frequency to minimize the isolation transformer size. The grid-interfacing stage also operates at high frequency to obtain sinusoidal grid currents and the desired power. Negative consequences of high-frequency switching include increased switching loss and the generation of large voltage harmonics that require filtering.

This dissertation proposes an alternative two-stage inverter topology aimed at reducing converter size and weight. This is achieved by reducing the number of high-frequency switching stages and associated filter requirements. The grid-interfacing stage is operated at the line frequency, while only the battery-interfacing stage operates at high frequency to shape the line currents and control power flow. The line-frequency operation generates negligible switching loss and minimal current harmonics in the grid-interfacing stage. As a result, the required filter is reduced in size. Hardware designs are performed and compared between the conventional and proposed converters to quantify expected size reduction. Control methods are developed and verified in simulation and experiment to obtain high-quality line currents at all power factors.

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ACRONYMS

DAB	dual-active bridge
DBSRC	dual-bridge series resonant converter
FPGA	field-programmable gate array
IGBT	insulated-gate bipolar transistor
LQR	linear quadratic regulator
MCT	minimum current trajectories
MOSFET	metal-oxide-semiconductor field-effect transistor
PLL	phase-locked loop
PI	proportional-integral
PR	proportional-resonant
PWM	pulse-width modulation
SVM	space-vector modulation
THD	total harmonic distortion
UPS	uninterruptible power supply
VSI	voltage source inverter
ZVS	zero voltage switching

CHAPTER 1

INTRODUCTION

1.1 Background

The increasing penetration of renewable power sources such as wind and solar into the existing power grid has presented challenges to grid stability and reliability. These challenges originate from the sources' highly variable output power and their dispersed locations. The imbalances between generation, distribution and consumption can be balanced by strategic use of energy storage systems [1].

There are different types of energy storage systems presently used in the electric grid [2]. The earliest and presently largest in capacity is the pumped hydro. Compressed air storage is also widely used. The fastest growing types are various forms of battery energy storage. The most mature battery chemistries are lead-acid, sodium-sulfur and lithium-ion. These different types of energy storage serve different purposes, with technologies high in capacity used infrequently but usually for extended periods in hours, and those high in power used more frequently but for short durations in minutes. Lithium-ion batteries typically fall in the latter category, where they are often used to improve power quality for industrial and residential users. Commercial solutions have been developed in both sectors. ABB has developed the DynaPeaQ line of products that use static var compensator techniques. They provide active power support through internal lithium-ion batteries and can supply active power of 50 MW for up to 60 min [3]. Tesla has developed the Power Wall for residential use [4]. There is also active research on grid integration of batteries in electric vehicles with vehicle-to-grid [5] and vehicle-to-home concepts [6–8].

Almost all grid-tied battery systems require an inverter to interface between ac voltages on the grid and dc voltage from the battery. The inverter acts as a power flow controller. The desired amount of power used to charge or discharge the battery is controlled via the

inverter. Similar amounts of power will be either received from or delivered to the grid. The difference in power is lost in the inverter. The power has both active and reactive components. The existing grid has compensation mechanisms to balance the active and reactive powers between supply and demand. The result is a well-maintained ac voltage magnitude and frequency. With higher penetration of grid-tied inverters, this compensation mechanism can also be built into the inverters, allowing automatic regulation of grid voltage and frequency.

A grid-tied inverter operating at below 100 kW and 500 V is typically implemented using a three-phase two-level voltage source inverter (VSI). The VSI switches are modulated at more than 20 times the fundamental grid frequency to output sinusoidal currents through an inductive filter. This filter, typically the *LCL* type, attenuates the high-order current harmonics beyond the switching frequency. These high-order harmonics are a result of the high-frequency switching in the VSI, which is necessary for current control. A well-controlled VSI provides suppression of low-order current harmonics, even under distorted grid voltages. The resulting line currents should be of sufficient quality to command the desired active and reactive powers. To reduce switching loss and ease thermal management in a hard-switched VSI using insulated-gate bipolar transistors (IGBTs), the switching frequency is usually limited to below 20 kHz [9,10]. This low switching frequency requires an even lower filter corner frequency to maintain the same attenuation at harmonic frequencies. This usually results in a large line filter.

In case of a grid failure due to voltage and frequency faults, the inverter will have to be disconnected from the grid to prevent energizing it. This is done to avoid hazards to grid maintenance personals. Early inverters, especially those designed for photovoltaic systems, are designed to simply disconnect from the grid. With this, the user loses access to voltages, similar to a blackout situation. More recent works have proposed to use battery-connected inverters to support critical loads when the grid is unavailable [6-8, 11]. This is known as an islanded or grid-forming mode. In this mode, the inverter is responsible for maintaining well-regulated ac voltage to the load. Similarly important is the ability to

smoothly disconnect from and reconnect to the grid and not interrupting voltage supply to the load. In this regard, the inverter behaves similar to a line-interactive uninterruptible power supply (UPS). A grid-interactive inverter designed to operate in both grid-tied and grid-forming modes shall maintain ac voltage and current regulation under load and grid disturbances and ensure smooth mode transitions.

It is common to install an isolation transformer between the inverter output and grid connection. The transformer is primarily used to ensure safety to both the end user and grid. Due to nonidealities in control and modulation, a VSI can output small amounts of zero-sequence and dc currents. These parasitic currents disrupt normal grid operations and should be limited to acceptable levels [12]. The use of isolation transformer blocks these currents from entering the grid [13]. Another purpose of the isolation transformer is in adjustment of inverter output voltage through its turns ratio [14], which is commonly selected to step up the output voltage. This is necessary with a low input dc voltage such as that from photovoltaic and battery sources, or for interfacing the inverter with a medium voltage grid (>1 kV) [10].

The drawbacks of the isolation transformer are its bulky size and weight, as it operates at line frequency. Many turns are required to reduce the peak flux density to avoid core saturation. In addition to increasing the VSI output voltage by the isolation transformer, the same can be achieved by increasing its input dc voltage. A boost dc-dc converter is inserted between the VSI and dc source to step up the source voltage. The resulting intermediate voltage between the boost and VSI stages is commonly referred as the dc-link voltage and is typically higher than the source voltage [10, 11, 15, 16].

There is great motivation to reduce converter size and weight and to retain benefits of the isolation transformer. The solution is to integrate isolation into the dc-dc converter. The dc-dc transformer size and weight are greatly reduced compared to a line-frequency transformer of similar ratings, due to much higher operating frequency. In addition to galvanic isolation, this high-frequency transformer is designed with a turns ratio used to step up the dc source voltage to the appropriate dc-link voltage required by the VSI. As

long as the zero-sequence and dc currents at the VSI output are kept within the required limits, the line-frequency transformer can be largely removed.

In battery systems, the isolated dc-dc converter is required to process bidirectional power. Among various suitable topologies, the dual-active bridge (DAB) dc-dc converter is widely used. There are many publications on the two-stage converter with DAB and VSI stages. The targeted applications include battery energy storage [17], electric vehicle battery charger [18, 19] and solid-state transformer [20].

1.2 Research Objectives

Motivated by further reduction in size and weight over the conventional DAB-VSI converter, this dissertation investigates a proposed two-stage converter topology based on a three-phase unfolding inverter (unfolder). There are two main research objectives. The first is to formulate design procedures of the proposed converter hardware and to quantify the size reduction. The second objective is in development of a suitable controller to operate the proposed converter in grid-tied mode.

The hardware design of the unfolding converter is studied in detail to highlight the reduction in line filter size. The filter size reduction is made possible through reducing the number of high-frequency switching stages. In a conventional two-stage converter, the VSI stage operates at high frequency to control and shape the line currents. The dc-dc stage also operates at high frequency to reduce converter size. In a hard-switched VSI, the high-frequency operation results in high switching loss and large voltage harmonics around and beyond the switching frequency. These harmonics require filtering before the VSI is connected to the grid.

In the unfolding converter, the unfolder stage operates at line frequency, generating negligible switching loss and minimal line current harmonics. Shaping of the line currents is performed by the high-frequency dc-dc stage. A line filter is still required to attenuate the dc-dc generated harmonics but is reduced in size through integration with existing dc-dc stage components. The line-frequency operation of the unfolder removes its ability to control the line currents. This control burden is placed on the dc-dc stage. This necessitates

the development of new models and control methods to achieve common control objectives of a grid-tied converter.

1.3 Dissertation Organization

Following this brief introduction, the remainder of this dissertation is divided into the following chapters.

Chapter 2 provides a comprehensive review of the existing literature on the design and control of a conventional two-stage DAB-VSI converter. The review focuses on the VSI filter design considerations in grid-tied and grid-forming modes, based on regulatory standards from IEEE and IEC. The designed filter has consequences on control of the VSI. The various control objectives of the VSI are reviewed. The design of the DAB is also reviewed, and a hardware design of a complete 10-kVA converter is carried out as a reference for comparison with the proposed converter.

Chapter 3 introduces the topology of the proposed converter. The derivation of the unfolder circuit is provided, and some background motivating its creation is provided from high power factor three-phase rectifiers. The design requirements on the dc-dc stage are summarized from analysis of the unfolder operation. The dc-dc stage is implemented using two dual-bridge series resonant converter (DBSRC) modules, due to their wide operating ranges and fast dynamic responses. A modulation strategy of the DBSRC is reviewed and is based on minimizing its resonant tank current.

Chapter 4 provides detailed design procedures on major passive and filter components in the unfolding converter. Estimates of component rms currents are provided to aid their design. The rms currents can be optimized by careful selection of the transformer turns ratio. The line filter is designed to comply with the IEEE 1547 current harmonic limits. A hardware design of a 10-kVA DBSRC-unfolding converter is conducted and compared with the DAB-VSI converter at same ratings. The reductions in filter and overall passive volumes are quantified.

Chapter 5 develops a feedforward controller for the grid-tied unfolding converter. To aid controller design, a dynamic converter model is derived and verified in simulation. The

model reveals distortion in line currents at non-unity power factors due to limited DBSRC response. A method to reduce distortion is proposed and tested.

Chapter 6 develops two feedback controllers to improve on the previous feedforward control. Integral control corrects for errors between actual and reference currents. State and output feedback ensure stability with large line inductances. Both approaches rely on a high closed-loop bandwidth to ensure accurate current tracking. Current regulation is good at unity power factor but worsens at non-unity power factors.

Chapter 7 develops a rotating-frame controller to improve on the previous stationary-frame controllers. The rotating-frame controller combines benefits of feedforward and feedback controllers. It can maintain a high current quality at all power factors and in presence of large parameter variation. Simulation results are provided on the 10-kVA converter designed in Chapter 4. Experimental results are provided on a 1-kVA hardware prototype.

Chapter 8 provides conclusions on the design and control of the unfolding converter. Some possible future research directions are highlighted.

CHAPTER 2

REVIEW OF ISOLATED BIDIRECTIONAL THREE-PHASE CONVERTERS

This chapter provides a review of conventional isolated bidirectional three-phase converters. The modulation, control and filter design aspects of the three-phase two-level VSI are covered. The control and filter design are reviewed for both grid-tied and grid-forming modes. The requirements on a dc-dc converter for use with the VSI are provided. They include capabilities such as isolation and voltage step-up.

2.1 Voltage Source Inverter

A two-level VSI is the preferred topology in low-voltage applications (<500 V and <100 kW). The VSI is needed to generate the desired ac output voltage or current, from a constant dc input voltage. The output voltage can be used to power ac loads while the utility grid is unavailable. The output current can be fed into or drawn from the ac grid.

Semiconductor switches in the VSI are operated at a fixed switching frequency that is more than 20 times the frequency of the desired signal. Pulse width of the switch voltage is modulated using one of many pulse-width modulation (PWM) methods. At the end of each switching period, the period-averaged switch voltage is approximately equal to the input signal sampled at the period's beginning. The desired output signal is obtained as a moving average of the modulated switch voltage.

2.1.1 Output Filter Design in Grid-Forming Mode

Consider a three-phase two-level VSI with LC filter outputting voltage into a resistive load in Fig. 2.1a. Gate pulses of the IGBT switches are generated using space-vector modulation (SVM), which offers better input voltage utilization and ripple rejection than sinusoidal PWM [21]. Depending on implementation, it can also reduce switching loss. The drawback of SVM is computational complexity but can be overcome using modern embed-

ded processors. The reference three-phase voltages (v_{ra} , v_{rb} , v_{rc}) are transformed into an equivalent rotating vector in stationary frame. In the illustrated open-loop implementation, the vector's $v_{r\alpha}$ and $v_{r\beta}$ components along with the input voltage V are inputs to the space-vector modulator. In a realistic closed-loop setup, the input vector is generated from a feedback loop on the output voltage.

The per-phase equivalent circuit of the VSI is shown in Fig. 2.2. The purpose of the LC filter is to attenuate dominant harmonics while leaving the fundamental unaffected. This is generally true for light loads, where voltage drop in the filter can be neglected. The filter offers -40 dB/dec of attenuation above its corner frequency f_c . Once the required attenuation is known, from standards such as the IEC 62040, f_c can be determined [22]. A large value of f_c usually implies smaller filter size, but requires increasing the switching frequency, and doing so increases switching loss.

Define the modulation index m_i as ratio between actual and maximum output vector magnitudes and the modulation frequency m_f as ratio of switching to fundamental frequencies. The three modulated switch voltages referenced to the neutral point of the output filter are visualized in Fig. 2.1b for $m_i = 0.75$ and $m_f = 10$. The reference voltages are also shown for comparison. In the harmonic spectrum shown in Fig. 2.3 for the same m_i but increasing m_f to 100, the switch voltage has fundamental magnitude slightly less than the reference, primarily due to open-loop control. It additionally has harmonics around integer multiples of m_f , with the dominant harmonics at $m_f \pm 2$. Magnitude of the dominant harmonic can be readily found from simulation but can also be derived analytically [21].

2.1.2 Line Filter Design in Grid-Tied Mode

In addition to the stand-alone application of regulating voltage into ac loads, the VSI is commonly used to interface with the grid and regulate power flow. In a grid-tied VSI, the control and quality of current is of major concern, as defined in standards such as the IEEE 1547 [12]. Consider a grid-tied three-phase two-level VSI with LCL filter in Fig. 2.4. The topology and modulator is same as the previous example. The main difference is the filter structure and grid connection. Most early designs have used the L filter [23, 24]. The

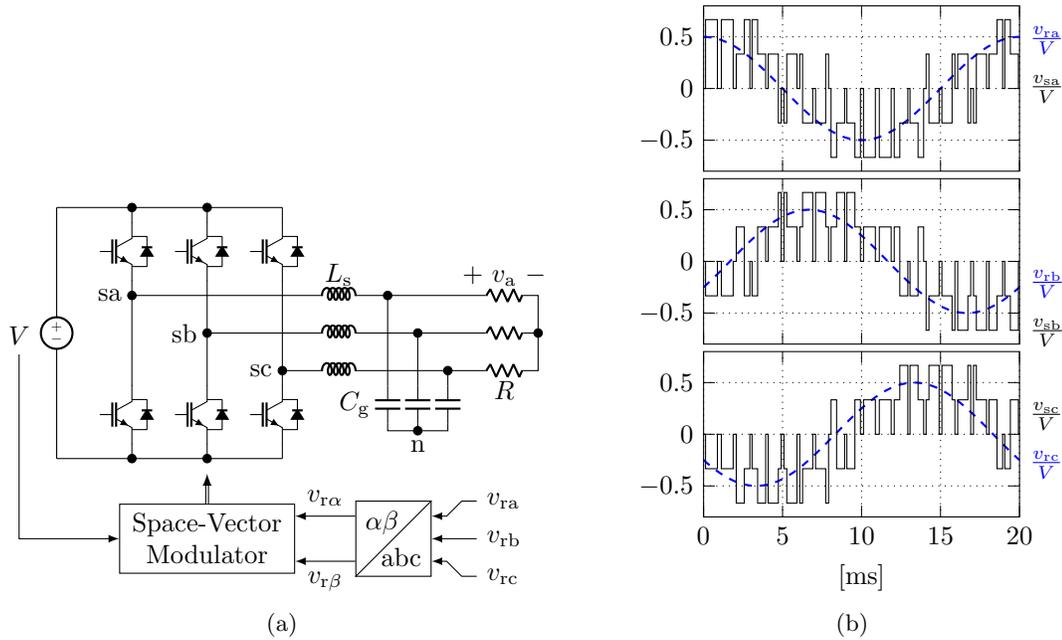


Fig. 2.1: VSI with LC filter connected to resistive load. (a) Circuit and controller. (b) Switch and reference voltages at modulation index of 0.75 and modulation frequency of 10 (50 Hz fundamental and 500 Hz switching frequencies).

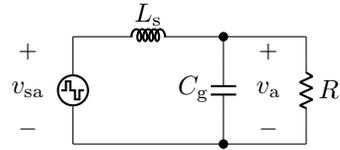


Fig. 2.2: Per-phase equivalent circuit of VSI with LC filter connected to resistive load.

drawback is the bulky inductor size due to a large inductance required to meet regulations. Later designs use the LCL filter that is smaller than L filter at the same attenuation. The drawback of LCL is possible resonance, which requires use of passive or active damping, and more susceptible to grid voltage distortions [25].

In the considered open-loop implementation, the per-phase equivalent circuit of Phase A is shown in Fig. 2.5. Both the switch and grid voltages can contain harmonics. Neglect the harmonics for now and consider only their fundamental components, represented as phasors. This gives a phasor equivalent circuit in Fig. 2.6a, where the two filter inductances can be combined below the filter's resonant frequency [26].

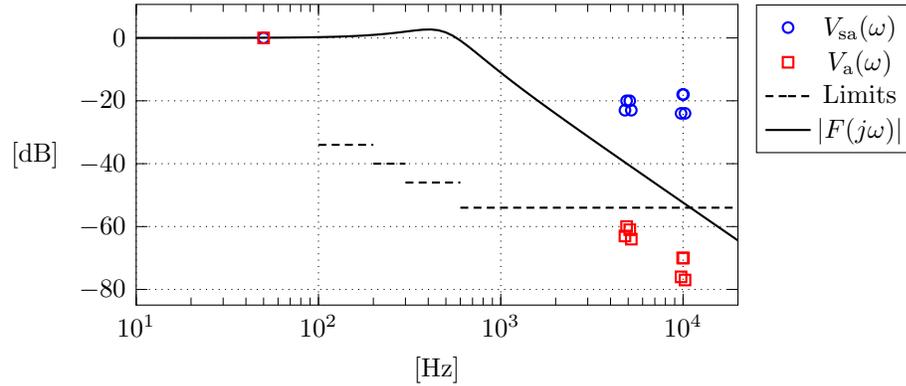


Fig. 2.3: Output filter design for a grid-forming VSI operating at modulation index of 0.75 and modulation frequency of 100 (50 Hz fundamental and 5 kHz switching frequencies), showing harmonic magnitudes of switch voltage $V_{sa}(\omega)$ and filtered output voltage $V_a(\omega)$, IEC 62040 limits and filter attenuation $F(s) = \frac{v_a(s)}{v_{sa}(s)}$.

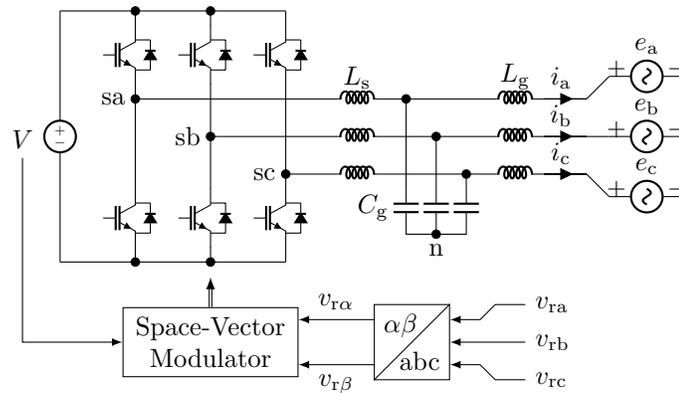


Fig. 2.4: VSI with LCL filter connected to three-phase grid.

The inductor or grid current is controlled by adjusting the magnitude and phase of the switch voltage relative to the grid voltage. This is visualized in Fig. 2.6b, where four symbolic points are identified. As the switch voltage moves to Point 1, the grid current and voltage become aligned, and power is delivered to the grid at unity power factor. Similarly, Point 2 means receiving power at unity power factor. Points 3 and 4 denote pure reactive and no active power. Any intermediate point means delivering or receiving a combination of active and reactive powers. Also note that the current magnitude is proportional to the applied voltage and inversely proportional to the inductance. So with a large inductance, a higher voltage is required to produce the same current. Using a small inductance will

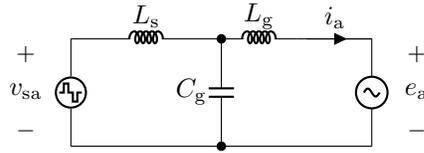


Fig. 2.5: Per-phase equivalent circuit of VSI with LCL filter connected to three-phase grid.

require fine adjustments in switch voltage to get the desired current. This is almost always accomplished by closed-loop control.

2.1.3 Example 10-kVA VSI Filter Design

Besides influencing control, the LCL filter is designed to attenuate the dominant current harmonics around the switching frequency. Referring to the equivalent circuit in Fig. 2.5, as previously stated, the switch voltage due to SVM produces dominant harmonics at $m_f \pm 2$. The filter admittance at these harmonic frequencies is chosen to produce the desired magnitude of the corresponding line current harmonics. The magnitude is determined based on the rated current and limits specified in IEEE 1547 [12]. Once the admittance is known, the filter component values can be selected for a specified switching frequency.

There is some freedom in value selection. In most cases, the size and cost of the filter are dominated by the filter inductors, and their sizes are to be optimized. Increasing the filter capacitance leads to lower inductance values. The drawback is more reactive current and more susceptible to grid voltage harmonics [25]. Beside energy storage requirements, losses are to be considered when designing the inductors. DC copper losses in both inductors

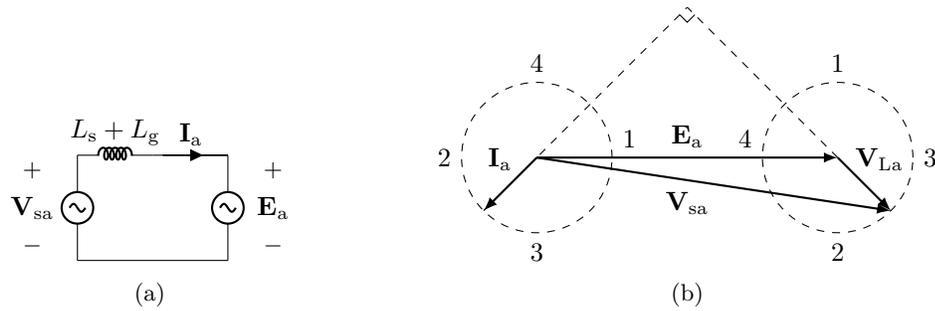


Fig. 2.6: VSI current control. (a) Phasor equivalent circuit. (b) Phasor diagram.

are evaluated using the rms line current and the respective winding's dc resistance. The inverter-side inductor L_s is subject to considerable core loss, which should be evaluated considering the varying peak flux density over the line period [27].

As example, Table 2.1 provides the designed *LCL* filter components for a 10-kVA three-phase two-level VSI switching at 10 kHz. The filter capacitor is chosen as 10 μF or 5% of base capacitance. The filter inductors are built with iron powder toroidal cores from Micrometals. The iron powder material is favored for properties such as low cost, high saturation flux density and distributed air gap. There are also many other suitable magnetic materials [28]. The inductor design uses a set of common constraints that include maximum temperature rise of 40 °C and maximum window fill factor of 40%. The two inductance values are fine-tuned to produce the minimum combined size and the required filter admittance at the specified filter capacitance value. Performance of the designed filter is evaluated in simulation and satisfies IEEE 1547, as shown in Fig. 2.7.

In the example design, the VSI filter size can be further reduced by increase in switching frequency. Burkart and Kolar claim that for a 10-kVA two-level VSI implemented with silicon carbide devices, increasing switching frequency beyond 20 kHz provides diminishing return on reduction of inductor volume [10]. The main reasons provided are increased switching loss, which requires more heat sink volume, and high-frequency inductor loss, which complicates inductor design.

2.1.4 Control in Grid-Tied Mode

The line current is controlled to obtain the desired amount of power. Assuming ideal grid voltage with only a fundamental component, the amount of power delivered to or received from the grid can be easily derived from the voltage and current phasors. In this case, by controlling magnitude and phase of the current, the active and reactive powers are controlled. To maintain the same amount of power output, the current will be dynamically adjusted as the voltage changes. Nevertheless, the core of VSI control in grid-tied mode is the regulation of line current. A direct control also ensures high current quality, free of harmonics and complying with international standards.

Table 2.1: 10-kVA grid-tied VSI line filter design.

Component	Parameter	Value
	Nominal DC Voltage	800 V
	Nominal AC Line-to-Line Voltage	480 V rms
	Nominal Three-Phase Power	10 kVA
	Switching Frequency	10 kHz
	Maximum Core Fill Factor	40%
	Maximum Temperature Rise	40 °C
	Cooling Method	Natural Convection
Inverter-Side	Inductance	1300 μ H
Inductor (L_s)	Core Size and Material	T400-34D
	Number of Turns	135
	Wire Size	9 AWG
	Estimated Loss	27 W
Grid-Side	Inductance	500 μ H
Inductor (L_g)	Core Size and Material	T249-34
	Number of Turns	96
	Wire Size	11 AWG
	Estimated Loss	12 W
Capacitor (C_g)	Capacitance	10 μ F
	Series	EPCOS B32796
	Specs	10 μ F 875 V

In case of a distorted grid voltage, there are two methods to control the line current. The first is to still only control the fundamental current component and suppress as much as possible the harmonics caused by the distorted voltage. Assume in the ideal case where only the fundamental current component exists. The active power is then produced by only the fundamental components of voltage and current. Reactive power can be produced by harmonics of the grid voltage in addition to its fundamental. This can lead to ripple in the instantaneous power. This control method is commonly adopted in high-performance and high-power inverters. The reason is to avoid further distorting the grid voltage and to comply with international standards.

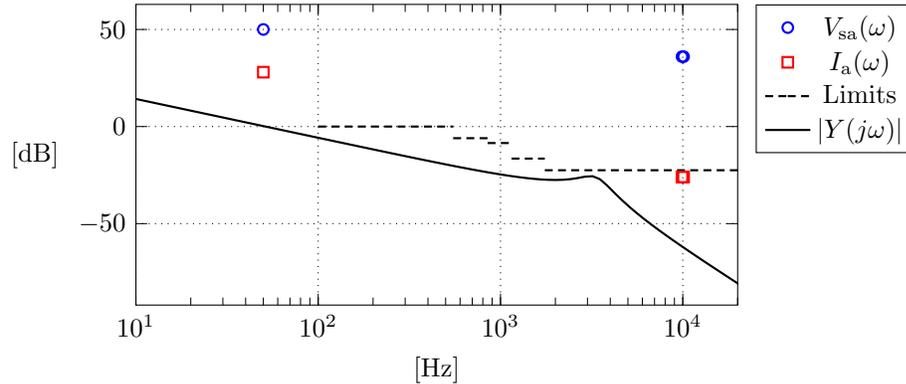


Fig. 2.7: Line filter design for a 10-kVA, 10-kHz grid-tied VSI operating at 800 V dc and 480 V rms line-to-line voltages, showing harmonic magnitudes of switch voltage $V_{sa}(\omega)$ and filtered line current $I_a(\omega)$, IEEE 1547 limits and filter admittance $Y(s) = \frac{i_a(s)}{v_{sa}(s)}$.

A second method controls the current harmonics in addition to the fundamental. A classic example is the boost power factor correction circuit, where the line current is commanded to track the instantaneous grid voltage. Ideal tracking will produce harmonics in the line current, and they are at same frequencies as the voltage harmonics. For the VSI, current harmonics can be controlled to cancel out those that are produced by a nearby system with distorted current. The operation will be similar to an active power filter. Inverters in this category will have more complex control, and different standards will apply.

Line current control of only the fundamental components using the three-phase VSI with *LCL* filter is now reviewed. The control references are provided as a two-dimensional vector in stationary or rotating frame representing the fundamental component. The controller is designed to minimize errors between fundamental components of reference and actual current signals, as well as suppressing low-order harmonics in the actual signal. Errors can come from a variety of sources, such as inaccuracies and delays caused by the modulator, variations in the input voltage, harmonics in the grid voltage, and inductor nonlinearities.

Linear control methods are widely used as the tuning procedures for stability and performance are well known. They are typically used with a pulse-width modulator. Different linear methods have been used to minimize the errors. Early methods attempt to minimize

the instantaneous error using a proportional-integral (PI) compensator. However, even with a high compensator gain, there is unavoidably still considerable error in the fundamental components [23,24]. A later method uses Clark and Park transformations to map the actual time-varying signals into a reference frame that rotates at the fundamental frequency [13]. The original fundamental components become dc components in this rotating frame. Errors between commanded and transformed dc components can be easily minimized with the integral term in the PI compensator. The drawback of this approach is the computation complexity of the transformations. A similar method also minimizes error on the fundamental components but uses a proportional-resonant (PR) controller, which has an extremely large gain at the fundamental frequency [24,29,30]. The controlled quantities are kept in the stationary frame, so transformations are not needed. This method is well suited in a grid-tied converter, as variation in grid frequency is usually small, so the controller's resonant frequency can be constant.

In either the rotating frame with PI or the stationary frame with PR controllers, the harmonic current components are suppressed by increasing the closed-loop regulation bandwidth [29–31]. Higher bandwidth also improves transient response to changes in reference commands, and can lead to reduced energy storage requirements on the dc-link capacitor [32,33]. Increase in bandwidth is usually limited by the switching frequency and to avoid instability. Using a low switching frequency or large filter values usually lowers the regulation bandwidth. As an example, the bandwidth of a VSI switching between 5 and 10 kHz is around 500 Hz and covers up to the seventh harmonic [26,27,29,34]. Nonlinear controllers such as dead-beat predictive control can be used to obtain faster closed-loop dynamics, but they have other limitations such as difficulty in minimizing the steady-state error [35].

2.1.5 Control in Grid-Forming Mode

Standalone or grid-forming inverters regulating ac voltage are predominantly used in uninterruptible power supplies (UPS), whose performance has to satisfy the IEC 62040 [22]. In particular, the load regulation characteristics are specified. The steady-state voltage

harmonic limits and total harmonic distortion (THD) are specified and need to be met with either linear or nonlinear loads. The dynamic voltage over and undershoot are specified for linear and nonlinear load steps. These stringent requirements are hardly, if ever, met with the basic open-loop controller in Fig. 2.1a, and closed-loop control is almost always used. Repetitive control of output voltage is based on the internal model principle and offers large loop gain only at harmonic frequencies [14,36,37]. It is able to produce high-quality voltage even with nonlinear loads and still ensures stability.

Other published works include additional feedback signals in addition to the output voltage. A popular method uses an inner current loop and an outer voltage loop [38–40]. The inner current loop ensures high regulation bandwidth and stability of the inductor current. It also allows monitoring of the inductor current for protection. The outer voltage loop is designed around the plant with compensated current loop. This compensated plant largely masks the inductor dynamics and eases the voltage loop design. The compensators are of PI in synchronous frame or PR in stationary frame to remove steady-state error on the fundamental voltage. Relying only on feedback is sometimes difficult to achieve satisfactory dynamic response with nonlinear loads and under load transients. The feedforward of load current in generation of PWM signals is used to improve dynamics [41, 42]. The feedforward action lowers the inverter’s output impedance and reduces the sensitivity to load disturbances [43].

2.1.6 Control in Grid-Interactive Mode

A significant feature of UPS is to provide uninterrupted supply of power to critical ac loads [44]. In a line-interactive UPS, the grid voltage is constantly monitored. When a grid fault is detected, the series switch between grid and load is opened, and the UPS starts to supply the entire load power. Recent grid-tied inverters have incorporated voltage controls that allow them to function similar to a line-interactive UPS during a grid fault [40,42,45]. As soon as a fault is detected, the inverter and loads are disconnected from the grid and form an island. The inverter also switches from line current to load voltage regulation. The process is reversed during reconnection to grid. The primary challenges are to ensure

smooth mode transitions, load voltage quality and line current quality.

In an island, it is often desired to share the load power evenly across multiple inverters. Various control schemes have been proposed to achieve this, including droop [11, 46–48], and master-slave methods [39, 49]. In the master-slave method, the master inverter regulates voltage, while the slave inverters regulate current. Communication is required between master and slave inverters. In the droop method, all inverters regulate voltage and frequency by adjusting their active and reactive powers based on a common droop curve. Sharing of load power occurs naturally, and communication between inverters is not required. The droop method can also be used in grid-tied mode to regulate grid voltage and frequency [47].

When grid voltage and frequency change depending on load, the inverters can be used to support the grid, by providing supporting features. The major difference between a grid-tied and grid-interactive inverter is in generation of phase angle and command references. In a grid-tied inverter, the angle directly comes from a phase-locked loop (PLL) that is synchronized with the grid voltage. However, studies have shown that this scheme can destabilize the grid if it is a microgrid formed by many inverters operating at the same time. In the microgrid, the inverters shall be controlled to stabilize the voltage and frequency. This can be accomplished by either a centralized approach or a distributed approach such as droop control. Most of these approaches keep the inner current loop mostly unchanged.

2.2 Two-Stage DAB-VSI Converter

It is common to install an isolation transformer between the inverter output and grid connection. The transformer is primarily used to ensure safety to both the end user and grid. Due to nonidealities in control and modulation, a VSI can output small amounts of zero-sequence and dc currents. These parasitic currents disrupt normal grid operation and should be limited to acceptable levels [12].

The use of isolation transformer blocks these currents from entering the grid [13]. Parasitic leakage current can flow on the earth ground connection due to the pulsating VSI switch voltage and capacitive coupling between the dc source and ground [50]. Excessive leakage current is unsafe to the user but can occur due to large parasitic capacitance to

ground. This is commonly the case when the dc source has significant surface area, such as in photovoltaic panels and electric vehicle battery packs [51,52]. Using isolation transformer reduces the effective parasitic capacitance and thereby lowers the leakage current.

Another purpose of the isolation transformer is in adjustment of the inverter output voltage through its turns ratio [14], which is commonly selected to step up the output voltage. This is necessary with a low input dc voltage such as that from photovoltaic and battery sources, and for interfacing the inverter with a medium voltage grid (>1 kV) [10]. Finally, parasitics of the isolation transformer, mainly its leakage inductance, can be used as part of the line filter [13]. The drawbacks of the isolation transformer are its bulky size and weight, as it operates at line frequency. A large number of turns is required to reduce the peak flux density to avoid core saturation.

In addition to increasing the VSI output voltage by the isolation transformer, the same can be achieved by increasing its input dc voltage. A boost dc-dc converter is inserted between the VSI and dc source to step up the source voltage. The resulting intermediate voltage between the boost and VSI stages is commonly referred as the dc-link voltage and is typically higher than the source voltage [10,11,15,16].

2.2.1 DC-DC Converter Selection

There is great motivation to reduce converter size and weight and to retain benefits of the isolation transformer. The solution is to integrate isolation into the dc-dc converter. The dc-dc transformer size and weight are greatly reduced compared to a line-frequency transformer of similar ratings, due to much higher operating frequency. In addition to galvanic isolation, this high-frequency transformer is designed with a turns ratio used to step up the dc source voltage to the appropriate dc-link voltage required by the VSI. As long as the zero-sequence and dc currents at the VSI output are kept within the required limits, the line-frequency transformer can be largely removed.

In battery systems, the isolated dc-dc converter is required to process bidirectional power. Among various suitable topologies, the dual-active bridge (DAB) dc-dc converter is widely used. There are many publications on the two-stage converter with DAB and VSI

stages, as shown in Fig. 2.8. The targeted applications include battery energy storage [17], electric vehicle battery charger [18,19] and solid-state transformer [20].

2.2.2 Example 10-kW DAB Design

For grid-tied battery energy storage applications, a DAB dc-dc converter can be used between the battery pack and VSI [17–19,53]. The DAB circuit has been shown in Fig. 2.8. The DAB transfers power between its input and output ports by adjusting the phase shift between its primary- and secondary-side bridges. For a narrow range of variation in input and output voltages, the single-angle modulation technique is adequate and is considered for subsequent DAB design. For larger variations, dual- or three-angle modulation techniques can yield lower circulating current and higher efficiency [54].

The DAB size and weight are largely influenced by its major passive components, which include the tank inductor, transformer, input and output capacitors. They have been selected for a 10-kW design. This design provides a reference for subsequent comparison with the proposed converter of similar ratings. A summary of the DAB design is provided in Table 2.2.

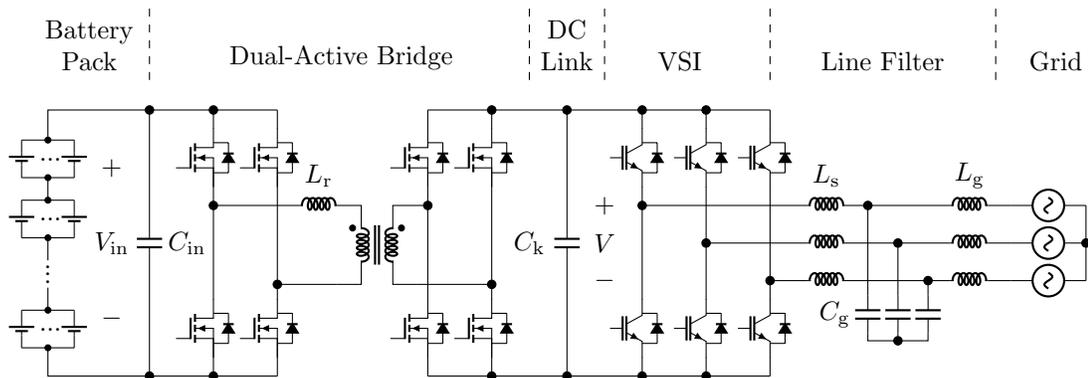


Fig. 2.8: Two-stage DAB-VSI converter.

Table 2.2: 10-kW DAB passive component design.

Component	Parameter	Value
	Nominal Input Voltage	300 V
	Nominal Output/DC-Link Voltage	800 V
	Nominal Power	10 kW
	Switching Frequency	50 kHz
	Maximum Core Fill Factor	40%
	Maximum Temperature Rise	40 °C
	Cooling Method	Natural Convection
Transformer	Turns Ratio	2.7
	Number of Cores	5
	Core Size	E65/32/27
	Number of Primary Turns	5
	Primary Wire Size	15 AWG ($\times 10$)
	Number of Secondary Turns	68
	Secondary Wire Size	17 AWG
	Estimated Loss Per Core	7.2 W
	Estimated Temperature Rise	38 °C
	Tank	Inductance
Inductor (L_r)	Number of Cores	4
	Core Size	E42/21/20
	Air Gap Length	3.7 mm
	Number of Turns	8
	Wire Size	15 AWG ($\times 8$)
	Estimated Loss Per Core	3.8 W
	Estimated Temperature Rise	39 °C
Input	Capacitance	40 μ F
Capacitor (C_{in})	Series	EPCOS B32774
	Specs	10 μ F 450 V ($\times 4$)
DC-Link	Capacitance	100 μ F
Capacitor (C_k)	Series	EPCOS B32778
	Specs	50 μ F 900 V ($\times 2$)

2.3 Improved Two- and Single-Stage Converters

Regulation of the dc-link voltage between the dc-dc and VSI stages in a cascaded converter is required. Poor regulation can degrade ac waveforms and create additional stress on the semiconductor devices [53]. The dc-link voltage variation is a function of the difference in instantaneous powers of the two stages and the amount of dc-link capacitance. The power difference is a result of different closed-loop dynamics between the two stages. Voltage regulation can be achieved either through the dc-dc converter or the VSI [53]. To reduce dc-link capacitance, it is beneficial to regulate voltage using the stage with faster dynamics [53]. Furthermore, the commanded power can be fed forward to the voltage controller to reduce voltage variation and capacitance requirement [33].

Existing works have presented various efforts to improve on the two-stage DAB-VSI topology. These works can be grouped into two classes. The first class of converters do not significantly deviate from the two-stage topology but apply incremental improvements, primarily in control. A stiff dc-link voltage is necessary for ensuring converter stability and typically requires significant amount of capacitance. The dc-link capacitance and associated energy storage requirement can be reduced while still ensuring stability through improvements in VSI control [55], or by coordinatively regulating the dc-link voltage using both stages [53]. The capacitance requirement is further relaxed by not requiring a stiff voltage but instead intentionally allowing a sixth harmonic ripple [56–59]. As the ripple is aligned with the peak line-to-line voltages, fewer switching actions are required of the VSI while still producing the desired output waveforms. The result is reduced switching loss.

The second class of converters apply more dramatic topological changes, typically resulting in just a single power conversion stage. These single-stage converters are identified by the absence of any decoupling capacitor. Single-stage converters first appeared as high power factor rectifiers [60], with advantages including reduced component count and improved efficiency. Similar concept has been applied to bidirectional converters [61, 62]. New modulation and control techniques are developed and reported along with these topologies.

2.4 Summary

This chapter has provided a review of the conventional DAB-VSI converter. The modulation, control and filter design aspects of the three-phase two-level VSI are reviewed. An example line filter design is provided in a 10-kVA grid-tied VSI to comply with IEEE 1547 limits. The requirements on a dc-dc converter for use with the VSI are provided, which include capabilities of isolation and voltage step-up. The design of the dc-link capacitor is highlighted. The DAB dc-dc topology is chosen. The design and selection of major passive components in a 10-kVA DAB-VSI converter are provided as a reference of comparison to the proposed converter of similar ratings.

CHAPTER 3

UNFOLDING CONVERTER TOPOLOGY AND OPERATION

This chapter introduces an alternative two-stage grid-tied converter whose operation is significantly different from the previous DAB-VSI topology. The grid-interfacing stage is a line-frequency unfolding inverter (unfolder). Its invention is inspired by high power factor rectifier topologies. The chapter starts with a review of two rectifier topologies, before introducing the three-phase unfolder. The unfolder operation and its implication on the dc-dc stage design are discussed. Subsequently, the selection and analysis of a suitable dc-dc converter are provided.

3.1 Review of Three-Phase Rectifiers

3.1.1 Single-Switch Rectifier

Three-phase active rectifiers are widely used in industry to obtain regulated dc output voltage and to actively shape the line currents to reduce harmonics. In Fig. 3.1a, one of the most basic topologies, the single-switch rectifier, is first considered [63]. It consists of a diode bridge followed by a boost converter. This topology is commonly used to obtain output voltages higher than the peak line-to-line voltage to supply a load. The load can be passive as depicted, or active such as an inverter in a motor drive.

The boost inductor current is controlled based on two objectives. The first is to obtain the desired amount of power to supply the load. This is achieved by control of the rms value of the fundamental line current. The second is to ensure high power factor. This is challenging due to a low current quality in this topology, as only two diodes in the bridge are conducting at any time, due to the peak detector nature of the diode bridge.

A simple and common method of controlling the rectifier is shown in Fig. 3.1b. In this scheme, the inductor current is controlled to a constant value I_r . This current flows on two

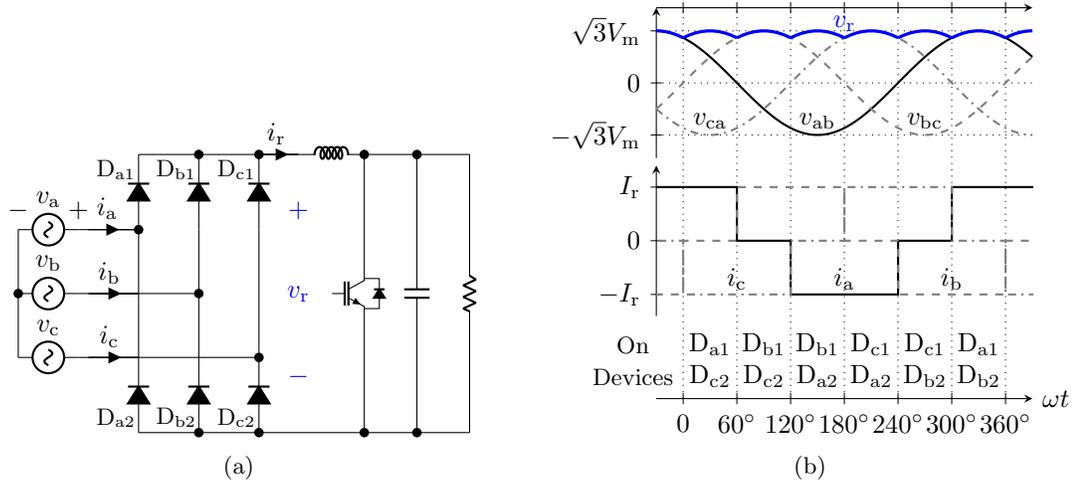


Fig. 3.1: Single-switch rectifier. (a) Circuit topology. (b) Typical waveforms.

out of three phases at any time, resulting in block-shaped line currents. The line current THD is high, at close to 30% [63].

3.1.2 Third-Harmonic Current Injection Rectifier

The single-switch rectifier suffers from low current quality due to 120° periods of non-conduction in each line current. To improve current quality, it is necessary to ensure continuous conduction of line currents. A topology known as the third-harmonic current injection rectifier has been designed for this purpose [63, 64].

The concept of this topology is shown in Fig. 3.2a. Notice its similarity with the single-switch rectifier, with the line phases connected to the diode bridge and a dc-dc converter, represented by current source i_r . The phases are additionally connected to an added current injection network, which consists of three four-quadrant switches (Q_a, Q_b, Q_c) and a second converter i_2 .

The injection network adds more versatility in line current control, which is not possible in the single-switch rectifier. Based on 60° sectors of the line voltages, the corresponding injection switch is turned on to connect the otherwise non-conducting phase to the injection source. The source currents i_r and i_2 are controlled to track 120° profiles as shown in

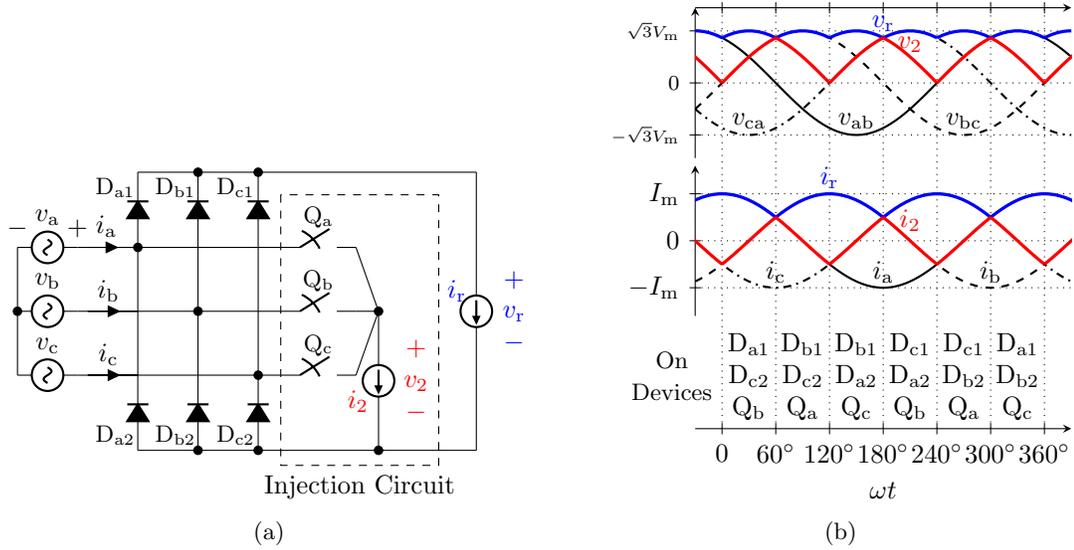


Fig. 3.2: Third-harmonic current injection rectifier. (a) Circuit topology. (b) Typical waveforms.

Fig. 3.2b. Both currents vary at the third-harmonic frequency to shape the fundamental-frequency line currents. The two current sources can also be treated as outputting segments of the line currents, and that these segments are reconstructed into sinusoidal currents by the diode bridge and injection network.

The additional controls offered in the third-harmonic current injection rectifier significantly improve current quality at unity power factor. THD values of line currents can be reduced below 5% [63, 64].

3.2 Three-Phase Unfolder

The third-harmonic current injection rectifier can be modified to enable bidirectional power flow and operation at non-unity power factors by replacing the bridge diodes with current bidirectional switches, while leaving the injection network intact. This results in the general circuit topology of the three-phase unfolding inverter (unfolder), depicted in Fig. 3.3a. It is fed by two symmetrical current sources in the dc link, although they may also be configured asymmetrically similar to the third-harmonic current injection rectifier in Fig. 3.2a.

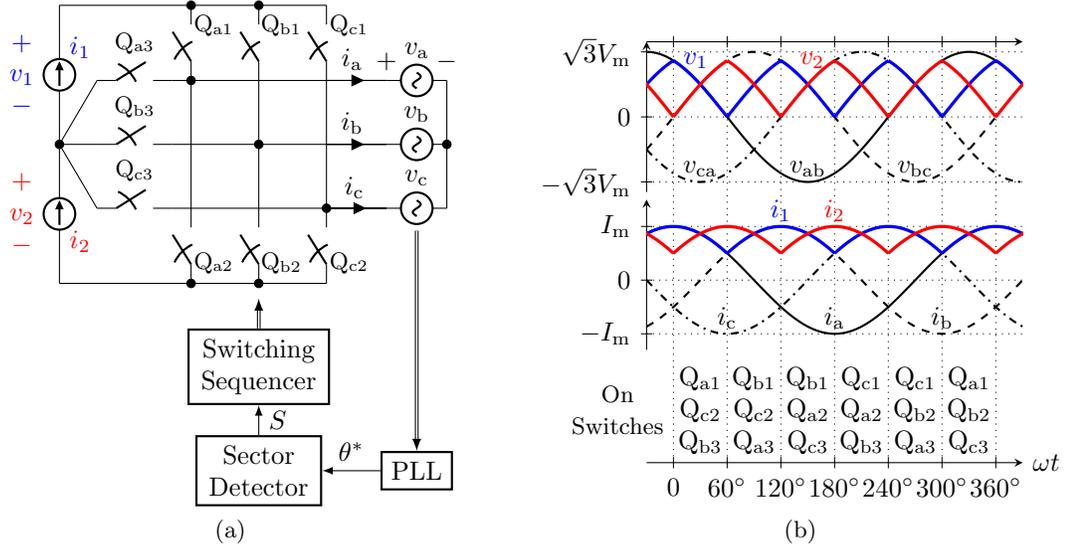


Fig. 3.3: Three-phase unfolding inverter. (a) Generic topology fed by symmetrical current sources. (b) Typical waveforms at unity power factor.

The unfolders switches are controlled using a switching sequence generated based on sectors identified from the unfolders output voltage. With the unfolders outputs directly connected to balanced grid voltages of fundamental magnitude V_m and angular frequency ω ,

$$\begin{cases} v_a = V_m \cos(\omega t) \\ v_b = V_m \cos(\omega t - \frac{2\pi}{3}) \\ v_c = V_m \cos(\omega t + \frac{2\pi}{3}) \end{cases}, \quad (3.1)$$

the voltage angle θ^* is estimated using a phase-locked loop (PLL) on the grid voltages,

$$\theta^* \approx \text{mod}(\omega t, 2\pi) = \omega t - \text{floor}\left(\frac{\omega t}{2\pi}\right) \cdot 2\pi, \quad 0 < \theta^* < 2\pi. \quad (3.2)$$

The sector variable S is then generated as an integer between one and six and is updated every 60° based on θ^* ,

$$S = \text{ceil}\left(\frac{\theta^*}{\pi/3}\right), \quad 1 \leq S \leq 6. \quad (3.3)$$

In each sector, a different set of unfolders switches are activated to generate dc-link voltages

v_1 and v_2 rectified from the grid voltages. As shown in Fig. 3.3b, the dc-link voltages overlap with portions of the line-to-line grid voltages and vary between zero and $1.5V_m$.

Application of this switching sequence results in a direct connection between each line and dc-link node. These connections establish voltage and current relationships between line and dc-link quantities in each sector, as identified in Table 3.1. The relationships describe the rectification of grid voltages into dc-link voltages as well as the required dc-link currents to produce the desired line currents. Waveforms of the dc-link currents required to produce line currents of fundamental magnitude I_m at unity power factor are shown in Fig. 3.3b, where each dc-link current varies between $0.5I_m$ and I_m .

The three-phase unfolder can be implemented with three-level inverter topologies [65]. The implementation using the neutral point clamped topology is shown in Fig. 3.4 [66]. Compared to a high-frequency switched VSI, the unfolder operates at line frequency and generates negligible switching loss and minimal line current harmonics, assuming proper control and filtering of the dc-link currents. The very low switching frequency, however, prohibits the unfolder from directly controlling the line currents. Instead, they are shaped by the dc-dc stage which controls the dc-link currents. Therefore, the performance of this two-stage unfolding converter depends very much on the design and control of the dc-dc stage.

The design requirements of the dc-dc stage can be obtained from the line voltages and currents and using the unfolder relationships. Consider desired line currents of fundamental

Table 3.1: Unfolder relationships.

Sector	$v_1 =$	$v_2 =$	$i_1 =$	$i_2 =$
1	v_{ab}	v_{bc}	i_a	$-i_c$
2	$-v_{ab}$	$-v_{ca}$	i_b	$-i_c$
3	v_{bc}	v_{ca}	i_b	$-i_a$
4	$-v_{bc}$	$-v_{ab}$	i_c	$-i_a$
5	v_{ca}	v_{ab}	i_c	$-i_b$
6	$-v_{ca}$	$-v_{bc}$	i_a	$-i_b$

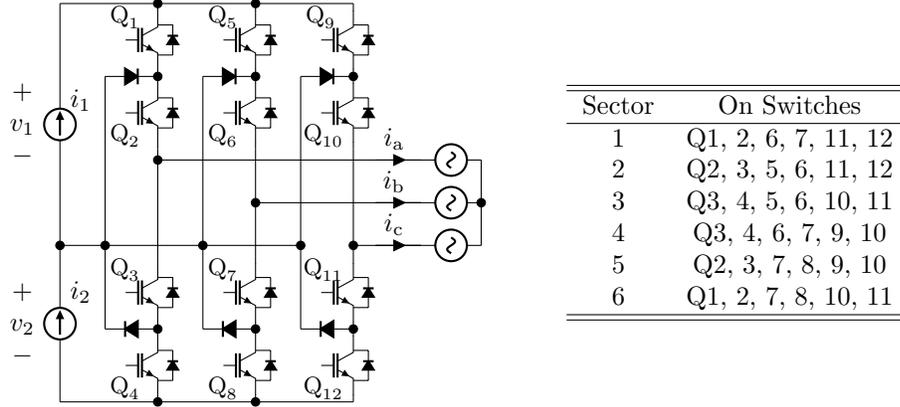


Fig. 3.4: Unfolder implemented with neutral point clamped topology.

magnitude I_m and phase shift ψ

$$\begin{cases} i_a = I_m \cos(\omega t - \psi) \\ i_b = I_m \cos(\omega t - \frac{2\pi}{3} - \psi) \\ i_c = I_m \cos(\omega t + \frac{2\pi}{3} - \psi) \end{cases} \quad (3.4)$$

where ψ determines the power factor as

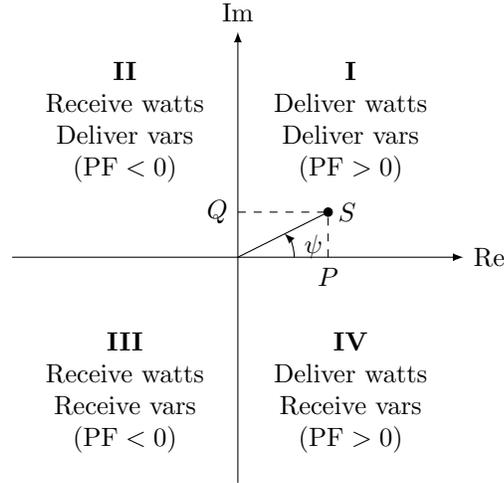
$$\text{PF} = \cos(\psi), \quad -1 \leq \text{PF} \leq 1. \quad (3.5)$$

Positive power factors imply generation of active power or inverter operation, while negative values represent absorption of active power or rectifier operation. Meanings of different power factors are defined from three-phase active power P , reactive power Q and complex power

$$S = P + jQ = \frac{3}{2} V_m I_m e^{j\psi} \quad (3.6)$$

in the PQ plane shown in Fig. 3.5 [67].

The required dc-link currents i_1 and i_2 to produce line currents at any power factor can be derived from Table 3.1. Waveforms of the first current are shown for several power factors in Fig. 3.6. The second current has the same wave shape but phase-shifted by 60° .

Fig. 3.5: PQ plane.

Notice at non-unity power factors, the dc-link currents abruptly reverse at sector beginnings. These current transients occur due to unequal line currents as the unfolded switches between sectors. As a result, the dc-link current variation increases as the power factor deviates from unity. To quantify, define the variation as the peak-to-peak value of each dc-link current,

$$I_{\text{pkpk}} = \max(i_1) - \min(i_1) = \max(i_2) - \min(i_2), \quad (3.7)$$

where it is plotted against power factor in Fig. 3.7a. The minimum variation of $0.5I_m$ occurs at unity power factors, while the maximum of $\sqrt{3}I_m$ occurs at zero power factor. The dc-dc stage is then required to output bidirectional currents containing large variation and fast transients at non-unity power factors. Compared to the large difference between maximum and minimum variations, the peak value of the dc-link currents stays fairly constant,

$$I_{\text{pk}} = \max(|i_1|) = \max(|i_2|), \quad (3.8)$$

where it is also plotted in Fig. 3.7a. As a result, the dc-dc stage shall be capable of outputting current peaks of I_m .

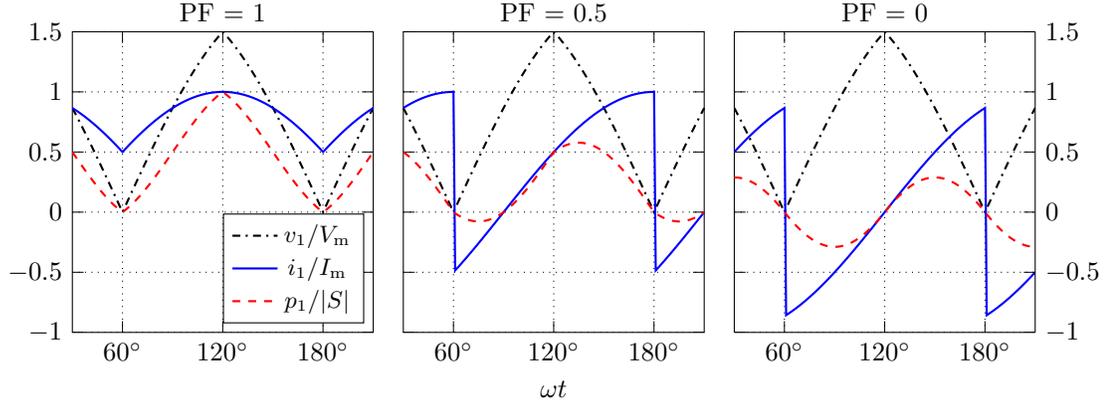


Fig. 3.6: Normalized dc-link voltage, current and power waveforms at various power factors.

Stemming from variations in the dc-link voltage and current, each dc-dc output port processes varying instantaneous power,

$$p_1 = v_1 i_1 \quad \text{and} \quad p_2 = v_2 i_2. \quad (3.9)$$

Waveforms of the first output power are shown for several power factors in Fig. 3.6. Because of momentary reversals in each dc-link current at non-unity power factors, the corresponding output power also at times reverses, even though the power flow to the grid is constant. The power reversals are due to the reactive power being circulated between the two output ports. They are best seen at zero power factor, where one port delivers power, and the other receives the same amount of power. The average output power

$$\bar{P} = \frac{1}{T} \int_0^T p_1 dt = \frac{1}{T} \int_0^T p_2 dt \quad (3.10)$$

is plotted against power factor in Fig. 3.7b. Notice that each dc-dc output port processes on average half the active power regardless of power factor, or $\bar{P} = 0.5P$. The peak output power

$$P_{pk} = \max(|p_1|) = \max(|p_2|) \quad (3.11)$$

is also plotted in Fig. 3.7b. As a result, each output port shall be capable of outputting power peaks of the full apparent power.

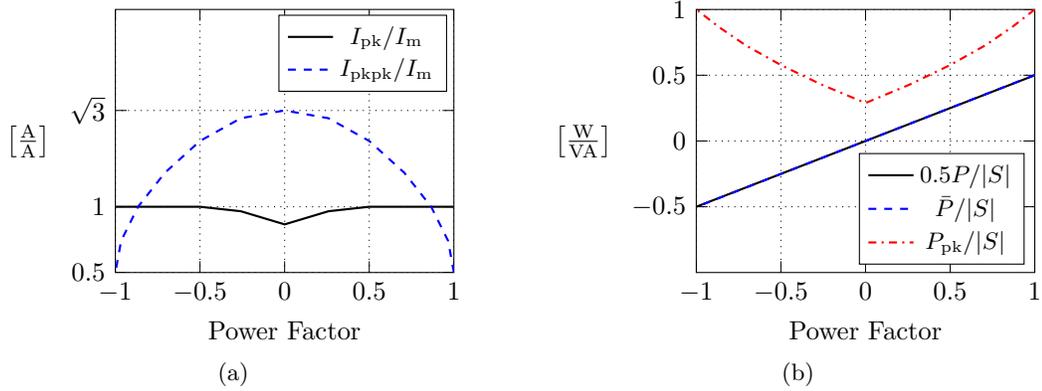


Fig. 3.7: Normalized dc-link quantities versus power factor. (a) Current. (b) Power.

From the above analysis of dc-link voltage, current and power, the following requirements can be summarized on each output port of the dc-dc stage:

- Operate with wide-varying output voltage between zero and $1.5V_m$ or close to the peak line-to-line voltage.
- Deliver I_m or the peak line current at any output voltage within its range.
- Produce fast-changing and bidirectional steps of output current with variations of up to $\sqrt{3}I_m$ at zero output voltage.
- Deliver average and peak powers of half and full values of the three-phase apparent power, respectively.

3.3 DBSRC Operation

Based on requirements identified from the three-phase unfold, an appropriate topology of the dc-dc stage shall be selected. The general topology is a three-port converter with its input port connected to an energy source and its two output ports connected to the unfold. The output ports shall be capable of independent and bidirectional control of currents. The converter shall operate efficiently under wide output voltage variation. Integrated three-port topologies satisfying these requirements are rare in existing literature.

Alternatively, the dc-dc stage can be implemented with two identical two-port converter modules by connecting their inputs in parallel and outputs in series.

Dual-active bridge (DAB) converters support bidirectional power flow and provide galvanic isolation between their primary and secondary circuits. Isolation ensures safe operation of multiple DAB modules connected input-parallel output-series. With the modules connected to the unfolded and the grid, isolation also provides the necessary safety barrier between the energy source and grid.

Various topological variants of the DAB have been compared by Zhao et al. [68]. Compared to non-resonant or resonant transition DAB topologies, the dual-bridge series resonant converter (DBSRC) offers reduced circulating current at non-unity voltage conversion ratios. Compared to other resonant variants, the phase-shift modulated DBSRC offers faster dynamic response. Therefore, the DBSRC topology is considered for the dc-dc stage of the unfolding converter.

The DBSRC power circuit is shown in Fig. 3.8a. Its operation is similar to the DAB, in that phase-shift modulation is used to control power flow. They are different in their tank current profiles, in that the DBSRC tank current is closer to a sinusoid, whereas the DAB tank current transitions are piecewise. Analysis of converter operation is also different. Fundamental approximation is used to analyze the DBSRC, by assuming the fundamental components of the resonant tank voltage and current are dominant. This approximation produces accurate results when the resonant and switching frequencies are close. The convenience of this technique is that linear analysis can be used, where the tank voltages and currents are treated as phasors at the switching frequency.

It is challenging to control the DAB and DBSRC at non-unity conversion ratios, as the circulating tank current can become excessive and degrades efficiency [68]. Compared to single-angle control, multi-angle control reduces the circulating current [54, 69]. Consider in Fig. 3.8b the switching voltage and its fundamental component in each leg. For analysis, each leg operates at a duty ratio of 50%. Actual duty ratio will be less due to dead time. Leg A is chosen as the reference leg, so that three angles (ϕ_{AB} , ϕ_{AD} , ϕ_{DC}) are used

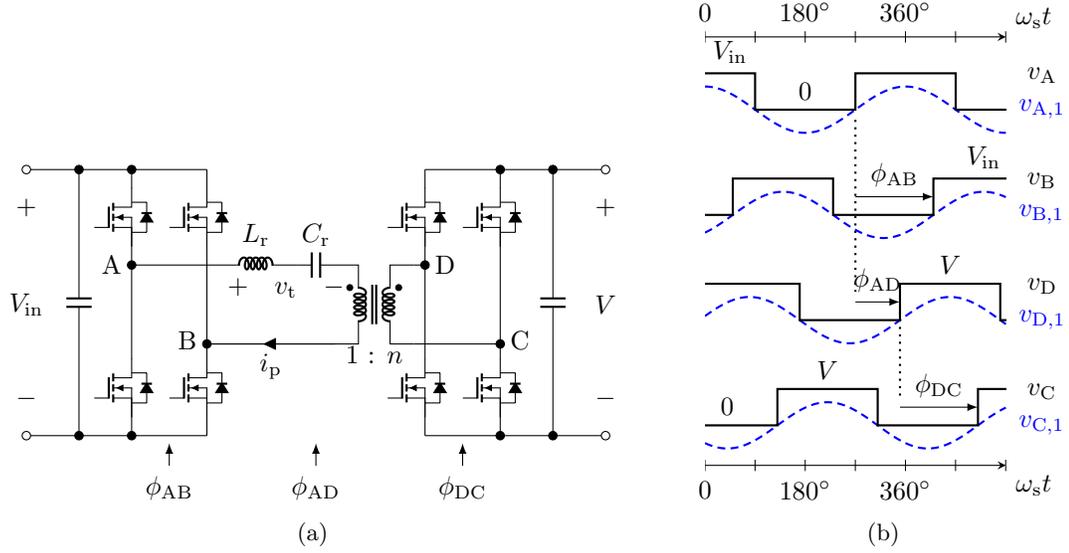


Fig. 3.8: DBSRC. (a) Power circuit. (b) Ideal waveforms.

to control the relative phases of the remaining three legs. The steady-state fundamental switching voltages $v_{X,1}$ and their phasors \mathbf{V}_X are

$$v_{A,1}(t) = \text{Re}\{\mathbf{V}_A e^{j\omega_s t}\}, \quad \text{where} \quad \mathbf{V}_A = \frac{2}{\pi} V_{in} e^{j0}, \quad (3.12)$$

$$v_{B,1}(t) = \text{Re}\{\mathbf{V}_B e^{j\omega_s t}\}, \quad \text{where} \quad \mathbf{V}_B = \frac{2}{\pi} V_{in} e^{j(-\phi_{AB})}, \quad (3.13)$$

$$v_{D,1}(t) = \text{Re}\{\mathbf{V}_D e^{j\omega_s t}\}, \quad \text{where} \quad \mathbf{V}_D = \frac{2}{\pi} V e^{j(-\phi_{AD})}, \quad (3.14)$$

$$v_{C,1}(t) = \text{Re}\{\mathbf{V}_C e^{j\omega_s t}\}, \quad \text{where} \quad \mathbf{V}_C = \frac{2}{\pi} V e^{j(-\phi_{AD}-\phi_{DC})}. \quad (3.15)$$

The range of ϕ_{AD} is between $-\pi$ and π . The ranges of ϕ_{AB} and ϕ_{DC} are both between 0 and 2π . The primary-side differential switching voltage is

$$\mathbf{V}_{AB} = \mathbf{V}_A - \mathbf{V}_B = \frac{4}{\pi} V_{in} \sin\left(\frac{\phi_{AB}}{2}\right) \cdot e^{j\left(\frac{\pi}{2} - \frac{\phi_{AB}}{2}\right)} = |\mathbf{V}_{AB}| \cdot e^{j\phi_1}, \quad (3.16)$$

where ϕ_1 is the phase of \mathbf{V}_{AB} . Similarly, the secondary-side differential switching voltage is

$$\mathbf{V}_{DC} = \mathbf{V}_D - \mathbf{V}_C = \frac{4}{\pi} V \sin\left(\frac{\phi_{DC}}{2}\right) \cdot e^{j\left(\frac{\pi}{2} - \phi_{AD} - \frac{\phi_{DC}}{2}\right)}. \quad (3.17)$$

This voltage is reflected to the transformer primary side as

$$\mathbf{V}_p = \frac{\mathbf{V}_{DC}}{n} = |\mathbf{V}_p| \cdot e^{j\phi_2}, \quad (3.18)$$

where ϕ_2 is the phase of \mathbf{V}_p .

Together, \mathbf{V}_{AB} and \mathbf{V}_p are applied to the resonant tank and result in the equivalent circuit in Fig. 3.9, where the primary-side tank current is

$$\mathbf{I}_p = \frac{\mathbf{V}_t}{Z_t} = \frac{\mathbf{V}_{AB} - \mathbf{V}_p}{Z_t}. \quad (3.19)$$

In this analysis, a lossless tank is assumed and has an impedance of

$$Z_t = jX_t = j \left(\omega_s L_r - \frac{1}{\omega_s C_r} \right). \quad (3.20)$$

To simplify analysis, a change of phase reference to \mathbf{V}_p is applied as

$$\hat{\mathbf{V}}_p = \mathbf{V}_p e^{j(-\phi_2)} = |\mathbf{V}_p| e^{j0}. \quad (3.21)$$

This also modifies \mathbf{V}_{AB} as

$$\hat{\mathbf{V}}_{AB} = \mathbf{V}_{AB} e^{j(-\phi_2)} = |\mathbf{V}_{AB}| e^{j(\phi_1 - \phi_2)} = |\mathbf{V}_{AB}| e^{j\phi}. \quad (3.22)$$

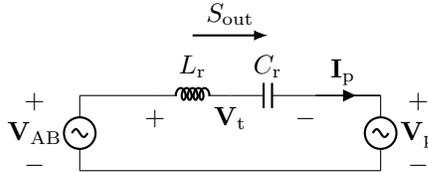


Fig. 3.9: Equivalent tank circuit.

The angle $\phi = \phi_{AD} + \frac{\phi_{DC} - \phi_{AB}}{2}$ represents the phase difference between \mathbf{V}_{AB} and \mathbf{V}_p . The modified tank current is now solved

$$\begin{aligned}\hat{\mathbf{I}}_p &= \frac{\hat{\mathbf{V}}_t}{Z_t} = \frac{\hat{\mathbf{V}}_{AB} - \hat{\mathbf{V}}_p}{Z_t} \\ &= \frac{V_{m1} \sin(\phi)}{X_t} + j \frac{V_{m2} - V_{m1} \cos(\phi)}{X_t} \\ &= \text{Re}\{\hat{\mathbf{I}}_p\} + j\text{Im}\{\hat{\mathbf{I}}_p\}.\end{aligned}\quad (3.23)$$

The tank output power is defined as the complex power received by \mathbf{V}_p ,

$$\begin{aligned}S_{\text{out}} &= \frac{1}{2} \mathbf{V}_p \mathbf{I}_p^* = \frac{1}{2} \hat{\mathbf{V}}_p \hat{\mathbf{I}}_p^* \\ &= \frac{1}{2} |\mathbf{V}_p| \left(\text{Re}\{\hat{\mathbf{I}}_p\} - j\text{Im}\{\hat{\mathbf{I}}_p\} \right) \\ &= \frac{|\mathbf{V}_{AB}| |\mathbf{V}_p| \sin(\phi)}{2X_t} + j \frac{|\mathbf{V}_{AB}| |\mathbf{V}_p| \cos(\phi) - |\mathbf{V}_p|^2}{2X_t} \\ &= P_{\text{out}} + jQ_{\text{out}}.\end{aligned}\quad (3.24)$$

There can be many values of ϕ that all provide the same active power but different reactive power. A modulation strategy minimizes the required tank current at any given active power. This is achieved by minimizing the reactive power, or equivalently minimizing the angle between \mathbf{V}_p and \mathbf{I}_p .

Neglecting converter losses, the active power at the tank output is losslessly transferred to the converter output. From Equation 3.24, the desired output power is obtained by applying the appropriate phase-shift angles

$$\begin{aligned}P_{\text{out}} &= \frac{8}{\pi^2} \frac{V_{\text{in}} V}{n X_t} \cdot \sin\left(\frac{\phi_{AB}}{2}\right) \sin\left(\frac{\phi_{DC}}{2}\right) \sin\left(\phi_{AD} + \frac{\phi_{DC} - \phi_{AB}}{2}\right) \\ &= P_{\text{max}} \cdot U,\end{aligned}\quad (3.25)$$

where P_{max} represents the maximum output power, and U is an applied power command with values between ± 1 . The power command expression hints at ways to obtain the desired power through adjustment of the control angles. Consider first setting $\phi_{AB} = \phi_{DC} = \pi$ to

provide maximum magnitudes on \mathbf{V}_{AB} and \mathbf{V}_{DC} . The maximum powers $\pm P_{\max}$ are then obtained at $\phi_{AD} = \pm \frac{\pi}{2}$. Zero power is obtained at $\phi_{AD} = 0$. Any intermediate power is obtained by controlling ϕ_{AD} on the α trajectory,

$$\begin{bmatrix} \phi_{AB} \\ \phi_{AD} \\ \phi_{DC} \end{bmatrix} = \begin{bmatrix} \phi_{AB,\alpha} \\ \phi_{AD,\alpha} \\ \phi_{DC,\alpha} \end{bmatrix} = \begin{bmatrix} \pi \\ \arcsin(U) \\ \pi \end{bmatrix}. \quad (3.26)$$

Although the DBSRC can be controlled using just a single angle ϕ_{AD} , doing so generates excessive circulating current, especially when the conversion ratio M deviates from unity, where

$$M = \frac{V}{nV_{\text{in}}}. \quad (3.27)$$

Wide-range operation is required when the DBSRC is used with the unfolders. The circulating current is minimized by simultaneously modulating three angles (ϕ_{AB} , ϕ_{AD} , ϕ_{DC}) based on values of both U and M . They consist of trajectories γ_{\pm} , λ_{\pm} and the previously provided α ,

$$\begin{bmatrix} \phi_{AB,\gamma_{\pm}} \\ \phi_{AD,\gamma_{\pm}} \\ \phi_{DC,\gamma_{\pm}} \end{bmatrix} = \begin{bmatrix} \pi \pm \pi \mp 2 \arcsin(\sqrt{M^2 + U^2}) \\ \frac{\phi_{AB,\gamma_{\pm}}}{2} + \arctan\left(\frac{U}{M}\right) - \frac{\pi}{2} \\ \pi \end{bmatrix}, \quad (3.28)$$

$$\begin{bmatrix} \phi_{AB,\lambda_{\pm}} \\ \phi_{AD,\lambda_{\pm}} \\ \phi_{DC,\lambda_{\pm}} \end{bmatrix} = \begin{bmatrix} \pi \\ -\frac{\phi_{DC,\lambda_{\pm}}}{2} + \arctan(UM) + \frac{\pi}{2} \\ \pi \pm \pi \mp 2 \arcsin\left(\sqrt{\frac{1}{M^2} + U^2}\right) \end{bmatrix}. \quad (3.29)$$

Together, they make up the family of minimum current trajectories (MCT) [69],

$$\begin{bmatrix} \phi_{AB} \\ \phi_{AD} \\ \phi_{DC} \end{bmatrix} = \begin{cases} \begin{bmatrix} \phi_{AB,\gamma\pm} & \phi_{AD,\gamma\pm} & \phi_{DC,\gamma\pm} \end{bmatrix}^\top, & \text{if } M < 1 \text{ and } |U| < \sqrt{1 - M^2}; \\ \begin{bmatrix} \phi_{AB,\alpha} & \phi_{AD,\alpha} & \phi_{DC,\alpha} \end{bmatrix}^\top, & \text{if } M < 1 \text{ and } |U| \geq \sqrt{1 - M^2}; \\ \begin{bmatrix} \phi_{AB,\lambda\pm} & \phi_{AD,\lambda\pm} & \phi_{DC,\lambda\pm} \end{bmatrix}^\top, & \text{if } M \geq 1 \text{ and } |U| < \sqrt{1 - \frac{1}{M^2}}; \\ \begin{bmatrix} \phi_{AB,\alpha} & \phi_{AD,\alpha} & \phi_{DC,\alpha} \end{bmatrix}^\top, & \text{if } M \geq 1 \text{ and } |U| \geq \sqrt{1 - \frac{1}{M^2}}. \end{cases} \quad (3.30)$$

These trajectories are visualized at two exemplary conversion ratios in Fig. 3.10. The detailed derivation of these trajectories has been provided by Corradini et al. [69].

The maximum DBSRC output power is limited by its resonant tank design and varies with the input and output voltages. In applications where a constant power characteristic is desired, the DBSRC may be replaced with the bidirectional zero voltage switching (ZVS) full-bridge dc-dc converter [70], whose maximum power is not limited by topology.

3.4 DBSRC-Unfolding Converter

The three-phase unfolding converter is constructed by connecting two identical DBSRC modules to the unfolder. As shown in Fig. 3.11, the two modules are connected input-parallel to a dc source and output-series to the dc link. Each module is phase-shift modulated using the MCT algorithm. Inputs of each modulator include the power command and the sensed input and dc-link voltages for computing the conversion ratio. The generation of phase-shift angles can be implemented using different approaches. One approach computes the angles on-line by directly applying the algorithm [71]. Another approach performs computations off-line and selects the appropriate angles using a look-up table. The second approach is preferred for flexibility in tuning and adaptability to other algorithms.

Besides modulating all three angles using MCT, the DBSRC can also be modulated using just a single angle. This earlier method does not require voltage sensing and uses only the α trajectory to modulate ϕ_{AD} , while keeping ϕ_{AB} and ϕ_{DC} at 180° . This method works well for a narrow range of operation around $M = 1$ but may generate excessive circulating

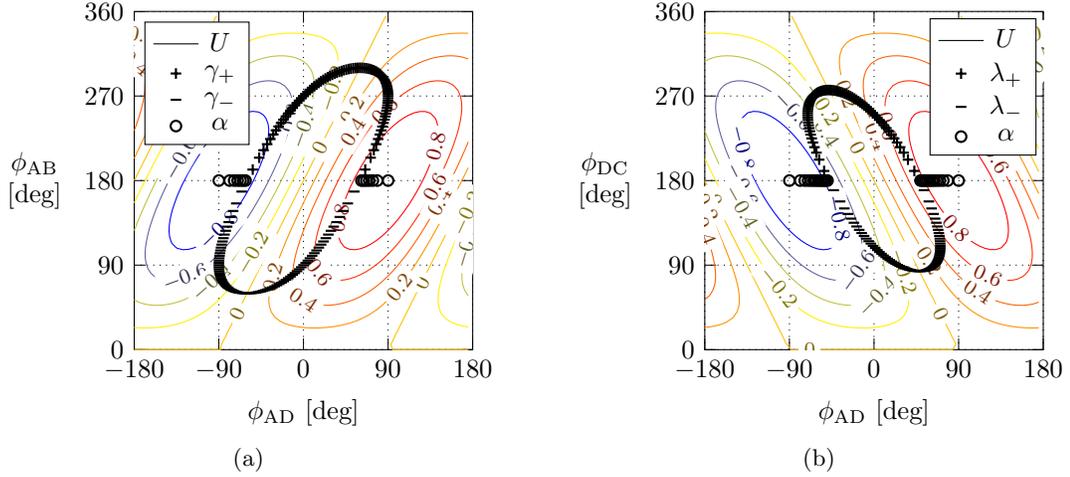


Fig. 3.10: DBSRC minimum current trajectories. (a) At $M = 0.5$. (b) At $M = 1.5$.

current in the resonant tank in wide range operation. To quantify the advantage of MCT modulation, it is compared with the single-angle modulation in the unfolding converter. Both methods are applied to an example DBSRC design. The transformer turns ratio is selected to operate at conversion ratios between zero and one. The tank inductance and capacitance are designed to operate at command values between 0.4 and 0.8 at rated power and unity power factor.

The trajectories of the conversion ratio M_1 and power command u_1 of the first DBSRC module are derived from its dc-link voltage and current and are shown in Fig. 3.12. The second module operates similarly and is omitted in this analysis. Also shown are two sets of tank phasors at three operating points on the trajectories, as identified by the phase angle. These points correspond to operations at low, medium and high values of M_1 and u_1 . At low values, operating on the α trajectory cannot adjust \mathbf{V}_{AB} and thus applies a larger-than-necessary tank voltage \mathbf{V}_t . This results in a large reactive component of \mathbf{I}_t . In contrast, operating on γ trajectory adjusts \mathbf{V}_{AB} and \mathbf{V}_t to eliminate the reactive component, resulting in 50% reduction in tank current magnitude at this point. At medium values, the amount of reduction is smaller at 20%, as the required \mathbf{V}_{AB} and \mathbf{V}_t magnitudes become larger in order to produce a larger \mathbf{I}_t due to increase in power. At high values, the MCT algorithm selects the α trajectory.

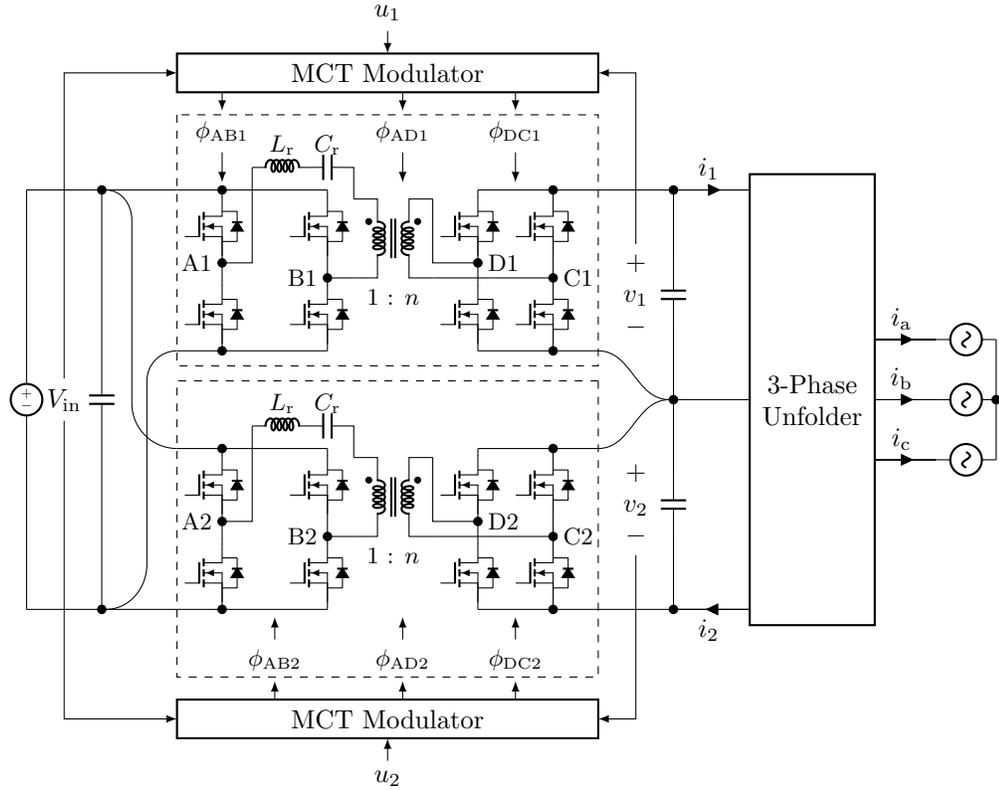


Fig. 3.11: MCT-modulated DBSRC modules with unfolders.

Since each module spends a majority of time at low to medium M and u values, the MCT modulation shall also reduce the overall tank current. This can be verified by comparing the tank rms currents over a line period,

$$I_{p,rms,line} = \sqrt{\frac{1}{T} \int_0^T i_p^2(t) dt} \approx \sqrt{\frac{1}{T} \int_0^T i_{p,rms}^2(t) dt}, \quad (3.31)$$

where $i_{p,rms}$ is the moving rms of the tank current over each switching period [72]. In the analysis conducted in Matlab, $i_{p,rms}$ is found for every point over a line period, using the phasor formula based on fundamental approximation. Then, the mean of all values of $i_{p,rms}^2$ is found, and its square root is taken to obtain $I_{p,rms,line}$. In the considered DBSRC design operating between $0 \leq M \leq 1$ and $0.4 \leq u \leq 0.8$, $I_{p,rms,line}$ is reduced by 25% using MCT over single-angle modulation. Similar amount of reduction is expected in most other designs used in the unfolding converter, as the conversion ratio drops to zero every 120° .

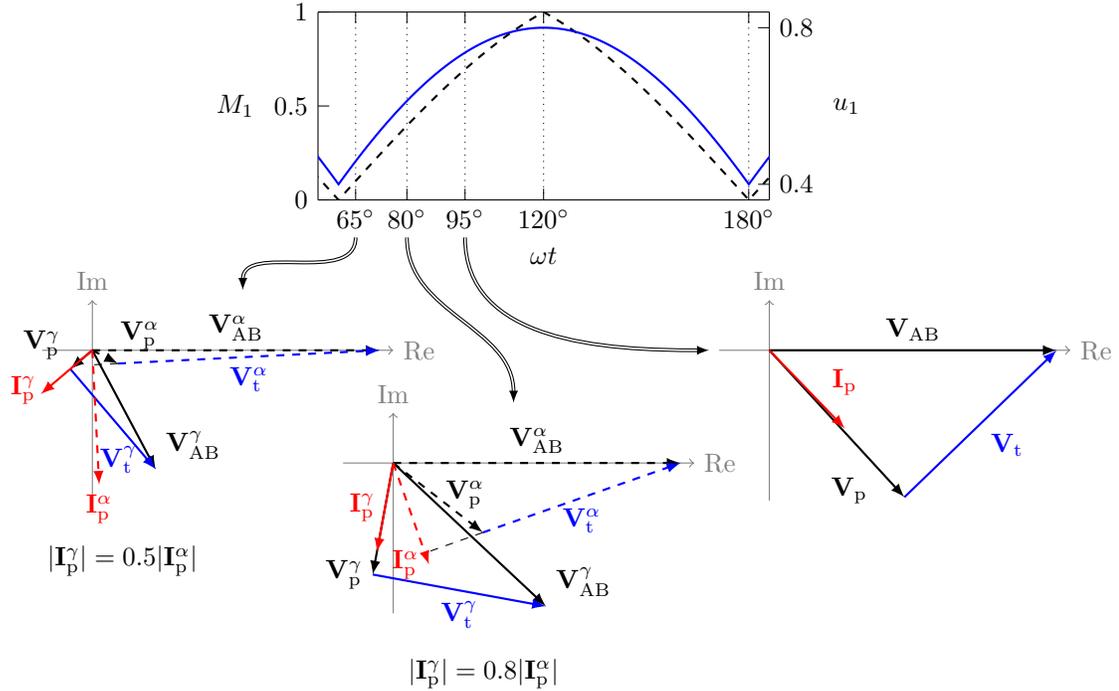


Fig. 3.12: Comparison of tank phasors of the first DBSRC module in an unfolding converter operating at unity power factor. \mathbf{X}^γ and \mathbf{X}^α represent phasors from using γ and α trajectories, respectively.

Based on the reduction in rms tank current and consequently the conduction loss using MCT, it is chosen as the preferred modulation scheme for analysis and implementation in subsequent chapters. A drawback of MCT is the neglect of switching loss. As a result, the DBSRC switches have limited ZVS ranges. The switching loss can be reduced by modulating the DBSRC on a ZVS trajectory [73], at the expense of slightly increased rms tank current and conduction loss. Alternatively, the ZVS range can be extended by adding and phase-shifting an auxiliary half-bridge leg to each main DBSRC leg [74], while retaining MCT and its benefits. This is the ZVS approach adopted in subsequent experimental setup. A fixed auxiliary-to-main phase-shift angle is used for simplicity, although it can be varied depending on converter operating point to further optimize ZVS.

3.5 Summary

This chapter introduces the topology and operation of the three-phase unfolding converter. The grid-interfacing stage is a line-frequency unfolding inverter (unfolder). Its invention is inspired by high power factor rectifier topologies, specifically the third-harmonic current injection rectifier. The unfolders are controlled using a switching sequence generated based on sectors of the grid voltages. This line-frequency switching generates negligible switching loss and minimal current harmonics. However, the unfolded is not able to actively control the line currents. Instead, they are shaped by the dc-dc stage. The power and dynamic requirements of the dc-dc stage are obtained by analyzing the unfolded dc-link voltages, currents and powers at all power factors. Two dual-bridge series resonant converter (DBSRC) modules are selected for the dc-dc stage for their power-bidirectional capability and high-frequency isolation between the dc source and ac grid. Fundamental approximation and phasor analysis are reviewed to derive the tank current and output power based on the applied phase-shift angles. A three-angle modulation technique based on minimum current trajectories (MCT) is reviewed and used to minimize the tank current at any given output power. The MCT technique is compared with single-angle modulation in the DBSRC-unfolding converter to highlight the reduction in rms tank current.

CHAPTER 4

UNFOLDING CONVERTER DESIGN AND COMPARISON

Chapter 3 reveals that each DBSRC module in the unfolding converter works over a wide range of operating points, due to periodic variations in its dc-link voltage and current. These variations complicate the design of DBSRC power components, as their rms currents need to be evaluated over a line period and may vary with power factor. The design procedure can be simplified by introducing two design parameters, which are peak conversion ratio and peak power command. The variations in rms currents are evaluated for different values of design parameters and power factor. It turns out that the rms currents can be minimized by optimizing the design parameters.

The resonant current in the DBSRC tank contributes to line current harmonics and necessitates filtering by the line inductors and dc-link capacitors. Formulas are provided to estimate the harmonic magnitudes and to design the required line filter.

The passive and filter components are then designed for a 10-kVA unfolding converter, using the obtained design guidelines. This chapter concludes with a comparison of physical component sizes between the unfolding converter and a conventional DAB-VSI converter. The advantages of the unfolding converter are highlighted in terms of significant reduction of line filter and dc-link capacitor volumes, leading to an overall reduction in passive volume.

4.1 DBSRC Design for Unfolding Converter

Consider now the design of each DBSRC module in a three-phase unfolding converter, as shown in Fig. 4.1. Each module is modulated with control angles generated from MCT. Compared with a DBSRC designed for dc operation, its design for use in the unfolding converter requires special considerations, due to periodic variations in its output voltage and power.

In a 10-kVA unfolding converter, each DBSRC shall be designed to output average

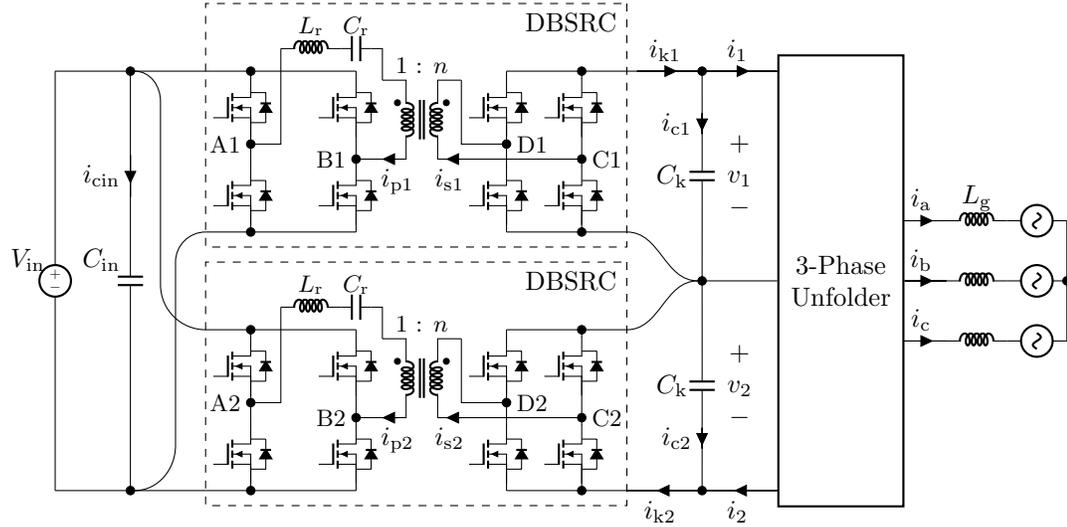


Fig. 4.1: Circuit diagram of grid-tied DBSRC-unfolding converter.

and peak powers of 5 and 10 kW, respectively. Its design specifications are summarized in Table 4.1. The nominal voltage and power ratings are same as those in the conventional DAB-VSI converter from Chapter 2.

The transformer turns ratio n is the first component parameter to be determined. A more general way to select n is to first express it in terms of the peak conversion ratio M_{pk} , which occurs at the peak output voltage V_{pk} ,

$$n = \frac{V_{pk}}{M_{pk} V_{in}}. \quad (4.1)$$

Thus, the selection of n becomes the selection of M_{pk} . It will become clear in subsequent analysis that M_{pk} has a significant impact on the tank current.

Once n has been determined, the tank reactance X_t can be found. From the previous steady-state DBSRC analysis, the tank reactance determines the maximum power of the DBSRC. Consider the maximum available power $P_{max,pk}$ from the resonant tank at the peak output voltage,

$$P_{max,pk} = \frac{8}{\pi^2} \frac{V_{in} V_{pk}}{n X_t} = \frac{P_{out,pk}}{U_{pk}} = \frac{|S|}{U_{pk}}. \quad (4.2)$$

Here, the tank is assumed to be lossless. The peak output power $P_{out,pk}$ of each module

Table 4.1: 10-kVA DBSRC-unfolding converter design specifications

Parameter	Value
Nominal DC Input Voltage	300 V
Nominal AC Line-to-Line Voltage	480 V rms
Nominal Three-Phase Power	10 kVA
Magnetics K_u	40%
Magnetics ΔT_{\max}	40 °C
DBSRC f_s	50 kHz
DBSRC M_{pk}	1
DBSRC U_{pk}	0.8
DBSRC r_0	0.6

is set equal to the nominal three-phase apparent power. This is the highest amount of instantaneous power that each module will process at nominal ratings. Operating at non-unity power factors will reduce the peak power. To aid the selection of X_t , the peak power command U_{pk} needs to be specified. This is the designed and expected value when each module operates at peak output voltage and power. It is necessary to set U_{pk} less than one. Reducing U_{pk} reduces X_t and will provide more power to handle overload conditions.

Thus far, two design parameters, M_{pk} and U_{pk} , have been identified to produce the transformer turns ratio n and the tank reactance X_t . The selection of these two parameters have consequences on component stresses. It is important to study how these stresses change with the parameter values. In addition, the stresses will have to be analyzed over a line period. The primary-side rms tank current over a line period is

$$I_{\text{p,rms,line}} = \sqrt{\frac{1}{T} \int_0^T i_{\text{p}}^2(t) dt} \approx \sqrt{\frac{1}{T} \int_0^T i_{\text{p,rms}}^2(t) dt}, \quad (4.3)$$

where $i_{\text{p,rms}}$ is the moving rms of the tank current over each switching period [72]. In the analysis conducted in Matlab, $i_{\text{p,rms}}$ is found for every point over a line period, using the phasor formula based on fundamental approximation. Then, the mean of all values of $i_{\text{p,rms}}^2$ is found, and its square root is taken to obtain $I_{\text{p,rms,line}}$. To illustrate, $i_{\text{p,rms}}$ is solved for

a design with $M_{pk} = 1$ and $U_{pk} = 0.8$ and is plotted over a line period in Fig. 4.2 at unity power factor. The simulation result is also shown for comparison.

In the converter design, the components shall be selected based on the worst-case operating condition. In the case of the rms tank current, the operating condition that produces its highest value needs to be found. At a given power factor, the use of MCT ensures that the tank current scales linearly with the line current. Thus, the highest tank current is expected at the full nominal power. The question that remains is how the current changes with power factor. The relationship is visualized in Fig. 4.3, where the line rms values of tank currents in both modules are obtained in both analysis and simulation. Notice that the worst-case tank current occurs at unity power factors. This worst-case current has been previously considered in Fig. 4.2.

Note that $I_{p,rms,line}$ will change depending on the selections of M_{pk} and U_{pk} . Their selections also affect the secondary-side tank current

$$I_{s,rms,line} = \frac{I_{p,rms,line}}{n}. \quad (4.4)$$

Both $I_{p,rms,line}$ and $I_{s,rms,line}$ are solved for a variety of M_{pk} and U_{pk} values at unity power factor. To remove their dependencies on the operating voltages, these rms values are normalized to the average input and rms line currents and are plotted in Fig. 4.4. Three U_{pk}

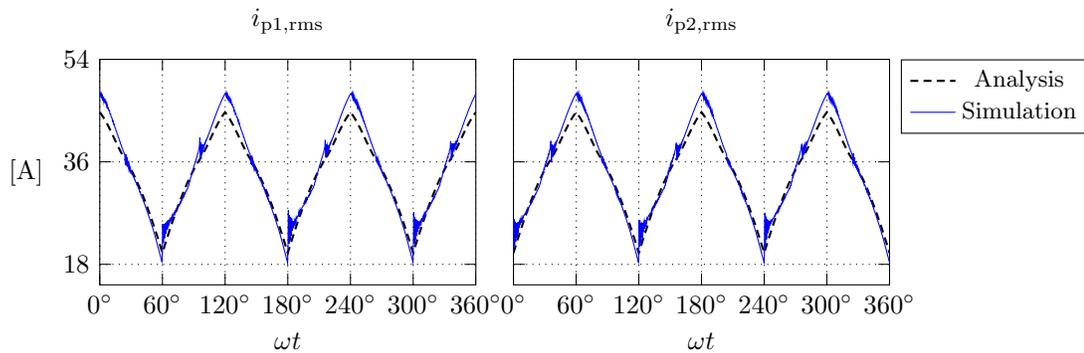


Fig. 4.2: Moving rms values of primary tank currents, $i_{p1,rms}$ and $i_{p2,rms}$, of each DBSRC module in an unfolding converter designed with $M_{pk} = 1$ and $U_{pk} = 0.8$ and operating at unity power factor.

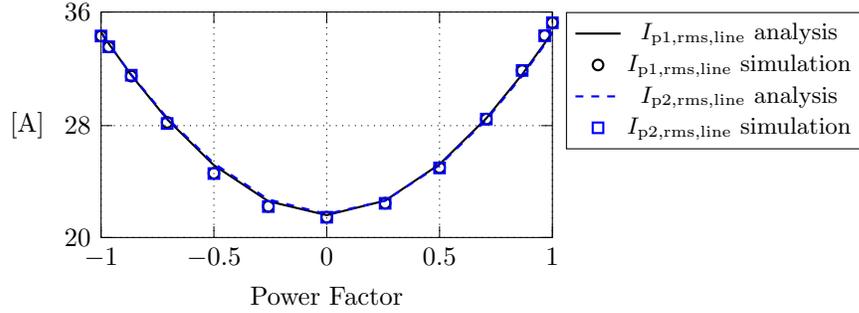


Fig. 4.3: Line rms values of primary tank currents, $I_{p1,rms,line}$ and $I_{p2,rms,line}$, plotted against power factor in an unfolding converter designed with $M_{pk} = 1$ and $U_{pk} = 0.8$.

values of 0.4, 0.6 and 0.8 are studied. The simulation results are also plotted to verify analysis. Notice that the dependency on U_{pk} is weak. Decreasing M_{pk} below one significantly increases $I_{p,rms,line}$ but has little influence on $I_{s,rms,line}$. On the other hand, increasing M_{pk} above two increases $I_{s,rms,line}$ but has little effect on $I_{p,rms,line}$. The increase in rms currents is due to increase in circulating currents on either side of the transformer, as its turns ratio is changed. In summary, the tank currents are minimized by choosing M_{pk} within an optimal range between one and two.

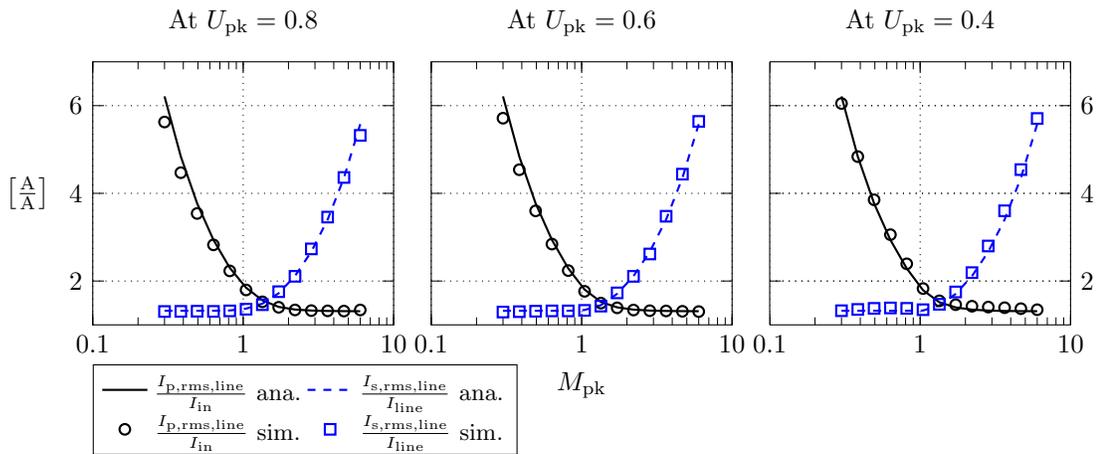


Fig. 4.4: Primary and secondary rms tank currents, $I_{p,rms,line}$ and $I_{s,rms,line}$, normalized respectively to input and line currents, I_{in} and I_{line} , and plotted against M_{pk} at various U_{pk} values, all at unity power factor.

4.2 Component RMS Currents

Following selections of M_{pk} and U_{pk} , the active and passive components can be designed based on converter specifications. They include the eight active switches in each DBSRC and passive components including the tank inductor, tank capacitor, transformer, input capacitor and dc-link capacitor. The design and selection of all of these components require knowledge of their rms currents over a line period. The dependencies of primary and secondary tank currents on power factor and M_{pk} and U_{pk} values have already been plotted in Figs. 4.3 and 4.4.

The line rms currents in the remaining components, namely the primary and secondary switches and the input and dc-link capacitors, are solved similarly as the tank currents, both analytically in Matlab and from simulation in Simulink/PLECS. Since these currents are usually found after the tank currents, their solutions are presented as normalized values to either the primary or secondary tank current, depending on where the component is located. They are solved for a variety of power factors, M_{pk} and U_{pk} values to determine a worst-case condition. The solution's dependency on power factor is analyzed using a design with $M_{pk} = 1$ and $U_{pk} = 0.8$. The dependency on design parameters M_{pk} and U_{pk} is analyzed at PF = 1.

The normalized rms primary and secondary switch currents, $\frac{I_{ps,rms,line}}{I_{p,rms,line}}$ and $\frac{I_{ss,rms,line}}{I_{s,rms,line}}$, are plotted in Fig. 4.5. From the analytical results, each switch carries about 70%, or $\frac{\sqrt{2}}{2}$ times, its corresponding tank current, regardless of power factor, tank design or transformer turns ratio. This is because each switch always conducts at close to 50% duty ratio. The analytical results are confirmed in simulation, with negligible discrepancy between the two.

The rms input capacitor current is normalized to the primary tank current, and the result $\frac{I_{cin,rms,line}}{I_{p,rms,line}}$ is plotted in Fig. 4.6. The input capacitor is shared between the parallel DBSRC inputs and shunts the input ripple current originating from the primary tank currents. Thus, $I_{cin,rms,line}$ is contributed by both DBSRC modules. This capacitor carries about 110% of each primary tank current in the worst case at PF = -1, $M_{pk} = 1$ and $U_{pk} = 0.8$.

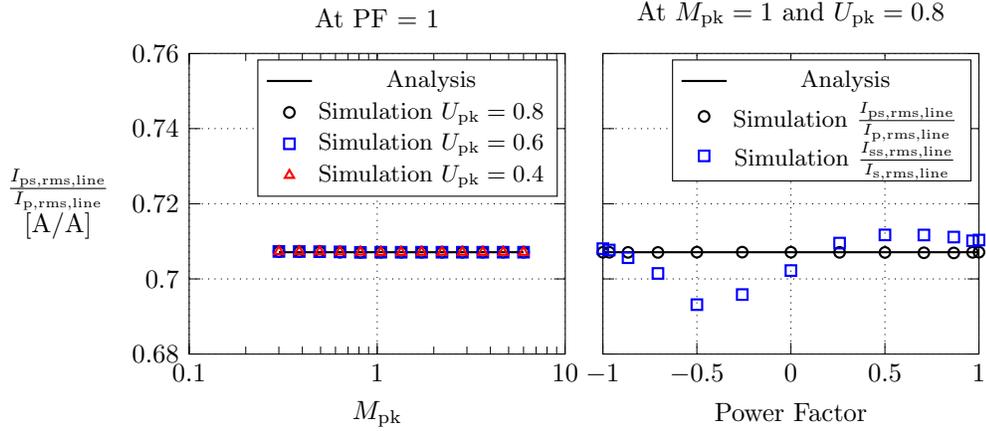


Fig. 4.5: Primary and secondary switch currents, $I_{ps,rms,line}$ and $I_{ss,rms,line}$, normalized to their respective tank currents, $I_{p,rms,line}$ and $I_{s,rms,line}$, and plotted against M_{pk} and U_{pk} and against power factor.

The rms dc-link capacitor current is normalized to the secondary tank current, and the result $\frac{I_{ck,rms,line}}{I_{s,rms,line}}$ is plotted in Fig. 4.7. $I_{ck,rms,line}$ is the same in both capacitors. Each dc-link capacitor shunts the output ripple current originating from each secondary tank current. It carries at most 70% of the secondary tank current and occurs at PF = 1, $M_{pk} = 1.5$ and $U_{pk} = 0.8$.

Based on the analysis and simulation results, the worst-case line rms currents in the converter components are summarized in Table 4.2. Also shown are their values in terms of the average input and rms line currents in an example design with $M_{pk} = 1$ and $U_{pk} = 0.8$ operating at unity power factor.

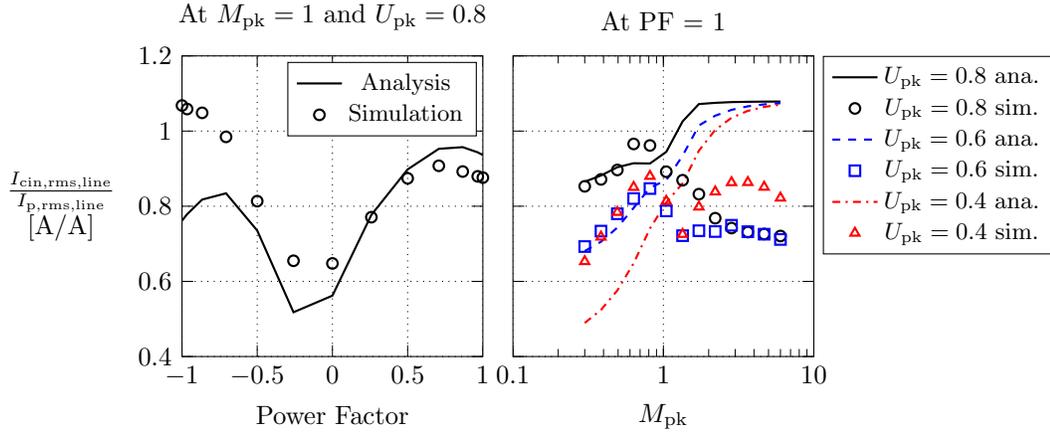


Fig. 4.6: Input capacitor current $I_{cin,rms,line}$ normalized to primary tank current $I_{p,rms,line}$ and plotted against power factor and against M_{pk} and U_{pk} .

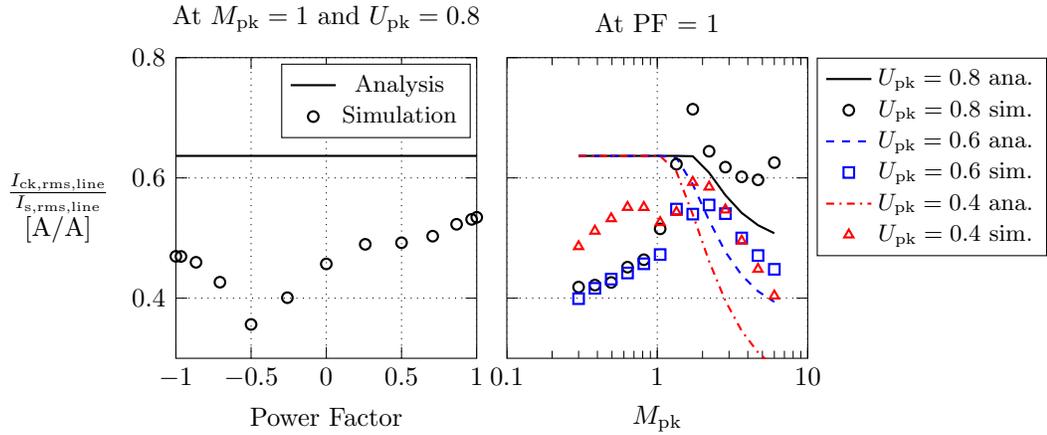


Fig. 4.7: DC-link capacitor current $I_{ck,rms,line}$ normalized to secondary tank current $I_{s,rms,line}$ and plotted against power factor and against M_{pk} and U_{pk} .

Table 4.2: Component rms currents over a line period, in worst cases and in an example design with $M_{pk} = 1$, $U_{pk} = 0.8$ and operating at unity power factor. Results are presented in terms of the converter's average input current I_{in} or rms line current I_{line} , depending on component location.

Component	Worst Case	Example Design
Primary Tank ($I_{p,rms,line}$)	-	$2I_{in}$
Secondary Tank ($I_{s,rms,line}$)	-	$1.4I_{line}$
Primary Switch ($I_{ps,rms,line}$)	$0.7I_{p,rms,line}$	$1.4I_{in}$
Secondary Switch ($I_{ss,rms,line}$)	$0.7I_{s,rms,line}$	I_{line}
Input Capacitor ($I_{cin,rms,line}$)	$1.1I_{p,rms,line}$	$2.2I_{in}$
DC-Link Capacitor ($I_{ck,rms,line}$)	$0.7I_{s,rms,line}$	I_{line}

4.3 Example 10-kVA Unfolding Converter Design

Having identified guidelines on design parameter selection and component rms currents, a physical design of the 10-kVA DBSRC-unfolding converter previously specified in Table 4.1 is carried out in this section. Its nominal voltage and power ratings are same as those in the conventional DAB-VSI converter from Chapter 2. The design focuses on obtaining physical sizes of passive components to facilitate a comparison with the conventional converter. Thus, the same magnetic design constraints are also used to ensure a fair comparison.

Each DBSRC is designed to output average and peak powers of 5 and 10 kW, respectively. Its tank design starts with selection of parameters M_{pk} and U_{pk} . M_{pk} is set to one, which falls within its optimal range as previously concluded. The selected M_{pk} along with nominal ratings determine the transformer turns ratio from Equation 4.1

$$n = \frac{V_{pk}}{M_{pk}V_{in}} = \frac{\frac{\sqrt{6}}{2} \times 480}{1 \times 300} \approx 2. \quad (4.5)$$

U_{pk} can be selected to provide the maximum required power at the minimum input and line voltages. In absence of these specifications, U_{pk} is set to 0.8 at the nominal ratings. The selected U_{pk} determines the tank reactance from Equation 4.2,

$$X_t = \frac{8 V_{in} V_{pk} U_{pk}}{\pi^2 |S|} = \frac{8 \times 300 \times \frac{\sqrt{6}}{2} \times 480 \times 0.8}{\pi^2 \times 10000} \Omega \approx 5.8 \Omega. \quad (4.6)$$

The switching frequency is selected as 50 kHz, which has been reported in a DBSRC designed at similar ratings using IGBTs [75]. To solve for the tank inductance and capacitance values, the ratio r_0 of resonant to switching frequency needs to be specified

$$r_0 = \frac{1}{\sqrt{L_r C_r} 2\pi f_s}. \quad (4.7)$$

In this design, r_0 is set to 0.6, to produce an inductive tank. This value of r_0 along with the tank reactance produce tank inductance and capacitance values of 29 μH and 1 μF , respectively. The rms primary and secondary tank currents over a line period are 32 and

16 A, respectively.

4.3.1 Tank Inductor

With the tank inductance and current determined, the physical design of the tank inductor can proceed. The design goal is to minimize the inductor core volume, while satisfying the temperature rise constraint in Table 4.1. Therefore, the inductor losses need to be kept in check. Only the core and dc copper losses are considered, while the high-frequency ac copper losses due to skin and proximity effects are neglected. At a given volume, the thermal resistance can be reduced by increasing the surface area. A popular approach is to use multiple smaller cores for the tank inductor [17, 76]. The same approach is adopted in this design, where multiple identical smaller inductors are used in series to make up the tank inductor. The tank inductance L_r is split into smaller inductances \hat{L}_r , where

$$L_r = N_L \hat{L}_r, \quad (4.8)$$

and N_L is the number of split inductors used.

The core loss in each split inductor is strongly dependent on its peak flux density. Since the envelop of the tank current varies at the third-harmonic line frequency, so will the peak flux density. The instantaneous peak flux density in each inductor is

$$B_{\text{pk}} = \frac{\hat{L}_r I_{\text{p,pk}}}{A_c N_t}, \quad (4.9)$$

where $I_{\text{p,pk}}$ is the envelop or instantaneous peak value of the primary-side tank current, A_c is the core cross-sectional area, and N_t is the number of turns in each inductor. Selection of appropriate N_t limits the maximum peak flux density $B_{\text{pk,max}}$ and avoids core saturation,

$$B_{\text{pk,max}} = \frac{\hat{L}_r I_{\text{p,pk,max}}}{A_c N_t}. \quad (4.10)$$

An air gap is needed in a ferrite core to produce the required inductance. The necessary gap length in each inductor is

$$l_g = \frac{\mu_0 A_c N_t^2}{\hat{L}_r}. \quad (4.11)$$

Large gap lengths shall be avoided to prevent excessive high-frequency copper loss due to fringe field in the gap. The instantaneous core loss is calculated from a curve-fit equation, in the form of Steinmetz's equation, as provided by the ferrite core manufacturer [77]

$$p_{fe} = a f_s^c B_{pk}^d, \quad (4.12)$$

where a , c and d are curve-fit parameters for a specific ferrite material as provided by the manufacturer. The average core loss over a line period is

$$P_{fe} = \frac{1}{T} \int_0^T p_{fe} dt. \quad (4.13)$$

The copper loss is dependent on the adopted winding design. A multi-strand copper wire approach is used. The cross-sectional area of each wire strand is determined from the effective window area

$$A_w = \frac{K_u W_a}{N_t N_w}, \quad (4.14)$$

where W_a is the core window area, K_u is the window fill factor, and N_w is the number of wire strands used for each turn. The copper resistance is

$$R_L = \frac{\rho N_t l_t}{A_w N_w}, \quad (4.15)$$

where ρ is the copper resistivity, and l_t is the mean-length-per-turn of the core geometry. The low-frequency copper loss is

$$P_{cu} = I_{p,rms,line}^2 R_L. \quad (4.16)$$

Neglecting high-frequency losses due to skin and proximity effects, the total loss in each split inductor is

$$P_{\hat{L}} = P_{\text{fe}} + P_{\text{cu}}. \quad (4.17)$$

The temperature rise of each inductor can be estimated from its thermal resistance based on the core volume, using a manufacturer curve-fit formula that assumes natural convection as cooling method [78]

$$R_{\text{th}} = 53V_{\text{c}}^{-0.53}, \quad (4.18)$$

where V_{c} is the core volume. The estimated temperature rise is

$$\Delta T = R_{\text{th}}P_{\hat{L}}. \quad (4.19)$$

The completed design for the 29 μH tank inductor uses four split inductors ($N_L = 4$). Each uses the E42/21/20 core and Magnetics P material. Each has an air gap length of 4 mm. Each has 10 turns, with each turn wound using 8 strands of 16 AWG copper wire. This produces a window fill factor of 40%. The estimated core and copper loss of each inductor are 2.1 and 1.6 W, respectively. The estimated temperature rise of each inductor is 37 °C.

4.3.2 Transformer

The transformer is designed using a similar procedure as the tank inductor. It also uses a split core approach. The transformer is implemented with N_T number of smaller transformers with their primary windings connected in series and their secondary windings connected in parallel. The core flux density can be found from either its primary or secondary voltage. Using the secondary voltage is more straightforward, as it is just equal to the secondary-side differential switching voltage $v_{\text{DC}}(t)$

$$v_{\text{DC}}(t) = N_s A_c \frac{dB}{dt} \quad (4.20)$$

Using the fundamental approximation on $v_{\text{DC}}(t)$ to solve for $B(t)$ results in

$$B(t) \approx \frac{|\mathbf{V}_{\text{DC}}|}{N_s A_c \omega_s} \sin(\omega_s t + \angle \mathbf{V}_{\text{DC}}). \quad (4.21)$$

The instantaneous peak flux density is

$$B_{\text{pk}} = \frac{|\mathbf{V}_{\text{DC}}|}{N_s A_c \omega_s} = \frac{\frac{4}{\pi} V \sin\left(\frac{\phi_{\text{DC}}}{2}\right)}{N_s A_c \omega_s}. \quad (4.22)$$

The maximum value of the peak flux density shall be limited to avoid core saturation. The instantaneous and average core losses can be solved from B_{pk} using Equations 4.12 and 4.13. The number of secondary turns N_s is selected to obtain a reasonable core loss. The number of primary turns N_p is then found,

$$N_p = \frac{N_s}{n N_T}. \quad (4.23)$$

Care must be taken on turns selection, as using more turns reduces core loss but increases copper loss.

The wire sizing requires knowledge on how to allocate the available window size. For this two-winding transformer, evenly splitting the window to primary and secondary windings minimizes the overall copper loss [72], or $K_{u,p} = K_{u,s} = 0.5K_u$. The primary and secondary copper resistances (R_p and R_s) can then be determined from Equations 4.14 and 4.15. The primary-side copper loss is

$$P_{\text{cu,p}} = I_{\text{p,rms,line}}^2 R_p. \quad (4.24)$$

The secondary-side copper loss is

$$P_{\text{cu,s}} = \left(\frac{I_{\text{s,rms,line}}}{N_T} \right)^2 R_s. \quad (4.25)$$

Neglecting high-frequency losses due to skin and proximity effects, the total loss in each split transformer is

$$P_T = P_{fe} + P_{cu,p} + P_{cu,s}. \quad (4.26)$$

The temperature rise of each transformer can be estimated using Equations 4.18 and 4.19.

The completed transformer design in each DBSRC is split into two smaller cores ($N_T = 2$). Each uses the E65/32/27 core and Magnetics P material. Using a window fill factor of 40%, the primary winding in each transformer has 7 turns, with each turn wound using 7 strands of 15 AWG copper wire. The secondary winding in each transformer has 28 turns, with each turn wound using 2 strands of 16 AWG copper wire. The estimated core, primary and secondary copper losses are 3.1, 1.9 and 2 W, respectively. The estimated temperature rise of each transformer is 37 °C.

4.3.3 Tank Capacitor

The resonant tank capacitor is implemented using the polypropylene film material. Its selection is primarily determined by the required capacitance and its rms voltage rating. The common optimization objective of size minimization still applies. Since the capacitor carries the full primary tank current, its voltage will vary at the switching frequency, while its envelop varies at the third-harmonic line frequency,

$$i_p(t) = C_r \frac{dv_{cr}}{dt} \approx |\mathbf{I}_p| \cos(\omega_s t + \angle \mathbf{I}_p). \quad (4.27)$$

Solve for the capacitor voltage

$$v_{cr}(t) = \frac{|\mathbf{I}_p|}{\omega_s C_r} \sin(\omega_s t + \angle \mathbf{I}_p). \quad (4.28)$$

The maximum peak capacitor voltage in a line period is

$$V_{cr,pk,max} = \frac{I_{p,pk,max}}{\omega_s C_r}. \quad (4.29)$$

The rms capacitor voltage over a line period is

$$V_{\text{cr,rms,line}} = \frac{I_{\text{p,rms,line}}}{\omega_s C_{\text{r}}}. \quad (4.30)$$

The film capacitor is selected based on both $V_{\text{cr,pk,max}}$ and $V_{\text{cr,rms,line}}$. The rated dc voltage shall be higher than $V_{\text{cr,pk,max}}$. The rated rms ac voltage at switching frequency shall be higher than $V_{\text{cr,rms,line}}$. Manufacturers often only provide the ac ratings at low frequency (e.g. 60 Hz). However, one must verify this rating at the switching frequency, as it is most often lower, due to capacitor losses. The 1 μF resonant capacitor is implemented using a parallel combination of ten 100 nF B32654 film capacitors from EPCOS. Each has rms voltage rating of 130 V at 50 kHz, which is higher than the estimated voltage of 105 V.

4.3.4 Input and DC-Link Capacitors

The input capacitor is shared by both DBSRC modules, as their inputs are connected in parallel. It is also implemented using the polypropylene film material. Its selection is based on a sufficient rms current rating and enough capacitance to limit the voltage ripple. The worst-case rms input capacitor current $I_{\text{cin,rms,line}}$ has been previously derived based on the rms tank current $I_{\text{p,rms,line}}$. The minimum capacitance required to generate peak-to-peak input voltage ripple of $V_{\text{in,pkpk,max}}$ is

$$C_{\text{in}} > \frac{I_{\text{ci,pkpk,max}}}{2\omega_s V_{\text{in,pkpk,max}}}, \quad (4.31)$$

where $I_{\text{ci,pkpk,max}}$ is the maximum peak-to-peak value of the input capacitor current. In the example design, the estimated input capacitor current is 30 A, and the minimum capacitance required is 14 μF for a peak-to-peak voltage ripple of 12 V or 4% of the nominal 300 V. It is implemented using four 10 μF , 450 V B32774 film capacitors from EPCOS. Each capacitor has rms current rating of 7 A at 100 kHz.

Each of the two dc-link capacitors is selected similarly as the input capacitor, based on its rms current and required capacitance. The dc-link capacitor is also part of the line filter.

From each DBSRC of the example design, the estimated rms dc-link capacitor current is 11 A, and the minimum capacitance required is 3 μF for a peak-to-peak voltage ripple of 24 V or 4% of the peak dc-link voltage of 588 V. It is implemented using a 5 μF , 1050 V B32794 film capacitor from EPCOS. It has rms current rating of 11 A at 10 kHz.

4.4 Line Filter Design

Thus far, all the passive components in a 10-kVA DBSRC-unfolding converter have been designed, except for the line filter that is necessary for grid connection. The filter is primarily needed to attenuate high-order ($h > 50$) line current harmonics due to switching ripple in the DBSRC output currents. The filter is made up of the existing DBSRC output capacitors in the dc link and the addition of series inductors on the grid connection. With each DBSRC output modeled as a controlled current source, the complete converter model for filter design is shown in Fig. 4.8a.

The low-order ($h < 50$) harmonics are mainly affected by control and not by filter. They are therefore neglected for filter design. With this assumption, the DBSRC output currents are assumed to have perfect tracking of their respective references, so the resulting line currents have negligible low-order harmonics. It is therefore safe to model the output currents, i_{k1} and i_{k2} , as amplitude-modulated sine waves at twice switching frequency,

$$\begin{cases} i_{k1} &= i_{r1} [\cos(2\omega_s t) + 1] \\ i_{k2} &= i_{r2} [\cos(2\omega_s t) + 1] \end{cases}, \quad (4.32)$$

where i_{r1} and i_{r2} are the reference currents. They are derived from the fundamental approximation and are valid when the DBSRC operates on the γ trajectory. Given a much higher switching frequency than line frequency, the output current averaged over each switching period \bar{i}_k can be considered equal to its reference.

The current sources along with the dc-link capacitors can be pushed to the grid side using the unfold relationships. This results in a per-phase equivalent circuit of Phase A shown in Fig. 4.8b, while Phase-B and -C circuits are similar. The equivalent Phase-A

output current is

$$i_{ka}(t) = I_m \cos(\omega t) [\cos(2\omega_s t) + 1], \quad (4.33)$$

The equivalent grid capacitance is $C_g \approx 3C_k$. It is desired to attenuate the switching-frequency harmonics in i_{ka} to produce the filtered grid current i_a . Exemplary waveforms illustrating i_{k1} , i_{k2} , i_{ka} and i_a are shown in Fig. 4.8c for a modulation frequency m_f of

$$m_f = \frac{f_s}{f} = 10. \quad (4.34)$$

Referring to the equivalent circuit in Fig. 4.8b, the relationship between harmonic magnitudes of the source current $I_{ka}(h)$ and the filtered current $I_a(h)$ is

$$I_a(h) = |F(jhw)| \cdot I_{ka}(h), \quad (4.35)$$

where $|F(jhw)|$ is the filter attenuation at harmonic order h and is determined from the impedances of L_g and C_g ,

$$F(s) = \frac{\frac{1}{sC_g}}{sL_g + \frac{1}{sC_g}}. \quad (4.36)$$

The dominant harmonic order is

$$h_d = 2m_f - 1, \quad (4.37)$$

as the source current is modulated at twice switching frequency. Using Fourier analysis, the relationship between magnitudes of the dominant source current harmonic $I_{ka}(h_d)$ and the fundamental is

$$I_{ka}(h_d) = \frac{I_m}{2}. \quad (4.38)$$

For the designed DBSRC switching at 50 kHz, the filtered grid current harmonic is to be attenuated to below the IEEE 1547 limit around 100 kHz as

$$I_a(h_d) < 0.003I_m. \quad (4.39)$$

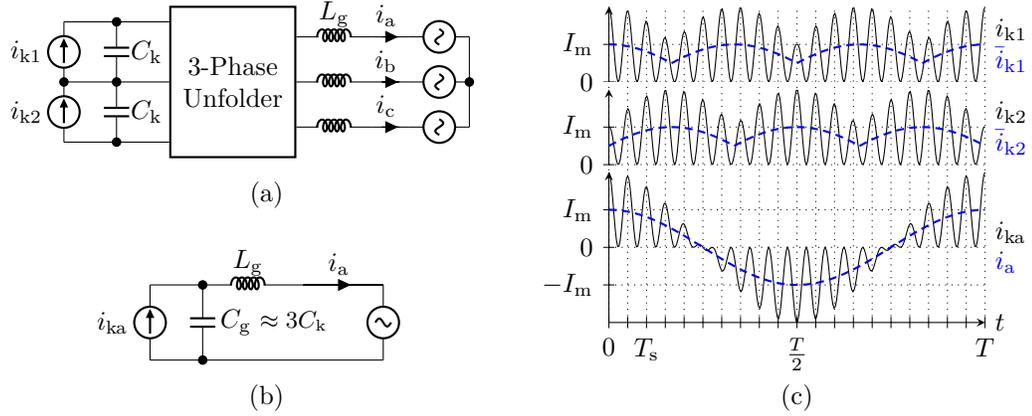


Fig. 4.8: Line filter design in a DBSRC-unfolding converter. (a) Full circuit. (b) Per-phase equivalent circuit. (c) Exemplary waveforms at $m_f = \frac{f_s}{f} = 10$.

The required filter attenuation at the dominant harmonic $|F(jh_{dw})|$ can then be found as -45 dB. With the filter capacitance C_g at $15 \mu\text{F}$, the required filter inductance L_g is $30 \mu\text{H}$. Using the same inductor design constraints in Table 4.1 results in a design of T106-34 core wound with 31 turns of 14 AWG wire for L_g .

4.5 Discussion and Comparison with Conventional Converter

In this section, the completed passive component designs in the proposed DBSRC-unfolding converter are summarized and compared with those in a conventional DAB-VSI converter. The comparisons highlight the reduction in total passive volume using the proposed converter. The reasons contributing to the volume reduction are discussed.

The passive component designs of the DAB stage in the conventional converter have been conducted in Section 2.2.2. The DAB operates at 50 kHz and is designed for nominal power of 10 kW and input and dc-link voltages of 300 and 800 V . For comparison, the passive components in each DBSRC module of the unfolding converter have been designed in Section 4.3. Each module also operates at 50 kHz but processes time-varying power of 5 kW average and 10 kW peak. The DAB and DBSRC designs are summarized and compared in Table 4.3.

The *LCL* line filter of the grid-tied VSI has been designed in Section 2.1.3 to meet the

IEEE 1547 harmonic current limits. The 10-kVA, 10-kHz VSI connects to grid line-to-line voltage of 480 V rms and dc-link voltage of 800 V. For comparison, the line filter design in the unfolding converter has been conducted in Section 4.4 to the same requirements. The line filter designs are summarized and compared in Table 4.4.

From the completed designs, the volume of each major passive component is identified in Table 4.5. The volume comparisons are evaluated in terms of the resonant tank, line filter, dc-link capacitor and the total volume. The DAB tank consists of the transformer and inductor L_r and has a volume of $92 + 395 = 487 \text{ cm}^3$. Each DBSRC tank consists of the transformer, inductor L_r and capacitor C_r . The volume of both DBSRC tanks is $184 + 316 + 160 = 660 \text{ cm}^3$. In comparison, the DBSRC tank is 36% larger than DAB. This is primarily due to the additional volume contributed by the tank inductor and capacitor in the DBSRC. However, the increase in volume is not double, as each DBSRC processes on average only half the three-phase active power.

The VSI line filter consists of L_s , C_g and L_g and takes up volume of $513 + 36 + 159 = 708 \text{ cm}^3$. In comparison, the line filter in the unfolding converter consists of L_g and C_k , with a total volume of just $15 + 52 = 67 \text{ cm}^3$. The significant reduction in filter volume is partly due to the higher switching frequency of 50 kHz in the DBSRC, compared to 10 kHz in the VSI. Another reason is the elimination of the converter-side inductor L_s , which is subject to significant core loss. This reason often prohibits the increase in switching frequency in the VSI [10, 79].

The conventional converter has a single dc-link capacitor between the DAB and VSI, with a designed size of 204 cm^3 . The dc link of the unfolding converter has a capacitor at the output of each DBSRC. These two capacitors have a combined volume of 52 cm^3 . In comparison, the dc-link capacitor volume is reduced by 70% in the unfolding converter. The volume reduction is due to the unfolding converter having much smaller capacitance ($10 \mu\text{F}$ versus $100 \mu\text{F}$), as the capacitors are not used for decoupling and are only needed to provide line filtering [33, 53].

Finally, the total volume of passive components (transformers, inductors and capacitors) in both converters are compared. The conventional converter has a total passive volume of 1447 cm³, while that of the unfolding converter is only 775 cm³. The volume reduction is 45%, or almost half, despite the increase in tank volume in the dc-dc stage. This is primarily a result of the significant volume reduction in the line filter and dc-link capacitor.

4.6 Summary

Chapter 3 reveals that the DBSRC modules in the unfolding converter each work over a wide range of operating points, due to periodic variations in the dc-link voltages and currents. These variations complicate the design of DBSRC power components. The design procedure can be simplified by introducing two design parameters, which are peak conversion ratio M_{pk} and power command U_{pk} . Converter rms currents are analyzed at different values of M_{pk} and U_{pk} and at different power factors. An optimal range for M_{pk} is found that minimizes rms currents compared to other values. This results in optimal selection of the transformer turns ratio for arbitrary converter specifications. These design guidelines are then applied to design passive components in a DBSRC rated at 5 kW average and 10 kW peak, for use in a 10-kVA unfolding converter.

The resonant current in the DBSRC tank contributes to line current harmonics and necessitates filtering by line inductors and dc-link capacitors. Formulas are provided to estimate the harmonic magnitudes and the required filter inductance value. A line filter is then designed for the 10-kVA unfolding converter.

Sizes of its passive and filter components are compared to those in a conventional DAB-VSI converter designed to the same specifications. The advantages of the proposed converter are highlighted in terms of significant reduction of line filter and dc-link capacitor volumes, leading to an overall reduction in passive volume.

Table 4.3: Comparison of dc-dc stage passive component designs between DAB-VSI and DBSRC-unfolding converters.

Component	Parameter	DAB	DBSRC (each)
Transformer	n	2.7	2
	N_T	5	2
	Core	E65/32/27	E65/32/27
	N_p	5	7
	N_p wire	15 AWG ($\times 10$)	15 AWG ($\times 7$)
	N_s	68	28
	N_s wire	17 AWG	16 AWG ($\times 2$)
	$P_{cu,p}$ [W]	1.9	1.9
	$P_{cu,s}$ [W]	1.9	2
	P_{fe} [W]	3.4	3.1
	ΔT [$^{\circ}\text{C}$]	38	37
L_r	Inductance [μH]	20	29
	N_L	4	4
	Core	E42/21/20	E42/21/20
	l_g [mm]	3.7	4
	N_t	8	10
	Wire	15 AWG ($\times 8$)	16 AWG ($\times 8$)
	P_{cu} [W]	1.9	1.6
	P_{fe} [W]	1.9	2.1
	ΔT [$^{\circ}\text{C}$]	39	37
C_r	Capacitance [μF]	-	1
	Series	-	EPCOS B32654
	Specs	-	100 nF 1250 V ($\times 10$)
C_{in}	Capacitance [μF]	40	
	Series	EPCOS B32774	
	Specs	10 μF 450 V ($\times 4$)	
C_k	Capacitance [μF]	100	5
	Series	EPCOS B32778	EPCOS B32794
	Specs	50 μF 900 V ($\times 2$)	5 μF 1050 V

Table 4.4: Comparison of line filter component designs between DAB-VSI and DBSRC-unfolding converters.

Component	Parameter	VSI	DBSRC-Unfolder
L_s	Inductance [μH]	1300	-
	Core	T400-34D	-
	Turns	135	-
	Wire	9 AWG	-
	P_{cu} [W]	14	-
	P_{fe} [W]	13	-
L_g	Inductance [μH]	500	30
	Core	T249-34	T106-34
	Turns	96	31
	Wire	11 AWG	14 AWG
	P_{cu} [W]	12	1.6
C_g	Capacitance [μF]	10	-
	Series	EPCOS B32796	-
	Specs	10 μF 875 V	-

Table 4.5: Comparison of passive component volumes between DAB-VSI and DBSRC-unfolding converters. Core volume is used for inductors and transformers. Case volume is used for capacitors. For a component designed using multiple cores or capacitors, its volume is expressed as quantity \times volume of each core or capacitor. All volumes are in cm^3 .

Component	DAB-VSI	DBSRC-Unfolder
Transformer	$5 \times 79 = 395$	$4 \times 79 = 316$
L_r	$4 \times 23 = 92$	$8 \times 23 = 184$
L_s	$3 \times 171 = 513$	-
L_g	$3 \times 53 = 159$	$3 \times 5 = 15$
C_{in}		$4 \times 12 = 48$
C_r	-	$20 \times 8 = 160$
C_k	$2 \times 102 = 204$	$2 \times 26 = 52$
C_g	$3 \times 12 = 36$	-

CHAPTER 5

MODELING AND FEEDFORWARD CONTROL OF UNFOLDING CONVERTER

The reduction in passive and filter sizes using the unfolding converter is only valuable if it achieves the basic control objectives of a grid-tied converter. These objectives are summarized below:

- Obtain the desired line currents with minimal distortion at all power factors. This is equivalent to ensuring minimal steady-state errors between actual and reference d- and q-axis currents.
- Provide fast dynamic response to changes in reference currents, to ease the design of higher-level voltage and power controllers.
- Ensure robust stability and performance to parameter variations, specifically the line inductance value, and disturbances, such as grid voltage harmonics.

An iterative process is used to find the most suitable controller for the unfolding converter. This chapter uses a basic feedforward controller, primarily aimed at developing and verifying a suitable converter model.

5.1 Feedforward Control of Grid-Tied Unfolding Converter

To facilitate the design of closed-loop controllers to satisfy the aforementioned control objectives, a suitable plant model of the unfolding converter is needed. The model is derived and verified using a basic feedforward controller, constructed as shown in Fig. 5.1. The feedforward controller can be divided into two interconnected parts.

The first part controls the folder by generating an appropriate switching sequence. Its implementation has been discussed in Section 3.2 but is briefly recapped here. The controller is first synchronized to grid voltages (e_a , e_b , e_c) with a phase-locked loop (PLL), which estimates the voltage angle θ^* . The estimated angle is then used to detect and

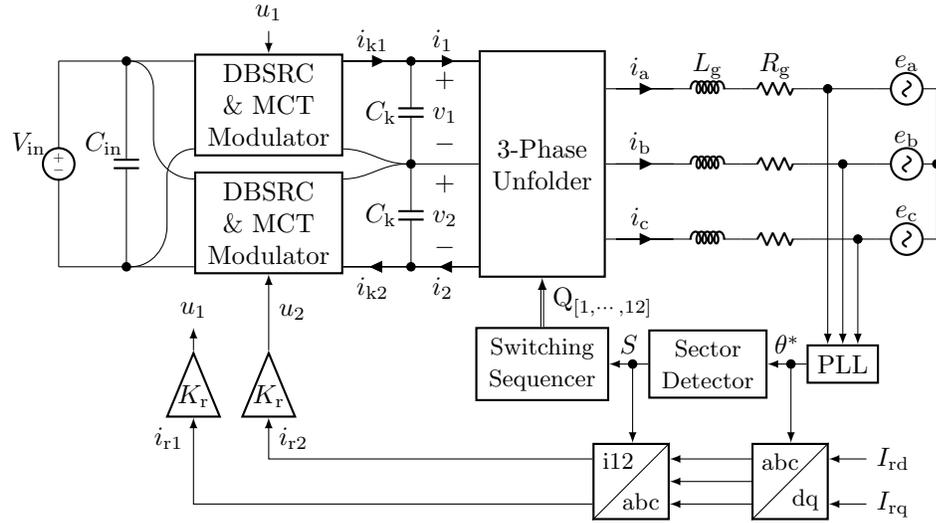


Fig. 5.1: Unfolding converter with feedforward control.

identify one of six operating sectors of the unfolder. A unique switching sequence is then applied based on the sector number S . The applied switching sequence allows the unfolder to rectify the line voltages into dc-link voltages v_1 and v_2 . It also establishes a relationship between line and dc-link currents in each sector for current control.

The second part deals with control of the two DBSRC modules, and specifically, in generation of their power commands u_1 and u_2 . They shall be generated based on the applied d- and q-axis reference currents, I_{rd} and I_{rq} . These references can be obtained from a higher-level power controller, to produce the desired active and reactive powers, P^* and Q^* . A basic power controller calculates the reference currents from the PLL-estimated grid voltage magnitude E_m^* [13],

$$I_{rd} = \frac{2}{3E_m^*} P^* \quad \text{and} \quad I_{rq} = -\frac{2}{3E_m^*} Q^*. \quad (5.1)$$

The dq references are then transformed into time-varying dc-link references i_{r1} and i_{r2} , from which the DBSRC modules use to shape the dc-link currents i_1 and i_2 and to obtain the desired line currents i_a , i_b and i_c . The transformation is applied in two steps. In the first step, a rotating to stationary frame transform, also known as Inverse Park Transform, is applied on I_{rd} and I_{rq} to obtain the three-phase references, i_{ra} , i_{rb} and i_{rc} , using the

estimated angle θ^* from the PLL,

$$\begin{bmatrix} i_{ra} \\ i_{rb} \\ i_{rc} \end{bmatrix} = \begin{bmatrix} \cos(\theta^*) & -\sin(\theta^*) \\ \cos(\theta^* - \frac{2\pi}{3}) & -\sin(\theta^* - \frac{2\pi}{3}) \\ \cos(\theta^* + \frac{2\pi}{3}) & -\sin(\theta^* + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} I_{rd} \\ I_{rq} \end{bmatrix}. \quad (5.2)$$

In the second step, the dc-link references i_{r1} and i_{r2} are derived from the three-phase references based on the sector number S and the unfolded current relationships defined in Table 3.1. This feedforward controller generates u_1 and u_2 from i_{r1} and i_{r2} through a proportion gain K_r , which is set to

$$K_r = \frac{1}{\bar{G}_0} \quad (5.3)$$

to equalize the DBSRC dc gain \bar{G}_0 so that $\bar{i}_{k1} \approx i_{r1}$ and $\bar{i}_{k2} \approx i_{r2}$. As will be seen later, this feedforward controller is able to obtain the desired dc-link and line currents, with small values of filter inductance and dc-link capacitance. More importantly, it allows analysis of converter plant dynamics to facilitate more sophisticated closed-loop controller design.

When line current flows through the filter inductor, a phase difference is generated between the unfolded output and grid voltages. In terms of unfolded control, the issue becomes whether to account for this phase difference in generating the switching sequence. In Fig. 5.1, the unfolded output voltages relative to the grid neutral point are v_a , v_b and v_c . It is then possible to express the dynamics between line voltages and currents as

$$\frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = -\frac{R_g}{L_g} \mathbf{I}_3 \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L_g} \mathbf{I}_3 \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \frac{1}{L_g} \mathbf{I}_3 \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}. \quad (5.4)$$

To ease analysis, the three-phase dynamic equation is transformed into the rotating frame synchronized to the grid voltages as

$$\frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R_g}{L_g} & \omega \\ -\omega & -\frac{R_g}{L_g} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_g} \mathbf{I}_2 \begin{bmatrix} v_d \\ v_q \end{bmatrix} - \frac{1}{L_g} \mathbf{I}_2 \begin{bmatrix} E_m \\ 0 \end{bmatrix}. \quad (5.5)$$

The steady-state unfolded output voltages are obtained by setting the derivative terms to zero

$$\begin{cases} V_d &= R_g I_d - \omega L_g I_q + E_m \\ V_q &= R_g I_q + \omega L_g I_d \end{cases}. \quad (5.6)$$

The phase difference ϕ_v between unfolded output and grid voltages is

$$\tan(\phi_v) = \frac{V_q}{V_d} = \frac{R_g I_q + \omega L_g I_d}{R_g I_d - \omega L_g I_q + E_m} \approx \phi_v, \quad (5.7)$$

where the use of small-angle approximation is justified as $V_d \gg V_q$ when E_m is large. Consider the previously designed 10-kVA unfolding converter with $L_g = 30 \mu\text{H}$ and $R_g = 10 \text{ m}\Omega$ and operating at rated voltage $E_m = 392 \text{ V}$, 60 Hz and rated currents at unity power factor $I_d \approx I_{rd} = 17 \text{ A}$ and $I_q \approx I_{rq} = 0 \text{ A}$. This results in a phase difference of just 0.03° or equivalently a time difference of only $1.3 \mu\text{s}$. The small phase and time differences allow them to be neglected in unfolded control when L_g is small. The difference may need to be accounted for large L_g or at low voltages, which are more applicable when the converter is used in a weak grid or as a motor drive.

5.2 Modeling of Grid-Tied Unfolding Converter Plant

In choosing the feedforward controller gain K_r , one needs to know the dc gain of the DBSRC. It can be derived from the steady-state output power expression in Equation 3.25,

$$P_{\text{out}} = P_{\text{max}} \cdot U = \frac{8}{\pi^2} \frac{V_{\text{in}} V}{n X_t} \cdot U = V I_k, \quad (5.8)$$

where I_k is the steady-state or long-term average value of the DBSRC output current i_k . The nominal dc gain \bar{G}_0 can then be expressed as

$$\bar{G}_0 = \frac{I_k}{U} = \frac{8}{\pi^2} \frac{V_{\text{in}}}{n X_t}. \quad (5.9)$$

These steady-state equations show that the DBSRC output current is insensitive to output

voltage variations and is proportional to the applied power command. The actual command to output current response will depend on dynamics of the resonant tank and modulator but can be approximated using a second-order actuator model [80–82],

$$G_{iu}(s) = \frac{\bar{i}_k}{u} = G_0 \frac{\omega_k^2}{s^2 + 2\zeta\omega_k s + \omega_k^2}, \quad (5.10)$$

where \bar{i}_k is the average value per switching period of i_k , or its short-term average value. The actual dc gain G_0 is modeled by its nominal value and deviation δ_G ,

$$G_0 = \bar{G}_0(1 \pm \delta_G), \quad (5.11)$$

where δ_G depends on factors such as variation in V_{in} , modulator dead time and converter losses. The DBSRC bandwidth ω_k depends on dynamics of the resonant tank and modulator.

Consider again the grid-tied unfolding converter with feedforward control as shown in Fig. 5.1. The converter plant consists of all components between and including the DBSRC output currents (i_{k1} and i_{k2}) and grid sources (e_a , e_b and e_c). Neglecting nonlinearities in DBSRC dynamics and passive components, the plant is still nonlinear as the unfolders switches from sector to sector. However, within a sector, there is no switching, and the unfolded directly connects between the dc link and ac lines. Thus in each sector, an equivalent circuit that is essentially linear can be constructed as shown in Fig. 5.2. Each of the voltage sources (e_1 , e_2 , e_3) represents the corresponding grid source that is connected to the respective dc-link node in each sector by the unfolded. In other words, each source is assigned to e_a , e_b or e_c depending on the sector number.

As a result of implementing the unfolded with the neutral point clamped topology, there are two clamping diodes in the dc link to ensure non-negative voltages on v_1 and v_2 . The diodes are normally reverse-biased and do not affect circuit operation. But they may conduct very briefly at sector beginnings, making the equivalent circuit nonlinear, as will be seen later. For now, it is safe to disregard the diodes, so that a linear dynamic equation

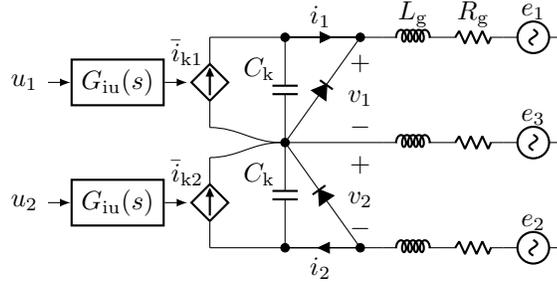


Fig. 5.2: Unfolding converter generalized equivalent circuit.

can be derived,

$$\frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} -\frac{R_g}{L_g} & 0 & \frac{2}{3L_g} & \frac{1}{3L_g} \\ 0 & -\frac{R_g}{L_g} & \frac{1}{3L_g} & \frac{2}{3L_g} \\ -\frac{1}{C_k} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_k} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 0 & 0 & -\frac{2}{3L_g} & \frac{1}{3L_g} & \frac{1}{3L_g} \\ 0 & 0 & -\frac{1}{3L_g} & \frac{2}{3L_g} & -\frac{1}{3L_g} \\ \frac{1}{C_k} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_k} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \bar{i}_{k1} \\ \bar{i}_{k2} \\ e_1 \\ e_2 \\ e_3 \end{bmatrix}. \quad (5.12)$$

The above dynamic equation is then augmented with the DBSRC dynamics in Equation 5.10 written in state-space form,

$$\frac{d}{dt} \begin{bmatrix} \bar{i}_k \\ \bar{i}'_k \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\omega_k^2 & -2\zeta\omega_k \end{bmatrix} \begin{bmatrix} \bar{i}_k \\ \bar{i}'_k \end{bmatrix} + \begin{bmatrix} 0 \\ G_0\omega_k^2 \end{bmatrix} u. \quad (5.13)$$

The result is a state model of the converter plant,

$$\dot{\mathbf{x}}_p = \mathbf{A}_p \mathbf{x}_p + \mathbf{B}_p \mathbf{u} + \mathbf{E} \mathbf{w}, \quad (5.14)$$

where the plant states, control and disturbance inputs are

$$\begin{cases} \mathbf{x}_p = \begin{bmatrix} i_1 & i_2 & v_1 & v_2 & \bar{i}_{k1} & \bar{i}'_{k1} & \bar{i}_{k2} & \bar{i}'_{k2} \end{bmatrix}^\top \\ \mathbf{u} = \begin{bmatrix} u_1 & u_2 \end{bmatrix}^\top \\ \mathbf{w} = \begin{bmatrix} e_1 & e_2 & e_3 \end{bmatrix}^\top \end{cases}. \quad (5.15)$$

The coefficient matrices in the state model of Equation 5.14 are

$$\mathbf{A}_p = \begin{bmatrix} -\frac{R_g}{L_g} & 0 & \frac{2}{3L_g} & \frac{1}{3L_g} & 0 & 0 & 0 & 0 \\ 0 & -\frac{R_g}{L_g} & \frac{1}{3L_g} & \frac{2}{3L_g} & 0 & 0 & 0 & 0 \\ -\frac{1}{C_k} & 0 & 0 & 0 & \frac{1}{C_k} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_k} & 0 & 0 & 0 & 0 & \frac{1}{C_k} & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\omega_k^2 & -2\zeta\omega_k & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega_k^2 & -2\zeta\omega_k \end{bmatrix} \quad (5.16)$$

and

$$\mathbf{B}_p = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ G_0\omega_k^2 & 0 \\ 0 & 0 \\ 0 & G_0\omega_k^2 \end{bmatrix} \quad \text{and} \quad \mathbf{E} = \begin{bmatrix} -\frac{2}{3L_g} & \frac{1}{3L_g} & \frac{1}{3L_g} \\ -\frac{1}{3L_g} & \frac{2}{3L_g} & -\frac{1}{3L_g} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}. \quad (5.17)$$

The state model is derived by moving the line-side components through the unfold to the dc-link side. The same state model applies to all unfold sectors. In each sector, the model is linear, provided that the clamping diodes do not conduct. However, due to unfold switching and as result the different dc-link and line relationships established in each sector, the disturbance inputs, output equations and initial conditions are set differently to relate to the corresponding line quantities in each sector. Thus, the overall model is piecewise linear over a line period. To use this piecewise linear model, the settings for disturbance inputs, output coefficients and initial conditions in each sector are provided in Table 5.1. The provided settings are made as general as possible to be applicable to a broad range of

cases. For instance, the independent inputs and initial conditions are given implicitly, so that distorted voltages and currents can be considered.

The disturbance inputs (e_1, e_2, e_3) are assigned to their respective grid voltages (e_a, e_b, e_c) in each sector. The plant outputs are the line currents

$$\mathbf{y}_p = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \mathbf{C}_p & \mathbf{0} \end{bmatrix} \mathbf{x}_p, \quad \text{where} \quad \mathbf{C}_p = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \\ C_{31} & C_{32} \end{bmatrix}. \quad (5.18)$$

The initial conditions on the DBSRC output currents I_{k10} and I_{k20} depend on the applied command. The initial conditions on their derivatives are set to zero for simplicity. In calculating the initial conditions on the dc-link voltages V_{10} and V_{20} , the voltage drop on the inductor is neglected for simplicity, but the resistor voltage is accounted for. In all the initial conditions, the values of the grid voltages and currents at sector beginnings are used to calculate the initial values on the states in each sector.

5.3 Model Verification

The obtained piecewise linear state model is applied to analyze the feedforward controlled grid-tied unfolding converter. A prerequisite is the explicit derivation of inputs and initial conditions to set up the model for analysis. They are explicitly derived using general formulas provided in Table 5.1. With balanced three-phase grid voltages, the resulting dc-link quantities show symmetry among all odd sectors and among all even sectors. The symmetry is exploited by introducing a new angle

$$\sigma = \theta^* - (S - 1)\frac{\pi}{3}, \quad 0 < \sigma < \frac{\pi}{3}, \quad (5.19)$$

where θ^* and S are the grid voltage angle and unfolder sector variable defined in Equations 3.2 and 3.3. As a result, the model settings can be reduced to just two sets, one for odd and another for even sectors, from the six sets in Table 5.1.

Referring to Fig. 5.1, the command inputs u_1 and u_2 are generated from the feedforward

Table 5.1: General settings for using the piecewise linear unfolding converter model.

Sector	Disturbance Inputs	Output Coefficients	Initial Conditions
1	$e_1 = e_a$ $e_2 = e_c$ $e_3 = e_b$	$C_{11} = C_{22} = 1$ $C_{21} = C_{32} = -1$	$I_{10} = I_{a0}$ $I_{20} = -I_{c0}$ $V_{10} = E_{a0} - E_{c0} + (I_{a0} - I_{c0})R_g$ $V_{20} = E_{c0} - E_{b0} + (I_{c0} - I_{b0})R_g$
2	$e_1 = e_b$ $e_2 = e_c$ $e_3 = e_a$	$C_{12} = C_{21} = 1$ $C_{11} = C_{32} = -1$	$I_{10} = I_{b0}$ $I_{20} = -I_{c0}$ $V_{10} = E_{a0} - E_{b0} + (I_{a0} - I_{b0})R_g$ $V_{20} = E_{b0} - E_{c0} + (I_{b0} - I_{c0})R_g$
3	$e_1 = e_b$ $e_2 = e_a$ $e_3 = e_c$	$C_{21} = C_{32} = 1$ $C_{12} = C_{31} = -1$	$I_{10} = I_{b0}$ $I_{20} = -I_{a0}$ $V_{10} = E_{b0} - E_{a0} + (I_{b0} - I_{a0})R_g$ $V_{20} = E_{a0} - E_{c0} + (I_{a0} - I_{c0})R_g$
4	$e_1 = e_c$ $e_2 = e_a$ $e_3 = e_b$	$C_{22} = C_{31} = 1$ $C_{12} = C_{21} = -1$	$I_{10} = I_{c0}$ $I_{20} = -I_{a0}$ $V_{10} = E_{b0} - E_{c0} + (I_{b0} - I_{c0})R_g$ $V_{20} = E_{c0} - E_{a0} + (I_{c0} - I_{a0})R_g$
5	$e_1 = e_c$ $e_2 = e_b$ $e_3 = e_a$	$C_{12} = C_{31} = 1$ $C_{11} = C_{22} = -1$	$I_{10} = I_{c0}$ $I_{20} = -I_{b0}$ $V_{10} = E_{c0} - E_{b0} + (I_{c0} - I_{b0})R_g$ $V_{20} = E_{b0} - E_{a0} + (I_{b0} - I_{a0})R_g$
6	$e_1 = e_a$ $e_2 = e_b$ $e_3 = e_c$	$C_{11} = C_{32} = 1$ $C_{22} = C_{31} = -1$	$I_{10} = I_{a0}$ $I_{20} = -I_{b0}$ $V_{10} = E_{c0} - E_{a0} + (I_{c0} - I_{a0})R_g$ $V_{20} = E_{a0} - E_{b0} + (I_{a0} - I_{b0})R_g$

controller with a proportional gain K_r from reference currents i_{r1} and i_{r2} . Thus, they each have a defined time trajectory based on the desired d- and q-axis references. The initial DBSRC output currents I_{k10} and I_{k20} are derived by assuming good tracking between reference and actual currents, which generally applies for a high DBSRC bandwidth, or $\omega_k \gg \omega$. The initial dc-link currents I_{10} and I_{20} account for the dc-link capacitor currents, as each capacitor is periodically charged and discharged by its varying dc-link voltage. Note that the capacitor currents are not corrected by the feedforward controller and contribute to regulation errors in the line currents. The initial dc-link voltages V_{10} and V_{20} account for the voltage drop due to grid resistance R_g but neglect the inductor voltage. The derived inputs and initial conditions are summarized in Table 5.2.

Using the derived inputs and initial conditions for a feedforward controlled unfolding converter, its piecewise linear state model is integrated in Matlab using ODE23. The analytical results are then compared with simulation results with the unfolders implemented with circuit model and the DBSRC implemented with actuator model. The comparison is conducted using parameters from the 10-kVA unfolding converter design. They are grid voltage $E_m = 392$ V and frequency $f = 60$ Hz, line inductance $L_g = 30$ μ H and resistance $R_g = 0.1$ Ω , dc-link capacitance $C_k = 5$ μ F, DBSRC bandwidth $f_k = 10$ kHz and damping ratio $\zeta = 0.7$.

The comparison is first conducted at unity power factor and 10 kW, by setting reference currents to $I_{rd} = 17$ A and $I_{rq} = 0$ A. The simulated line currents are shown over a line period in Fig. 5.3a. The current profiles are sinusoidal, but current oscillation and distortion exist at sector beginnings. The dc-link voltage and current as well as the DBSRC output current are compared between simulation and analysis in Sector 2 in Fig. 5.3b. Notice that the integrated state model using the derived inputs and initial conditions can reproduce both the low-frequency trajectories and the high-frequency oscillation in simulation. The close matching between the two results verifies accuracy of the converter plant model.

Table 5.2: Piecewise linear model settings for a feedforward controlled unfolding converter.

Sector	Inputs	Initial Conditions
Odd	$u_1 = K_r I_{rd} \cos(\sigma) - K_r I_{rq} \sin(\sigma)$ $u_2 = K_r I_{rd} \sin(\sigma + \frac{\pi}{6}) + K_r I_{rq} \cos(\sigma + \frac{\pi}{6})$ $e_1 = E_m \cos(\sigma)$ $e_2 = E_m \cos(\sigma + \frac{2\pi}{3})$ $e_3 = E_m \cos(\sigma - \frac{2\pi}{3})$	$I_{10} = I_{rd} - \frac{\sqrt{3}}{2} E_m \omega C_k$ $I_{20} = \frac{1}{2} I_{rd} + \frac{\sqrt{3}}{2} I_{rq} - \frac{3\sqrt{3}}{2} E_m \omega C_k$ $V_{10} = \frac{3}{2} E_m + \frac{3}{2} I_{rd} R_g + \frac{\sqrt{3}}{2} I_{rq} R_g$ $V_{20} = -\sqrt{3} I_{rq} R_g$ $I_{k10} = I_{rd}$ $I_{k20} = \frac{1}{2} I_{rd} - \frac{\sqrt{3}}{2} I_{rq}$
Even	$u_1 = K_r I_{rd} \sin(\sigma + \frac{\pi}{6}) + K_r I_{rq} \cos(\sigma + \frac{\pi}{6})$ $u_2 = K_r I_{rd} \cos(\sigma) - K_r I_{rq} \sin(\sigma)$ $e_1 = E_m \cos(\sigma - \frac{\pi}{3})$ $e_2 = -E_m \cos(\sigma)$ $e_3 = E_m \cos(\sigma + \frac{\pi}{3})$	$I_{10} = \frac{1}{2} I_{rd} + \frac{\sqrt{3}}{2} I_{rq} - \frac{3\sqrt{3}}{2} E_m \omega C_k$ $I_{20} = I_{rd} - \frac{\sqrt{3}}{2} E_m \omega C_k$ $V_{10} = -\sqrt{3} I_{rq} R_g$ $V_{20} = \frac{3}{2} E_m + \frac{3}{2} I_{rd} R_g + \frac{\sqrt{3}}{2} I_{rq} R_g$ $I_{k10} = \frac{1}{2} I_{rd} - \frac{\sqrt{3}}{2} I_{rq}$ $I_{k20} = I_{rd}$

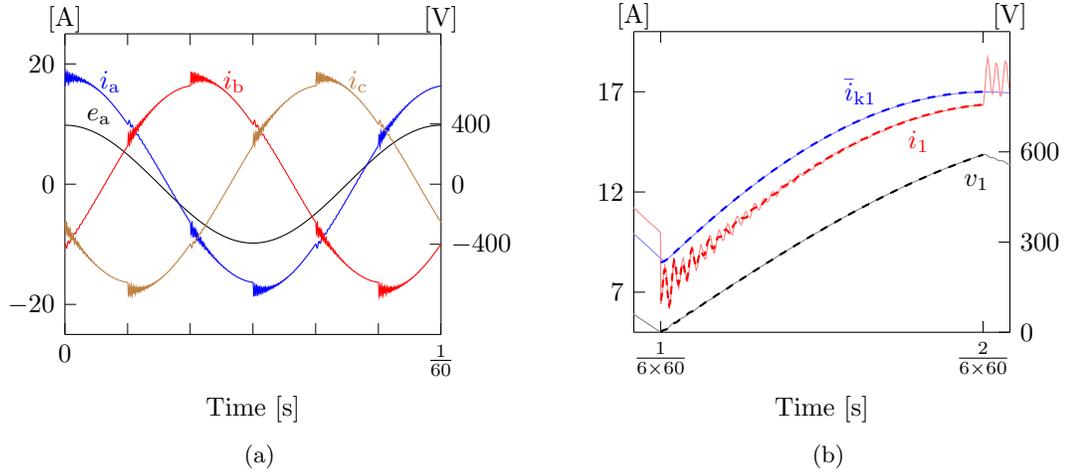


Fig. 5.3: Model verification at unity power factor with $I_{rd} = 17$ A and $I_{rq} = 0$ A. (a) Simulated line currents over a line period. (b) Simulated (solid) and state model (dashed) results of dc-link voltage v_1 , current i_1 and DBSRC output current \bar{i}_{k1} in Sector 2.

5.4 Analysis of Current Distortion at Non-Unity Power Factors

This section begins by continuing with the simulation verification of the state model of the unfolding converter plant. The analytical and simulation results of the feedforward controlled converter are compared using the same parameters but operated at a non-unity power factor of 0.7 (capacitive) with $I_{rd} = I_{rq} = 12$ A. In the simulated line currents shown in Fig. 5.4a, noticeable differences from unity power factor are larger initial current excursions at sector beginnings and weakly damped current oscillations.

At the same power factor, the dc-link voltage and current are compared between simulation and analysis in Sector 2 in Fig. 5.4b. The analytical model predicts larger voltage and current oscillations than simulation. The discrepancies are not due to error in the state model, as both results converge and match after oscillations have subdued. Instead, they are due to conduction of the unfolder clamping diode at sector beginnings. The diode conduction makes circuit operation nonlinear and is not considered in the state model.

To more accurately model and predict circuit behavior at sector beginnings, it is necessary to analyze circuit operation during diode conduction. The simulation waveforms are studied at the beginning of Sector 2 in Fig. 5.5, where the first dc link current is switched from Phase A to B. Both the unfolder and reference enter Sector 2 at T_0 . The dc-link capacitor has been fully discharged, and thus the dc-link voltage has fallen to zero at T_0 . The capacitor cannot be discharged further, and any additional discharge current will flow through the clamping diode,

$$i_D(T_0) = i_b(T_0) - i_1(T_0) = i_b(T_0) - \bar{i}_{k1}(T_0). \quad (5.20)$$

During diode conduction, a short exists across the top dc link, and the dc-link current follows the DBSRC output current and increases until it is equal to Phase-B current, and the diode stops conducting. In the same period, the short is also applied between Phases A and B, causing Phase-B current to drop and Phase-A current to rise. The equivalent circuit during diode conduction is shown in Fig. 5.6. The diode will conduct as long as $i_b > \bar{i}_{k1}$. During diode conduction, \bar{i}_{k1} rises due to the step increase in command u_1 , while i_b falls as

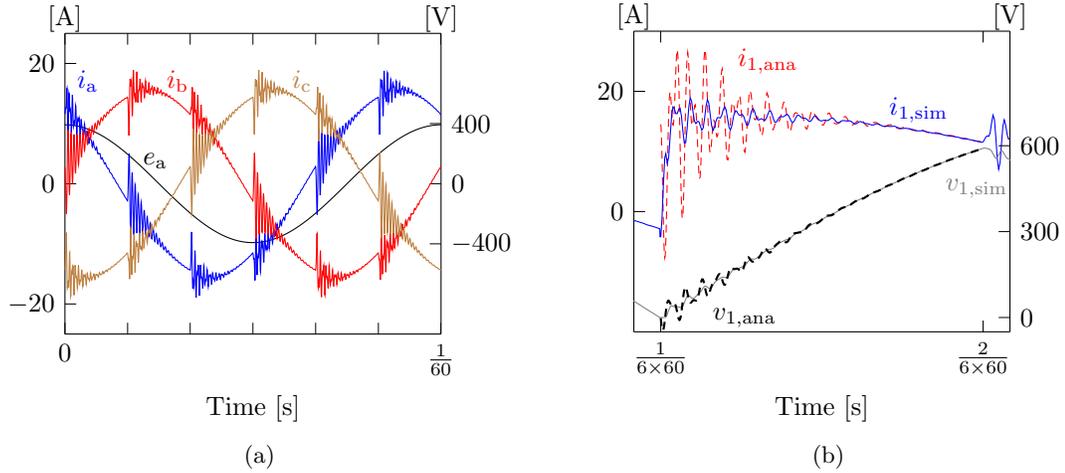


Fig. 5.4: Model verification at power factor of 0.7 (capacitive) with $I_{rd} = I_{rq} = 12$ A. (a) Simulated line currents over a line period. (b) Simulated (solid) and state model (dashed) results of dc-link voltage v_1 and current i_1 in Sector 2.

the Phase-B inductor is discharged. Referring back to Fig. 5.5, the two currents converge at T_1 , or $i_b(T_1) = \bar{i}_{k1}(T_1)$, and the diode stops conducting.

It is of interest to estimate and limit the amount of current excursion ΔI_b on i_b , where $\Delta I_b = |i_b(T_1) - i_b(T_0)|$, as it increases distortion and induces oscillation on the line currents. Intuitively, the current excursion can be decreased in two ways. The first is to reduce the diode conduction time. This can be accomplished by increasing the DBSRC bandwidth but is not practical as it is ultimately limited by the switching frequency. Alternatively, a second method is to reduce the rate of change in i_b by increasing the line inductance. The drawback is increased inductor size.

Before further investigating these remedies, it is first necessary to estimate the expected current excursion ΔI_b . This involves solving for the diode conduction time $\Delta T = T_1 - T_0$. To do that, it is necessary to obtain expressions for $i_b(T_0 + \Delta t)$ and $\bar{i}_{k1}(T_0 + \Delta t)$, where the variable Δt is the elapsed time from T_0 and has values between zero and ΔT . For \bar{i}_{k1} , this is straightforward by approximating it with a constant slope,

$$\bar{i}_{k1}(T_0 + \Delta t) = \bar{i}_{k1}(T_0) + K_i \Delta t. \quad (5.21)$$

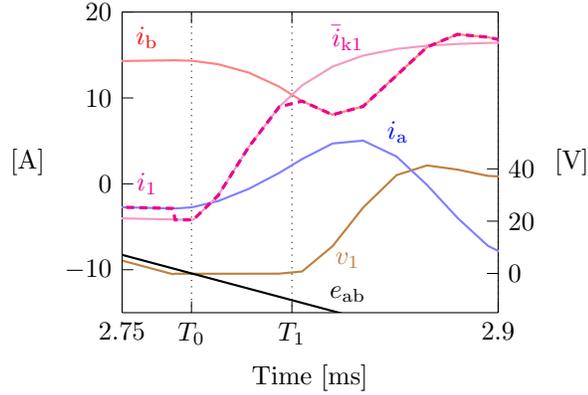


Fig. 5.5: Simulated converter waveforms at beginning of Sector 2 at power factor of 0.7 (capacitive) with $I_{rd} = I_{rq} = 12$ A.

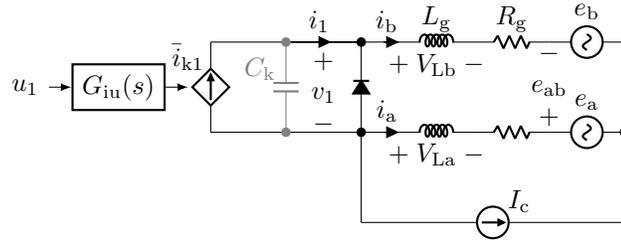


Fig. 5.6: Unfolding converter equivalent circuit in Sector 2 during conduction of clamping diode.

The slope K_i can be estimated using parameters in the DBSRC actuator model.

The rate of change on i_b largely depends on the line inductance L_g and its applied voltage v_{Lb} . For simplicity, the line resistance R_g and its voltage drop are neglected in subsequent analysis. Due to equal line inductance in Phases B and A, the two inductors will equally share the line-to-line grid voltage e_{ab} ,

$$v_{Lb} = -v_{La} = \frac{1}{2}e_{ab}. \quad (5.22)$$

Phase-B current is then obtained by integrating the inductor voltage,

$$i_b(T_0 + \Delta t) = \frac{1}{L_g} \int_{T_0}^{T_0 + \Delta t} v_{Lb} dt + i_b(T_0). \quad (5.23)$$

The integral is solved by assuming ideal grid voltage $e_{ab} = \sqrt{3}E_m \cos(\omega t + \frac{\pi}{6})$,

$$i_b(T_0 + \Delta t) = \frac{\sqrt{3}E_m}{2\omega L_g} [\cos(\omega\Delta t) - 1] + i_b(T_0). \quad (5.24)$$

By setting $\Delta t = \Delta T = T_1 - T_0$, Phase-B and DBSRC output currents at T_1 are obtained. By knowing that they are equal, $i_b(T_1) = \bar{i}_{k1}(T_1)$, the following equation is set up to solve for ΔT ,

$$\frac{\sqrt{3}E_m}{2\omega L_g} [\cos(\omega\Delta T) - 1] + i_b(T_0) = K_i\Delta T + \bar{i}_{k1}(T_0). \quad (5.25)$$

The small values of ΔT in the range of microseconds, compared to a line period of milliseconds, justifies the use of small-angle approximation,

$$\cos(\omega\Delta T) \approx 1 - \frac{(\omega\Delta T)^2}{2}. \quad (5.26)$$

Applying the approximation simplifies Equation 5.25 into

$$\frac{\sqrt{3}E_m\omega}{4L_g}(\Delta T)^2 + K_i\Delta T + \bar{i}_{k1}(T_0) - i_b(T_0) = 0. \quad (5.27)$$

The diode conduction time ΔT can then be readily solved using the quadratic formula, once all the coefficients are known. For the feedforward controlled converter, the initial currents $\bar{i}_{k1}(T_0)$ and $i_b(T_0)$ can be found using Table 5.2,

$$\begin{cases} \bar{i}_{k1}(T_0) &= \frac{1}{2}I_{rd} - \frac{\sqrt{3}}{2}I_{rq} \\ i_b(T_0) &= \frac{1}{2}I_{rd} + \frac{\sqrt{3}}{2}I_{rq} - \frac{3\sqrt{3}}{2}E_m\omega C_k \end{cases}. \quad (5.28)$$

The current slope K_i of \bar{i}_{k1} can be estimated based on the relationship between rise time and bandwidth of a well-damped second-order model,

$$K_i \approx \frac{(0.9 - 0.1) \cdot [i_{r1}(T_1) - \bar{i}_{k1}(T_0)]}{\frac{0.35}{f_k}} \approx 4f_k I_{rq}. \quad (5.29)$$

Plug the obtained coefficients into Equation 5.27 and solve for ΔT ,

$$\frac{\sqrt{3}E_m\omega}{4L_g}(\Delta T)^2 + 4f_k I_{rq}\Delta T - \sqrt{3}I_{rq} + \frac{3\sqrt{3}}{2}E_m\omega C_k = 0. \quad (5.30)$$

Finally, the solution of ΔT is used to find the amount of current excursion in i_b ,

$$\Delta I_b = |i_b(T_1) - i_b(T_0)| = \frac{\sqrt{3}E_m}{2\omega L_g} [1 - \cos(\omega\Delta T)] \approx \frac{\sqrt{3}E_m\omega}{4L_g}(\Delta T)^2. \quad (5.31)$$

The analytical solutions for ΔT and ΔI_b are compared with simulation results using the same parameters from the previously provided 10-kVA unfolding converter design. They are grid voltage $E_m = 392$ V and frequency $f = 60$ Hz, line inductance $L_g = 30$ μ H and resistance $R_g = 0.1$ Ω , dc-link capacitance $C_k = 5$ μ F, DBSRC bandwidth $f_k = 10$ kHz and damping ratio $\zeta = 0.7$. The converter is operated at a power factor of 0.7 (capacitive) with $I_{rd} = I_{rq} = 12$ A. The diode conduction time is 34 and 33 μ s in analysis and simulation, respectively. The current excursion is 2.5 and 2.8 A in analysis and simulation, respectively. Another case is considered by increasing L_g to 60 μ H. There is little change in ΔT , but ΔI_b is reduced to 1.4 and 1.6 A in analysis and simulation, respectively.

5.5 Mitigation of Current Distortion at Non-Unity Power Factors

This section provides a control method to mitigate the current distortion at sector beginnings at non-unity power factors. The method reduces current distortion without altering physical converter parameters, such as line inductance or switching frequency. The method works by phase-shifting the sector variables used to generate the unfold switching sequence and the reference currents. The added phase shift compensates for limited DBSRC bandwidth by taking advantage of the conduction periods of the unfold clamping diodes. The amount of phase shift is analytically derived and generalized to all power factors. The reduction in current distortion is quantified in simulation. Finally, a sector-adjusting algorithm is provided to implement this method.

5.5.1 Capacitive Case

Consider in Fig. 5.7 the converter waveforms under same operating conditions as in Fig. 5.5 but with both unfolder and reference sectors advanced in time by ΔT_a . Thus, both unfolder and reference enter Sector 2 at T_{0-} , where $T_{0-} = T_0 - \Delta T_a$. The dc-link capacitor is rapidly discharged due to the difference between Phase-B and DBSRC output currents. Subsequently, the clamping diode conducts. Due to a short discharge duration compared with ΔT_a , it is neglected, and the diode is assumed to conducted at T_{0-} in the following analysis. The sector advances cause the clamping diode to conduct earlier.

The equivalent circuit during diode conduction is the same as in Fig. 5.6. However, it is noted that the waveforms behave differently, where Phase-B current first rises then falls. Specifically, notice that i_b increases between T_{0-} and T_0 and decreases between T_0 and T_1 . This is due to a polarity change in the inductor voltage v_{Lb} , as it tracks the grid voltage e_{ab} during diode conduction. The diode stops conducting at T_1 when the DBSRC output current rises to where Phase-B current has fallen to.

The amount of current excursion can be controlled by adjusting the advanced time. The method can also be understood as providing extra time for the DBSRC output current to rise to Phase-B current and thus compensating for limited DBSRC bandwidth. Define the positive excursion in i_b as $\Delta I_{b+} = |i_b(T_0) - i_b(T_{0-})|$, and the negative excursion as $\Delta I_{b-} = |i_b(T_1) - i_b(T_0)|$. The overall current excursion is then $\Delta I_b = \max(\Delta I_{b+}, \Delta I_{b-})$. Whereas previously ΔI_b is primarily mitigated by increasing L_g , it can now be reduced by adjusting ΔT_a , which can be understood as providing more time for \bar{i}_{k1} to rise.

The question then becomes how to choose ΔT_a to minimize ΔI_b . To do that, it is necessary to obtain ΔI_{b+} and ΔI_{b-} from solving the inductor current. Similar to previous analysis, R_g is neglected to simplify analysis, so that each inductor shares e_{ab} equally,

$$i_b(T_{0-} + \Delta t) = \frac{1}{L_g} \int_{T_{0-}}^{T_{0-} + \Delta t} \frac{1}{2} e_{ab} dt + i_b(T_{0-}). \quad (5.32)$$

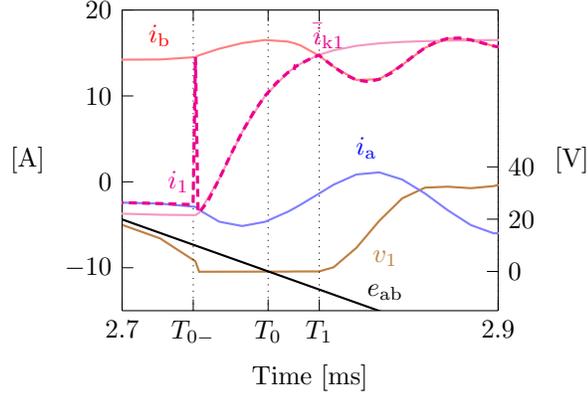


Fig. 5.7: Simulated converter waveforms at beginning of Sector 2 at power factor of 0.7 (capacitive) with $I_{rd} = I_{rq} = 12$ A and advancing both unfolder and reference sectors by $40 \mu\text{s}$.

Assuming ideal grid voltages, the positive current excursion is solved,

$$\Delta I_{b+} = |i_b(T_0) - i_b(T_{0-})| = \frac{\sqrt{3}E_m}{2\omega L_g} [1 - \cos(\omega\Delta T_a)] \approx \frac{\sqrt{3}E_m\omega}{4L_g} (\Delta T_a)^2. \quad (5.33)$$

To find the negative current excursion, the diode conduction time ΔT is solved using the same earlier procedure by equating Phase-B and DBSRC output currents at T_1 ,

$$\begin{aligned} i_b(T_1) &= \frac{\sqrt{3}E_m}{2\omega L_g} [\cos(\omega\Delta T - \omega\Delta T_a) - \cos(\omega\Delta T_a)] + i_b(T_{0-}) \\ &= K_i\Delta T + \bar{i}_{k1}(T_{0-}) = \bar{i}_{k1}(T_1). \end{aligned} \quad (5.34)$$

After applying small-angle approximation and using expressions for the initial currents in Equation 5.28 and the current slope in Equation 5.29, the following quadratic equation of ΔT is obtained,

$$\frac{\sqrt{3}E_m\omega}{4L_g} (\Delta T)^2 + \left(4f_k I_{rq} - \frac{\sqrt{3}E_m\omega}{2L_g} \Delta T_a \right) \Delta T - \sqrt{3}I_{rq} + \frac{3\sqrt{3}}{2} E_m\omega C_k = 0. \quad (5.35)$$

The solution of ΔT then allows estimation of the negative current excursion,

$$\Delta I_{b-} = |i_b(T_1) - i_b(T_{0-})| \approx \frac{\sqrt{3}E_m\omega}{4L_g} [(\Delta T)^2 - 2\Delta T\Delta T_a]. \quad (5.36)$$

Comparing Equations 5.36 to 5.31, which is the negative current excursion without sector advances, it is noted that increasing ΔT_a reduces ΔI_{b-} . However, care should be taken as doing so increasing the positive current excursion from Equation 5.33. There exists an optimal amount of advanced time that yields minimal overall current excursion for given converter parameters and operating condition. The optimal value of ΔT_a is obtained by setting $\Delta I_{b+} = \Delta I_{b-} = \Delta I_b$, and a relationship between ΔT_a and ΔT is found,

$$\Delta T = (\sqrt{2} + 1)\Delta T_a. \quad (5.37)$$

Combining this with Equation 5.35 provides a solvable quadratic equation on the optimal value of ΔT_a ,

$$\frac{\sqrt{3}E_m\omega}{4L_g}(\Delta T_a)^2 + 4(\sqrt{2} + 1)f_k I_{rq}\Delta T_a - \sqrt{3}I_{rq} + \frac{3\sqrt{3}}{2}E_m\omega C_k = 0. \quad (5.38)$$

The effect of advancing the unfolded and reference sectors is compared between analysis and simulation using the same parameters from the previously provided 10-kVA unfolding converter design. The converter is operated at a power factor of 0.7 (capacitive) with $I_{rd} = I_{rq} = 12$ A. In analysis, the optimal value of advanced time is obtained as $16 \mu\text{s}$, and the current excursion is 0.5 A. With this time applied in simulation, the current excursion is 1.2 A, which is higher than analysis but is much less than the 2.8 A without sector advances. In the line current waveforms shown in Fig. 5.8, the reduction in distortion is visible over case without sector advances.

5.5.2 Inductive Case

Thus far, the considered non-unity power factors have all been capacitive. The converter behavior with inductive loads can be quite different. The simulated line current waveforms are shown over a line period in Fig. 5.9a at a power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12$ A. Notice the larger current distortion and oscillation at sector beginnings, compared to the capacitive case.

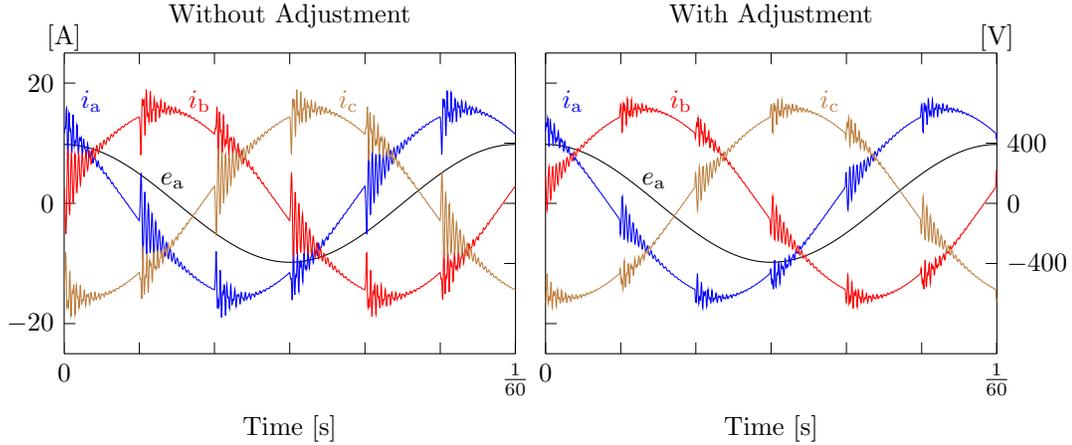


Fig. 5.8: Comparison of simulated line currents over a line period with and without sector adjustment of $\Delta T_a = 40 \mu\text{s}$ at power factor of 0.7 (capacitive) with $I_{rd} = I_{rq} = 12 \text{ A}$.

The closeup waveforms at beginning of Sector 2 are shown in Fig. 5.9b. There are no sector advances, so both the unfolders and reference enter Sector 2 at T_0 . A noticeable difference from the capacitive case is the large current excursion in i_b between T_0 and T_D . This is because the DBSRC output current now has to fall to Phase-B current, which is initially negative. The difference between Phase-B and DBSRC output currents charges the dc-link capacitor as $\bar{i}_{kl}(T_0) > 0$ and $i_b(T_0) < 0$. The stored energy in the capacitor is then transferred to Phase-B and -A inductors through a half-period resonance, which ends when the clamping diode conducts at T_D . During the resonance, the line current excursions can be significant, especially with a small line inductance and a large reactive current. In Fig. 5.9b, the excursion in i_b is $i_b(T_D) - i_b(T_0) = 25 \text{ A}$, compared with a reference current magnitude of $\sqrt{I_{rd}^2 + I_{rq}^2} = 17 \text{ A}$. Obviously, the amount of excursion needs to be reduced.

From the analysis of Fig. 5.9b, it can be deduced that to reduce the large excursion in line currents at sector beginnings at inductive power factors, the rapid charging of the dc-link capacitor shall be avoided. In other words, it is necessary to reduce the difference between the DBSRC output current and the upcoming line current. This is accomplished by advancing the reference sectors and delaying the unfolders. Doing so causes the capacitor to be initially discharged, instead of being charged.

The simulation waveforms with the same duration ΔT_a applied to advance reference

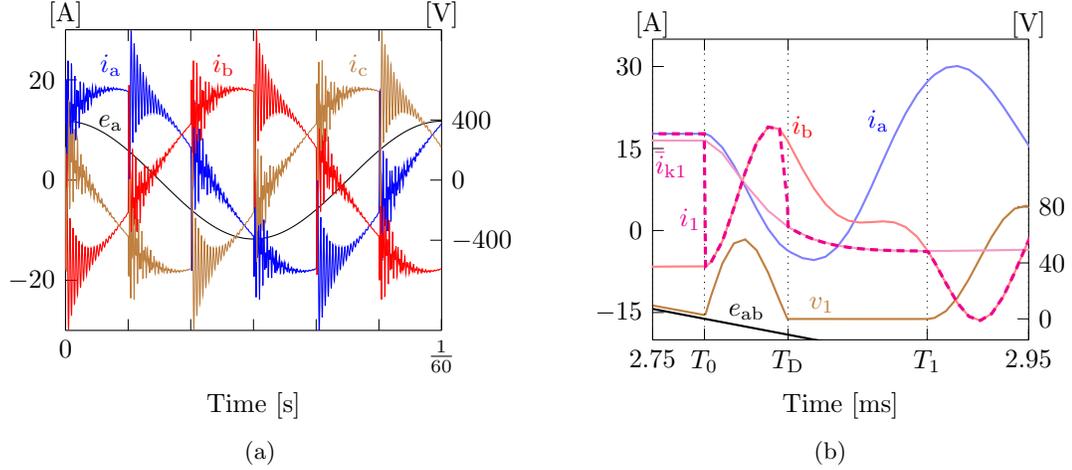


Fig. 5.9: Simulated converter waveforms at power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12$ A. (a) Line currents over a line period. (b) Waveforms at beginning of Sector 2.

and delay unfold sectors are shown in Fig. 5.10. The reference sector is advanced from the original T_0 and enters Sector 2 at $T_{0-} = T_0 - \Delta T_a$. The unfold remains in Sector 1 until $T_1 = T_0 + \Delta T_a$ when it enters Sector 2. Between T_{0-} and T_1 , the equivalent circuit of Sector 1 shown in Fig. 5.11 applies and is used in subsequent analysis. Soon after T_{0-} , the dc-link capacitor is discharged by the difference between Phase-A current and the falling DBSRC output current. The capacitor is completely discharged at T_D , and the clamping diode starts to conduct. The conducting diode shorts Phases A and B, so that the grid voltage e_{ab} is applied on the inductors. The circuit behavior during diode conduction is similar to that at capacitive power factors, in that i_b first rises till T_0 and then falls, while i_a changes in the opposite manner. Neglecting T_D or the capacitor discharge time, the positive excursion in i_b is calculated using Equation 5.33. The diode stops conducting at T_1 as the unfold enters Sector 2.

It can be seen that during the period $T_1 - T_{0-} = 2\Delta T_a$, \bar{i}_{k1} is allowed to fall to $\bar{i}_{k1}(T_1)$. The value of $\bar{i}_{k1}(T_1)$ can be adjusted by changing ΔT_a . But one can observe that past T_1 , the current excursion is minimized if $\bar{i}_{k1}(T_1) \approx i_b(T_1)$. For the feedforward controlled converter, this is achieved by choosing ΔT_a so that $\bar{i}_{k1}(T_1) = i_{r1}(T_1)$. The desired adjustment can then

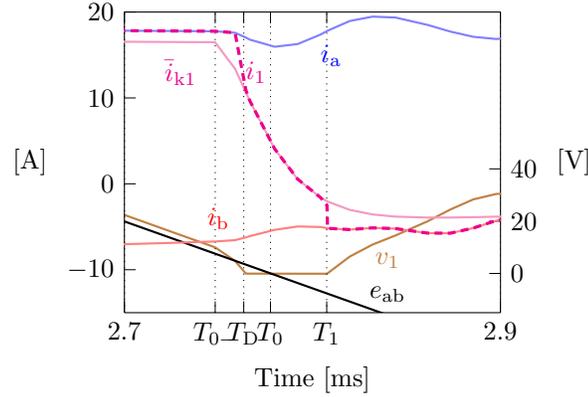


Fig. 5.10: Simulated converter waveforms at beginning of Sector 2 at power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12$ A and advancing reference and delaying unfold sectors both by $30 \mu\text{s}$.

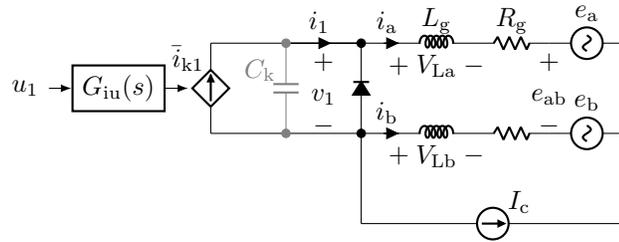


Fig. 5.11: Unfolding converter equivalent circuit in Sector 1 during conduction of clamping diode.

be solved based on Equations 5.21 and 5.29,

$$\begin{aligned}
 \Delta T_a &= \frac{T_1 - T_{0-}}{2} = \frac{\bar{i}_{k1}(T_1) - \bar{i}_{k1}(T_{0-})}{2K_i} \\
 &= \frac{i_{r1}(T_1) - \bar{i}_{k1}(T_{0-})}{2K_i} \\
 &\approx \frac{\frac{1}{2}I_{rd} + \frac{\sqrt{3}}{2}I_{rq} - (\frac{1}{2}I_{rd} - \frac{\sqrt{3}}{2}I_{rq})}{2 \cdot 4f_k I_{rq}} \\
 &\approx \frac{0.2}{f_k}.
 \end{aligned} \tag{5.39}$$

The overall current excursion can then be estimated based on Equation 5.33,

$$\Delta I_b \approx \Delta I_{b+} = |i_b(T_0) - i_b(T_{0-})| \approx \frac{\sqrt{3}E_m\omega}{4L_g} (\Delta T_a)^2. \tag{5.40}$$

The sector adjustments at inductive power factors are compared between analysis and simulation using the same parameters from the previously provided 10-kVA unfolding converter design. The converter is operated at a power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12$ A. In analysis, the optimal value of adjustment is obtained as 20 μ s, and the current excursion is 0.9 A. With this time applied in simulation, the current excursion is also 0.9 A and much less than the 25 A without sector adjustments. In the line current waveforms shown in Fig. 5.12, significant reduction in distortion is visible over case without adjustments.

5.5.3 Sector-Adjusting Algorithm

Based on conclusions on adjustments to the unfolders and reference sectors, the feed-forward controller is modified as shown in Fig. 5.13. The unfolders are generated by first phase-shifting the estimated grid voltage angle θ^* by an amount ϕ_f ,

$$\theta_f = \theta^* + \phi_f. \quad (5.41)$$

The resulting unfolder angle θ_f is then used to generate the unfolder sector variable

$$S_f = \text{ceil} \left(\frac{\theta_f}{\pi/3} \right). \quad (5.42)$$

The reference sector variable S_r is generated in the same manner using ϕ_r ,

$$\theta_r = \theta^* + \phi_r, \quad (5.43)$$

$$S_r = \text{ceil} \left(\frac{\theta_r}{\pi/3} \right). \quad (5.44)$$

The phase shifts ϕ_f and ϕ_r are produced from a sector-adjusting algorithm. The algorithm inputs are the estimated grid frequency ω^* and the q-axis reference current I_{rq} . Internally, there is also an adjustable threshold I_{th} (> 0). The algorithm is based on the

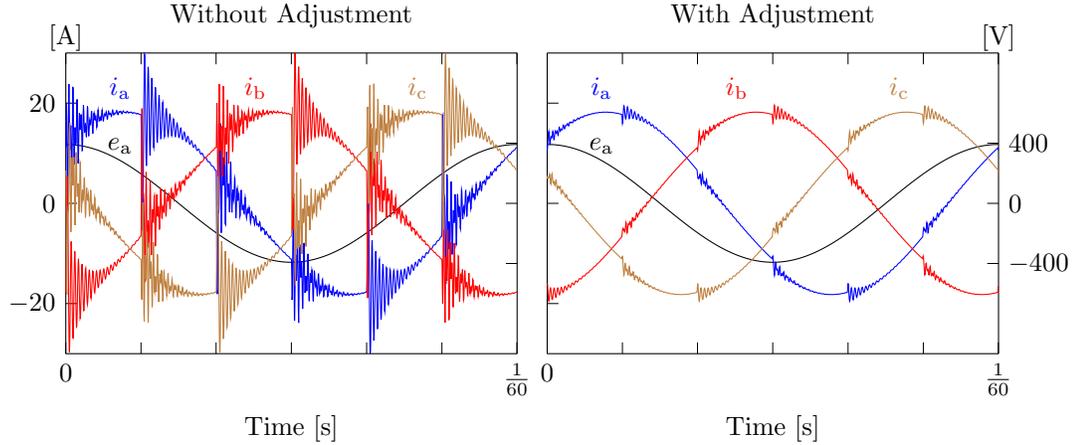


Fig. 5.12: Comparison of simulated line currents over a line period with and without sector adjustment of $\Delta T_a = 30 \mu\text{s}$ at power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12 \text{ A}$.

derived formulas for time ΔT_a but specifically on Equation 5.39. If $I_{rq} > I_{th}$,

$$\phi_f = \phi_r = \frac{0.2\omega^*}{f_k}; \quad (5.45)$$

else if $I_{rq} < -I_{th}$,

$$\phi_f = -\phi_r = -\frac{0.2\omega^*}{f_k}; \quad (5.46)$$

else,

$$\phi_f = \phi_r = 0. \quad (5.47)$$

5.6 Summary

This chapter starts with a review of basic control objectives in a grid-tied converter. They can be classified by the converter's steady-state and dynamic performance. In the unfolding converter, a suitable controller is developed to achieve these performance objectives. The controller development is an iterative process, where multiple controllers for the same system are designed, evaluated and compared before settling on the most suitable choice.

Fundamental to any controller design is the development of a suitable model of the plant to be controlled. This chapter develops a piecewise linear state model of the unfolding

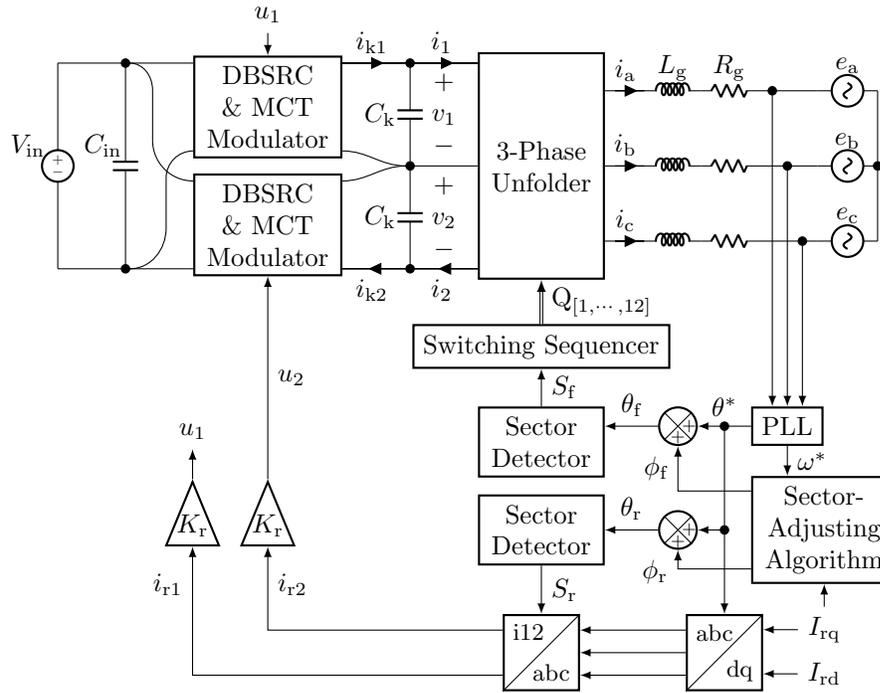


Fig. 5.13: Unfolding converter with feedforward control and sector adjuster.

converter. The model is based on a dc-link-side equivalent circuit of the converter. Each DBSRC output is modeled as a dependent current source controlled by the power command through a second-order actuator model. In the piecewise model, the same state equation is valid in all sectors, but different inputs and initial conditions have to be applied in each sector. The model is verified in simulation using a basic feedforward controller.

The model also reveals current distortion at sector beginnings, which becomes significant at non-unity power factors. From analysis of the equivalent circuit, the distortion origins are traced to the finite DBSRC rise time when responding to step changes in applied command. A remedy that takes advantage of the conduction of the unfolders clamping diodes is proposed and tested by phase-shifting the unfolders and reference sectors.

CHAPTER 6

FEEDBACK CONTROL IN STATIONARY FRAME

Recall the primary control objective of a grid-tied converter, which is to obtain the desired line currents with minimal distortion and error with the reference. In the unfolding converter, with the unfolder stage properly synchronized to the grid voltages and switching at the correct instants, six sectors are identified. In each sector, each line is directly connected to its corresponding dc-link node. With a known relationship between the line and dc-link currents in each sector, the control objective is then achieved by shaping each dc-link current to a desired profile that is defined by the desired line currents in that sector.

In Chapter 5, it has been observed that the current relationship in each sector holds true unless the clamping diodes conduct. The diode conduction creates a short between two phases and shunts the dc-link current from the line currents. Although diode conduction changes the unfolder circuit behavior and may cause current distortion, when controlled properly, the diode conduction time can be leveraged to compensate for the limited DBSRC bandwidth.

Disregarding deviations from the ideal current relationship, to achieve the control objective, each DBSRC module is controlled to produce the desired dc-link current. In the feedforward controller, the module commands are directly generated from the references through a simple proportional gain. This method produces module output currents that rapidly track step reference changes, fully utilizing the available open-loop bandwidth, but does not correct for errors between actual and reference currents.

6.1 Integral Control

The sources of error can be deduced by studying the output circuit of a single DBSRC module in open loop as shown in Fig. 6.1. The circuit can be considered redrawn from Fig. 5.2, neglecting the influences from the second module, and merging the components of

two phases. The dc-link current i is affected by both the module output current \bar{i}_k and the dc-link capacitor current i_c ,

$$i = \bar{i}_k - i_c. \quad (6.1)$$

The error between i and reference current i_r can be contributed by both \bar{i}_k and i_c . Although the output current \bar{i}_k is primarily dependent on the applied command, it can still be affected by other factors, such as the output or dc-link voltage. Considering that such dependencies are minor due to the inherent insensitivity from output voltage to current in the DBSRC, error can still be caused by the capacitor current i_c . Neglecting L_g and R_g for simplicity, the capacitor current is

$$i_c \Big|_{\substack{L_g=0 \\ R_g=0}} = -C_k \frac{de}{dt}. \quad (6.2)$$

Thus, variation and distortion in the grid voltage e affect both i_c and i . It is considered as a disturbance on the dc-link current and is characterized by the following transfer function

$$G_{ic}(s) = \frac{i(s)}{e(s)} \Big|_{u=0} = - \frac{i_c(s)}{e(s)} \Big|_{u=0}. \quad (6.3)$$

The feedforward controller does not actively reject this disturbance, making the dc-link current easily affected by the grid voltage.

6.1.1 Controller Design

The tracking error between the reference and dc-link currents can be corrected by feedback control. A basic closed-loop controller is constructed in Fig. 6.2, by generating the

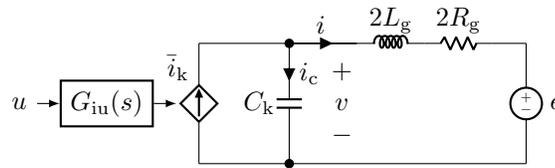


Fig. 6.1: Output port model of each DBSRC module in the unfolding converter.

module command from a compensator $K(s)$ that acts on the error between the reference and sensed currents. The current sensor is modeled by a second-order model,

$$H_i(s) = \frac{x_i(s)}{i(s)} = H_{i0} \frac{\omega_i^2}{(s + \omega_i)^2}. \quad (6.4)$$

The closed-loop converter block diagram is shown in Fig. 6.3. The compensator can be designed using the frequency-domain design approach based on the loop gain $L(s)$, which consists of sensor, compensator and converter plant dynamics,

$$L(s) = H_i(s)K(s)G_{iu}(s)G_{ii}(s), \quad (6.5)$$

where $G_{ii}(s)$ is the module output to dc-link current response.

The closed-loop reference to dc-link current response is

$$T_r(s) = \frac{i(s)}{i_r(s)} \Big|_{e=0} = \frac{H_{i0}}{H_i(s)} \frac{L(s)}{1 + L(s)}. \quad (6.6)$$

The closed-loop disturbance to dc-link current response is

$$T_w(s) = \frac{i(s)}{e(s)} \Big|_{i_r=0} = \frac{G_{ie}(s)}{1 + L(s)}. \quad (6.7)$$

Notice that the closed-loop $|T_w|$ is reduced over the open-loop $|G_{ie}|$ with a large loop gain, resulting in better disturbance rejection.

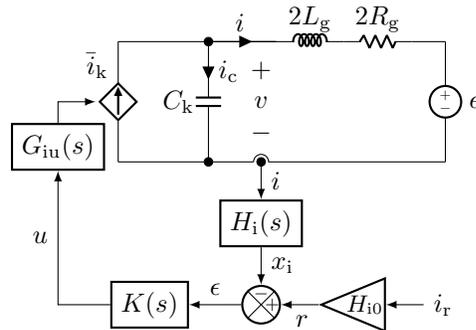


Fig. 6.2: Feedback control of each DBSRC module in the unfolding converter.

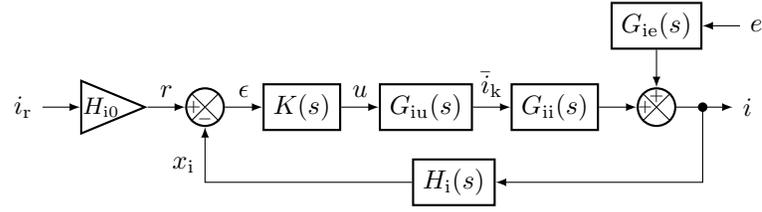


Fig. 6.3: Block diagram of a feedback controlled DBSRC module.

The compensator is selected as the integral type,

$$K(s) = \frac{K_e}{s}, \quad (6.8)$$

and the integral gain K_e is tuned to obtain a high closed-loop bandwidth for accurate reference tracking. Stability concerns usually limit the closed-loop bandwidth to several times lower than the open-loop bandwidth.

6.1.2 Controller Tuning

To evaluate the effectiveness of integral control, the compensator is designed for the 10-kVA unfolding converter. The DBSRC actuator model has a dc gain of $G_0 = 22$ and bandwidth of $f_k = 10$ kHz. The current sensor model has an attenuation of $H_{i0} = 0.05$ and bandwidth of $f_i = 10$ kHz. The converter component values are $C_k = 5 \mu\text{F}$, $L_g = 30 \mu\text{H}$ and $R_g = 0.1 \Omega$.

The integral gain is selected as $K_e = 5000$ to obtain a loop gain crossover frequency of about 1 kHz and phase margin of 70° , as shown in Fig. 6.4. A high crossover frequency is required for tracking of the reference current, which varies at 180 Hz. But further increase is difficult due to degradation in phase margin.

The closed-loop reference to dc-link current response is shown in Fig. 6.5. It has a unity gain and provides accurate reference tracking up to a closed-loop bandwidth of about 1 kHz. But notice that its phase drops to -10° at 180 Hz. This will result in a phase error between actual and reference currents.

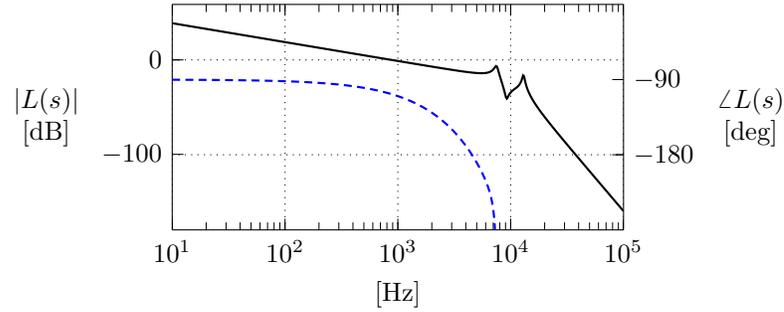


Fig. 6.4: Bode plot of loop gain $L(s)$ with integral gain of $K_e = 5000$.

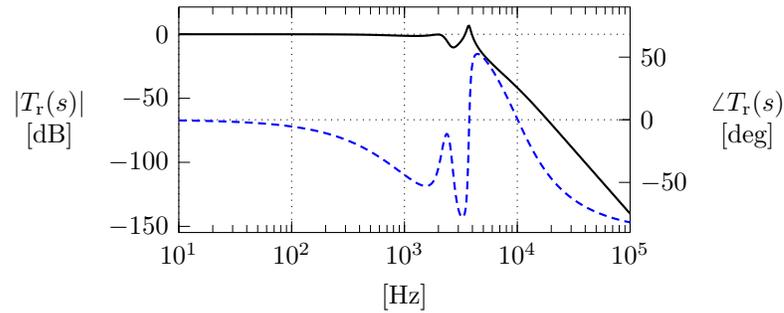


Fig. 6.5: Bode plot of closed-loop reference to dc-link current response $T_r(s)$ with integral gain of $K_e = 5000$.

The closed-loop and open-loop disturbance to dc-link current responses are compared in Fig. 6.6. There is a reduction of 15 dB at 180 Hz using integral control.

6.1.3 Simulation Results

The designed integral controller is verified in simulation with the unfolded implemented with circuit model and the DBSRC implemented with actuator model. The simulation is constructed as shown in Fig. 6.7. The simulation is conducted using the selected integral gain of $K_e = 5000$ and same sensor and converter plant parameters used in controller tuning. They are grid voltage $E_m = 392$ V and frequency $f = 60$ Hz, line inductance $L_g = 30$ μ H and resistance $R_g = 0.1$ Ω , dc-link capacitance $C_k = 5$ μ F, DBSRC dc gain $G_0 = 22$ and bandwidth $f_k = 10$ kHz, current sensor attenuation $H_{i0} = 0.05$ and bandwidth $f_i = 10$ kHz.

The simulation is first conducted at unity power factor and reduced power of 3 kW, by setting the reference currents to $I_{rd} = 5$ A and $I_{rq} = 0$ A. The simulated Phase-A

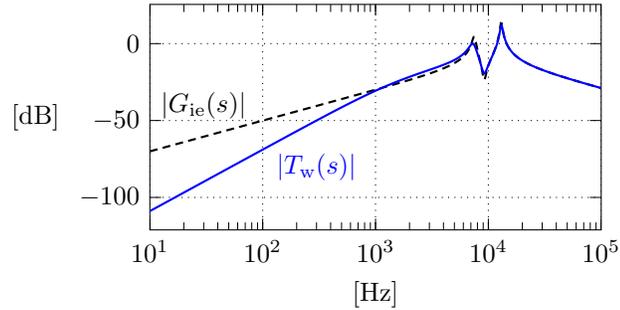


Fig. 6.6: Magnitude plots of open-loop and closed-loop grid voltage to dc-link current responses, $G_{ie}(s)$ and $T_w(s)$, with integral gain of $K_e = 5000$.

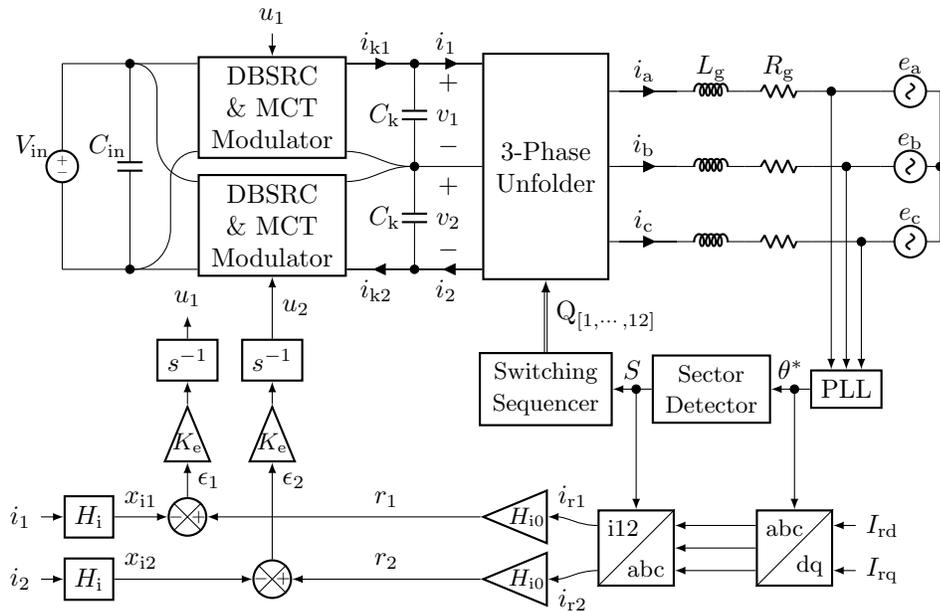


Fig. 6.7: Unfolding converter with integral feedback control.

current is compared to that in the feedforward controlled converter in Fig. 6.8. Notice that amplitude and phase differences exist between the reference and actual feedforward controlled line currents, otherwise known as steady-state amplitude and phase errors [24]. Operating at reduced power amplifies these errors in the feedforward controlled line current, as the capacitor current becomes more dominant. In contrast, the integral controller reduces these errors so that the actual line current more closely follows its reference.

Two weaknesses are associated with integral control. The first is a small but noticeable phase error, primarily due to limited tracking performance with the integral controller. This

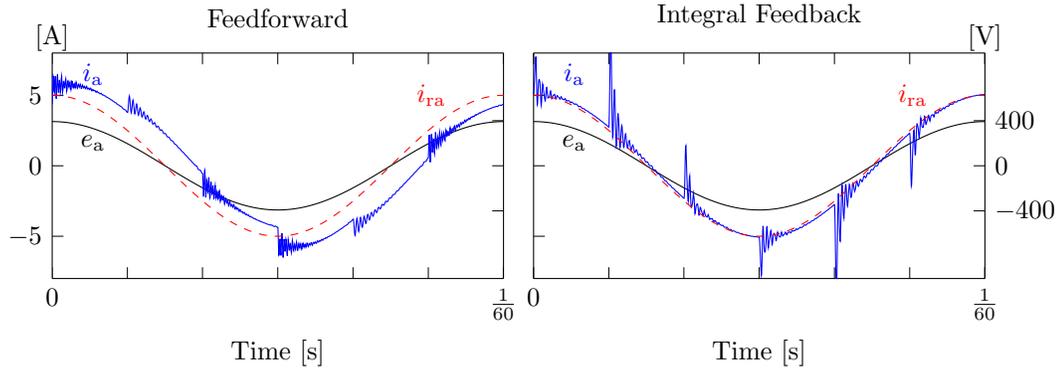


Fig. 6.8: Simulation results comparing reference and actual line currents with feedforward and integral feedback controllers, at unity power factor and low (30%) power to highlight error due to capacitor current.

has been observed from the phase plot of $T_r(s)$ in Fig. 6.5, as a small but negative phase exists at 180 Hz. Further increasing the integral gain may reduce the phase error but will likely compromise stability.

Another weakness with the integral controller is the increased current distortion at sector beginnings. It is primarily contributed by the slow closed-loop response. This weakness is further exposed in Fig. 6.9, as the converter is operated at power factor of 0.7 (inductive), with $I_{rd} = -I_{rq} = 12$ A. The feedforward controller fully utilizes the DBSRC bandwidth of 10 kHz and can produce higher-quality line current, with appropriate sector adjustments. In comparison, the integral controller has to limit the closed-loop bandwidth to 1 kHz to avoid instability and as a result slowed down the DBSRC response.

6.2 State and Output Feedback

Previously, the merit of integral over feedforward control has been demonstrated as the correction of current error due to grid voltage disturbance. Drawbacks of the integral controller has been summarized as non-minimal error and high distortion due to limited tracking performance.

Another shortcoming with both controllers is the inability to damp oscillation between line inductor and dc-link capacitor. Without adding a physical damping network, the oscillation is only damped by the grid resistance in these two systems. Prolonged oscillation

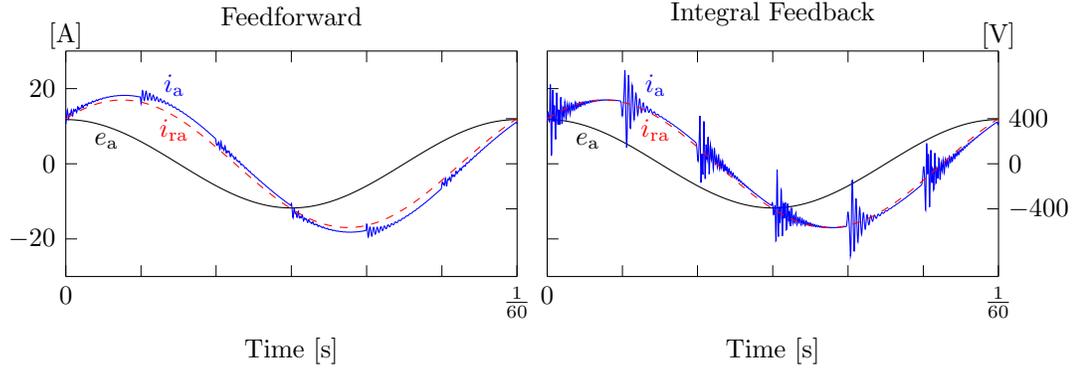


Fig. 6.9: Simulation results comparing actual line currents with feedforward and integral feedback controllers, at power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12$ A, to highlight higher distortion due to slower closed-loop response.

or even instability can occur especially with large inductance values. A larger than designed line inductance is often encountered in installed converters due to factors such as extra inductors added for more current filtering, leakage inductance of a utility transformer or winding inductance of a motor-generator.

This is visualized from the pole locations and their damping ratios of the feedforward and integral controlled 10-kVA unfolding converter in Fig. 6.10, where the line inductance is increased from the original $30 \mu\text{H}$ to $300 \mu\text{H}$. With feedforward control, the dominant poles at

$$\frac{1}{2\pi\sqrt{3L_g C_k}} = 2.4 \text{ kHz} \quad \text{and} \quad \frac{1}{2\pi\sqrt{L_g C_k}} = 4.1 \text{ kHz} \quad (6.9)$$

have minimal damping ratios of 0.006 and 0.01, respectively. With integral control, these poles are moved to the right half plane, making the converter unstable.

6.2.1 Controller Design

State feedback control can be used to increase damping ratio and stabilize a system. The states associated with the dominant poles are the two dc-link currents and voltages. The dc-link currents have been sensed and controlled to track the references, and the current sensor dynamics have been provided. Each dc-link voltage has also been sensed and used in the DBSRC MCT modulator. Thus, the existing sensors provide enough information on

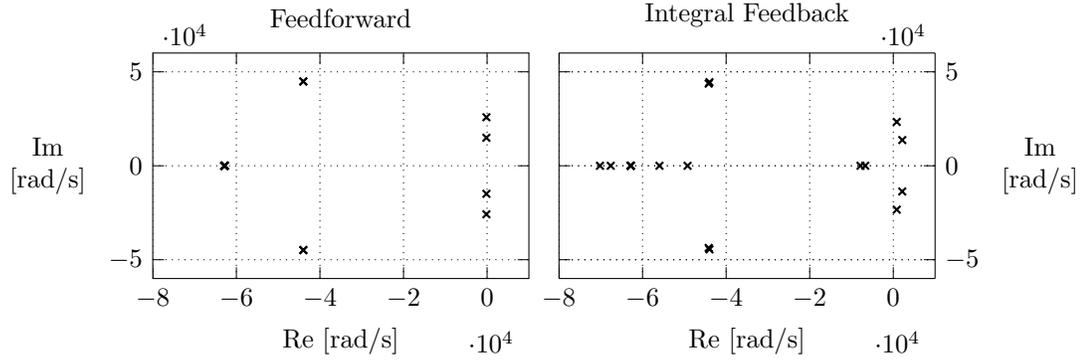


Fig. 6.10: Pole locations of feedforward and integral controlled unfolding converters with a large line inductance of $300 \mu\text{H}$.

the critical states, and no new sensors are needed. The voltage sensor is modeled similarly as the current sensor,

$$H_v(s) = \frac{x_v(s)}{v(s)} = H_{v0} \frac{\omega_v^2}{(s + \omega_v)^2}. \quad (6.10)$$

To facilitate state feedback design, the converter plant model in Equation 5.14 is augmented with the current and voltage sensor states,

$$\dot{\hat{\mathbf{x}}}_p = \hat{\mathbf{A}}_p \hat{\mathbf{x}}_p + \hat{\mathbf{B}}_p \mathbf{u} + \hat{\mathbf{E}} \mathbf{w}. \quad (6.11)$$

The state vector $\hat{\mathbf{x}}_p$ of the augmented plant contains sixteen states and is defined as

$$\hat{\mathbf{x}}_p = \begin{bmatrix} x_{i1} & x_{i2} & x_{v1} & x_{v2} & x'_{i1} & x'_{i2} & x'_{v1} & x'_{v2} \\ i_1 & i_2 & v_1 & v_2 & \bar{i}_{k1} & \bar{i}_{k2} & \bar{i}'_{k1} & \bar{i}'_{k2} \end{bmatrix}^T, \quad (6.12)$$

where the first four states are current and voltage sensor outputs. The next four states are their derivatives. The remaining eight states are same as and brought over from \mathbf{x}_p in the original plant. The coefficient matrix $\hat{\mathbf{A}}_p$ is obtained from \mathbf{A}_p by augmenting it with parameters describing the sensor dynamics. The other two coefficient matrices $\hat{\mathbf{B}}_p$ and $\hat{\mathbf{E}}$ are adjusted from \mathbf{B}_p and \mathbf{E} by filling with zeros. The outputs of the augmented plant are

selected as the sensed currents and voltages

$$\hat{\mathbf{y}}_p = \begin{bmatrix} x_{i1} & x_{i2} & x_{v1} & x_{v2} \end{bmatrix}^\top = \hat{\mathbf{C}}_p \hat{\mathbf{x}}_p = \begin{bmatrix} \mathbf{I}_4 & \mathbf{0} \end{bmatrix} \hat{\mathbf{x}}_p. \quad (6.13)$$

State feedback alone provides stability but no error correction. The integral compensation is retained to provide error correction and reference tracking. The result is an integral state feedback controller as shown in Fig. 6.11. The error vector is

$$\mathbf{e} = \mathbf{r} - \begin{bmatrix} x_{i1} \\ x_{i2} \end{bmatrix} = \mathbf{r} - \mathbf{C}_i \hat{\mathbf{x}}_p = \mathbf{r} - \begin{bmatrix} \mathbf{I}_2 & \mathbf{0} \end{bmatrix} \hat{\mathbf{x}}_p. \quad (6.14)$$

The plant control input is contributed by both the integral compensator and state feedback

$$\mathbf{u} = \mathbf{K}_e \int \mathbf{e} dt - \mathbf{K}_x \hat{\mathbf{x}}_p. \quad (6.15)$$

The gain matrices \mathbf{K}_e and \mathbf{K}_x shall be designed to drive the error \mathbf{e} and state derivative $\dot{\hat{\mathbf{x}}}_p$ to zero. This is achieved by designing a state feedback for the plant augmented with error states

$$\dot{\mathbf{z}} = \begin{bmatrix} -\dot{\mathbf{e}} \\ \ddot{\hat{\mathbf{x}}}_p \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \mathbf{C}_i \\ \mathbf{0} & \hat{\mathbf{A}}_p \end{bmatrix} \begin{bmatrix} -\mathbf{e} \\ \dot{\hat{\mathbf{x}}}_p \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \hat{\mathbf{B}}_p \end{bmatrix} \dot{\mathbf{u}} = \mathbf{A}_z \mathbf{z} + \mathbf{B}_z \dot{\mathbf{u}}. \quad (6.16)$$

The state feedback is

$$\dot{\mathbf{u}} = -\mathbf{K}_z \mathbf{z} = - \begin{bmatrix} \mathbf{K}_e & \mathbf{K}_x \end{bmatrix} \begin{bmatrix} -\mathbf{e} \\ \dot{\hat{\mathbf{x}}}_p \end{bmatrix}. \quad (6.17)$$

The resulting closed-loop system is described as

$$\dot{\mathbf{z}} = \mathbf{F}_z \mathbf{z} = (\mathbf{A}_z - \mathbf{B}_z \mathbf{K}_z) \mathbf{z}. \quad (6.18)$$

The state feedback gain matrix \mathbf{K}_z can be obtained using a linear quadratic regulator (LQR) design based on weight matrices \mathbf{Q} and \mathbf{R} . In actual controller implementation, only the two error states in \mathbf{e} and first four sensor states in $\hat{\mathbf{x}}_p$ are available. Thus, it is

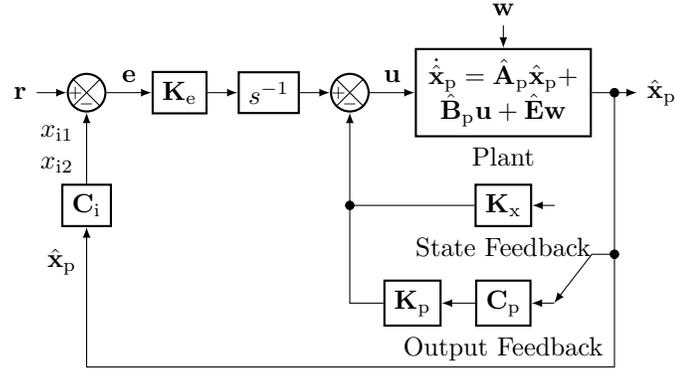


Fig. 6.11: Block diagram of a state and output feedback controlled unfolding converter.

necessary to modify the full state feedback into an output feedback design, using a partial number of states. There are several suitable methods, but the common goal is to retain as much of the closed-loop dynamics of the state feedback system as possible. In a static output feedback approach, a static gain is used [83],

$$\dot{\mathbf{u}} = -\mathbf{K}_y \mathbf{y} = -\mathbf{K}_y \mathbf{C}_z \mathbf{z}, \quad (6.19)$$

where the output coefficient matrix is $\mathbf{C}_z = [\mathbf{I}_6 \quad \mathbf{0}]$ in the considered system and assigns the available states for output feedback. This results in the following closed-loop system,

$$\dot{\mathbf{z}} = \mathbf{F}_y \mathbf{z} = (\mathbf{A}_z - \mathbf{B}_z \mathbf{K}_y \mathbf{C}_z) \mathbf{z}. \quad (6.20)$$

With $n_y = 6$ outputs, the same number of eigenvalues and their associated eigenvectors (out of $n_z = 18$) can be retained from the state feedback system,

$$\mathbf{F}_y \mathbf{V}_y = \mathbf{F}_z \mathbf{V}_y = \mathbf{V}_y \mathbf{\Lambda}_y, \quad (6.21)$$

where $\mathbf{\Lambda}_y$ is a diagonal matrix of the n_y eigenvalues to be retained, and each column in \mathbf{V}_y contains the corresponding eigenvector. The output feedback gain matrix is then solved by

algebraic manipulation,

$$\mathbf{K}_y = \mathbf{K}_z \mathbf{V}_y (\mathbf{C}_z \mathbf{V}_y)^{-1} = \begin{bmatrix} \mathbf{K}_e & \mathbf{K}_p \end{bmatrix}. \quad (6.22)$$

In actual design, the output feedback gains are selected to retain the dominant eigenvalues or poles in the state feedback system.

6.2.2 Controller Tuning

The state feedback gains are generated using the LQR method based on diagonal weight matrices configured as

$$\mathbf{Q} = \begin{bmatrix} q_e \mathbf{I}_2 & & \\ & q_i \mathbf{I}_2 & \\ & & \mathbf{0} \end{bmatrix} \quad \text{and} \quad \mathbf{R} = \mathbf{I}_2, \quad (6.23)$$

where \mathbf{Q} and \mathbf{R} penalize the states and control inputs, respectively. The applied tuning procedure fixes \mathbf{R} while adjusts parameters in \mathbf{Q} . The parameter q_i applies equal penalties to the two sensed currents x_{i1} and x_{i2} . The parameter q_e applies equal penalties to the two errors states in \mathbf{e} . Intuitively, increasing q_e produces gains that reduce the errors.

The state feedback gains are now tuned for the 10-kVA unfolding converter plant with the following values, circuit of $L_g = 300 \mu\text{H}$, $R_g = 0.1 \Omega$ and $C_k = 5 \mu\text{F}$, DBSRC actuator of $G_0 = 22$ and $f_k = 10 \text{ kHz}$, sensors of $H_{i0} = 0.05$, $H_{v0} = 1.5 \times 10^{-3}$ and $f_i = f_v = 10 \text{ kHz}$. The tuning methodology is to first apply the largest possible q_e without making the system unstable and to obtain a high closed-loop bandwidth. Next, q_i is increased to damp the dominant poles and not degrade the bandwidth. The final values are $q_e = 10^8$ and $q_i = 0$. The closed-loop poles, or eigenvalues of \mathbf{F}_z , are visualized in Fig. 6.12. The six dominant poles at 1.3, 1.6, 2.7 and 4.3 kHz have damping ratios of 1, 1, 0.23 and 0.15, respectively. Notice the increased damping on poles at 2.7 and 4.3 kHz compared to feedforward control, demonstrating effectiveness of state feedback.

After the state feedback gains are obtained, they are converted to output feedback

gains by retaining the six dominant poles in the closed-loop system using the available states. This results in the following integral and output feedback gain matrices,

$$\mathbf{K}_e = \begin{bmatrix} 2980 & 0 \\ 0 & 2980 \end{bmatrix} \quad \text{and} \quad \mathbf{K}_p = \begin{bmatrix} -0.2 & 0 & 1 & 0 \\ 0 & -0.2 & 0 & 1 \end{bmatrix}, \quad (6.24)$$

where the off-diagonal gains are small and have been removed to simplify implementation. The closed-loop poles with these output feedback gains also shown in Fig. 6.12. Notice the same locations of the six dominant poles compared to the state feedback system, verifying the output feedback design.

Although using output feedback ensures stability, the closed-loop system can become more sensitive to disturbance. This is seen by comparing the grid voltage to current response, $\frac{i_1(s)}{e_1(s)}$, between feedforward and output feedback controllers in Fig. 6.13. Notice that the disturbance rejection is worsened by 6 dB with output feedback.

6.2.3 Simulation Results

The designed output feedback controller is verified in simulation with the unfolded implemented with circuit model and the DBSRC implemented with actuator model. The simulation is constructed as shown in Fig. 6.14. The largest source of disturbance is the periodic variation in the grid voltage. To reduce its effect on current, the estimated voltage

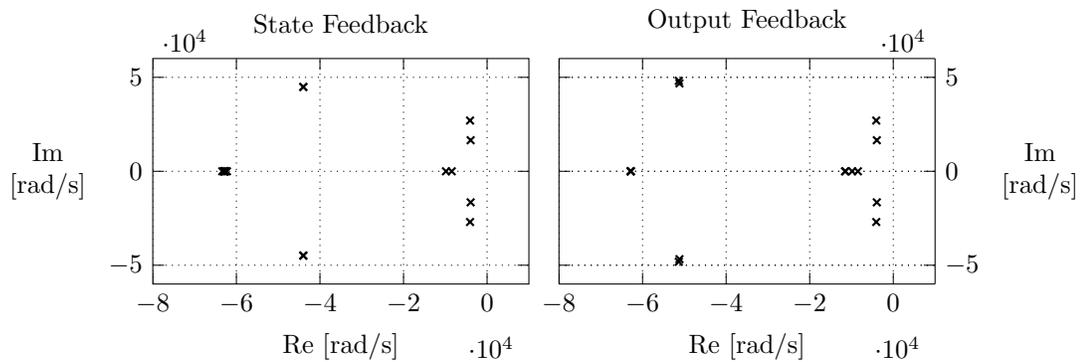


Fig. 6.12: Pole locations of state and output feedback controlled unfolding converter with a large line inductance of $300 \mu\text{H}$.

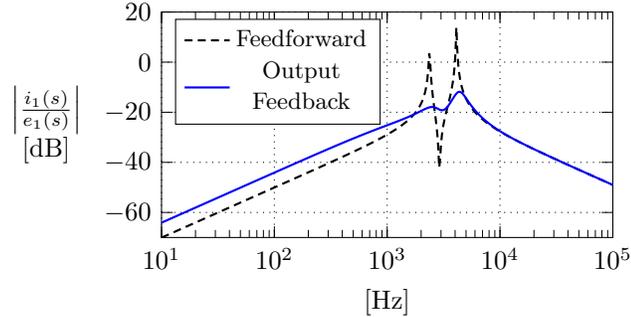


Fig. 6.13: Comparison of grid voltage to current response, $\frac{i_1(s)}{e_1(s)}$, between feedforward and output feedback controllers.

is fed forward in command generation. The simulation is conducted using the selected gains in Equation 6.24 and same sensor and converter plant parameters used in controller tuning. They are grid voltage $E_m = 392$ V and frequency $f = 60$ Hz, line inductance $L_g = 300$ μ H and resistance $R_g = 0.1$ Ω , dc-link capacitance $C_k = 5$ μ F, DBSRC dc gain $G_0 = 22$ and bandwidth $f_k = 10$ kHz, sensors of $H_{i0} = 0.05$, $H_{v0} = 1.5 \times 10^{-3}$ and $f_i = f_v = 10$ kHz.

The simulated line current at unity power factor and 10 kW is shown in Fig. 6.15. It is compared with the feedforward controller with the same converter plant parameters. Notice the sustained current oscillation with feedforward control that is excited at beginning of each sector. In comparison, using output feedback damps any potential oscillation and improves current quality. The results verify the closed-loop stability ensured by using output feedback. In contrast, the previous integral controller is unstable at this line inductance of 300 μ H.

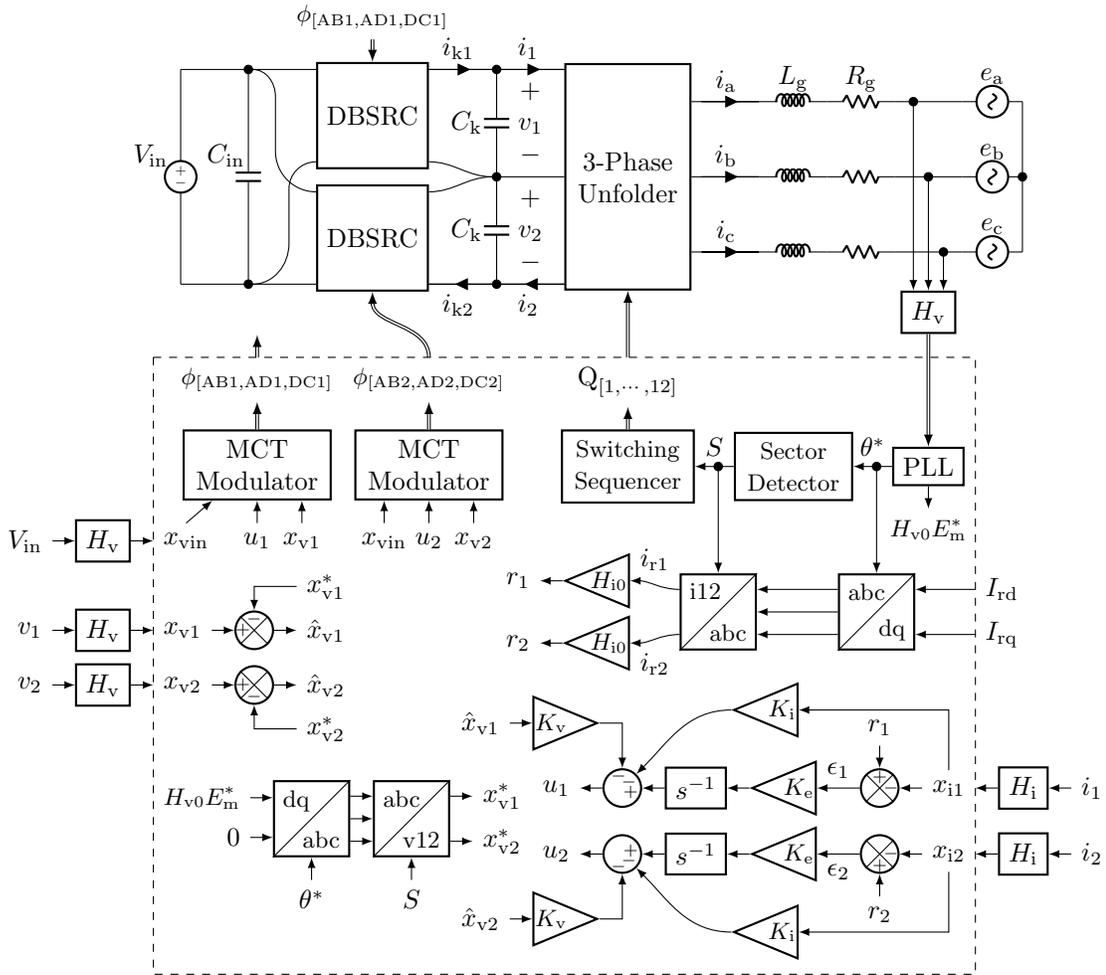


Fig. 6.14: Unfolding converter with output feedback controller and feedforward of estimated dc-link voltages.

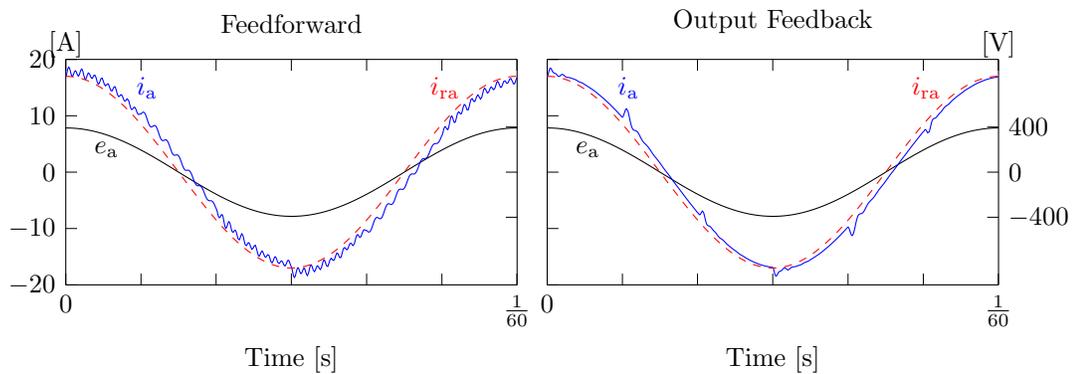


Fig. 6.15: Comparison of simulated line currents between feedforward and output feedback controllers with a large line inductance of $300 \mu\text{H}$ and operating at unity power factor and 10 kW.

6.3 Summary

This chapter provides feedback controller designs to address the lack of error correction and weak damping of current oscillation in the previous feedforward controlled unfolding converter. The sources of error between actual and reference dc-link currents are identified, using a single DBSRC module. A basic feedback controller is introduced by applying integral action on the errors. The basic design methodology is to apply a high integral gain to obtain a high closed-loop bandwidth for accurate tracking of the time-varying reference.

The high gain makes the system prone to instability, especially with large line inductances. Using state feedback together with the integral compensator retains benefit of error correction and improves stability but requires access to all plant states. The state feedback performance is maintained by retaining the dominant closed-loop poles using an appropriate output feedback design. Simulation results verify the error-correcting and oscillation-damping capabilities of the feedback controllers.

CHAPTER 7

CONTROL IN SYNCHRONOUS ROTATING FRAME

The previous feedback controllers in Chapter 6 all act directly on the time-varying quantities in a stationary reference frame. Their shortcomings are summarized below.

- The existence of a steady-state tracking error, which is exemplified by a phase difference between actual and reference line currents, as observed in simulation results. Although increasing the closed-loop bandwidth can reduce the tracking error, some phase difference always exists, as seen from the Bode plot of the closed-loop transfer function.
- The low current quality especially at non-unity power factors. A low closed-loop bandwidth degrades current quality.

Feedforward control provides higher current quality at non-unity power factors. The benefits of feedforward and feedback controllers can be combined in a rotating reference frame synchronized to the grid voltage. The applied converter commands are no longer limited by the closed-loop bandwidth at sector beginnings, as the time-varying command trajectory is fed forward by the transformation block based on the phase angle. Combined with appropriate adjustments to the unfold and command sectors, this approach improves current quality at non-unity power factors, even with small line inductances. In addition, the application of output feedback becomes less prone to periodic variation of the grid voltage, while still improving stability with large line inductances.

7.1 Line-Side Component Models

To design the rotating-frame controller, a suitable plant model in rotating frame needs to be derived.

7.1.1 DBSRC Output Currents

The DBSRC output current has been modeled as a dependent current source \bar{i}_k that is controlled by command u . Neglecting other contribution to \bar{i}_k from disturbances, it becomes solely dependent on u , based on a second-order actuator model $G_{iu}(s)$. The two current sources \bar{i}_{k1} and \bar{i}_{k2} exist in the dc link, and produce the line currents (i_{ka} , i_{kb} , i_{kc}) through the unfolder, as shown in Fig. 7.1. The modeling objective is to push sources \bar{i}_{k1} and \bar{i}_{k2} to the line side and form three equivalent sources (i_{ka} , i_{kb} , i_{kc}), as shown in Fig. 7.2.

The unfolder itself can be viewed as a transformation that converts the dc-link currents into line currents. The transformation is based on the current relationship identified in each unfolder sector. The relationship is valid as long as the clamping diodes do not conduct. The relationship is different in each sector, making the unfolder only piecewise linear, and necessitating the use of a different output matrix for each sector in the piecewise linear model.

The nonlinearity can be linearized by considering the generation of commands u_1 and u_2 via an inverse transformation from a balanced combination of u_a , u_b and u_c , or $u_a + u_b + u_c = 0$. Consider in Sector 1, where $i_{ka} = \bar{i}_{k1}$ in the unfolder, and $u_1 = u_a$ in the command transformation. The command and current are related via $\bar{i}_{k1} = G_{iu}(s)u_1$. Considering all three relationships, the overall response from u_a to i_{ka} becomes $i_{ka} = G_{iu}(s)u_a$. The same analysis can be performed on the remaining phases and sectors. The conclusion is that each phase current is related to the corresponding command by $G_{iu}(s)$, resulting in a linearized

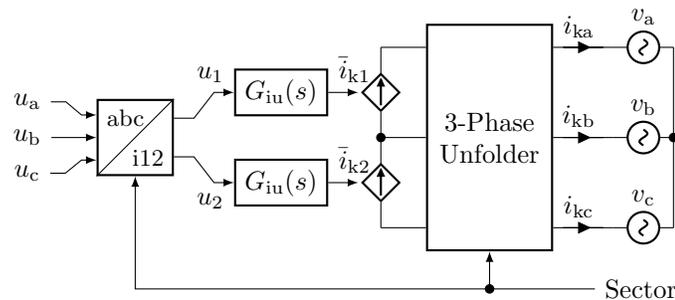


Fig. 7.1: Partial unfolding converter plant model with DBSRC commands generated using three-phase components.

model in Fig. 7.2.

The linearization is possible by making use of the two-way validity on the unfold current relationship. It shall be noted that this equivalent model assumes non-conduction of the clamping diode, whose conduction time is short enough given a high open-loop bandwidth and can be neglected when considering longer term dynamics. If diode conduction is of concern, especially when studying converter behavior at sector beginnings, the piecewise linear model shall be used.

7.1.2 DC-Link Capacitors

The next step in the modeling process is to push the dc-link capacitors to the line side. This starts by considering a basic system with only capacitors in the dc link, as shown in Fig. 7.3. They are periodically charged and discharged by the grid voltages through the unfold. Using the established unfold current relationship in each sector, the line currents can be derived from the dc-link currents, which in this case are solely dependent on the capacitor currents.

Consider first a case of three capacitors in the dc link, each with capacitance C_k . In Sector 1, the Phase-A current can be expressed as

$$\begin{aligned}
 i_a = i_1 &= -i_{c1} - i_{c3} \\
 &= -C_k \frac{d}{dt} v_{ab} - C_k \frac{d}{dt} (v_{ab} + v_{bc}) \\
 &= -3C_k \frac{dv_a}{dt},
 \end{aligned} \tag{7.1}$$

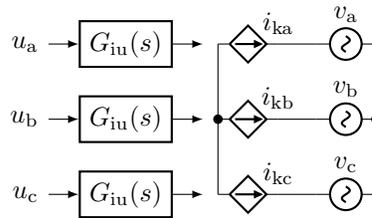


Fig. 7.2: Linearized partial unfolding converter plant model with equivalent line-side DB-SRC output currents.

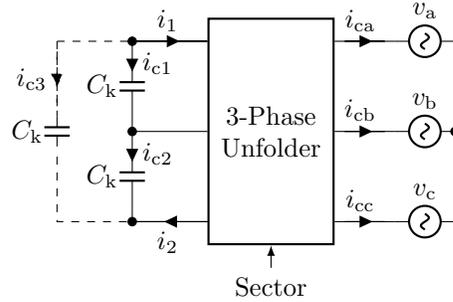


Fig. 7.3: Partial unfolding converter plant model with only dc-link capacitors.

where the last step assumes balanced grid voltages, $v_a + v_b + v_c = 0$. The same analysis can be performed on the remaining phases and sectors. The conclusion is that the same relationship always holds, resulting in an equivalent circuit in Fig. 7.4. The three dc-link capacitors can be equivalently represented by three wye-connected capacitors on the line side each having capacitance of $3C_k$, which produce the same line currents. Note that with ideal grid voltage, the current in each equivalent line-side capacitor is smooth, while that in each actual dc-link capacitor contains steps at sector beginnings, due to changes in the slope of its the dc-link voltage. The addition of a third dc-link capacitor balances the current steps in the existing two capacitors, making the overall current appears smooth.

In the actual converter, this third dc-link capacitor is to be avoided, as it adds extra volume. The line currents due to only two dc-link capacitors are re-derived. To facilitate a comparison with the prior case with three capacitors, ideal grid voltage is assumed. To reveal the symmetry in capacitor currents among odd and even sectors, a new angle σ is

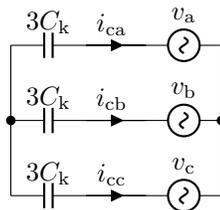


Fig. 7.4: Equivalent line-side model of the dc-link capacitors.

introduced and limited to $\frac{\pi}{3}$ and reset to zero at sector beginnings,

$$\sigma = \text{mod} \left(\omega t, \frac{\pi}{3} \right), \quad 0 < \sigma < \frac{\pi}{3}. \quad (7.2)$$

In Sector 1, the Phase-A current is

$$\begin{aligned} i_{ca} = i_1 = -i_{c1} \\ &= -C_k \frac{d}{dt} v_{ab} \\ &= -C_k \frac{d}{dt} \left[\sqrt{3} V_m \cos \left(\sigma + \frac{\pi}{6} \right) \right] \\ &= \sqrt{3} V_m \omega C_k \sin \left(\sigma + \frac{\pi}{6} \right). \end{aligned} \quad (7.3)$$

Similarly, the Phase-C current is

$$\begin{aligned} i_{cc} = -i_2 = i_{c2} \\ &= C_k \frac{d}{dt} v_{bc} \\ &= C_k \frac{d}{dt} \left[\sqrt{3} V_m \cos \left(\sigma - \frac{2\pi}{3} + \frac{\pi}{6} \right) \right] \\ &= \sqrt{3} V_m \omega C_k \cos(\sigma). \end{aligned} \quad (7.4)$$

Finally, the Phase-B current is

$$i_{cb} = i_{c1} - i_{c2} = -3V_m \omega C_k \sin \left(\sigma + \frac{\pi}{3} \right). \quad (7.5)$$

Note the different magnitudes among the phase currents in Sector 1, where Phases A and C are smaller than B. In comparison, the phase currents with a third dc-link capacitor all have the same magnitude. The same analysis is applied to other sectors, and the results are summarized in Table 7.1. It is noted that each dc-link capacitor current has the same variation among odd sectors and another variation among even sectors. The difference in variations causes step changes in the phase currents at sector beginnings.

To facilitate deriving an equivalent line-side circuit with only two dc-link capacitors, its

Table 7.1: DC-link capacitor current in each unfolder sector assuming ideal grid voltages, where $\sigma = \text{mod}(\omega t, \frac{\pi}{3})$, $I_{\text{cm}} = 3V_m\omega C_k$, $i_{c\alpha} = -\frac{\sqrt{3}}{3}I_{\text{cm}}\sin(\sigma + \frac{\pi}{6})$, $i_{c\beta} = \frac{\sqrt{3}}{3}I_{\text{cm}}\cos(\sigma)$, $i_{c\gamma} = I_{\text{cm}}\sin(\sigma + \frac{\pi}{3})$.

Sector	$i_{c1} =$	$i_{c2} =$	$i_{ca} =$	$i_{cb} =$	$i_{cc} =$
1	$i_{c\alpha}$	$i_{c\beta}$	$-i_{c\alpha}$	$-i_{c\gamma}$	$i_{c\beta}$
2	$i_{c\beta}$	$i_{c\alpha}$	$i_{c\gamma}$	$-i_{c\beta}$	$i_{c\alpha}$
3	$i_{c\alpha}$	$i_{c\beta}$	$i_{c\beta}$	$-i_{c\alpha}$	$-i_{c\gamma}$
4	$i_{c\beta}$	$i_{c\alpha}$	$i_{c\alpha}$	$i_{c\gamma}$	$-i_{c\beta}$
5	$i_{c\alpha}$	$i_{c\beta}$	$-i_{c\gamma}$	$i_{c\beta}$	$-i_{c\alpha}$
6	$i_{c\beta}$	$i_{c\alpha}$	$-i_{c\beta}$	$i_{c\alpha}$	$i_{c\gamma}$

Phase-A current over a line period is shown in Fig. 7.5a. In comparison to the current with three dc-link capacitors, the two currents share the same peak value of $3V_m\omega C_k$. Thus, it is expected they will have similar fundamental component values. To confirm, its frequency spectrum is shown in Fig. 7.5b. Its fundamental component is 94% of the sinusoidal current with three capacitors. Thus, it is concluded that the same equivalent circuit in Fig. 7.4 can be used to model a system with only two dc-link capacitors.

7.2 Three-Phase Converter Model

Using the equivalent line-side models of the DBSRC and dc-link capacitors, the unfolding converter plant can be modeled with a three-phase model depicted using a per-phase circuit shown in Fig. 7.6. The process to model a three-phase plant in rotating frame is to first derive the three-phase dynamic equations and group them by the same states such as current and voltage, and then transform each state equation into rotating frame, and finally combine them to obtain the complete model in rotating frame.

The amplitude-invariant Park transformation is used [84],

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \mathbf{K}_r \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}. \quad (7.6)$$

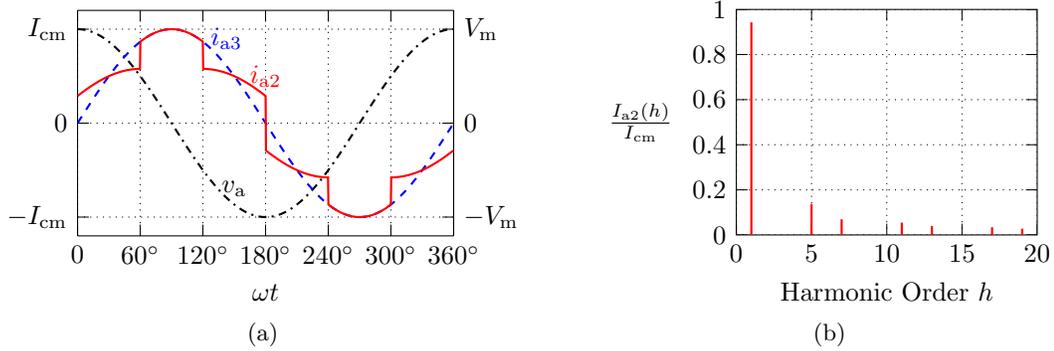


Fig. 7.5: Phase-A current due to charge and discharge of the dc-link capacitors by the grid voltage. (a) Comparison of the time-domain current waveforms due to two and three dc-link capacitors, i_{a2} and i_{a3} . (b) Frequency spectrum of i_{a2} , normalized to I_{cm} .

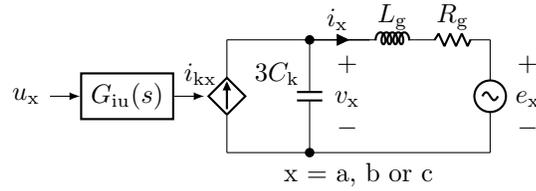


Fig. 7.6: Per-phase equivalent circuit of the three-phase unfolding converter plant.

The inverse transformation is defined as

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \mathbf{K}_r^{-1} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix}. \quad (7.7)$$

The three-phase dynamic equations based on the per-phase equivalent circuit in Fig. 7.6, excluding the DBSRC dynamics, are

$$\frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = -\frac{R_g}{L_g} \mathbf{I}_3 \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L_g} \mathbf{I}_3 \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \frac{1}{L_g} \mathbf{I}_3 \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (7.8)$$

and

$$\frac{d}{dt} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = -\frac{1}{3C_k} \mathbf{I}_3 \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{3C_k} \mathbf{I}_3 \begin{bmatrix} i_{ka} \\ i_{kb} \\ i_{kc} \end{bmatrix}. \quad (7.9)$$

Transform the dynamic equation on line currents by expressing the three-phase quantities in their dq0 equivalent and multiplying both sides of the equation by \mathbf{K}_r ,

$$\mathbf{K}_r \frac{d}{dt} \left(\mathbf{K}_r^{-1} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \right) = -\frac{R_g}{L_g} \mathbf{K}_r \mathbf{K}_r^{-1} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \frac{1}{L_g} \mathbf{K}_r \mathbf{K}_r^{-1} \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} - \frac{1}{L_g} \mathbf{K}_r \mathbf{K}_r^{-1} \begin{bmatrix} e_d \\ e_q \\ e_0 \end{bmatrix}, \quad (7.10)$$

where in simplifying the derivative, the following general formula is used,

$$\mathbf{K}_r \frac{d}{dt} (\mathbf{K}_r^{-1}) = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}. \quad (7.11)$$

The same process is applied to derive the dynamic equation of the line voltages in rotating frame. The current and voltage equations are then combined to obtain the complete plant model excluding DBSRC dynamics,

$$\frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ v_d \\ v_q \end{bmatrix} = \begin{bmatrix} -\frac{R_g}{L_g} & \omega & \frac{1}{L_g} & 0 \\ -\omega & -\frac{R_g}{L_g} & 0 & \frac{1}{L_g} \\ -\frac{1}{3C_k} & 0 & 0 & \omega \\ 0 & -\frac{1}{3C_k} & -\omega & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ v_d \\ v_q \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{3C_k} & 0 \\ 0 & \frac{1}{3C_k} \end{bmatrix} \begin{bmatrix} i_{kd} \\ i_{kq} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L_g} & 0 \\ 0 & -\frac{1}{L_g} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} e_d \\ e_q \end{bmatrix}. \quad (7.12)$$

Note that the x_0 terms are discarded because all three-phase quantities are assumed to be balanced, $x_a + x_b + x_c = 0$.

To facilitate subsequent controller design in rotating frame, the actuator and sensor dynamics are also transformed into their rotating-frame equivalents. Consider the actuator

model from Fig. 7.2,

$$\begin{bmatrix} i_{ka} \\ i_{kb} \\ i_{kc} \end{bmatrix} = \begin{bmatrix} G_{iu}(s) & 0 & 0 \\ 0 & G_{iu}(s) & 0 \\ 0 & 0 & G_{iu}(s) \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}, \quad (7.13)$$

where $G_{iu}(s)$ is the previous second-order model used to approximate the DBSRC control to output current response,

$$G_{iu}(s) = G_0 \frac{\omega_k^2}{s^2 + 2\zeta\omega_k s + \omega_k^2}. \quad (7.14)$$

The three-phase state equations of the actuator model can then be written as

$$\frac{d}{dt} \begin{bmatrix} i_{ka} \\ i_{kb} \\ i_{kc} \end{bmatrix} = \begin{bmatrix} i'_{ka} \\ i'_{kb} \\ i'_{kc} \end{bmatrix} \quad (7.15)$$

and

$$\frac{d}{dt} \begin{bmatrix} i'_{ka} \\ i'_{kb} \\ i'_{kc} \end{bmatrix} = -\omega_k^2 \mathbf{I}_3 \begin{bmatrix} i_{ka} \\ i_{kb} \\ i_{kc} \end{bmatrix} - 2\zeta\omega_k \mathbf{I}_3 \begin{bmatrix} i'_{ka} \\ i'_{kb} \\ i'_{kc} \end{bmatrix} + G_0\omega_k^2 \mathbf{I}_3 \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}. \quad (7.16)$$

This set of state equations is then transformed into the rotating frame,

$$\frac{d}{dt} \begin{bmatrix} i_{kd} \\ i_{kq} \\ i'_{kd} \\ i'_{kq} \end{bmatrix} = \begin{bmatrix} 0 & \omega & 1 & 0 \\ -\omega & 0 & 0 & 1 \\ -\omega_k^2 & 0 & -2\zeta\omega_k & \omega \\ 0 & -\omega_k^2 & -\omega & -2\zeta\omega_k \end{bmatrix} \begin{bmatrix} i_{kd} \\ i_{kq} \\ i'_{kd} \\ i'_{kq} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ G_0\omega_k^2 & 0 \\ 0 & G_0\omega_k^2 \end{bmatrix} \begin{bmatrix} u_d \\ u_q \end{bmatrix}. \quad (7.17)$$

The three-phase current and voltage sensor dynamics can be transformed into their rotating-frame equivalents using a similar process, due to their approximations using second-order models, $H_i(s)$ and $H_v(s)$, as defined previously. The current sensor outputs (x_{ia} , x_{ib} ,

x_{ic}) and their derivatives (x'_{ia} , x'_{ib} , x'_{ic}) are transformed into their rotating-frame equivalents x_{id} and x_{iq} , and x'_{id} and x'_{iq} , respectively,

$$\frac{d}{dt} \begin{bmatrix} x_{id} \\ x_{iq} \\ x'_{id} \\ x'_{iq} \end{bmatrix} = \begin{bmatrix} 0 & \omega & 1 & 0 \\ -\omega & 0 & 0 & 1 \\ -\omega_i^2 & 0 & -2\omega_i & \omega \\ 0 & -\omega_i^2 & -\omega & -2\omega_i \end{bmatrix} \begin{bmatrix} x_{id} \\ x_{iq} \\ x'_{id} \\ x'_{iq} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ H_{i0}\omega_i^2 & 0 \\ 0 & H_{i0}\omega_i^2 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix}. \quad (7.18)$$

Similarly, the voltage sensor outputs (x_{va} , x_{vb} , x_{vc}) and their derivatives (x'_{va} , x'_{vb} , x'_{vc}) are transformed into their rotating-frame equivalents x_{vd} and x_{vq} , and x'_{vd} and x'_{vq} , respectively,

$$\frac{d}{dt} \begin{bmatrix} x_{vd} \\ x_{vq} \\ x'_{vd} \\ x'_{vq} \end{bmatrix} = \begin{bmatrix} 0 & \omega & 1 & 0 \\ -\omega & 0 & 0 & 1 \\ -\omega_v^2 & 0 & -2\omega_v & \omega \\ 0 & -\omega_v^2 & -\omega & -2\omega_v \end{bmatrix} \begin{bmatrix} x_{vd} \\ x_{vq} \\ x'_{vd} \\ x'_{vq} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ H_{v0}\omega_v^2 & 0 \\ 0 & H_{v0}\omega_v^2 \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix}. \quad (7.19)$$

The equivalent circuit, DBSRC actuator, current and voltage sensor models are combined to form an open-loop plant model in rotating frame that is used in subsequent controller design,

$$\dot{\mathbf{x}}_p = \mathbf{A}_p \mathbf{x}_p + \mathbf{B}_p \mathbf{u} + \mathbf{E} \mathbf{w}. \quad (7.20)$$

There are sixteen states

$$\mathbf{x}_p = \begin{bmatrix} x_{id} & x_{iq} & x_{vd} & x_{vq} & x'_{id} & x'_{iq} & x'_{vd} & x'_{vq} \\ i_d & i_q & v_d & v_q & i_{kd} & i_{kq} & i'_{kd} & i'_{kq} \end{bmatrix}^T, \quad (7.21)$$

and two control and two disturbance inputs

$$\mathbf{u} = \begin{bmatrix} u_d \\ u_q \end{bmatrix} \quad \text{and} \quad \mathbf{w} = \begin{bmatrix} e_d \\ e_q \end{bmatrix}. \quad (7.22)$$

The coefficient matrices, \mathbf{A}_p , \mathbf{B}_p and \mathbf{E} , are obtained from Equations 7.12, 7.17, 7.18 and 7.19. Only the first four states (sensor outputs) are directly accessible by the controller, so they are assigned as outputs

$$\mathbf{y}_p = \begin{bmatrix} x_{id} & x_{iq} & x_{vd} & x_{vq} \end{bmatrix}^T = \mathbf{C}_p \mathbf{x}_p = \begin{bmatrix} \mathbf{I}_4 & \mathbf{0} \end{bmatrix} \mathbf{x}_p. \quad (7.23)$$

7.3 Rotating-Frame Controller

This section provides the design procedure of the integral output feedback controller in rotating frame. Following the derivation of the open-loop plant, a block diagram of the proposed controller is constructed. The design procedure is similar to that in stationary frame. A full state feedback design is first conducted using the LQR tuning method based on different weights assigned to states. Next, an output feedback design using the available states is performed, using the full state feedback design as a reference, and modifying the controller gains to retain the dominant closed-loop poles.

The controller gains are tuned to achieve two objectives, which are to ensure robust stability within uncertainty ranges for L_g and G_0 , and to achieve a high closed-loop bandwidth. To achieve these objectives, the closed-loop stability and performance are evaluated using different LQR weight penalties. The loop gain and closed-loop reference to output and disturbance to output transfer functions are evaluated using both frequency and step responses. To facilitate analysis, the state-space models of the controller, loop gain and closed-loop system are derived. In the controller tuning process, some conclusions are drawn on how changes in weights affect stability and performance.

7.3.1 Controller Design

The same controller architecture of integral state feedback used previously in stationary frame is kept for its stabilizing and error-correcting properties. The primary difference is that the states and inputs are now in the rotating frame, but the process for selecting the controller gains is largely similar. The process begins with establishing a closed-loop model suitable for controller design based on the closed-loop block diagram in Fig. 7.7.

The errors are due to differences between reference and sensed currents,

$$\mathbf{e} = \mathbf{r} - \begin{bmatrix} x_{id} \\ x_{iq} \end{bmatrix} = \mathbf{r} - \mathbf{C}_i \mathbf{x}_p = \mathbf{r} - \begin{bmatrix} \mathbf{I}_2 & \mathbf{0} \end{bmatrix} \mathbf{x}_p. \quad (7.24)$$

The closed-loop controller design model $\dot{\mathbf{z}}$ is derived by augmenting the open-loop plant model $\dot{\mathbf{x}}_p$ with error states,

$$\dot{\mathbf{z}} = \begin{bmatrix} -\dot{\mathbf{e}} \\ \ddot{\mathbf{x}}_p \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \mathbf{C}_i \\ \mathbf{0} & \mathbf{A}_p \end{bmatrix} \begin{bmatrix} -\mathbf{e} \\ \dot{\mathbf{x}}_p \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \mathbf{B}_p \end{bmatrix} \dot{\mathbf{u}} = \mathbf{A}_z \mathbf{z} + \mathbf{B}_z \dot{\mathbf{u}}, \quad (7.25)$$

and applying state feedback

$$\dot{\mathbf{u}} = -\mathbf{K}_z \mathbf{z} = - \begin{bmatrix} \mathbf{K}_e & \mathbf{K}_x \end{bmatrix} \begin{bmatrix} -\mathbf{e} \\ \dot{\mathbf{x}}_p \end{bmatrix}. \quad (7.26)$$

Combining the two equations forms the state feedback design model,

$$\dot{\mathbf{z}} = \mathbf{F}_z \mathbf{z} = (\mathbf{A}_z - \mathbf{B}_z \mathbf{K}_z) \mathbf{z}. \quad (7.27)$$

The state feedback gain matrix \mathbf{K}_z can be obtained using the LQR method based on weight matrices \mathbf{Q} and \mathbf{R} .

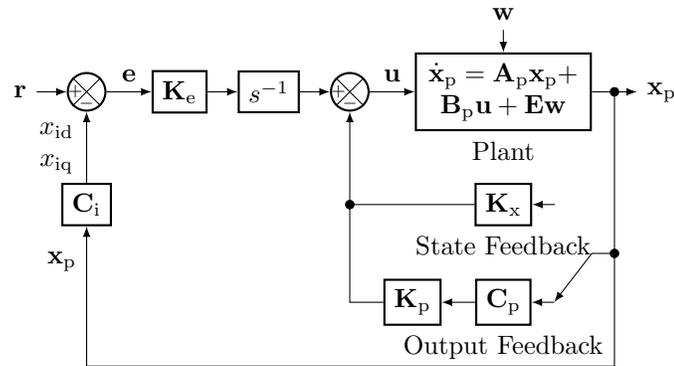


Fig. 7.7: Block diagram of a state and output feedback controlled unfolding converter.

The implemented controller uses the static output feedback [83],

$$\dot{\mathbf{u}} = -\mathbf{K}_y \begin{bmatrix} -\mathbf{e} \\ \dot{\mathbf{y}}_p \end{bmatrix} = -\mathbf{K}_y \mathbf{C}_z \mathbf{z} = -\mathbf{K}_y \begin{bmatrix} \mathbf{I}_6 & \mathbf{0} \end{bmatrix} \mathbf{z}, \quad (7.28)$$

resulting in the following closed-loop output feedback design model,

$$\dot{\mathbf{z}} = \mathbf{F}_y \mathbf{z} = (\mathbf{A}_z - \mathbf{B}_z \mathbf{K}_y \mathbf{C}_z) \mathbf{z}. \quad (7.29)$$

The output feedback gain matrix \mathbf{K}_y is selected to retain the six dominant eigenvalues (poles) and their associated eigenvectors \mathbf{V}_y in the state feedback design,

$$\mathbf{K}_y = \mathbf{K}_z \mathbf{V}_y (\mathbf{C}_z \mathbf{V}_y)^{-1} = \begin{bmatrix} \mathbf{K}_e & \mathbf{K}_p \end{bmatrix}. \quad (7.30)$$

In designing the feedback gains, the stability and performance of the closed-loop system shall be evaluated. The diagram in Fig. 7.7 can be simplified by representing the entire controller with its own model $\dot{\mathbf{x}}_c$ in the following general form,

$$\begin{cases} \dot{\mathbf{x}}_c &= \mathbf{A}_c \mathbf{x}_c + \mathbf{B}_{c1} \mathbf{x}_p + \mathbf{B}_{c2} \mathbf{r} \\ \mathbf{u} &= \mathbf{C}_c \mathbf{x}_c + \mathbf{D}_c \mathbf{x}_p \end{cases}. \quad (7.31)$$

Applying the general controller model to the output feedback controller results in the following coefficient matrices,

$$\mathbf{A}_c = \mathbf{0}, \quad \mathbf{B}_{c1} = -\mathbf{K}_e \mathbf{C}_i, \quad \mathbf{B}_{c2} = \mathbf{K}_e, \quad \mathbf{C}_c = \mathbf{I} \quad \text{and} \quad \mathbf{D}_c = -\mathbf{K}_p \mathbf{C}_p. \quad (7.32)$$

The connection of the controller and open-loop plant models results in the closed-loop system model shown in Fig. 7.8,

$$\begin{bmatrix} \dot{\mathbf{x}}_p \\ \dot{\mathbf{x}}_c \end{bmatrix} = \begin{bmatrix} \mathbf{A}_p + \mathbf{B}_p \mathbf{D}_c & \mathbf{B}_p \mathbf{C}_c \\ \mathbf{B}_{c1} & \mathbf{A}_c \end{bmatrix} \begin{bmatrix} \mathbf{x}_p \\ \mathbf{x}_c \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \mathbf{B}_{c2} \end{bmatrix} \mathbf{r} + \begin{bmatrix} \mathbf{E} \\ \mathbf{0} \end{bmatrix} \mathbf{w}. \quad (7.33)$$

This model is used to analyze the closed-loop stability and performance.

The general controller model can also be used to derive the loop gain model shown in Fig. 7.9,

$$\begin{cases} \begin{bmatrix} \dot{\mathbf{x}}_p \\ \dot{\mathbf{x}}_c \end{bmatrix} = \begin{bmatrix} \mathbf{A}_p & \mathbf{0} \\ -\mathbf{B}_{c1} & \mathbf{A}_c \end{bmatrix} \begin{bmatrix} \mathbf{x}_p \\ \mathbf{x}_c \end{bmatrix} + \begin{bmatrix} \mathbf{B}_p \\ \mathbf{0} \end{bmatrix} \mathbf{u}_{in} \\ \mathbf{u}_{out} = \begin{bmatrix} -\mathbf{D}_c & \mathbf{C}_c \end{bmatrix} \begin{bmatrix} \mathbf{x}_p \\ \mathbf{x}_c \end{bmatrix} \end{cases} . \quad (7.34)$$

7.3.2 Controller Tuning for Robustness

The derived loop gain and closed-loop system models allow evaluation of closed-loop stability and performance with different controller gains. The state feedback gains are generated using the LQR method based on diagonal weight matrices configured as

$$\mathbf{Q} = \begin{bmatrix} q_e \mathbf{I}_2 & & \\ & q_i \mathbf{I}_2 & \\ & & \mathbf{0} \end{bmatrix} \quad \text{and} \quad \mathbf{R} = \mathbf{I}_2, \quad (7.35)$$

where \mathbf{Q} and \mathbf{R} penalize the states and control inputs, respectively. The applied tuning procedure fixes \mathbf{R} while adjusts parameters in \mathbf{Q} . The parameter q_i applies equal penalties to the two sensed currents x_{id} and x_{iq} . The parameter q_e applies equal penalties to the two error states in \mathbf{e} . Intuitively, increasing q_e produces gains that reduce the errors. The dependence of closed-loop stability and performance on the two tuning parameters will be summarized using an example design. After the state feedback gains are obtained, they are

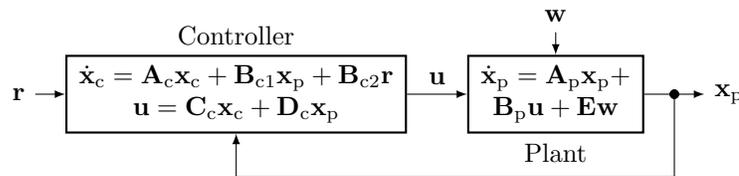


Fig. 7.8: Block diagram of the closed-loop system model.

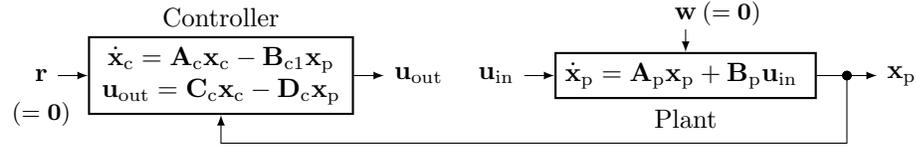


Fig. 7.9: Block diagram of the loop gain model.

converted to output feedback gains by retaining the dominant eigenvalues in the closed-loop system using the available states.

The output feedback gains are now designed using the LQR method for the 10-kVA unfolding converter plant with the following nominal values, circuit of $\bar{L}_g = 300 \mu\text{H}$, $R_g = 0.1 \Omega$ and $C_k = 5 \mu\text{F}$, rotating frequency of $f = 60 \text{ Hz}$, DBSRC actuator of $\bar{G}_0 = 22$ and $f_k = 10 \text{ kHz}$, sensors of $H_{i0} = 0.05$, $H_{v0} = 1.5 \times 10^{-3}$ and $f_i = f_v = 10 \text{ kHz}$. In addition, the following uncertainties are considered on parameters L_g and G_0 ,

$$L_g = \bar{L}_g 10^{(\pm\delta_L)} \quad \text{and} \quad G_0 = \bar{G}_0 (1 \pm \delta_G), \quad (7.36)$$

where the anticipated variations are $\delta_L = 1$ for inductance values between $30 \mu\text{H}$ and 3 mH , and $\delta_G = 0.5$ or 50% variation on the actuator's dc gain.

The adjustment of q_e primarily impacts the closed-loop bandwidth, which is reflected in the rise time of the step response from i_{rd} to i_d . In Fig. 7.10a, the step responses are shown for the plant with nominal parameters but with controller gains produced from two values of q_e , 10^5 and 10^6 . The same value of $q_i = 0.1$ is used. The results show that increasing q_e reduces rise time of the step response and increases the closed-loop bandwidth. Be aware that increasing q_e too much tends to compromise stability, especially when large variations exist in plant parameters, as is the case in the considered design.

The adjustment of q_i primarily impacts stability, which is also observed in the step response from i_{rd} to i_d . In Fig. 7.10b, the step responses are shown for the plant with nominal parameters but with controller gains produced from two values of q_i , 10^{-3} and 0.1 . The same value of $q_e = 10^6$ is used. The results show that increasing q_i reduces the current oscillation and improves stability. Be aware that increasing q_i too much tends to result

in larger gains on the sensed voltages, which reduces disturbance rejection. This is seen in the frequency response from e_d to i_d shown in Fig. 7.11, where the low-frequency gain increases as q_i is made larger. Note however that the rejection of fundamental-frequency voltage variation is not impacted, as it is converted to dc values in rotating frame.

Based on trends learned from tuning of q_e and q_i , they are selected respectively as 10^6 and 0.1 with nominal plant parameters. This results in the following integral and output feedback gain matrices,

$$\mathbf{K}_e = \begin{bmatrix} 726 & 0 \\ 0 & 726 \end{bmatrix} \quad \text{and} \quad \mathbf{K}_p = \begin{bmatrix} -0.15 & 0 & 1.7 & 0 \\ 0 & -0.15 & 0 & 1.7 \end{bmatrix}, \quad (7.37)$$

where the off-diagonal gains are small and have been removed to simplify implementation.

The stability and performance of the closed-loop system with these gains but with uncertain plant parameters are now verified. The step responses from i_{rd} to i_d are shown in Fig. 7.12 with combinations of maximum and minimum values of L_g and G_0 within their anticipated variations. In comparison with the response with nominal values, a smaller G_0 results in slower response. The system is stable with all parameter combinations.

The frequency responses from i_{rd} to i_d with the selected gains but with different L_g values are shown in Fig. 7.13. The closed-loop bandwidth is fairly uniform at about 200 Hz.

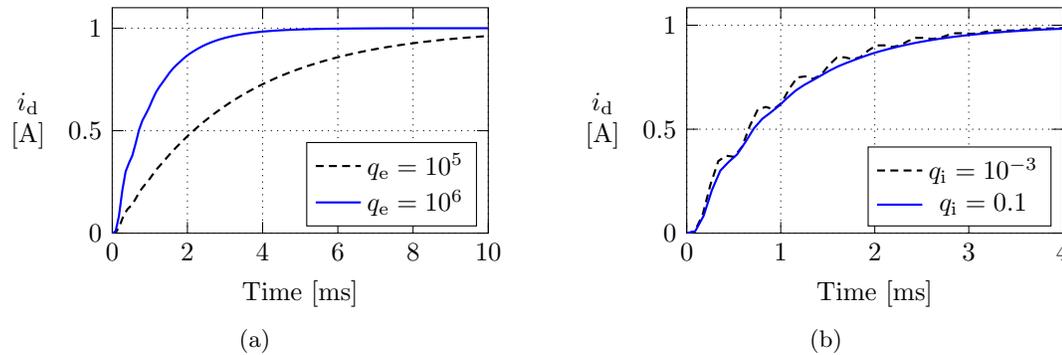


Fig. 7.10: Step response of i_{rd} to i_d at nominal plant parameters. (a) For same $q_i = 0.1$ but different q_e values, to show faster response by increasing q_e . (b) For same $q_e = 10^6$ but different q_i values, to show better stability by increasing q_i .

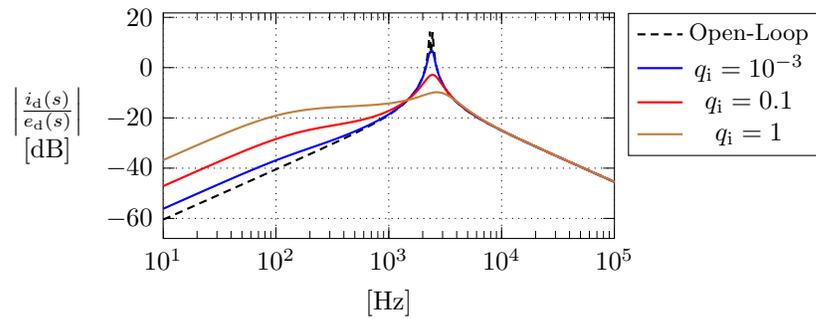


Fig. 7.11: Magnitude plots of grid voltage to current response, $\frac{i_d(s)}{e_d(s)}$, at nominal plant parameters for same $q_e = 10^6$ but different q_i values, to show worse disturbance rejection with increasing q_i .

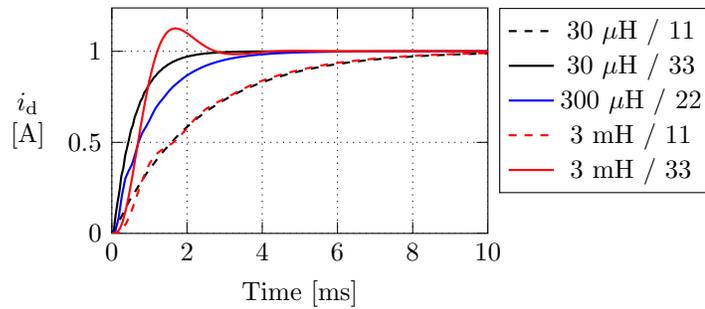


Fig. 7.12: Step response of i_{rd} to i_d with selected gains using $q_e = 10^6$ and $q_i = 0.1$ but with different L_g and G_0 values.

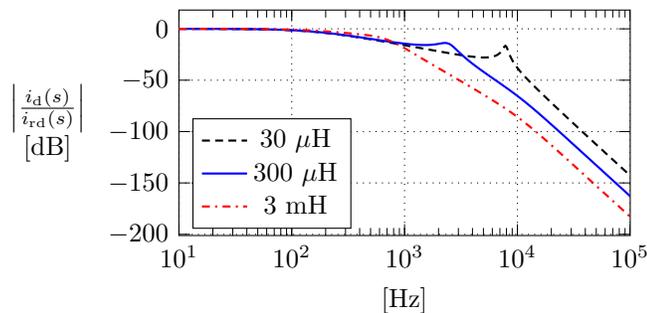


Fig. 7.13: Magnitude plots of reference to actual current response, $\frac{i_d(s)}{i_{rd}(s)}$, with selected gains using $q_e = 10^6$ and $q_i = 0.1$ and nominal $G_0 = 22$ but with different L_g values.

7.3.3 Implementation of Transformations

The rotating-frame controller is to be constructed in simulation and experiment. Critical to its construction is the implementation of the various transformation functions. Consider first the generation of sensed currents in rotating frame. In a typical three-phase inverter, the line currents are sensed and transformed into rotating frame using the Park transformation. This same approach can be applied to the unfolding converter but requires additional line current sensors. Existing current sensors are installed in the DBSRC modules for output current regulation. When used in the unfolding converter, these sensors measure the dc-link currents. The measured dc-link currents can be used to derive the line currents using the unfold relationships. The derived line currents are then transformed into the rotating frame using the Park transformation. Using this approach avoids adding additional line current sensors to the unfolding converter. This current sensing approach using two transformations can be visualized in Fig. 7.14. The unfold transformation is based on the sector variable S having six states. The current relationship in each sector is valid as long as the clamping diode does not conduct.

The double-transform approach is still cumbersome, as it requires the derivation of the intermediate three-phase line currents, which are not used anywhere else. A simplified single-transform approach is also shown in Fig. 7.14 and combines the two transformations into one. This approach is derived by exploiting symmetries among odd and among even sectors and simplifies the current relationships from six to just two. The estimated phase angle θ is between 0 and 2π . The sector variable S is an integer between 1 and 6. Consider in Sector 1,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix}_{S=1} = \begin{bmatrix} \mathbf{I}_2 & \mathbf{0} \end{bmatrix} \mathbf{K}_r \begin{bmatrix} i_1 \\ i_2 - i_1 \\ -i_2 \end{bmatrix} = \frac{2\sqrt{3}}{3} \begin{bmatrix} \cos(\theta + \frac{\pi}{6}) & \sin(\theta) \\ -\sin(\theta + \frac{\pi}{6}) & \cos(\theta) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \quad (7.38)$$

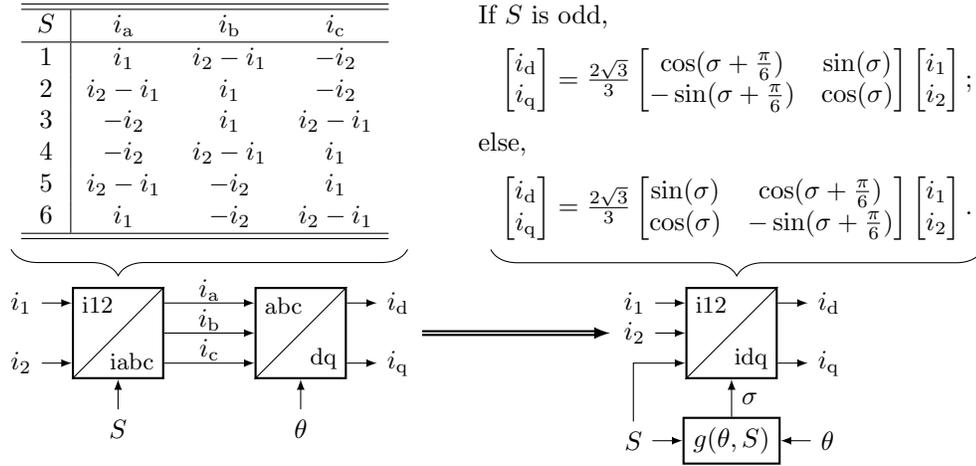


Fig. 7.14: Simplification of the dc-link to rotating-frame current transformation, from two steps to one step, by exploiting symmetries among odd and among even sectors.

Consider in Sector 2 but with θ substituted with $\sigma = \theta - \frac{\pi}{3}$,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix}_{S=2} = \begin{bmatrix} \mathbf{I}_2 & \mathbf{0} \end{bmatrix} \mathbf{K}_r \begin{bmatrix} i_2 - i_1 \\ i_1 \\ -i_2 \end{bmatrix} = \frac{2\sqrt{3}}{3} \begin{bmatrix} \sin(\sigma) & \cos(\sigma + \frac{\pi}{6}) \\ \cos(\sigma) & -\sin(\sigma + \frac{\pi}{6}) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \quad (7.39)$$

Similarly, consider in Sector 3 but with θ substituted with $\sigma = \theta - \frac{2\pi}{3}$,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix}_{S=3} = \begin{bmatrix} \mathbf{I}_2 & \mathbf{0} \end{bmatrix} \mathbf{K}_r \begin{bmatrix} -i_2 \\ i_1 \\ i_2 - i_1 \end{bmatrix} = \frac{2\sqrt{3}}{3} \begin{bmatrix} \cos(\sigma + \frac{\pi}{6}) & \sin(\sigma) \\ -\sin(\sigma + \frac{\pi}{6}) & \cos(\sigma) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}, \quad (7.40)$$

which is same as in Sector 1 but with θ substituted with σ . The same process can be applied to the remaining sectors, by setting σ as

$$\sigma = g(\theta, S) = \theta - (S - 1) \frac{\pi}{3}, \quad (7.41)$$

and the following generalized relationships are obtained,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix}_{S \text{ odd}} = \frac{2\sqrt{3}}{3} \begin{bmatrix} \cos(\sigma + \frac{\pi}{6}) & \sin(\sigma) \\ -\sin(\sigma + \frac{\pi}{6}) & \cos(\sigma) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}, \quad (7.42)$$

and

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix}_{S \text{ even}} = \frac{2\sqrt{3}}{3} \begin{bmatrix} \sin(\sigma) & \cos(\sigma + \frac{\pi}{6}) \\ \cos(\sigma) & -\sin(\sigma + \frac{\pi}{6}) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \quad (7.43)$$

This converts the sensed dc-link currents into rotating-frame quantities in one step. This single-transform approach is implemented as shown in Fig. 7.14. It shall be noted that σ is not necessarily between zero and $\frac{\pi}{3}$, depending on how S and θ are generated, but is so in the simple case where S is directly generated from θ , or $S = \text{ceil}\left(\frac{\theta}{\pi/3}\right)$.

In the rotating-frame model of the DBSRC actuator, the actual commands u_1 and u_2 are generated from three-phase quantities u_a , u_b and u_c based on the unfolded current relationships. The rotating-frame controller generates commands u_d and u_q . They are converted into three-phase quantities using the inverse Park transformation. This two-step implementation is shown in Fig. 7.15. It can be simplified by using a similar process as the dc-link to rotating-frame current transformation, by substituting θ with σ based on S . The resulting dc-link currents (commands) are same among odd and among even sectors,

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix}_{S \text{ odd}} = \begin{bmatrix} \cos(\sigma) & -\sin(\sigma) \\ \sin(\sigma + \frac{\pi}{6}) & \cos(\sigma + \frac{\pi}{6}) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix}, \quad (7.44)$$

and

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix}_{S \text{ even}} = \begin{bmatrix} \sin(\sigma + \frac{\pi}{6}) & \cos(\sigma + \frac{\pi}{6}) \\ \cos(\sigma) & -\sin(\sigma) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix}. \quad (7.45)$$

This single-step rotating-frame to dc-link current (command) transformation is implemented as shown in Fig. 7.15.

The rotating-frame controller requires the sensed unfolded line-to-neutral output voltages. These three-phase voltages can be sensed and converted into rotating-frame quantities

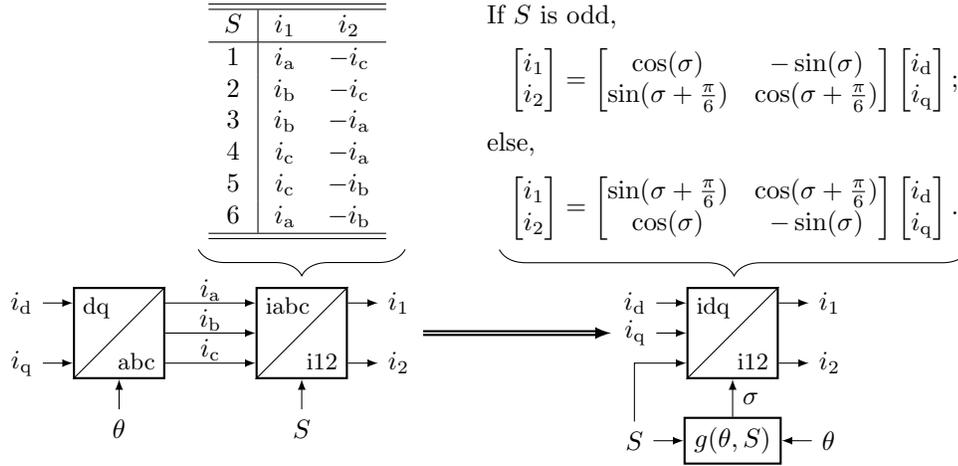


Fig. 7.15: Simplification of the rotating-frame to dc-link current transformation, from two steps to one step, by exploiting symmetries among odd and among even sectors.

using the Park transformation. But they can be derived using the unfolded voltage relationships and the measured dc-link voltages from the existing voltage sensors at the DBSRC outputs. This two-step implementation is shown in Fig. 7.16. It can be simplified by using a similar process as the dc-link to rotating-frame current transformation, by substituting θ with σ based on S . The resulting rotating-frame voltages are same among odd and among even sectors,

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix}_{S \text{ odd}} = \frac{2}{3} \begin{bmatrix} \cos(\sigma) & \sin(\sigma + \frac{\pi}{6}) \\ -\sin(\sigma) & \cos(\sigma + \frac{\pi}{6}) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}, \quad (7.46)$$

and

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix}_{S \text{ even}} = \frac{2}{3} \begin{bmatrix} \sin(\sigma + \frac{\pi}{6}) & \cos(\sigma) \\ \cos(\sigma + \frac{\pi}{6}) & -\sin(\sigma) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \quad (7.47)$$

This single-step dc-link to rotating-frame voltage transformation is implemented as shown in Fig. 7.16.

7.4 Controller Construction and Verification

The derived transformation blocks are then combined with the output feedback controller to form a core controller block shown in Fig. 7.17. The actual dc-link currents i_1 and i_2 are sensed with current sensors having dc gain of H_{I0} . The sensed currents x_{i1} and

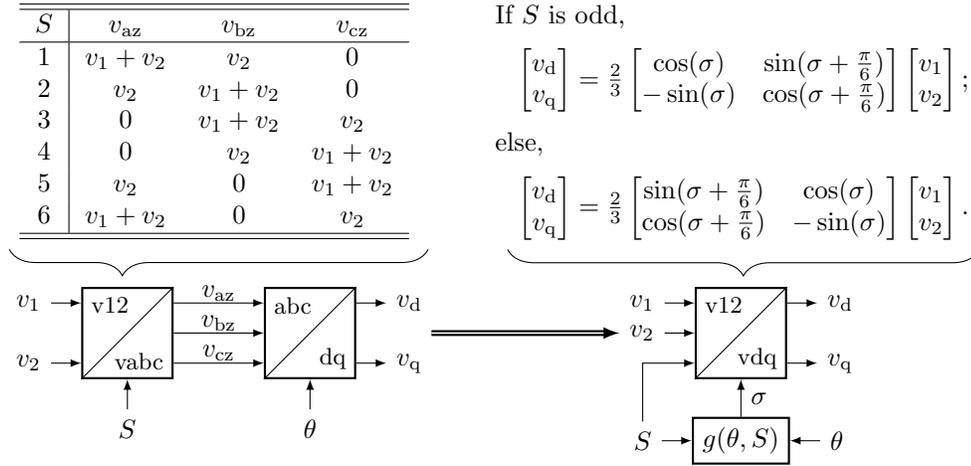


Fig. 7.16: Simplification of the dc-link to rotating-frame voltage transformation, from two steps to one step, by exploiting symmetries among odd and among even sectors.

x_{i2} are passed to the dc-link to rotating-frame current transformation in the controller core. Similarly, the sensed dc-link voltages x_{v1} and x_{v2} , obtained from voltage sensors H_{v0} , are passed to the voltage transformation. The transformations are driven by the unfold sector variable S_f , which is also used to generate the unfold switching sequence.

The transformations rely on the unfold current and voltage relationships, which are accurate given non-conduction of the clamping diodes. In actual converter, these diodes unavoidably conduct for short durations at sector beginnings. The diode conduction introduces errors in the transformed quantities. These errors, typically fast-varying glitches, are suppressed using a low-pass filter. For simplicity, the filter bandwidth is treated as the same f_i and f_v used in the sensor models. In addition to S_f , the transformations also require the sector angle σ_f that is generated based on S_f and the estimated grid voltage angle θ^* from the PLL,

$$\sigma_f = g(\theta^*, S_f) = \theta^* - (S_f - 1) \frac{\pi}{3}. \quad (7.48)$$

The grid angle is used to keep the rotating frame synchronized to the grid voltages. Note that this is different from the angle θ_f used to generate S_f , where

$$S_f = f(\theta_f) = \text{ceil} \left(\frac{\theta_f}{\pi/3} \right) = \text{ceil} \left(\frac{\theta^* + \phi_f}{\pi/3} \right). \quad (7.49)$$

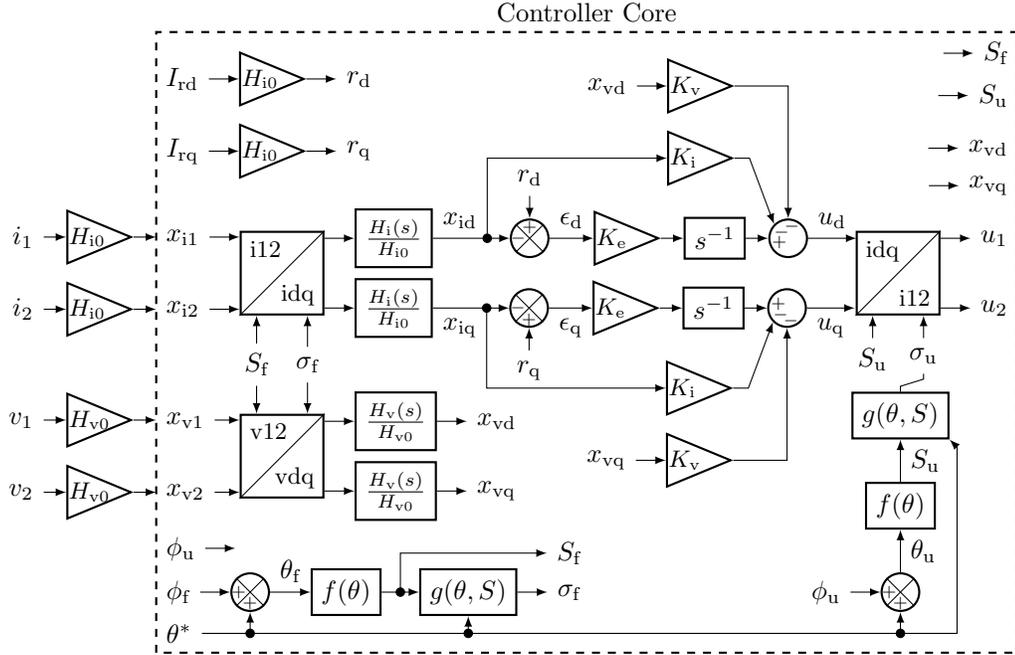


Fig. 7.17: Block diagram of the rotating-frame controller core.

The phase shift ϕ_f added to θ^* used to generate θ_f is an input to the controller core and can be obtained from the previous sector-adjusting algorithm introduced in Chapter 5.

The sensed and transformed quantities along with the references are passed to the integral output feedback controller, which then generates the converter commands. The off-diagonal gain terms are removed to simplify controller implementation. The removed gain terms cause little impact, as they are much smaller than the diagonal terms.

The final and perhaps most critical step in the controller core is the generation of actual converter commands u_1 and u_2 . This is accomplished with an inverse current transformation on u_d and u_q . The time-varying trajectories on u_1 and u_2 are mostly fed forward from the sector angle σ_u , whereas u_d and u_q adjust their magnitudes and phase shifts. This characteristic is similar to a rotating-frame controller for VSI and usually results in near-constant u_d and u_q values. Unique to the unfolding converter is the additional sector input S_u to the inverse transformation in command generation. The required step changes in the

time-varying trajectories are generated by S_u . It is obtained from the angle θ_u ,

$$S_u = f(\theta_u) = \text{ceil} \left(\frac{\theta_u}{\pi/3} \right) = \text{ceil} \left(\frac{\theta^* + \phi_u}{\pi/3} \right). \quad (7.50)$$

The phase shift ϕ_u added to θ^* used to generate θ_u is another input to the controller core and can be different from θ_f based on the sector-adjusting algorithm. Subsequently, the sector angle σ_u is generated based on the grid angle θ^* and S_u ,

$$\sigma_u = g(\theta^*, S_u) = \theta^* - (S_u - 1) \frac{\pi}{3}. \quad (7.51)$$

The combination of feedforward action from S_u and σ_u and the sector-adjusting algorithm result in improved current quality especially at non-unity power factors with the rotating-frame controller, compared to earlier approaches.

7.4.1 Sector Adjuster and Simulation Results

The required phase-shift inputs ϕ_f and ϕ_u to the controller core can be directly generated using the sector-adjusting algorithm based on the q-axis reference I_{rq} . The algorithm was derived using the feedforward controller and assumed small values of line inductance L_g . It does not account for the phase shift ϕ_v of the unfolder voltage due to L_g , which can become significant for large inductances.

A complete implementation of the sector adjuster accounts for ϕ_v in generating the phase shifts,

$$\hat{\phi}_f = \phi_f + \phi_v \quad \text{and} \quad \hat{\phi}_u = \phi_u + \phi_v, \quad (7.52)$$

where ϕ_f and ϕ_u are from the original algorithm. The theoretical formula for ϕ_v has previously been derived and is repeated below,

$$\tan(\phi_v) = \frac{V_q}{V_d} = \frac{R_g I_q + \omega L_g I_d}{R_g I_d - \omega L_g I_q + E_m} \approx \phi_v. \quad (7.53)$$

It can then be estimated using the sensed and transformed dc-link voltages from the controller core,

$$\phi_v = \frac{\bar{x}_{vq}}{\bar{x}_{vd}}, \quad (7.54)$$

where \bar{x}_{vd} and \bar{x}_{vq} are averaged values over a line period. This estimation of ϕ_v combined with the sector-adjusting algorithm forms the complete sector adjuster applicable to a wide range of L_g values and is shown in Fig. 7.18.

The sector adjuster and controller core are combined with the PLL, unfold switching sequencer and DBSRC modulators to form the complete rotating-frame controller as shown in Fig. 7.19. The complete system is simulated with plant and controller parameters in the previous 10-kVA unfolding converter design. The plant parameters are grid voltage $E_m = 392$ V and frequency $f = 60$ Hz, line inductance $L_g = 30 \sim 3000$ μ H and resistance $R_g = 0.1$ Ω , dc-link capacitance $C_k = 5$ μ F, DBSRC dc gain $G_0 = 22$ and bandwidth $f_k = 10$ kHz, sensor attenuations $H_{i0} = 0.05$ and $H_{v0} = 1.5 \times 10^{-3}$ and bandwidth $f_i = f_v = 10$ kHz. The controller gains are $K_e = 726$, $K_i = -0.15$ and $K_v = 1.7$.

The performance of the rotating-frame controller is first compared with the stationary-frame integral controller, using a line inductance of 30 μ H and operating at power factor of 0.7 (inductive), with $I_{rd} = -I_{rq} = 12$ A. This example was previously used to demonstrate the difficulty of obtaining high current quality at non-unity power factors using the stationary-frame controller, due to its slow command generation. The results at the same inductance and operating condition using the rotating-frame controller are shown in Fig. 7.20.

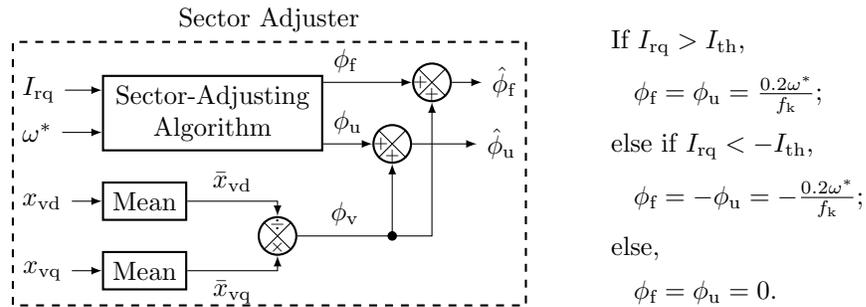


Fig. 7.18: Block diagram of the sector adjuster for use with the rotating-frame controller core.

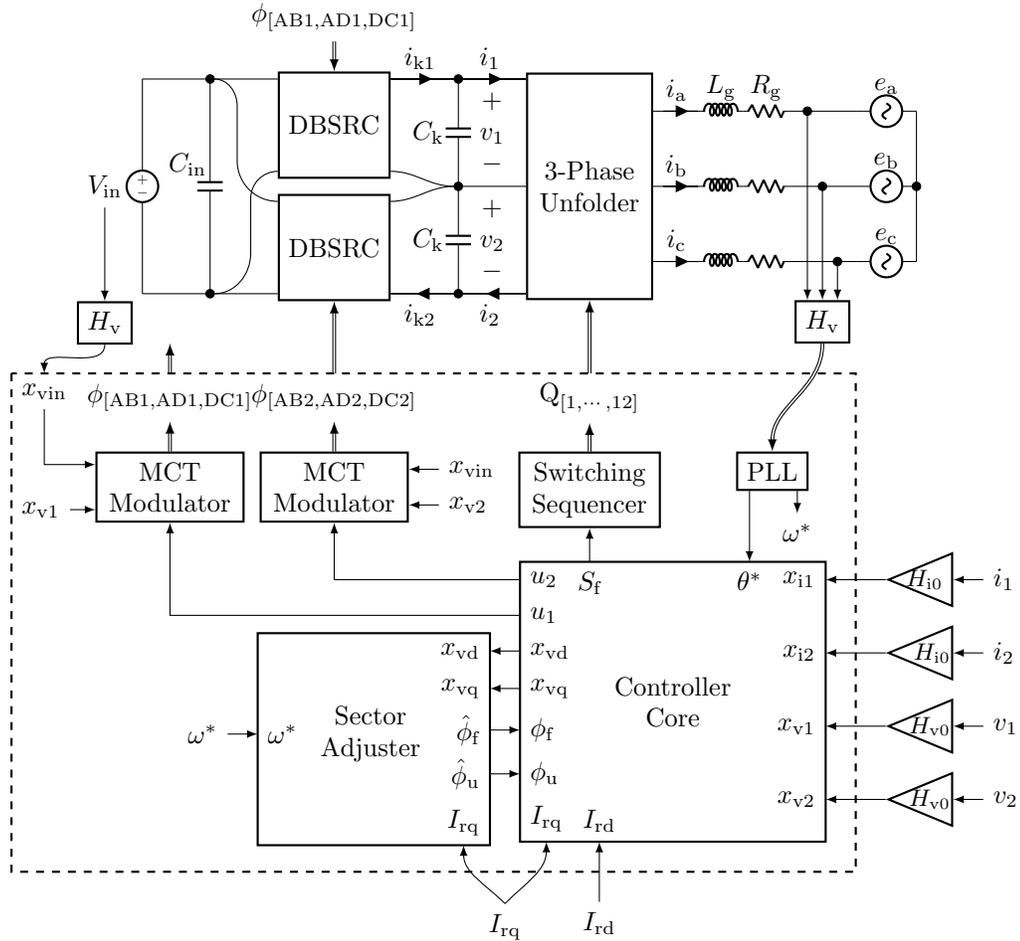


Fig. 7.19: Unfolding converter with the full rotating-frame controller.

Note the improvement in current quality primarily presented as reduced current oscillation at sector beginnings. This is attributed to the rotating-frame controller's ability to produce step changes in commands u_1, u_2 . This benefit is retained from the feedforward controller.

Despite the fast response of feedforward control, it is unable to damp any current oscillation or correct for errors between actual and reference currents. In Fig. 7.21, the rotating-frame controller is simulated at $I_{rd} = -I_{rq} = 12$ A with different values of L_g within its expected range of variation. The increase in L_g lowers the oscillation frequency and allows the controller to damp any oscillation at sector beginnings due to unfold switching. This effect in turn improves the current quality with increase in L_g . The error integrators minimize steady-state errors between actual and reference currents.

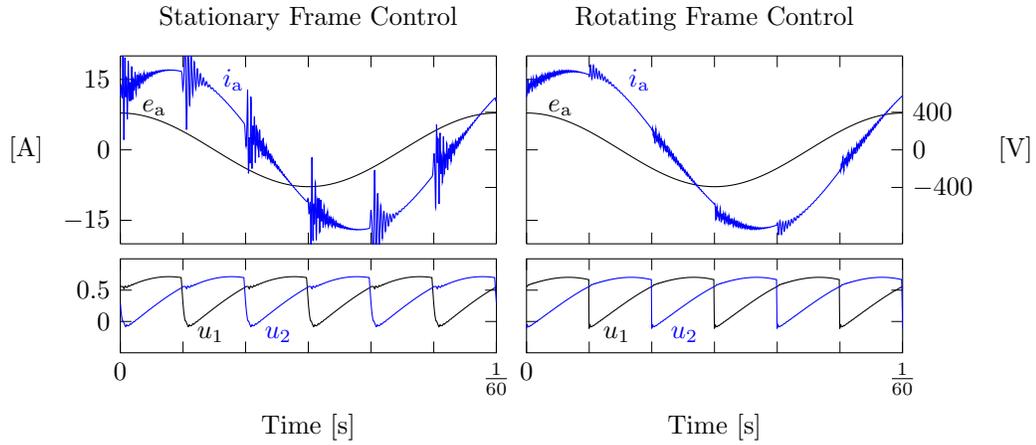


Fig. 7.20: Simulation results comparing actual line currents with stationary- and rotating-frame controllers, at power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12$ A, to highlight lower distortion with rotating-frame control due to faster actuation of commands.

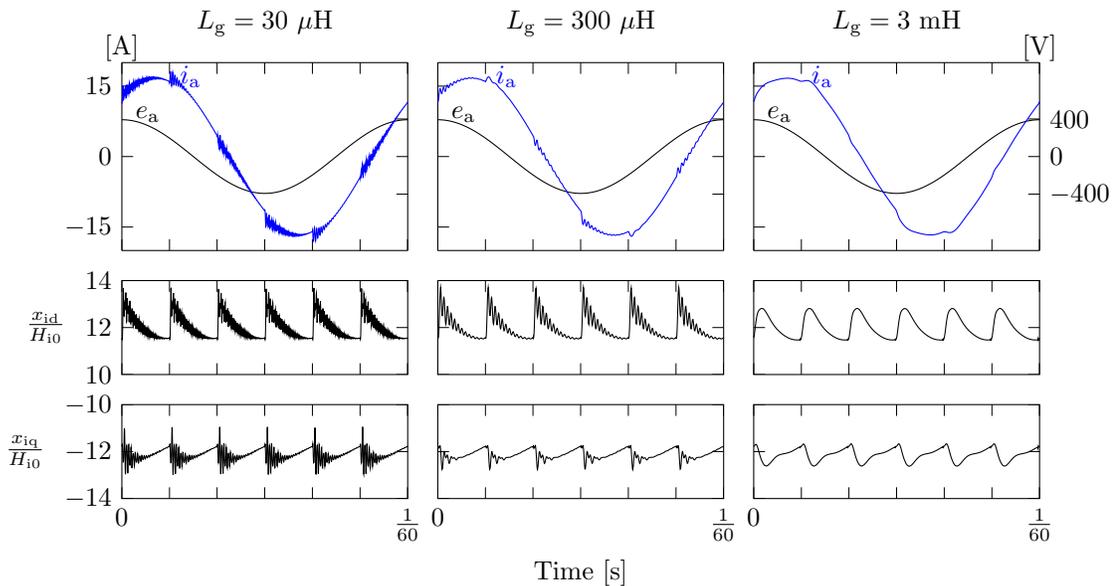


Fig. 7.21: Simulation results comparing actual line currents with different line inductance values with the rotating-frame controller, at power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12$ A, to highlight robust stability and error correction.

7.4.2 Capacitor Current Cancellation and Simulation Results

Despite the benefits of robust stability and correction of average errors offered by the rotating-frame controller, it has limited ability to correct for fast-varying errors. This can be seen as the variation in the sensed d- and q-axis currents in Fig. 7.21. Although these fast-varying errors can be reduced by increasing the closed-loop bandwidth, doing so tends to compromise stability. These errors are caused by the dc-link capacitor currents. Analytical formulas of the capacitor currents have been previously provided. The conclusion is that as the inverter switches from one sector to the next, each capacitor current is stepped to a different value.

Consider the top capacitor current i_{c1} , while i_{c2} behaves similarly. In odd sectors, based on Table 7.1, i_{c1} changes from

$$i_{c1,\text{odd}}(\sigma = 0) = -\frac{\sqrt{3}}{6}I_{\text{cm}} \quad \text{to} \quad i_{c1,\text{odd}}\left(\sigma = \frac{\pi}{3}\right) = -\frac{\sqrt{3}}{3}I_{\text{cm}}, \quad (7.55)$$

where $I_{\text{cm}} = 3V_{\text{m}}\omega C_{\text{k}}$. In even sectors, it changes from

$$i_{c1,\text{even}}(\sigma = 0) = \frac{\sqrt{3}}{3}I_{\text{cm}} \quad \text{to} \quad i_{c1,\text{even}}\left(\sigma = \frac{\pi}{3}\right) = \frac{\sqrt{3}}{6}I_{\text{cm}}. \quad (7.56)$$

From an odd to even sector, it steps from

$$i_{c1,\text{odd}}\left(\sigma = \frac{\pi}{3}\right) = -\frac{\sqrt{3}}{3}I_{\text{cm}} \quad \text{to} \quad i_{c1,\text{even}}(\sigma = 0) = \frac{\sqrt{3}}{3}I_{\text{cm}}. \quad (7.57)$$

From an even to odd sector, it steps from

$$i_{c1,\text{even}}\left(\sigma = \frac{\pi}{3}\right) = \frac{\sqrt{3}}{6}I_{\text{cm}} \quad \text{to} \quad i_{c1,\text{odd}}(\sigma = 0) = -\frac{\sqrt{3}}{6}I_{\text{cm}}. \quad (7.58)$$

These step changes cause distortion in line currents, as seen previously in Fig. 7.5a. Although adding a third capacitor can equalize these step changes, it increases converter volume and component count.

An intelligent approach is to cancel these steps instead using converter currents. Consider again the top dc-link current,

$$i_1 = \bar{i}_{k1} - i_{c1}. \quad (7.59)$$

Consider the converter current generated in two components, an original component \hat{i}_{k1} from the feedback controller, and a capacitor current canceling component i_{k1c} ,

$$\bar{i}_{k1} = \hat{i}_{k1} + i_{k1c}. \quad (7.60)$$

The component i_{k1c} will depend on the algorithm used. Assuming an ideal case with full cancellation, applying $i_{k1c} = i_{c1}$ results in $i_1 = \hat{i}_{k1}$. The resulting dc-link and line currents will not be affected by the capacitor currents.

The implemented algorithm is simplified by applying a constant canceling component in each sector,

$$i_{k1c} = \begin{cases} i_{k1c, \text{odd}} = \bar{i}_{c1, \text{odd}} = \frac{1}{2} \left(-\frac{\sqrt{3}}{6} I_{\text{cm}}^* - \frac{\sqrt{3}}{3} I_{\text{cm}}^* \right) = -\frac{\sqrt{3}}{4} I_{\text{cm}}^* \\ i_{k1c, \text{even}} = \bar{i}_{c1, \text{even}} = \frac{1}{2} \left(\frac{\sqrt{3}}{3} I_{\text{cm}}^* + \frac{\sqrt{3}}{6} I_{\text{cm}}^* \right) = \frac{\sqrt{3}}{4} I_{\text{cm}}^* \end{cases}, \quad (7.61)$$

where the average capacitor current in each sector, $\bar{i}_{c1, \text{odd}}$ or $\bar{i}_{c1, \text{even}}$, is estimated using

$$I_{\text{cm}}^* = 3V_{\text{m}}^* \omega^* C_{\text{k}} = 3 \frac{\sqrt{\bar{x}_{\text{vd}}^2 + \bar{x}_{\text{vq}}^2}}{H_{\text{v0}}} \omega^* C_{\text{k}}. \quad (7.62)$$

The magnitude V_{m}^* of the unfolded output voltage is estimated using the sensed and averaged d- and q-axis voltages. The line frequency ω^* is estimated by the PLL. The component i_{k1c} is generated by an equivalent command component u_{1c} , where

$$u_1 = \hat{u}_1 + u_{1c}. \quad (7.63)$$

The original component \hat{u}_1 comes from the feedback controller, and a capacitor current canceling component u_{1c} is generated as

$$u_{1c} = \begin{cases} u_{1c,\text{odd}} = -\frac{\sqrt{3}I_{cm}^*}{4G_0} \\ u_{1c,\text{even}} = \frac{\sqrt{3}I_{cm}^*}{4G_0} \end{cases}, \quad (7.64)$$

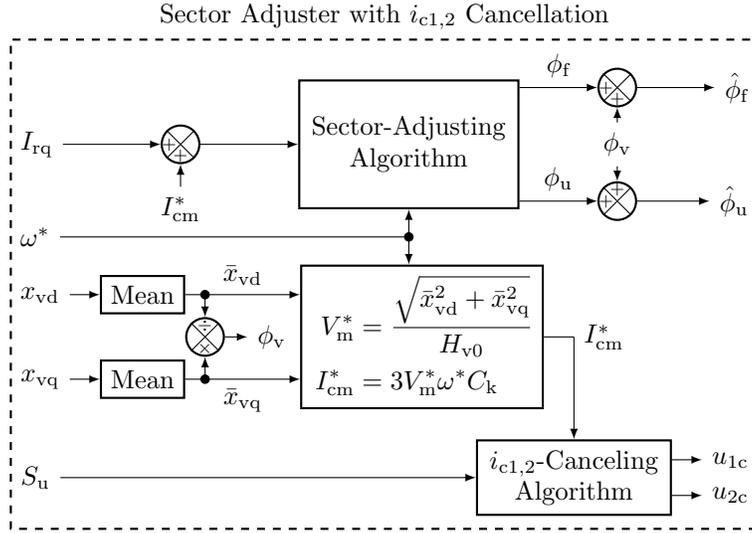
where G_0 is the dc gain in the DBSRC actuator model. The second DBSRC command is modified similarly,

$$u_2 = \hat{u}_2 + u_{2c}, \quad \text{where} \quad u_{2c} = \begin{cases} u_{2c,\text{odd}} = \frac{\sqrt{3}I_{cm}^*}{4G_0} \\ u_{2c,\text{even}} = -\frac{\sqrt{3}I_{cm}^*}{4G_0} \end{cases}. \quad (7.65)$$

The resulting applied capacitor current canceling component is a square wave that switches depending on the command sector variable S_u from the controller core. The sectors are phase-shifted by ϕ_u to compensate for the limited DBSRC response. Thus, the generation of ϕ_u shall account for the capacitor current. This is achieved by adding I_{cm}^* to the q-axis reference when applying the sector-adjusting algorithm. The complete sector adjuster with capacitor current cancellation is shown in Fig. 7.22.

The sector adjuster with capacitor current cancellation is integrated with the controller core and other parts of the rotating-frame controller in Fig. 7.23. The systems with and without cancellation are compared in simulation using the same 10-kVA plant and controller parameters. The results are shown in Fig. 7.24 with $L_g = 3$ mH and operating at $I_{rd} = -I_{rq} = 12$ A. Notice that without cancellation, the line current appear compressed. Adding cancellation improves current quality, by altering profiles of commands u_1 and u_2 . The improvement in current quality is also evident in the reduced variations in the sensed d- and q-axis currents.

The improvement in current quality is quantified by compared THD with and without capacitor current cancellation in Table 7.2 at various L_g values and different power factors. The results show uniformly reduced THD values by using cancellation. The results also show



If S_u is odd,

$$u_{1c} = -\frac{\sqrt{3}I_{cm}^*}{4G_0},$$

$$u_{2c} = \frac{\sqrt{3}I_{cm}^*}{4G_0};$$

else,

$$u_{1c} = \frac{\sqrt{3}I_{cm}^*}{4G_0},$$

$$u_{2c} = -\frac{\sqrt{3}I_{cm}^*}{4G_0}.$$

Fig. 7.22: Block diagram of the sector adjuster with capacitor current cancellation.

highest THD at small inductance values. This is due a current oscillation frequency beyond the sensor bandwidth, and thus the controller offers no correction. In actual converter, a passive damping network can be added, if oscillation becomes significant.

Dynamic performance of the rotating-frame controller is verified by stepping the d- and q-axis current references through the four quadrants of the PQ plane. The reference steps are applied every half line period, and the sensed and transformed currents are observed in Fig. 7.25. The settling time of current in either axis is 3 ms and matches with that from controller design. Also notice minimal cross coupling between the axes, presented as minimal transient on one axis as the other is stepped.

The simulation results demonstrate high current quality in steady state regardless of power factor and line inductance value, and in fast tracking of dynamic changes in dq current references.

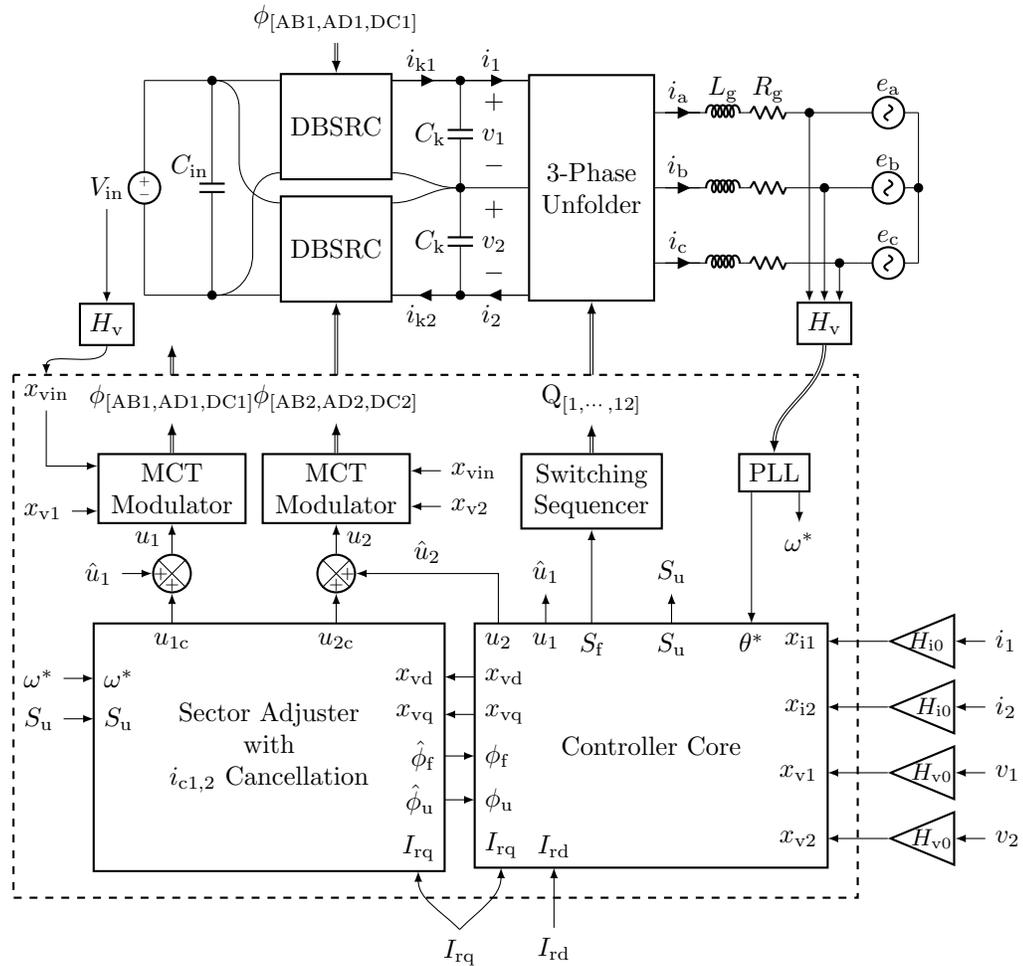


Fig. 7.23: Unfolding converter with the full rotating-frame controller with capacitor current cancellation.

Table 7.2: Current THD with and without capacitor current cancellation.

Conditions			THD [%] at $L_g =$		
I_{rd}	I_{rq} [A]		$30 \mu\text{H}$	$300 \mu\text{H}$	3 mH
17	0	w/o	5.2	3.5	2.9
		w/	3.3	1.4	1.2
12	-12	w/o	4.5	3.4	3.2
		w/	2.3	1.5	1.4

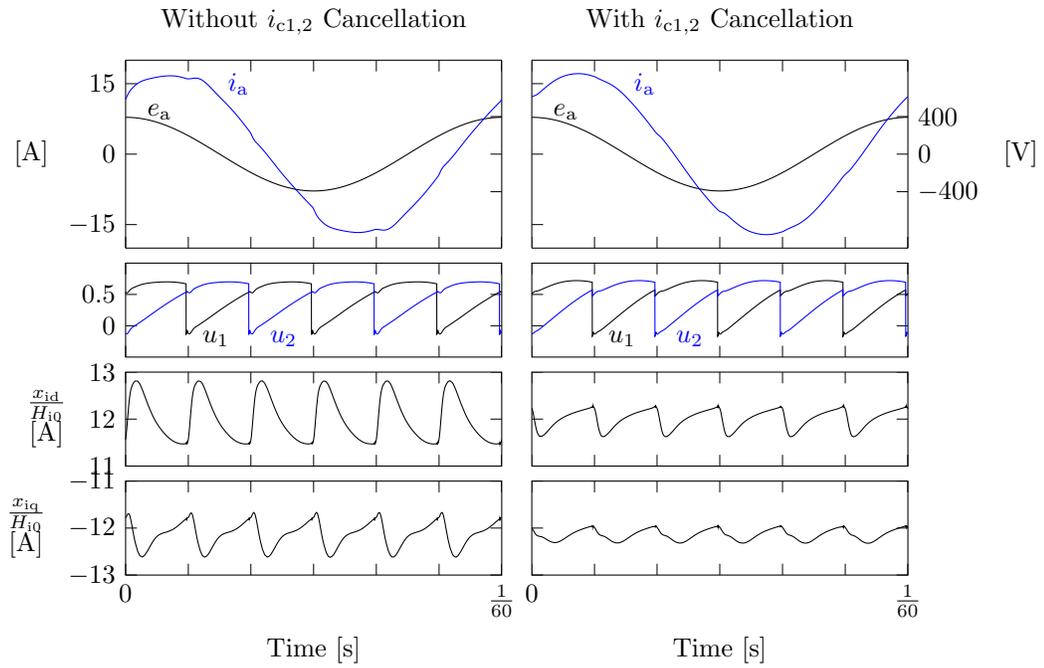


Fig. 7.24: Simulation results demonstrating improved current quality with capacitor current cancellation by comparing to without cancellation, at power factor of 0.7 (inductive) with $I_{rd} = -I_{rq} = 12$ A.

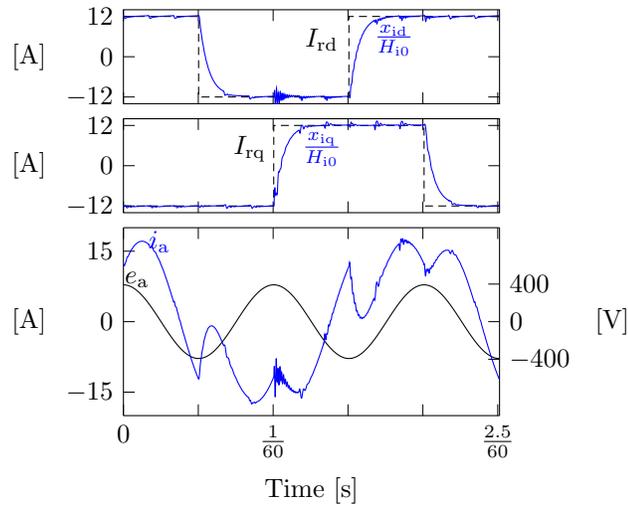


Fig. 7.25: Simulation results showing dynamic response by stepping through the four quadrants in the PQ plane.

7.5 Experimental Verification

An experimental prototype of the unfolding converter has been constructed with parameters in Table 7.3 and connected as shown in Fig. 7.23 with the rotating-frame controller to evaluate its line current regulation and dynamic response. A photo of the prototype is shown in Fig. 7.26. Each DBSRC module is phase-shift modulated using MCT angles to reduce conduction loss. Furthermore, an auxiliary half-bridge leg is inductively coupled to and phase-shifted from each main DBSRC leg to reduce switching loss. In addition to their power circuits, the unfolder and DBSRC modules contain all associated gate-drive circuits, while each DBSRC additionally contains voltage and current sensors and analog-to-digital converters. All of the control and signal processing blocks are implemented digitally in a Xilinx Virtex-5 field-programmable gate array (FPGA). The MCT modulator is implemented using a look-up table approach. The control angles are tuned to linearize the command to output current gain.

7.5.1 DBSRC Gain Linearization

Recall that the DBSRC command to output current response has been modeled using a linear actuator model $G_{iu}(s)$. Due to converter nonidealities such as losses and dead times, the response in actual hardware becomes nonlinear. The nonlinearity is depicted as variation in the response's dc gain G_0 with the applied command U . In addition, the

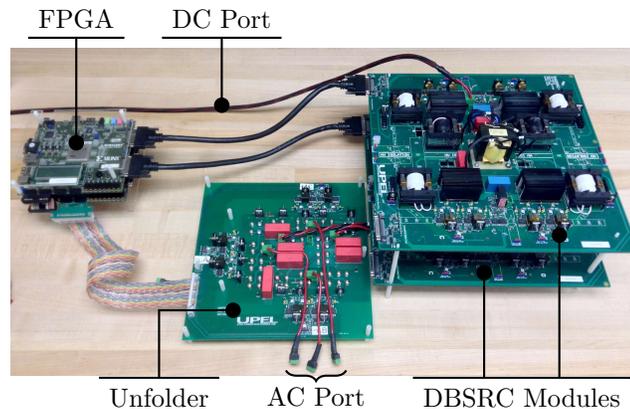


Fig. 7.26: Photo of 1-kVA unfolding converter hardware prototype.

Table 7.3: Specifications of hardware prototype.

	Parameter	Value
Nominal Ratings	DC Input Voltage	500 V
	AC Line-to-Line Voltage	208 V rms
	Three-Phase Power	1 kVA
DBSRC	Switching Frequency	100 kHz
	Transformer Turns Ratio	1
	Resonant Inductance	200 μ H
	Resonant Capacitance	34 nF
	Input Capacitance	1 μ F
	Output/DC-Link Capacitance	1 μ F
	MOSFET Switches	APT34N80LC3
Unfolder	IGBT Switches	APT75GP120JDQ3
	Filter Inductance	15 μ H

output current becomes more sensitive to variation in output voltage, which also changes G_0 and affects the overall response.

To quantify the variation on G_0 , the DBSRC hardware in Table 7.3 is tested in dc operation by applying input voltage of 400 V. The output voltage is swept between zero and 400 V, and the command is swept between ± 1 . The dc output current I_k is measured and plotted in Fig. 7.27b. Also shown are the expected current values based an ideal G_0 value of 4 at this input voltage. Notice at the same U value, I_k varies and deviates from its expected value. In the resulting plot of $G_0 = \frac{I_k}{U}$, notice that gain variation exists and becomes larger at small command values. The worst-case gain variation is 60%.

In ac operation with the unfolder, each DBSRC module sees wide-varying output voltage and applied command. Any variation in its dc gain will cause instantaneous error between output and reference currents. This fast-varying error is not sufficiently corrected by the feedback controller, due to a limited closed-loop bandwidth. The alternative approach used here is feedforward linearization, based on the measured gain variation. A gain linearizer is added before the MCT modulator in Fig. 7.27a. It modifies the command u from the feedback controller and outputs $u^* = u + \Delta u$ to the modulator. The adjustment

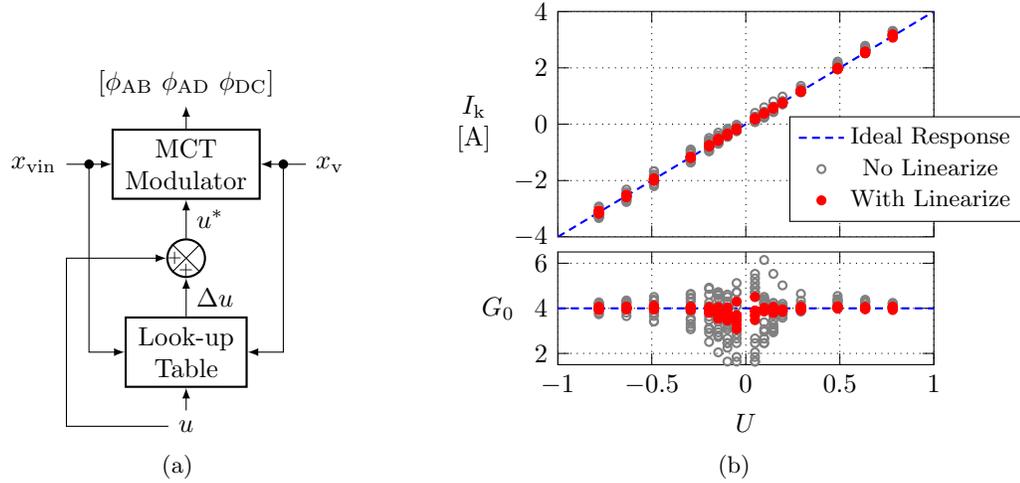


Fig. 7.27: DBSRC gain linearization. (a) Block diagram. (b) DC measurements.

Δu is selected from a look-up table based on u and the computed voltage conversion ratio M , which is also used in the modulator. To obtain a linearized gain, the table entries Δu are obtained by interpolating the earlier dc measurements.

The DBSRC output current is measured again with the added gain linearizer by sweeping the output voltage and applied command. In Fig. 7.27b, the resulting dc gain has less variation, with a worst-case value of only 20%. This look-up table approach has been used in radio-frequency power amplifiers to predistort their input signals and obtain a linear amplifier response [85–88]. The designed gain-linearized modulator is used in subsequent experiments on the DBSRC-unfolding converter.

7.5.2 Grid-Tied Results

All results are obtained at the nominal dc input voltage of 500 V and ac line-to-line voltage of 208 V rms. A filter inductance of 15 μH is used in all experiments. The steady-state line current waveforms at unity power factor are shown in Fig. 7.28a. The experiment is conducted for positive power flow or delivering 1.2 kW to grid. The line-to-neutral voltage of Phase A is also displayed to show phase relationship. The oscilloscope data for current i_a is used to obtain the harmonic spectrum in Fig. 7.28b. All harmonics are within the IEEE 1547 limits. The corresponding THD is 2.5%.

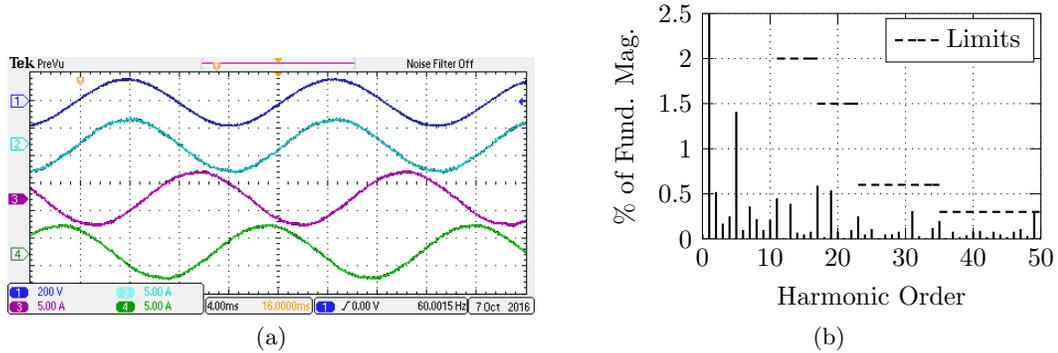


Fig. 7.28: Experimental results at unity power factor and 1.2 kW. (a) Waveforms displaying Channels 1 through 4 as line-to-neutral grid voltage e_a , line currents i_a , i_b and i_c respectively. (b) Harmonic spectrum of i_a and IEEE 1547 limits.

Operation at power factor of 0.8 (inductive) is verified in Fig. 7.29. The displayed dc-link currents show expected profile as required at this power factor. The measured THD of 4% is slightly higher than at unity power factor. Further controller optimization is expected to reduce THD.

The line currents during a power reversal transient are shown in Fig. 7.30a. Prior to the event, the converter is delivering 500 W to grid. A positive-to-negative step change is then applied to d-axis reference current. The high closed-loop bandwidth causes both dc-link currents to settle within 1 ms, as shown in Fig. 7.30b. This results in line currents that receive 500 W from grid. The instantaneous active power is obtained from data points in Fig. 7.30a and plotted in Fig. 7.30c. The small settling time on active power demonstrates fast converter dynamics.

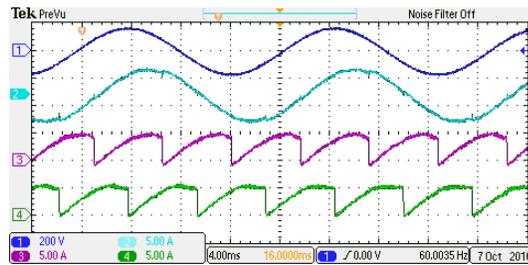


Fig. 7.29: Experimental waveforms at power factor of 0.8 (inductive) and 1.2 kVA, displaying Channels 1 through 4 as e_a , i_a and dc-link currents i_1 and i_2 respectively.

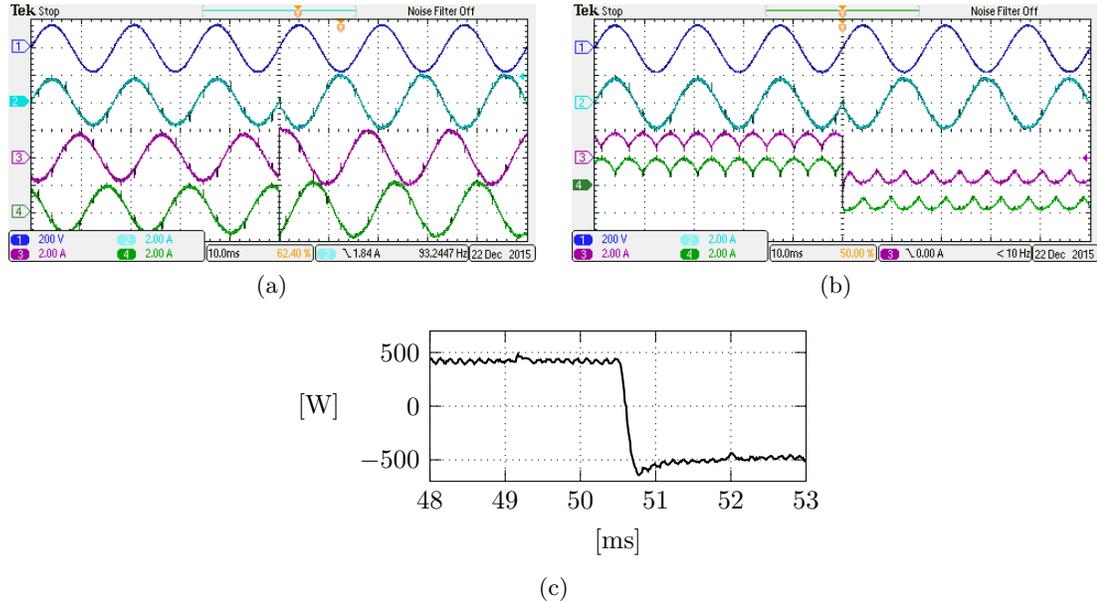


Fig. 7.30: Experimental results for a step change in d-axis reference current to reverse three-phase active power from 500 to -500 W. (a) Waveforms displaying Channels 1 through 4 as line-to-neutral grid voltage e_a , line currents i_a , i_b and i_c respectively. (b) Waveforms displaying Channels 1 through 4 as e_a , i_a and de-link currents i_1 and i_2 respectively. (c) Calculated instantaneous active power from waveforms.

Converter efficiency and line current THD are plotted against active power in Fig. 7.31. Efficiency reaches 91% at 500 W and continues to increase to 93% at 1.2 kW at both power flow directions. Reasonable efficiency is maintained over a wide range of power due to reduced conduction loss using MCT-based multi-angle modulation in the DBSRC modules and reduced switching loss using the auxiliary legs for ZVS. It can be improved by further optimizing the DBSRC power stage component design and extending the soft-switching range. Minimum line current THD of 2.5% is reached at 1.2 kW. The low distortion is due to the linearized DBSRC gain and fast command actuation from the rotating-frame controller.

7.6 Summary

The integral and output feedback controllers in stationary frame suffer from a small but finite phase error between actual and reference line currents, as well as worse current

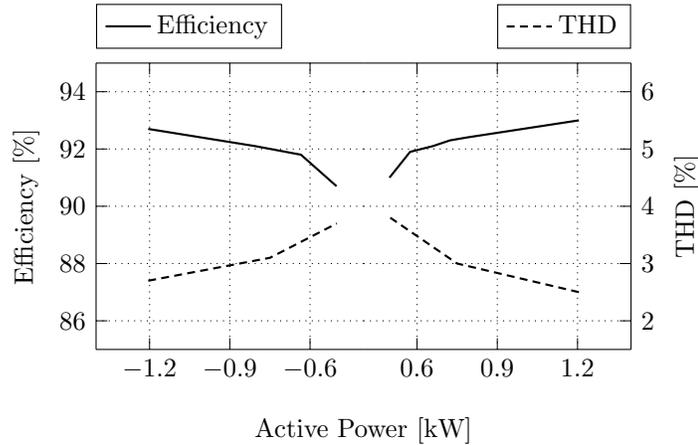


Fig. 7.31: Experimental unfolding converter efficiency and line current THD versus three-phase active power.

quality at non-unity power factors compared to feedforward control. The integral output feedback controller is retained but acts on sensed quantities transformed into rotating frame. Errors on fundamental components become constant quantities in rotating frame and are driven to zero by the integrators. The generation of converter commands through inverse transformation removes tracking requirement on controller gains through feedforward of the phase angle. In addition, the feedforward of the sector variable allows generation of step command changes, which are required for and improves current quality at non-unity power factors. The current quality is further improved by feedforward of anticipated dc-link capacitor currents in command generation, so that the line currents become less affected. The rotating-frame controller is verified in simulation and experiment and demonstrates high current quality and fast dynamics regardless of values of line inductance and power factor.

CHAPTER 8

CONCLUSIONS

The work in this dissertation is focused on a recently proposed three-phase unfolding inverter for integrating battery energy storage to a low-voltage ac grid. The inverter is designed to control power exchange between the battery and grid, where it is commanded to delivery or receive a combination of active and reactive power to and from the grid. The same application has long been served using the pulse-width modulated two-level voltage source inverter (VSI). This topology generates current harmonics around and beyond the switching frequency, and requires a large line filter to provide sufficient attenuation to meet regulatory requirements. The same application also typically requires step up of the battery voltage to provide a sufficient dc-link voltage for the VSI, depending on magnitude of the grid voltage. This is traditionally accomplished using a boost dc-dc converter but has more recently being replaced by a dual-active bridge (DAB) converter, as it offers galvanic isolation and soft-switching properties.

The advent of the unfolding inverter is motivated by the integration of some functions of the VSI into the dc-dc stage. Specifically, the dc-dc stage is now controlled to shape the dc-link currents into sinusoidal segments. The unfolder stage then joins the segments into sinusoidal ac. A benefit of doing so is the virtual elimination of switching loss in the unfolder, as it switches at line frequency. Another benefit stemming from line-frequency switching is non-generation of line current harmonics by the unfolder stage. A line filter is still required, however, as harmonics are being generated by the dc-dc stage, but its size is reduced. Two dual-bridge series resonant converter (DBSRC) modules are selected for the dc-dc stage, owing to a low tank current over a wide operating range when modulated on minimum current trajectories (MCT). This dissertation has investigated the power circuit and controller designs of the DBSRC-unfolding converter for grid-tied application.

8.1 Summary of Contributions

The five major contributions of this work all associated with the proposed DBSRC-unfolder for grid-tied application are summarized here.

Design and Optimization of Passive and Filter Components

Equations of rms currents over a line period of the DBSRC tank components (resonant inductor and capacitor and transformer) and input and dc-link capacitors are provided. The results facilitate dimensioning of components in new designs, as well as to estimate ratings of the DBSRC-unfolder using an existing DBSRC design. An optimal range of the transformer turns ratio is provided and results in minimized primary- and secondary-side rms currents. A formula is provided to estimate the line current harmonics that originate from the DBSRC tanks. Correspondingly, a line filter design procedure is provided to attenuate these harmonics.

Passive and Filter Size Comparison With Conventional DAB-VSI Converter

The components in both converters are designed and dimensioned under same ratings of 10 kW, 480 V rms line-to-line and 300 V input voltages, which are representative of actual systems in this application, and constraints of 50 kHz DAB/DBSRC and 10 kHz VSI switching frequencies, which are achievable using commercially available silicon MOSFET and IGBT devices and ferrite and iron powder materials and have been reported in existing literature. Comparison of component sizes reveals larger dc-dc stage volume in the proposed converter, due to its use of two separate DBSRC tanks and each having additional tank capacitors. However, the inverter stage is much smaller, due to significantly reduced filter inductance and dc-link capacitance. This contributes to an overall 40% reduction in total passive volume in the proposed topology. The comparison demonstrates size reduction and power density improvements using the proposed converter with a different topology and without using exotic devices or materials.

Modeling and Feedforward Control

The objective has been to design an appropriate controller tailored to the unfolding converter to achieve performance that meets regulatory requirements and matches or exceeds that of comparable grid-tied converters. To this end, various controllers are designed, starting with a basic feedforward controller. The first step taken is the derivation of an equivalent circuit based on dc-link quantities and an associated piecewise linear state model. The circuit and model accurately predict and describe the current distortion and oscillation occurring at beginning of each unfolder sector that are observed in simulation. At non-unity power factors, current distortion can become significant due to finite DBSRC rise time when responding to step changes in applied command. A remedy that takes advantage of conduction of unfolder clamping diodes is proposed and tested by phase-shifting the unfolder and reference sectors. The proposed sector-adjusting algorithm is simple to apply and effective in reducing current excursion and distortion at sector beginnings.

Feedback Control in Stationary Frame

The previous feedforward controller offers fast response but no error correction and no damping of resonance. An integral output feedback controller is designed to address both issues. Each converter command is generated from a combination of sensed dc-link current and voltage as well as integrated error between sensed and reference dc-link currents. A high integral gain is needed to reduce tracking error, while applying proper gains on sensed outputs damps the resonant poles. The gains are tuned using the linear quadratic regulator (LQR) and then converting the full state feedback gains into static output feedback gains by retaining dominant poles. This control scheme is tested in simulation and offers improved current quality at unity power factors and with large line inductances over feedforward control.

Feedback Control in Synchronous Rotating Frame

Control in stationary frame suffers from a small but finite phase error between actual and reference line currents, as well as worse current quality at non-unity power factors com-

pared to feedforward control. The integral output feedback controller is retained but acts on sensed quantities transformed into rotating frame. Errors on fundamental components become constant quantities in rotating frame and are driven to zero by the integrators. The generation of converter commands through inverse transformation removes tracking requirement on controller gains through feedforward of phase angle. In addition, the feedforward of the sector variable allows generation of step command changes, which are required for and improves current quality at non-unity power factors. The current quality is further improved by feedforward of anticipated dc-link capacitor currents in command generation, so that the line currents become less affected. The rotating-frame controller is verified in simulation and experiment and demonstrates high current quality and fast dynamics regardless of values of line inductance and power factor.

8.2 Future Work

This dissertation has focused on an unfolding converter with two DBSRC modules in the dc-dc stage. Although the DBSRC represents a well-rounded choice due to minimized tank current over wide operating range when modulated using MCT, this implementation is by no means unique and has its drawbacks. One is the high number of active switches. Another is room for improvement in converter efficiency. A future direction is thus reduction in component count and efficiency optimization. Both issues shall be considered together to result in combined improvements.

Preliminary work has been conducted on a candidate topology, derived by combining primary-side circuits of two DBSRC modules. This results in one primary leg shared by two converter halves and a reduction of two switches and associated gate-drive circuits compared to two modules. The two resonant tanks and secondary-side circuits are kept unchanged. The rms current in the combined leg can be reduced by modulating the converter halves on different MCT branches. Further work on this topology includes a comprehensive evaluation of conduction and switching loss with the unfold.

This dissertation has devised controllers using static relationships and gains. The robustness against parameter variations is ensured by careful tuning of the static controller

gains. This static approach is limited by its performance (e.g. closed-loop bandwidth) and generality (e.g. retuning required for different systems). By investigating a more adaptive controller, better performance and more flexibility can be obtained. This adaptivity can be explored in the look-up table used to implement the MCT modulator. Specifically, the table entries can be dynamically updated to linearize the instantaneous command to output current gain of the DBSRC. A linearized gain rejects grid voltage disturbances as well as nonidealities due to converter losses and dead times. This adaptive look-up table based modulator can also be implemented for schemes other than MCT, such as ZVS trajectories.

The developed methods control the unfolding converter in grid-tied mode. Recent applications have evolved to demand multi-mode operation in the same converter. An example is in electric vehicle drivetrain, where it is desired to integrate charging features into the drivetrain inverter. Doing so eliminates a dedicated on-board charger and potentially increases charging power. Most existing works require a customized motor that connects to the grid and functions as a filter inductor in charger mode. The drivetrain VSI can be replaced with the unfolding converter that operates either in drive or charger mode. The benefit is no need of motor customization, and conventional three-phase motors can be used. This is a result of minimal line filter requirements in charger mode. This application requires a controller of the unfolding converter in drive mode. Fortunately, the existing grid-tied controller can be easily modified for motor drive as it is already designed in rotating frame. Another benefit of an unfolding drive is the reduced common-mode current and electromagnetic interference due to sinusoidal unfolded output voltages.

Another application requiring multi-mode operation is a grid-interactive inverter, as introduced in Chapter 2. This inverter can operate in either grid-tied or grid-forming modes. The motivations of designing a grid-interactive unfolding converter are its compact size and galvanic isolation. This application requires a controller of the unfolding converter in grid-forming mode. The challenges include ensuring robust voltage regulation subjective to load uncertainties and smooth mode transitions depending on grid condition.

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