

ECE 5470/6470

VLSI Design

Description: This course addresses advanced issues in VLSI design, covering the following topics: design methodologies and IP design, CMOS circuit scaling, advanced logic circuit styles, noise sources and signal integrity in digital design, design techniques for dynamic and static power reduction, power supply issues, interconnect analysis, clocking and synchronization, process variation, and performance verification. The course also introduces the standard cell library based ASIC design flow. Students are expected to complete a substantial design project as part of the course, which involves extensive use of CAD tools.

Instructor: Dr. Sanghamitra Roy

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Lectures: TR 1.30pm-2.45pm

Office hours: TR 3.00pm-4.00pm (or by appointment)

Prerequisites: ECE 5530 or equivalent and ECE 5460/6460

Textbook: A. Chandrakasan, W. Bowhill, F. Fox, *Design of High-Performance Microprocessor Circuits*, IEEE Press, 2000.

References (Optional):

- Neil Weste and David Harris, **CMOS VLSI Design – A Circuits and Systems Perspective**, Third edition, Addison Wesley.
- Selected material from recent publications.

Course Webpage: <http://www.engr.usu.edu/ece/faculty/sroy/5470.html>

Homework: There will be homework assignments given approximately on a biweekly basis to help understand the concepts. Some of the homework assignments will involve programming and usage of CAD tools to familiarize students with CAD design flows. Students are expected to work 8 to 10 hours per week on the CAD tool assignments.

Computer Use: This course will involve several CAD tool assignments using the Synopsys and Cadence packages in the Design Automation lab.

Final Project: This course involves a substantial design project. The final project will be done in groups of two or three students. The instructor will provide a list of potential topics and resources, but teams will also be given freedom to propose their own topic. Teams are required to submit a proposal, a midterm progress report, a final report and all implementation files. Each team will also prepare a presentation to demonstrate their results.

Exams: There will be one midterm and a final exam. The exams will be open book and calculators will be allowed. Hand-held computers (PDAs) or laptops are not allowed.

Grading: The following weights will be used:

Homework and Labs: 25%

Midterm: 20%

Final exam: 20%

Final project: 30%

Class participation: 5%

Grading is based on a conventional fixed scale:

A > 90%

A- > 80%

B+ > 75%

B > 70%

B- > 65%

C+ > 60%

C > 55%

C- > 50%

D+ > 47%

D > 44%

D- > 40%

F < 40%

The instructor reserves the right to curve up the scores at the end of the semester.

Late policy: Late submissions will not be accepted without prior approval by the instructor.

Disabilities: In cooperation with the Disability Resource Center, reasonable accommodation will be provided for qualified students with disabilities. Please meet with the instructor during the first week of class to discuss possible arrangements.

Cheating and Plagiarism: Cheating and plagiarism is not permitted. The instructor reserves the right to fail any student who is caught cheating and/or plagiarizing.

Course outline: The following topics will be covered with some variations.

- 1) CMOS Transistor Theory
- 2) CMOS Scaling
- 3) Process Variation
- 4) Circuit Design Styles
- 5) Noise sources, analysis
- 6) Timing Verification
- 7) Low Leakage design
- 8) Interconnect & Inductance
- 9) Clocking, synchronization & metastability
- 10) Packaging and Power Supply

In addition, the following topics will be covered if time permits:

- 1) Dynamic power reduction
- 2) Electromigration reliability
- 3) Hot carrier reliability and NBTI
- 4) Testing of high-performance microprocessors
- 5) Asynchronous design